`include "config.sv"

module boot\_rom\_wrap

#(

parameter ADDR\_WIDTH = `ROM\_ADDR\_WIDTH,

parameter DATA\_WIDTH = 32

)(

// Clock and Reset

input logic clk,

input logic rst\_n,

input logic en\_i,

input logic [ADDR\_WIDTH-1:0] addr\_i,

output logic [DATA\_WIDTH-1:0] rdata\_o

);

boot\_code

boot\_code\_i

(

.CLK ( clk ),

.RSTN ( rst\_n ),

.CSN ( ~en\_i ),

.A ( addr\_i[ADDR\_WIDTH-1:2] ),

.Q ( rdata\_o )

);

endmodule