`ifndef DEBUG\_BUS\_SV

`define DEBUG\_BUS\_SV

`include "config.sv"

interface DEBUG\_BUS

#(

parameter ADDR\_WIDTH = 15

);

logic req;

logic gnt;

logic rvalid;

logic [ADDR\_WIDTH-1:0] addr;

logic we;

logic [31: 0] wdata;

logic [31: 0] rdata;

// Master Side

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

modport Master

(

output req, addr, we, wdata,

input gnt, rvalid, rdata

);

// Slave Side

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

modport Slave

(

input req, addr, we, wdata,

output gnt, rvalid, rdata

);

endinterface

`endif