Module-1

- Computer Types - S.A
- Functional units
- Basic operational concepts
- Bus structure - SN
- Software performance
- computer Generations
- Multiprocessors vs multicomputer

- Data representations
- Fixed point floatingpoint.

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conversions

- Binary to Hexa Decimal Octal

Hexa - Binary
Octal
Decimal

Octal - Binal
Hexa
Decimal

complements - 1's comple

1001
0110
+1
2's co 0111

Signed - A+B, A-B
(A<B, A>B, A=B)

- Binary codes

Digital logic circuits — Module - 2

- Minimization of logic - K-Map

- universal gates (nand, NOR)
- Basic gates (AND, OR, NOT)

A

combinational circuits

H.A, F.A, MUX, DEMUX, Encoder, Decoder

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sequential circuits ~~Digital logic circ~~ -II

B

Flipflops - S-R, D, J-K, T

SR, D → Register

J K, T → counter

Shift register [SR, D, JK]

counters [JK, T]

PLD's

Module 3

Signed
: Fixed point Arithematic
- Addition | subtraction (with Example)
- Multiplication [Booth, Normal]
- Division

A - Floating point →
- Addition | substraction
- Multiplication
- Division

already

with H/w Implementation

Instruction set

Addressing Modes

B

+ Basic Machine Instructions

IA-32 pentium excpl

21 14 14 36 3 25 1 16 16 27 5
7 4 25 7

Module 4: (2)

Processor organization

A

1Q

Reddall as one question 12 only you may get any of the TOPIC⇒ cover

- Introduction to CPU — LA
- Register Transfer — LA
- Execution of Instruction — LA
- Multiple BUS organization — LA
- CU (control unit)
  - Hardwired control — LA
  - Microprogrammed control — LA

Memory organization

B

- concept of Memory (2 marks)
- RAM, ROM (1K×11) (4) 5,6 — Memory organization
- Memory hierarchy — (13, 14)
- cache memories (2 marks)
- virtual memories (2 marks)
- secondary Storage.
- Memory Management

Module 5:

- unit I Introduction to I/O - [1-3]
- unit-II Interrupts - H/w -
- unit-III Enabling & disabling interrupts (4-5)
- unit-IV Device control (Device control Document) DMA → separate
- unit V Interface circuits [pointer to processor connect, Key Board to Processor connect...]
- unit VI (12-13)

unit VI Standard I/O - [14-17]

Long answer

Imp → Threesets

DMA | Interface circuit | Standard I/O

Short Ans

Introduction to I/O

Device control

12

Interrupts & Enabling disabling