--Austin Koch Mak Petersen 3130--

LIBRARY ieee ;

USE ieee.std\_logic\_1164.all ;

ENTITY Wash IS

PORT( Resetn, Clock, TCD, START, FULL : IN STD\_LOGIC ;

H, C, AGT, SPIN, NS, LD, EC : OUT STD\_LOGIC);

END Wash;

ARCHITECTURE LogicFunc OF Wash IS

TYPE State\_type IS ( S0, SF, SA, SP );

Signal y : State\_type;

BEGIN

PROCESS (y, FULL, START, TCD, Clock, Resetn )

BEGIN

IF resetn = '0' THEN

y <= S0;

ELSIF (Clock'EVENT AND Clock = '1') THEN

CASE y IS

WHEN S0 =>

IF START = '1' THEN

y <= SF;

ELSE y <= S0;

END IF ;

WHEN SF =>

IF FULL = '1' THEN

y <= SA;

ELSE

y <= SF;

END IF;

WHEN SA =>

IF TCD = '1' THEN

y <= SP;

ELSE

y <= SA;

END IF;

WHEN SP =>

IF TCD = '1' THEN

y <= S0;

ELSE

y <= SP;

END IF;

END CASE;

END IF;

END PROCESS;

PROCESS (y, FULL, TCD)

BEGIN

H <= '0'; --Defaults value to low

C <= '0';

AGT <= '0';

SPIN <= '0';

LD <= '0';

NS<= '0';

EC <= '0';

CASE y IS

WHEN S0 =>

--No conditions on Start state

WHEN SF =>

--Hot and Cold are always high on refill

IF FULL = '1' THEN

LD <= '1';

NS <= '1';

END IF;

H <= '1';

C <= '1';

WHEN SA =>

IF TCD = '1' THEN

LD <= '1';

NS <= '0';

END IF;

IF TCD = '0' AND FULL = '1' THEN

NS <= '1';

EC <= '1';

AGT <= '1';

ELSIF TCD = '0' AND FULL = '0' THEN

H <= '1';

END IF;

WHEN SP =>

--When TCD is 0, sets line to 7 and counts down to zer

If TCD = '0' THEN

NS <= '0';

EC <= '1';

SPIN <= '1';

END IF;

END CASE ;

END PROCESS ;

END LogicFunc;

--Counter--

LIBRARY ieee ;

USE ieee.std\_logic\_1164.all ;

USE ieee.std\_logic\_signed.all;

ENTITY COUNTER IS

PORT (CLK, Resetn, EC : IN STD\_LOGIC;

COUNTin, Datain : IN STD\_LOGIC\_VECTOR(3 downto 0);

COUNTo : OUT STD\_LOGIC\_Vector(3 downto 0);

TCD : OUT STD\_LOGIC);

END COUNTER;

ARCHITECTURE LogicFunc OF COUNTER IS

Signal COUNT : STD\_LOGIC\_VECTOR(3 downto 0);

BEGIN

COUNT <= COUNTin;

PROCESS (EC,CLK, Datain)

BEGIN

IF (CLK'EVENT AND CLK = '1') THEN

IF COUNT = "0000" THEN

TCD <= '1';

END IF;

IF EC = '1' AND DATAin = "0000" THEN

COUNTo <= COUNT - '1';

ELSIF Datain = "1001" THEN

COUNTo <= "1001";

TCD <= '0';

ELSIF Datain = "0111" THEN

COUNTo <= "0111";

TCD <='0';

ELSE

COUNTo <= COUNT;

END IF;

END IF;

END PROCESS;

END LogicFunc;

LIBRARY ieee ;

USE ieee.std\_logic\_1164.all ;

USE ieee.std\_logic\_signed.all;

ENTITY Multiplexor IS

PORT (SEL, NS : IN STD\_LOGIC;

Data : OUT STD\_LOGIC\_VECTOR(3 DOWNTO 0));

END Multiplexor;

ARCHITECTURE Behavior of Multiplexor IS

BEGIN

PROCESS (SEL, NS)

--SEL is the NS from the controller

--N and S are hardwired so they don't need any sort of determinate in the code

BEGIN

IF SEL = '1' AND NS = '1' THEN

Data <= "1001";

ELSIF SEL = '1' AND NS = '0' THEN

Data <= "0111";

ELSE

Data <= "0000";

END IF;

END PROCESS;

END Behavior;





