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3 // EE 371
4 // Lab 6, task #2
5 //
6 // Inputs:
7 // CLOCK_50: Timer to indicate the functionality of our module.
8 // 4-bit KEY: KEY[0] is the only key used in this lab, it increments the hour
9 // count of our module.
10 // 10-bit SW: SW[9] is set to 'reset', SW[8] is set to 'start' signal.
11 // 13-bit V_GPIO: Inout signals that tells us the current functionality of the
12 // the Parking lot.
13 //
14 // Outputs:
15 // 7-bit HEX0: Tells us how many spots are available in our parking lot.
16 // Goes blank when hour 8 hits.
17 // It also tells if the parking lot is full or not.
18 // 7-bit HEX1: Before hour 8, HEX1 tells us if the parking lot is full.
19 // After hour 8, it tells us the total number of cars
20 // that has entered our parking lot at certain hours of the day.
21 // 7-bit HEX2: Before hour 8, HEX2 tells us if the parking lot is full.
22 // After hour 8, HEX2 cycles through 7 different hours,
23 // which represents the hour of operations during our rush hour day.
24 // It also represents the read address needed to get the total car
25 // count that has entered the parking lot that day.
26 // 7-bit HEX3: Before hour 8, HEX3 tells us if the parking lot is full.
27 // After hour 8, HEX3 tells us if rush hour ended or not.
28 // 7-bit HEX4: Before hour 8, HEX4 is blank, since it does not serve a purpose here.
29 // After hour 8, HEX4 tells us if rush hour started or not.
30 // 7-bit HEX5: Before hour 8, HEX5 tells us the current hour of operation.
31 // After hour 8, HEX5 goes blank.
32 // 10-bit LEDR: Only Certain LEDRs are used in this module. Main job
33 // is to signal the operations of various V_GPIO wires, i.e.
34 // parking lot is full, there's a car entering, parking spot 1 is filled, etc.
35 //
36 // Logics:
37 // 4-bit current_hour: tells us the current hour, range: 0 -> 8.
38 // 8th hour is not important to this lab.
39 // 4-bit rush_start: tells us at what hour, rush hour started, or not.
40 // 4-bit rush_end: tells us at what hour, rush hour ended, or not.
41 // 7-bit rush_start_hex: HEX representation of when rush hour started.
42 // 7-bit rush_end_hex: HEX representation of when rush hour ended.
43 // 7-bit final_rush_start_hex: Helps us decide if rush hour started, or
44 // just a '-' representing that rush hour did not start.
45 // 7-bit final_rush_end_hex: Helps us decide if rush hour ended, or
46 // just a '-' representing that rush hour did not end.
47 // full_final: tells us if the parking lot is full.
48 // outDD: signal from double flip flop to avoid metastability, used for ~KEY[0].
49 // no_meta_dd: Stable signal for KEY[0].
50 // outDD1: signal from double flip flop to avoid metastability, used for V_GPIO[31].
51 // no_meta_dd1: Stable signal for V_GPIO[31].
52 // 3-bit num_spots_avail: Tells us how many spots are available in the parking lot.
53 // 7-bit num_spots_avail_hex: HEX representation of how many spots are available in the
54 // parking lot.
55 // en1: Occurs after hour 7, signifies the start of cycling through RAM, to retrieve the
56 // total cars that entered the parking lot at certain hours.
57 // 3-bit rd_addr_count: Representing the read address (hour), used to retrieve the total
58 // number of cars that entered parking at certain hour of the day.
59 // 16-bit rd_data: Represents the total car count that has entered the parking at certain
60 // time.
61 // 7-bit rd_data_hex: HEX representation of how many cars entered the parking lot at
62 // certain hours.
63 // Count is in HEXADECIMAL.
64 // 7-bit rd_addr_hex: HEX representation of current hour that's being cycled through.
65 // 7-bit current_hour_hex: HEX representation of current hour of operation.
66 // 7-bit HEX0_temp: Temp register for HEX0.
67 // 7-bit HEX1_temp: Temp register for HEX1.
68 // 7-bit HEX2_temp: Temp register for HEX2.
69 // 7-bit HEX3_temp: Temp register for HEX3.
70 // Summary: The DE1_SoC module is the top-level module for our parking lot system. It is
71 // responsible for
72 // running all the submodules that contribute to our parking lot system as well as

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69 connecting our
// parking lot logic to the appropriate corresponding FPGA inputs and outputs such as SW,
70 KEY,
71 // LEDR, or HEX.
72 `timescale 1 ps / 1 ps
73 module DE1_SoC (CLOCK_50, HEX0, HEX1, HEX2, HEX3, HEX4, HEX5, KEY, SW, LEDR, V_GPIO);
74     input logic CLOCK_50;
75     output logic [6:0] HEX0, HEX1, HEX2, HEX3, HEX4, HEX5;
76     input logic [3:0] KEY;
77     input logic [9:0] SW;
78     output logic [9:0] LEDR;
79     inout logic [35:23] V_GPIO;
80
81     // Generate clk off of CLOCK_50, whichClock picks rate.
82     logic [31:0] div_clk;
83
84     parameter whichClock = 24.25; // 0.75 Hz clock // soft answer
85     clock_divider cdiv (.clock(CLOCK_50),
86                         .reset(reset),
87                         .divided_clocks(div_clk));
88
89     // Clock selection; allows for easy switching between simulation and board
90     // clocks
91     logic clkSelect;
92     // Uncomment ONE of the following two lines depending on intention
93     //assign clkSelect = CLOCK_50; // for simulation
94     assign clkSelect = div_clk[whichClock]; // for board
95
96     // FPGA output
97     assign V_GPIO[26] = V_GPIO[28]; // LED parking 1
98     assign V_GPIO[27] = V_GPIO[29]; // LED parking 2
99     assign V_GPIO[32] = V_GPIO[30]; // LED parking 3
100    assign V_GPIO[34] = V_GPIO[28] & V_GPIO[29] & V_GPIO[30]; // LED full
101    assign V_GPIO[31] = V_GPIO[23] & ~V_GPIO[34]; // SW[4]; // Open entrance // tell me
when to enter
102    assign V_GPIO[33] = V_GPIO[24]; // SW[5]; // Open exit // tell me when to exit
103    logic [3:0] current_hour;
104    logic [3:0] rush_start, rush_end;
105    logic [6:0] rush_start_hex, rush_end_hex;
106    logic [6:0] final_rush_start_hex, final_rush_end_hex;
107    logic full_final;
108    logic outDD;
109    logic outDD1, no_meta_dd1;
110    logic no_meta_dd;
111    logic [2:0] num_spots_avail;
112    logic [6:0] num_spots_avail_hex;
113    logic en1;
114    logic [2:0] rd_addr_count;
115    logic [15:0] rd_data;
116    logic [6:0] rd_data_hex, rd_addr_hex, current_hour_hex;
117    logic [6:0] HEX0_temp, HEX1_temp, HEX2_temp, HEX3_temp;
118    logic outDD11, no_meta_dd11;
119
120    // assigns the "en1" signal (which is essentially an enable signal) to when
"current_hour" equals
121    // 8, signaling that the day is over.
122    assign en1 = (current_hour == 8);
123
124    // module 'flipFlop', named 'DD' is used as a flip flop for our input of KEY[0] to
ensure that
125    // the output will be the same after a few clock cycles to prevent metastability
126    flipFlop DD (.clk(CLOCK_50), .reset(SW[9]), .in(~KEY[0]), .out(outDD));
127
128    // module 'user_input', named 'no_meta' is used to ensure that our KEY[0] input will only
129    // produce an output for one clock cycle. this is to prevent any unnecessary increments in
130    // current hour of the day
131    user_input no_meta(.clock(CLOCK_50), .reset(SW[9]), .in(outDD), .out(no_meta_dd));
132
133    // module 'flipFlop', named 'DD_new' is used as a flip flop for our V_GPIO[31] input that
134    // indicates when a car is waiting to enter the car. it is to ensure that the output
will be the same
135    // after a few clock cycles to prevent metastability.
136    flipFlop DD_new (.clk(CLOCK_50), .reset(SW[9]), .in(V_GPIO[31]), .out(outDD1));

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137
138 // module 'user_input', named 'no_meta_new' is used to ensure that our V_GPIO[31] input
will
139 // only produce an output for one clock cycle. this is to prevent any unnecessary
increments in
140 // the total car count
141 user_input no_meta_new (.clock(CLOCK_50), .reset(SW[9]), .in(outDD1), .out(no_meta_dd1));
142
143 // module 'flipFlop', named 'DD_newer' is used as a flip flop for our V_GPIO[33] input
that
144 // indicates when a car is waiting to enter the car. it is to ensure that the output
will be the same
145 // after a few clock cycles to prevent metastability.
146
147 flipFlop DD_newer (.clk(CLOCK_50), .reset(SW[9]), .in(V_GPIO[33]), .out(outDD11));
148
149 // module 'user_input', named 'no_meta_newer' is used to ensure that our V_GPIO[33]
input will
150 // only produce an output for one clock cycle. this is to prevent any unnecessary
increments in
151 // the total car count
152 user_input no_meta_newer (.clock(CLOCK_50), .reset(SW[9]), .in(outDD11), .out(
no_meta_dd11));
153
154 // module 'rushhr', named 'rush_hour' is used to implement our rush hour algorithm.
There is a
155 // controller and datapath component as well as other submodules to help implement the
156 // algorithm. Rush hour starts when the parking lot first becomes full and it ends when
the
157 // parking lot first becomes empty after it becomes full. If there exists a rush hour,
outputs that
158 // represent the starting and ending hour of rush hour will be output as a number from
0-7. If
159 // there does not exist a rush hour, the outputs will be the number 8 which signifies
that a rush
160 // hour never happened. Additionally, this module is responsible for counting the total
number of
161 // cars that have entered the parking lot throughout the day.
162 rushhr rush_hour (.clk(CLOCK_50), .reset(SW[9]), .in(no_meta_dd1), .out(no_meta_dd11),
163 .end_hour(rush_end), .start_hour(rush_start), .start(SW[8]),
164 .key0(no_meta_dd), .full_final, .cur_hour(current_hour), .rd_addr(
rd_addr_count), .q(rd_data));
165
166 // module 'count_spots', named 'count_it_pls' is used to keep track of the remaining
number of
167 // parking spaces in the lot. the number of remaining parking spaces is equal to the
number of
168 // occupied parking spaces subtracted from 3. a parking space is occupied if it detects
a car in a
169 // parking space (thanks to the V_GPIOs)
170 count_spots Count_it_pls(.car1(V_GPIO[26]), .car2(V_GPIO[27]), .car3(V_GPIO[32]), .
spot_left(num_spots_avail));
171
172 // module 'counter', named 'coun' is used to cycle through the hours of the day in an
orderly
173 // manner once the day is over (aka after the 8th hour). when the day is over, an enable
signal
174 // will be sent in to let the module know it's okay to cycle through the hours. The
cycling of the
175 // hours are needed for display on HEX2 after the day is completed. The hours cycling is
also
176 // used for write/read addresses for our RAM.
177 counter coun(.clk(clkSelect), .reset(SW[9]), .en(en1), .out(rd_addr_count));
178
179 // module 'HEX_RAM', named 'hex5' is used to display the data needed for HEX5 during the
180 // parking lot simulation. HEX5 displays the current hour of the day so it outputs a
7-segment
181 // display of a number from 0-7 depending on the current hour.
182 HEX_RAM hex5(.in(current_hour), .out(current_hour_hex));
183
184 // module 'HEX_RAM', named 'hex4' is used to display the data needed for HEX4 during the
185 // parking lot simulation. HEX4 displays the starting hour of rush hour so it outputs a
7-segment
186 // display of a number from 0-7 depending on the starting hour or a dash if there's no

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rush hour.
187     HEX_RAM hex4(.in(rush_start), .out(rush_start_hex));
188
189     // module 'HEX_RAM', named 'hex3' is used to display the data needed for HEX3 during the
190     // parking lot simulation. HEX3 displays the ending hour of rush hour so it outputs a
7-segment
191     // display of a number from 0-7 depending on the ending hour or a dash if there's no
rush hour.
192     HEX_RAM hex3(.in(rush_end), .out(rush_end_hex));
193
194     // module 'HEX_RAM', named 'hex0' is used to display the data needed for HEX0 during the
195     // parking lot simulation. HEX0 displays the remaining number of parking spaces so it
outputs a
196     // 7-segment display of a number from 1-3 depending on the remaining number of parking
197     // spaces.
198     HEX_RAM hex0(.in(num_spots_avail), .out(num_spots_avail_hex));
199
200     // module 'HEX_RAM', named 'hex1' is used to display the data needed for HEX1 during the
201     // parking lot simulation. HEX1 displays and cycles in intervals of 1 second through the
total
202     // number of cars that have entered the parking lot by a certain hour of the day so it
outputs a
203     // 7-segment display of a hexadecimal number depending on the total number of cars
entered at
204     // that hour.
205     HEX_RAM hex1(.in(rd_data), .out(rd_data_hex));
206
207     // module 'HEX_RAM', named 'hex2' is used to display the data needed for HEX2 during the
208     // parking lot simulation. HEX2 displays and cycles in intervals of 1 second through the
hours of
209     // the day so it outputs a 7-segment display of a number from 0-7 depending on the hour
of the
210     // day.
211     HEX_RAM hex2(.in(rd_addr_count), .out(rd_addr_hex));
212
213     // Logic to decide whether rush hour started or ended, or not.
214     // If rush hour started and ended, HEX 4 and 3 will output
215     // the HEX representation of the hour that rush hour started and
216     // the hour that rush hour ended.
217     // Else, HEX 4 and 3 will output a '-' to demonstrate
218     // that rush hour was not successfully completed.
219     always_comb begin
220         if ((rush_end == 8) && (rush_start == 8)) begin
221             final_rush_start_hex = 7'b0111111; // '-'
222             final_rush_end_hex = 7'b0111111; // '-'
223         end else begin
224             final_rush_start_hex = rush_start_hex;
225             final_rush_end_hex = rush_end_hex;
226         end
227     end
228
229     // logic before hour 8,
230     // if the parking lot is full, HEX3 - 0
231     // will spell out 'FULL'.
232     // Else, HEX0 will show how many spots are available in
233     // the parking lot.
234     always_comb begin
235         if (V_GPIO[34]) begin
236             //full state here
237             HEX3_temp = 7'b0001110; // F
238             HEX2_temp = 7'b1000001; // U
239             HEX1_temp = 7'b1000111; // L
240             HEX0_temp = 7'b1000111; // L
241         end else begin
242             HEX3_temp = '1;
243             HEX2_temp = '1;
244             HEX1_temp = '1;
245             HEX0_temp = num_spots_avail_hex;
246         end
247     end
248
249     // HEX operations before and after hour 8.
250     // Before hour 8:
251     // HEX 5: show current hour count.

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252 // HEX 4: blank.
253 // HEX 3 - 0: functions are outlined in the above always_comb block.
254 //
255 // After hour 8:
256 // HEX 5: blank.
257 // HEX 4: show whether or not we started rush hour.
258 // HEX 3: show whether or not we ended rush hour.
259 // HEX 2: show the current hour that we cycling through.
260 // RANGE: 0 -> 7.
261 // HEX 1: show the number of cars that entered the parking
262 // lot during certain hours.
263 // HEX 0: blank.
264 always_comb begin
265     if (~(current_hour == 8)) begin
266         HEX5 = current_hour_hex;
267         HEX4 = '1;
268         HEX3 = HEX3_temp;
269         HEX2 = HEX2_temp;
270         HEX1 = HEX1_temp;
271         HEX0 = HEX0_temp;
272     end else begin
273         HEX5 = '1;
274         HEX4 = final_rush_start_hex;
275         HEX3 = final_rush_end_hex;
276         HEX2 = rd_addr_hex;
277         HEX1 = rd_data_hex;
278         HEX0 = '1;
279     end
280 end
281
282
283
284 // FPGA input
285 assign LEDR[0] = V_GPIO[28]; // Presence parking 1
286 assign LEDR[1] = V_GPIO[29]; // Presence parking 2
287 assign LEDR[2] = V_GPIO[30]; // Presence parking 3
288 assign LEDR[3] = V_GPIO[23]; // Presence entrance
289 assign LEDR[4] = V_GPIO[24]; // Presence exit
290 assign LEDR[5] = V_GPIO[34]; // full
291
292 endmodule // DE1_SoC
293
294 // This test bench is designed specifically to examine how the top module 'DE1_SoC'
295 // Interfaces with the submodule functions. Essentially, we want to see what would happen
296 // when we incorporate the use of switches and keys from DE1_SoC.
297 // We are testing 2 different cases in this test bench.
298 // 1) The start and end of rush hour
299 // 2) rush hour doesn't start
300 // We are making sure that the SWS and KEYS we use from the FPGA will work accordingly
301 // with the code that we wrote the for the submodules that controls the functionality of
302 // rush hour and car count.
303 module DE1_SoC_testbench();
304     logic CLOCK_50;
305     logic [6:0] HEX0, HEX1, HEX2, HEX3, HEX4, HEX5;
306     logic [3:0] KEY;
307     logic [9:0] SW;
308     logic [9:0] LEDR;
309     wire [35:23] V_GPIO;
310
311     // use SWS to simulate the signals form V_GPIO wires
312     // The functions of V_GPIO pins are outlined above
313     assign V_GPIO[28] = SW[7];
314     assign V_GPIO[29] = SW[6];
315     assign V_GPIO[30] = SW[5];
316     assign V_GPIO[24] = SW[4];
317     assign V_GPIO[23] = SW[3];
318
319     DE1_SoC dut1 (.*));
320
321     parameter clock_period = 100;
322     initial begin
323         CLOCK_50 <= 0;
324         forever #(clock_period / 2) CLOCK_50 <= ~CLOCK_50;
325     end

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326     end
327
328   initial begin
329     // Initialize the inputs
330     SW[9] <= 1; SW[8] <= 0; KEY[0] <= 1; @(posedge CLOCK_50);
331     SW[9] <= 0; SW[8] <= 1; @(posedge CLOCK_50);
332     // start of rush hour
333     SW[8] <= 0; @(posedge CLOCK_50);
334     // Increment rush hour
335     // Increment car count here
336     SW[7] <= 1; SW[3] <= 1; @(posedge CLOCK_50);
337     KEY[0] <= 0; @(posedge CLOCK_50);
338     KEY[0] <= 1; @(posedge CLOCK_50);
339     SW[6] <= 1; SW[3] <= 1; @(posedge CLOCK_50);
340     KEY[0] <= 0; @(posedge CLOCK_50);
341     KEY[0] <= 1; @(posedge CLOCK_50);
342     // rush hour starts after this point
343     SW[5] <= 1; SW[3] <= 1; @(posedge CLOCK_50);
344     KEY[0] <= 0; @(posedge CLOCK_50);
345     KEY[0] <= 1; @(posedge CLOCK_50);
346     // start ending rush hour here
347     SW[7] <= 0; SW[4] <= 1; @(posedge CLOCK_50);
348     KEY[0] <= 0; @(posedge CLOCK_50);
349     KEY[0] <= 1; @(posedge CLOCK_50);
350     SW[6] <= 0; SW[4] <= 1; @(posedge CLOCK_50);
351     KEY[0] <= 0; @(posedge CLOCK_50);
352     KEY[0] <= 1; @(posedge CLOCK_50);
353     // rush hour ends here
354     SW[5] <= 0; SW[4] <= 1; @(posedge CLOCK_50);
355     SW[4] <= 0; @(posedge CLOCK_50);
356     KEY[0] <= 0; @(posedge CLOCK_50);
357     KEY[0] <= 1; @(posedge CLOCK_50);
358     KEY[0] <= 0; @(posedge CLOCK_50);
359     KEY[0] <= 1; @(posedge CLOCK_50);
360     KEY[0] <= 0; @(posedge CLOCK_50);
361     KEY[0] <= 1; @(posedge CLOCK_50);
362     // Operation day ends here
363     for (int i = 0; i < 10; i++) begin
364       @(posedge CLOCK_50);
365     end
366     // Another case,
367     // Testing what happens when we don't
368     // finish rush hour
369     SW[9] <= 1; SW[8] <= 0; @(posedge CLOCK_50);
370     SW[9] <= 0; @(posedge CLOCK_50);
371     SW[8] <= 1; @(posedge CLOCK_50);
372     SW[8] <= 0; @(posedge CLOCK_50);
373     // Increment hour to the end without
374     // rush hour functionality.
375     for (int i = 0; i < 8; i++) begin
376       KEY[0] <= 0; @(posedge CLOCK_50);
377       KEY[0] <= 1; @(posedge CLOCK_50);
378     end
379     for (int i = 0; i < 10; i++) begin
380       @(posedge CLOCK_50);
381     end
382     $stop;
383   end
384
385 endmodule
386
387
388
389
390
```