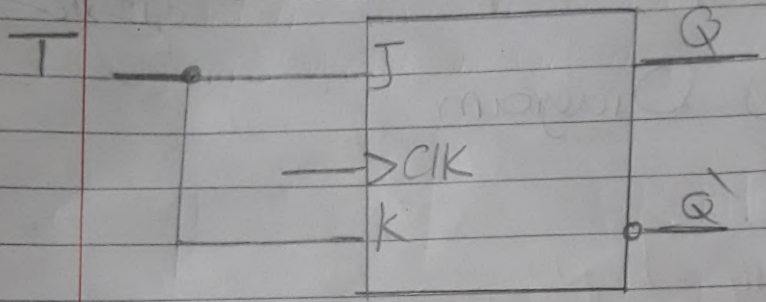
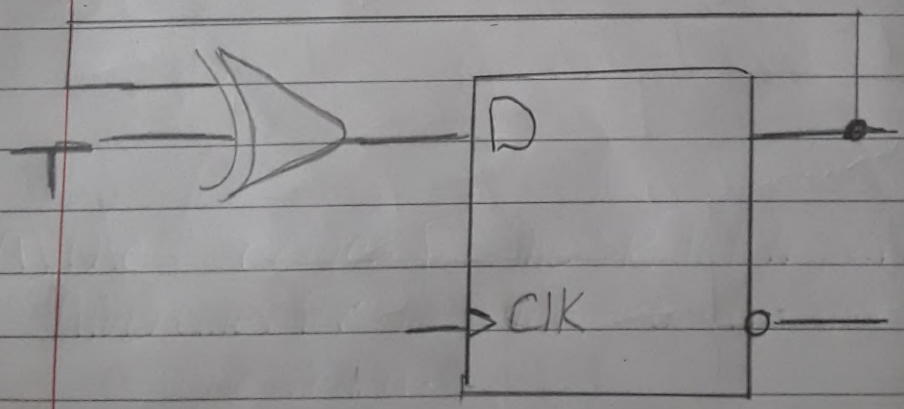
★ T- Flip Flop:

★ Created from JK or D- Flip Flop

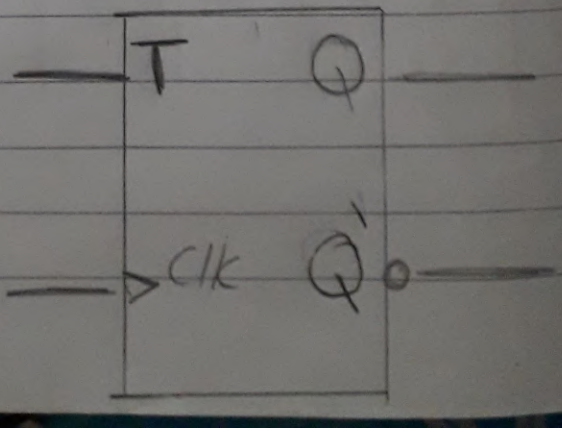
① T- Flip Flop from JK Flip Flop



② T- Flip Flop from D- Flip Flop



T- Flip Flop



★ T- Flip Flop:

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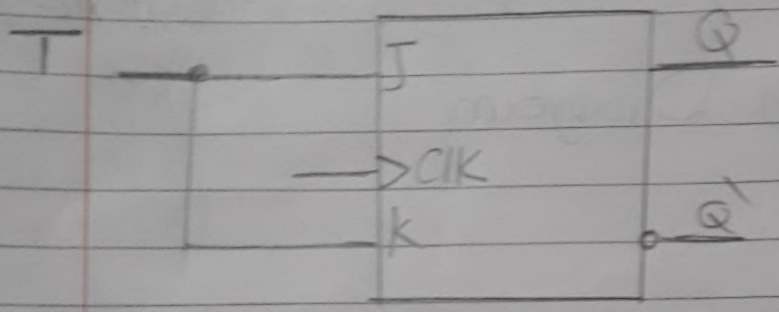
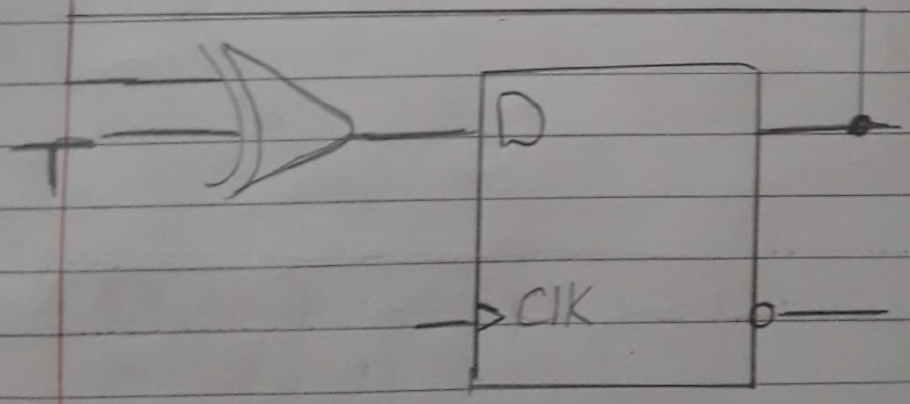
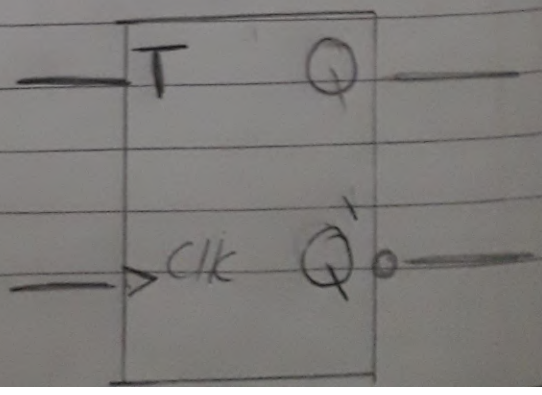
① T- Flip Flop from JK Flip Flop



② T- Flip Flop from D- Flip Flop

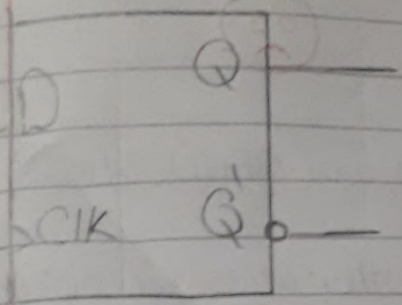


T- Flip Flop



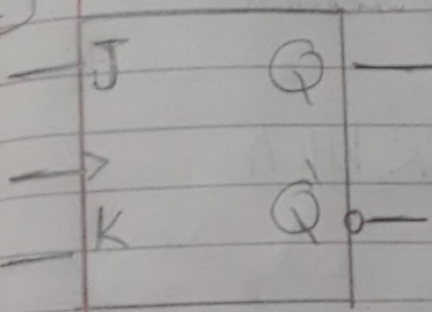
1

$Q(t+1) = D$



D	Q(t+1) (Next State)
0	0
1	1

2



J	K	Q(t+1) (Next State)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

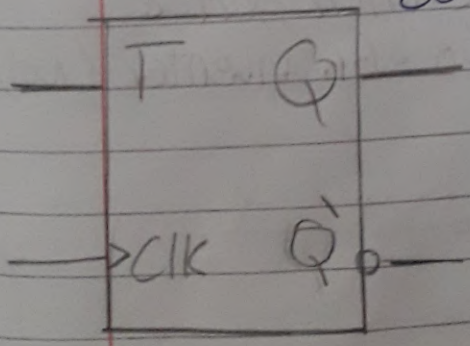
$\therefore Q(t+1) = J\,Q'(t) + K'\,Q(t)$

$J=1 \quad (1\times1) + (1\times0) = 1$ ←

$K=0$

3

$\therefore Q(t+1) = T\,Q'(t) + T'\,Q(t)$



T	Q(t+1)
0	Q(t)
1	Q'(t)

Note :- $T=1 \quad Q \rightarrow Q'$

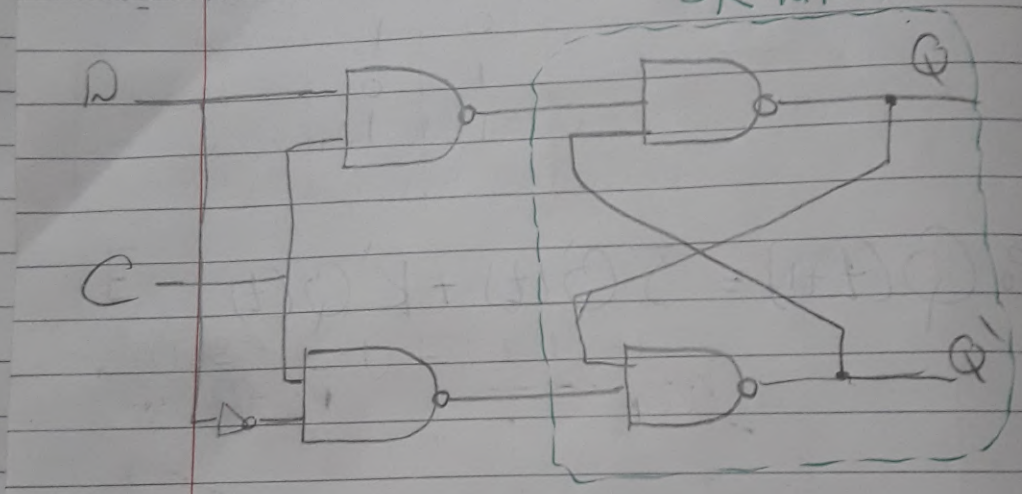
$T=0 \quad Q \rightarrow Q$

Questions:

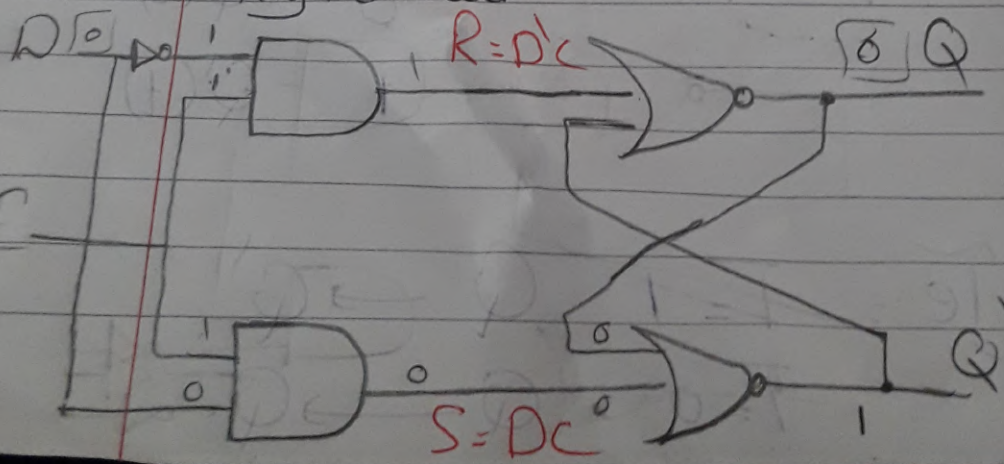
5.1 The D latch is constructed with four NAND Gates & inverter (not)

- Consider the following three other ways for obtaining a D latch & in each case Draw the logic Diagram & Verify the Circuit operation.

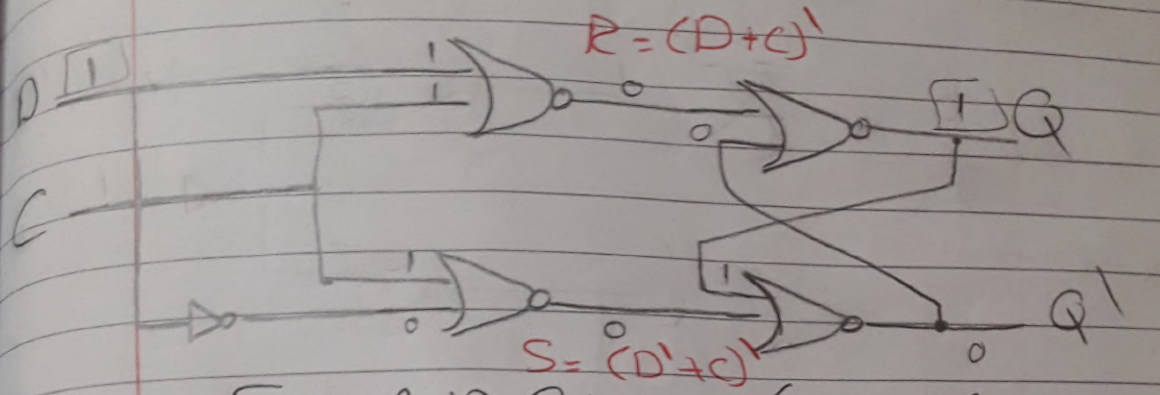
D latch



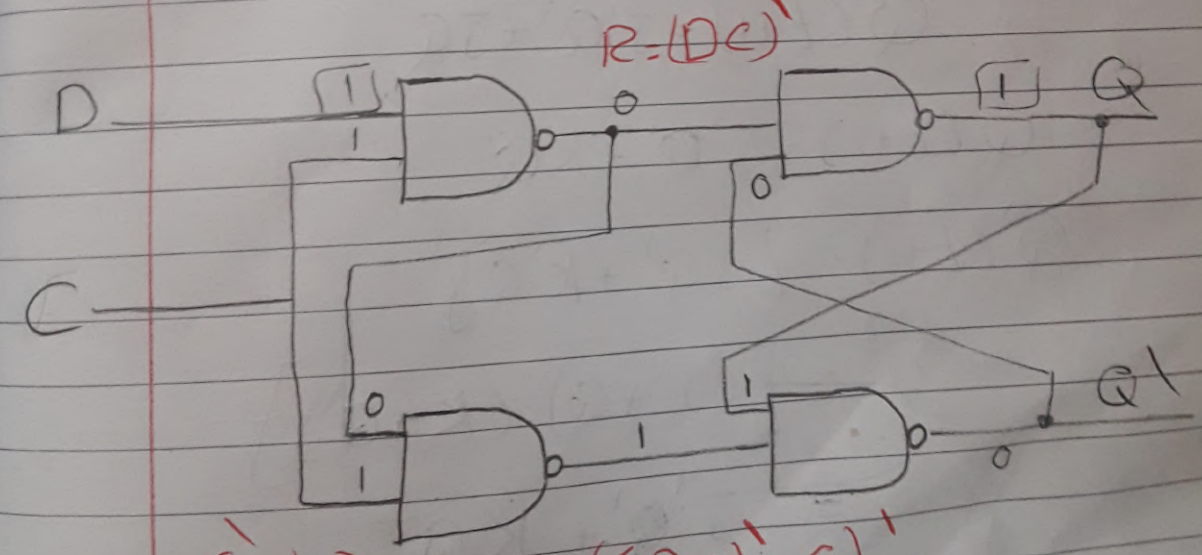
(a) Use Nor Gates For the SR latch part & AND Gates For the other Two. An inverter (not) May be needed.



(B) use NOR Gates For all Four Gates, Inventer (not) may be needed.



(C) use Four NAND Gates only (without Any inventor)
This Can Done by Connecting the output of Upper Gate (The Gate that Goes to SR latch) To The input To The lower Gates (instead of The inventer output).



$DC + C'$

$(D+C')(C+C')$

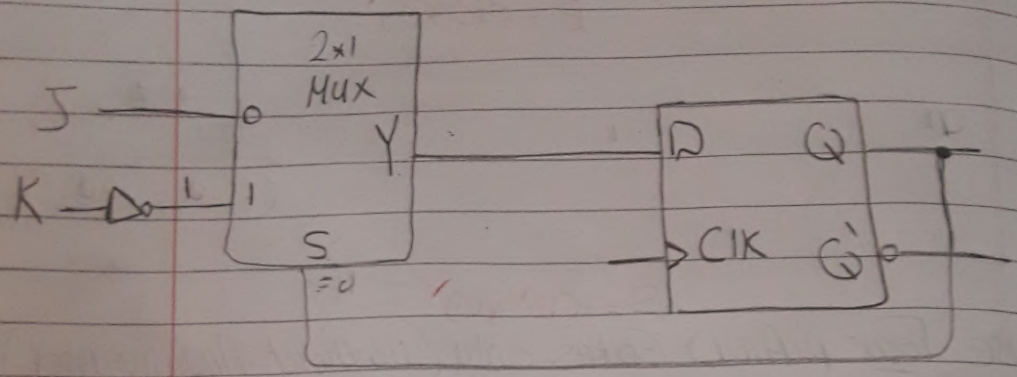
$S = ((DC)' \cdot C)'$

$= [(D'+C') \cdot C]'$

$= DC + C'$

$= D + C' = (D'C)'$

5.2 Construct JK Flip-Flop, using a D Flip Flop, a Two-to-one Multiplixer & inverter (not).



5.3 Show That The characteristic Equation For The Complement output of JK Flip Flop is

$$Q'(t+1) = J'Q' + JQ$$

$$\therefore Q(t+1) = JQ' + K'Q$$

$$Q'(t+1) = [JQ' + K'Q]'$$

$$= [(J' + Q)(K + Q')]$$

$$= J'Q' + KQ$$

5.4 A PN flipflop has four [4] operations.
- clear to 0
- no change
- Complement
- Set to 1

When input P & N are 00, 01, 10 & 11 Respectively

(a) Tabulate the characteristic Table.

P	N	Q(t+1)
0	0	0
0	1	Q(t)
1	0	Q'(t)
1	1	1

[b] Drive Characteristic Equation.

P	N	Q(t)	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1 x
1	1	1	1 x

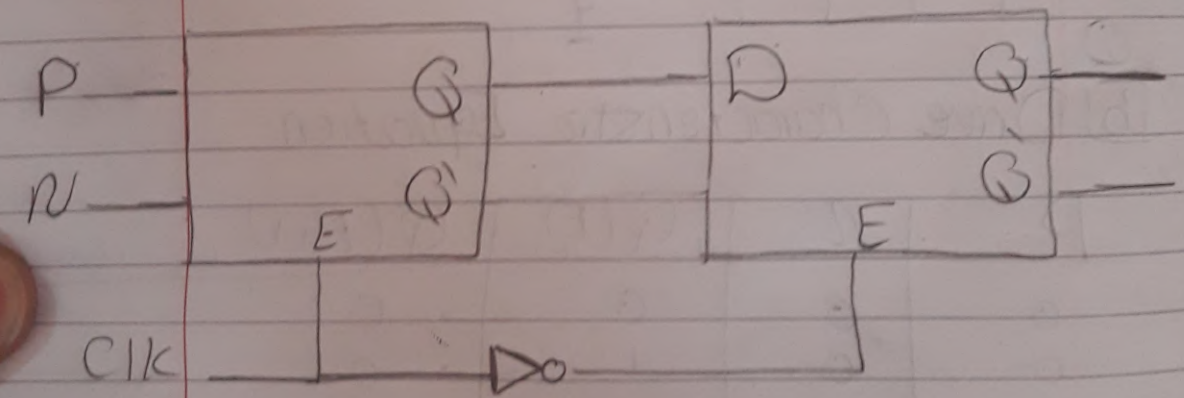
Equation:-

$$Q(t+1) = PQ' + NQ$$

(c) Tabulate the excitation table

Q(t)	Q(t+1)	P	N
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	1

(d) Show How the PN Flip-Flop Can be Converted to D-Flip Flop



5.5 Explain the Differences among a Truth table, state table, a characteristic Table, & an excitation table.

Also: Explain the Difference among a Boolean Equation, a state Equation, a characteristic Equation & Flip Flop input Equation.

[1] Truth Table.
↳ Describe Combinational Circuit

[2] State Table.
↳ Describe Sequential Circuit

[3] Characteristic Table
↳ Describe The operation of a Flip Flop

[4] Excitation Table
↳ Gives The values of Flip Flop inputs For a Given state Transition.

• The four Equations Correspond to The Algebric Expression of The four Tables.

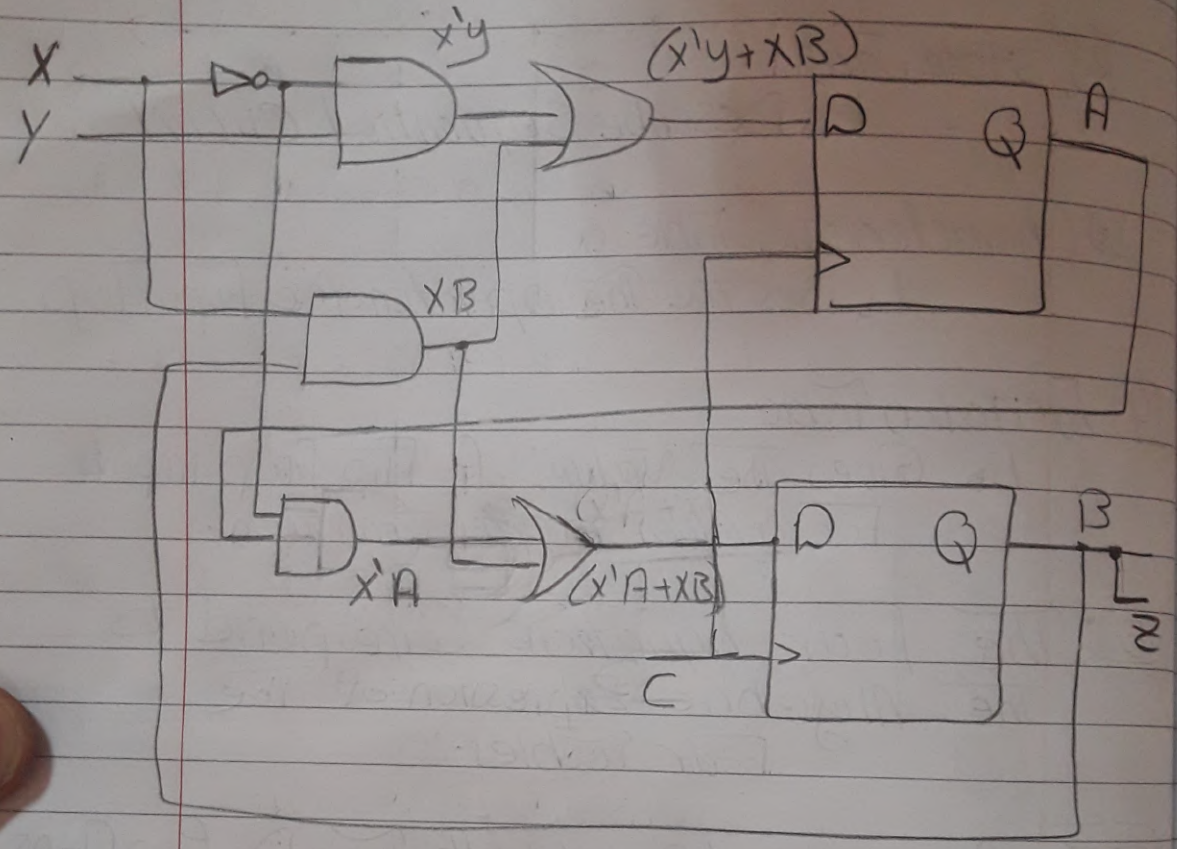
5.6 A sequential Circuit with Two D-Flip flops A and B, Two inputs x & y & one output z is specified by The Following next state & output Equation

$$A(t+1) = x'y + xB$$

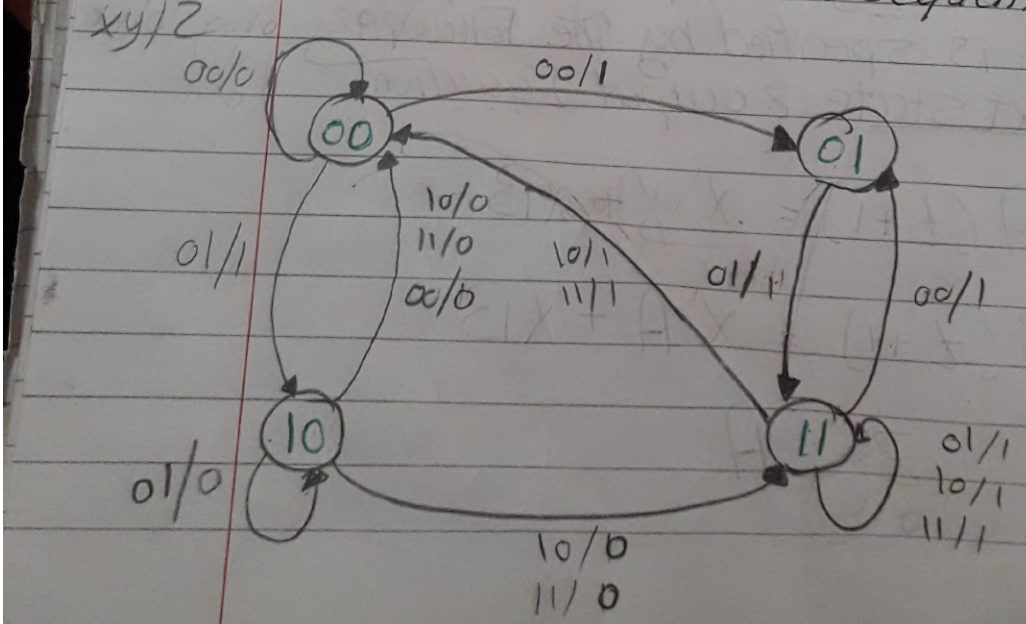
$$B(t+1) = x'A + xB$$

$$z = A$$

[a] Draw the logic Diagram of the circuit.



[b] list the state Table for the sequental circuit

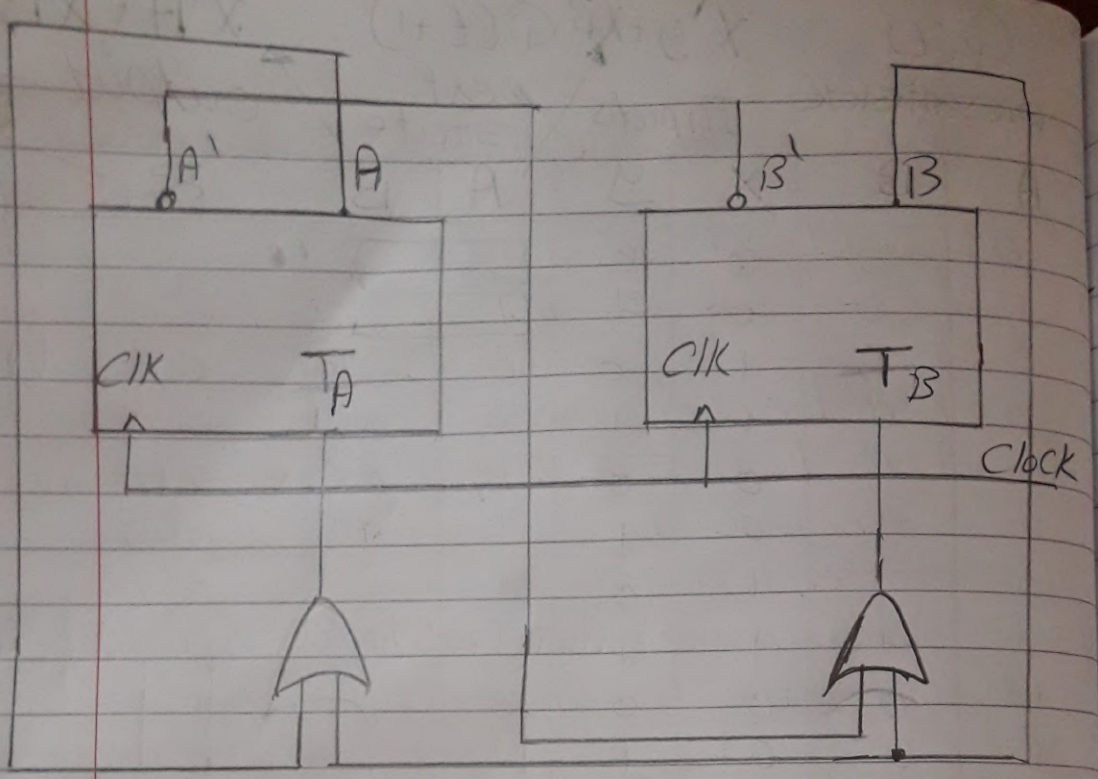


Q(t) $x'y+xB$ Q(t+1) $x'A+xB$

present state		Inputs		next state		output
A	B	x	y	A	B	z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	1	0	0
0	1	1	0	1	1	0
0	1	1	1	1	1	0
1	0	0	0	0	1	1
1	0	0	1	1	1	1
1	0	1	0	0	0	1
1	0	1	1	0	0	1
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

z = A

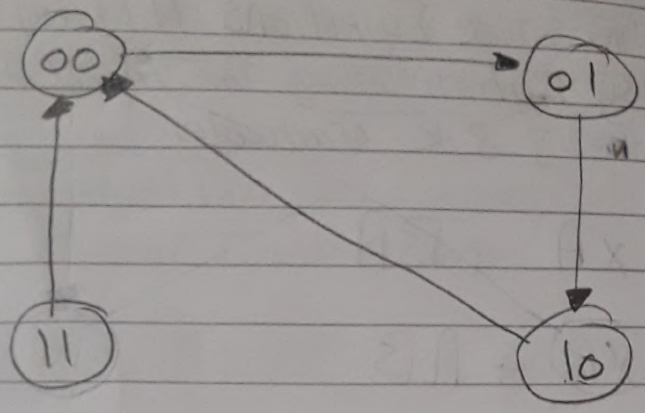
5.8 Drive the state Table & The state Diagram of the Sequential Circuit shown in Fig Explain the function that The circuit perform



* State Table

(Q(t)) present state		(Q(t+1)) Next state		Flip Flop Inputs	
A	B	A	B	T_A	T_B
0	0	0	1	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	0	1	1

$T_A = A + B$ $\quad$ $T_B = A' + B$



5.9] A sequential Circuit has Two JK Flip Flops A & B & one input X.

The Circuit is Described by the Following Flip Flop input Equations:

$$J_A = X \qquad K_A = B'$$

$$J_B = X \qquad K_B = A$$

$$\therefore A(t+1) = J_A A' + K_A' A$$

$$= XA' + (B')' A = \boxed{XA' + BA}$$

$$\therefore B(t+1) = J_B B' + K_B' B$$

$$= \boxed{XB' + AB}$$

(a) Derive the state Equations $A(t+1)$ & $B(t+1)$ By Substituting the input Equations for the J & K variables

$$A(t+1) = xA' + BA$$

$$B(t+1) = xB' + AB$$

(b) Draw the state Diagram of the circuit.

5.10 A sequential circuit has two JK Flip Flops A & B, two inputs x & y & one output z

The Flip Flop Input Equations & circuit output Equation are.

$$J_A = Bx + B'y' \qquad K_A = B'xy'$$

$$J_B = A'x \qquad K_B = A + xy'$$

$$z = Ax'y' + Bx'y'$$

(a) Draw logic Diagram of the circuit.