

Section 4

- 5-11.** Show the contents in hexadecimal of registers *PC*, *AR*, *DR*, *IR*, and *SC* of the basic computer when an ISZ indirect instruction is fetched from memory and executed. The initial content of *PC* is 7FF. The content of memory at address 7FF is EA9F. The content of memory at address A9F is 0C35. The content of memory at address C35 is FFFF. Give the answer in a table with five columns, one for each register and a row for each timing signal. Show the contents of the registers after the positive transition of each clock pulse.

Solution

5.11

	PC	AR	DR	IR	SC
Initial	7FF	—	—	—	0
T ₀	7FF	7FF	—	—	1
T ₁	800	7FF	—	EA9F	2
T ₂	800	A9F	—	EA9F	3
T ₃	800	C35	—	EA9F	4
T ₄	800	C35	FFFF	EA9F	5
T ₅	800	C35	0000	EA9F	6
T ₆	801	C35	0000	EA9F	0

- 5-12.** The content of *PC* in the basic computer is 3AF (all numbers are in hexadecimal). The content of *AC* is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F.
- What is the instruction that will be fetched and executed next?
 - Show the binary operation that will be performed in the *AC* when the instruction is executed.
- c.** Give the contents of registers *PC*, *AR*, *DR*, *AC*, and *IR* in hexadecimal and the values of *E*, *I*, and the sequence counter *SC* in binary at the end of the instruction cycle.

Solution

5.12

(a) $9 = (1001)$

$\begin{array}{c} 1 \overline{001} \\ I=1 \text{ ADD} \end{array}$
 $\text{ADD } I \text{ } 32E$

Memory

3AF	932E
32E	09AC
9AC	8B9F

AC = 7EC3

(b)

$\begin{array}{rcl} \text{AC} & = & 7EC3 \quad (\text{ADD}) \\ \text{DR} & = & \underline{8B9F} \\ & & 0A62 \end{array}$

(E=1)

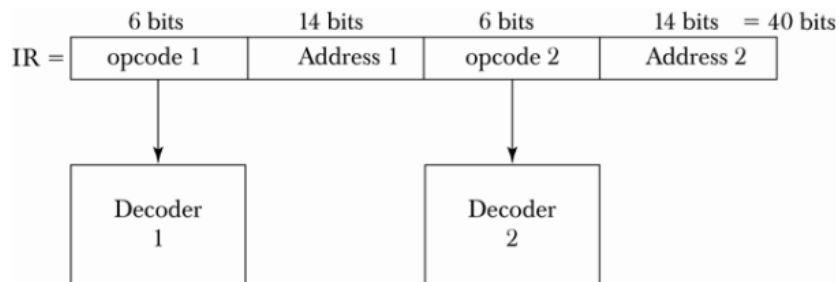
(c)

$\begin{array}{l} \text{PC} = 3AF + 1 = 3BO \\ \text{AR} = 7AC \\ \text{DR} = 8B9F \\ \text{AC} = 0A62 \end{array}$	$\begin{array}{l} \text{IR} = 932E \\ E = 1 \\ I = 1 \\ \text{SC} = 0000 \end{array}$
---	---

- 5-17.** A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit). Two instructions are packed in one memory word, and a 40-bit instruction register *IR* is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer.

Solution

5.17



1. Read 40-bit double instruction from memory to IR and then increment PC.
2. Decode opcode 1.
3. Execute instruction 1 using address 1.
4. Decode opcode 2.
5. Execute instruction 2 using address 2.
6. Go back to step 1.