Flip Flop Lecture

* **SR latch:**

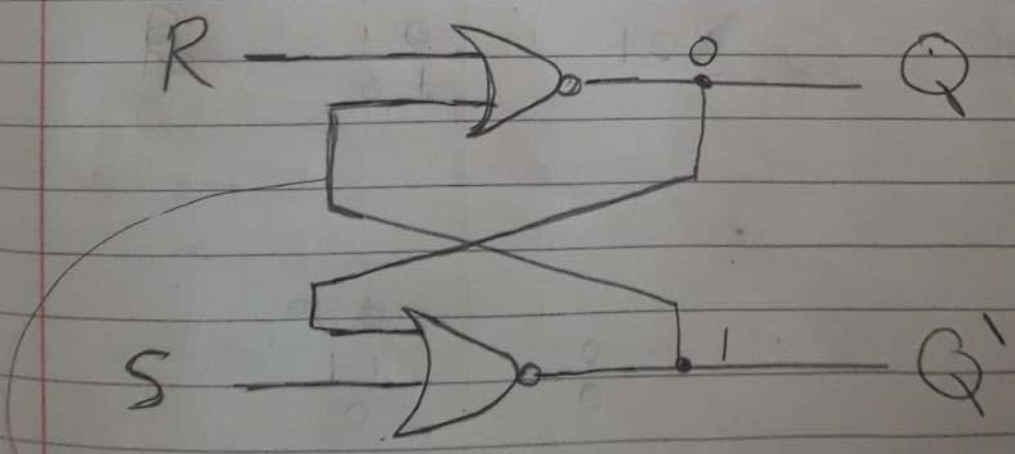
It's a Device used To Control Signals & Relies on Two only States.

S → Set

R → Reset.

* SR Can Implemented using Nor Gates OR NAND Gates.

① **NOR Gates:** SR latch



→ Feedback

R	S	$Q=(S+R)'$	$Q'=[(S+R)']'=S+R$
0	0	0	1
0	1	1	0
1	0	0	1
1	1	0	0

S	R	Q	Q'
0	0	0	1

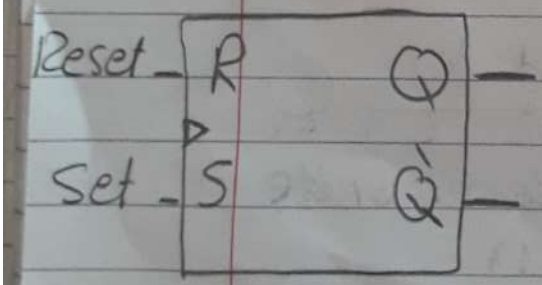
★ الحالة دى Memory state

لغتى لو جربتها مرة هتطلع الـ Result

S	R	Q	Q'
0	0	0	1

ولو جربتها تانى هتطلع

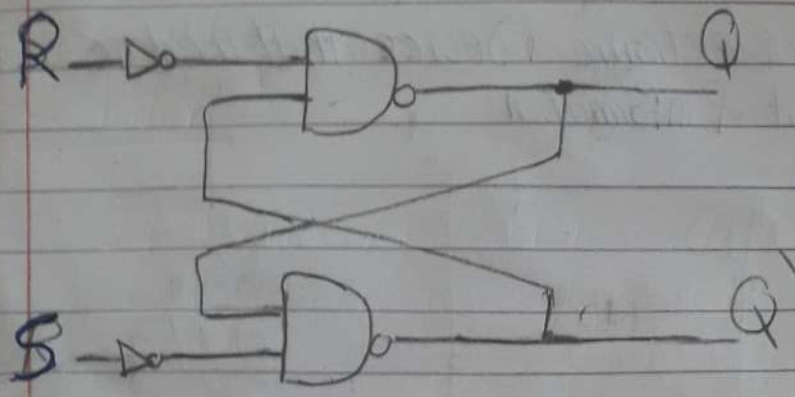
نفس الـ Result



R	S	Q
0	0	0 (Hold)
0	1	1 → Set state
1	0	0 → Reset state
1	1	Disallow

لأنه الـ Q و Q' هيكونوا الناتج ليهم 0

* NAND Gates — $\overline{SR}$ latch. *



R	S	R'	S'	Q = (S·R)'	Q' = S·R
0	0	1	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	1	0	0	1	1

R'	S'	Q
0	0	0 → Hold.
0	1	1 → Set state
1	0	0 → Reset state
1	1	Disallow.

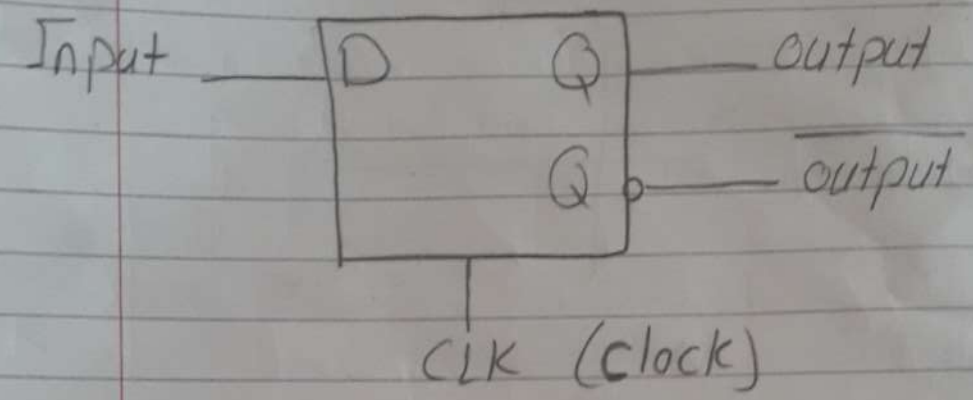
NOTE

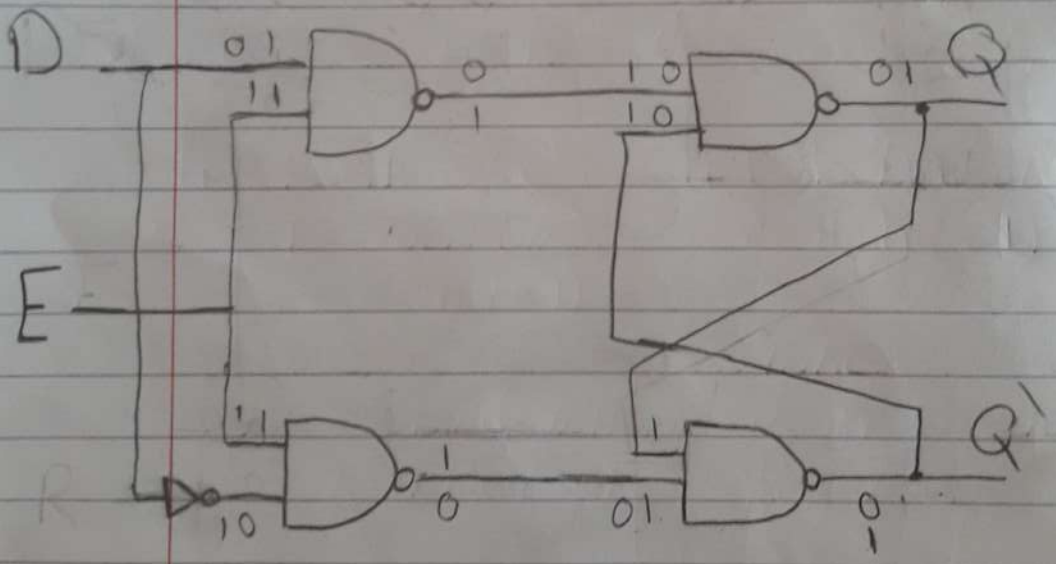
When Q = 1 Set state

Q = 0 Reset state.

D- latch

- It's electronic Device that used to store one Bit of information.





Note

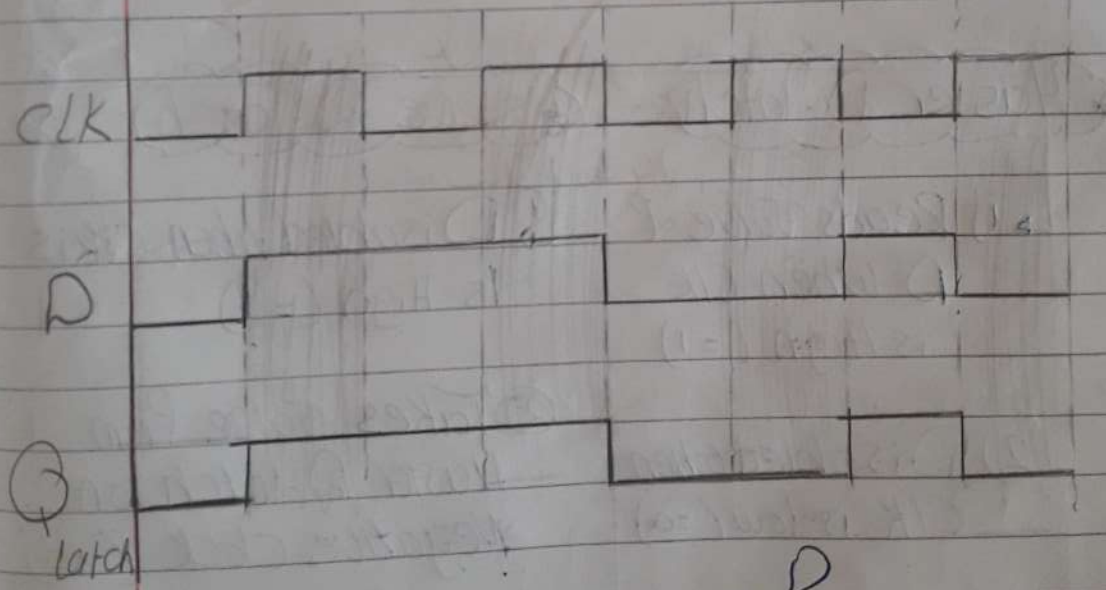
Enable للتحكم في عملية التخزين
لأنه لو E=1 معناها إنه فتح عملية
تخزين لقيم الفيجه D
إذا كانت E=0 معناها مفيش تغير لأنه مفيش
عملية تخزين لقيم زهلة.

X ⟶ mean Don't Care Value.

E	D	Q	Q'
0	X	Memory state - (E=0 لأن الخرج ثابت)	
1	1	1	0 ⟶ (Q=1 ⟶ Set)
1	0	0	1 ⟶ (Q=0 ⟶ Reset)

* Timing Diagram:

Note: In D-latch Data is stored while Clock is High.

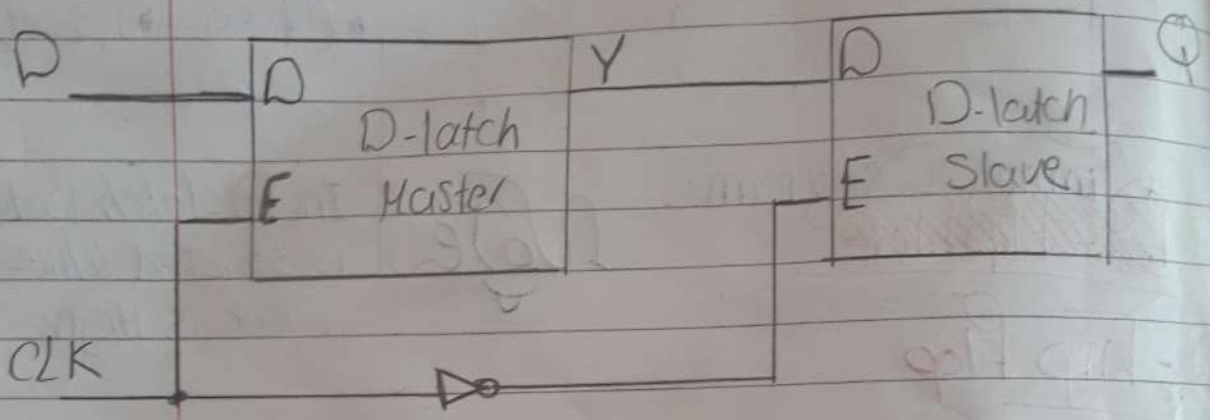


Clock High: Input (Data) passes To output (Q)

Clock Low: latch Holds its output (Q).

★ D-Flip Flop

* D-Flip Flop Construct From Two D-latches:



* Master D-latch

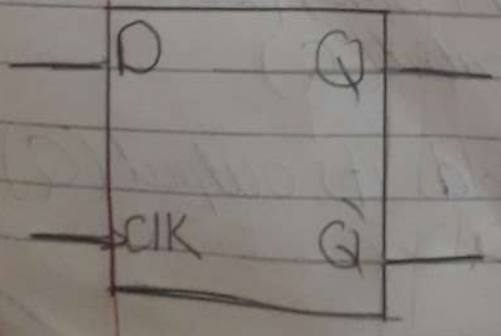
1) Reads value of D when CLK is High (=1)

2) Disabled when CLK is low (=0)

* slave D-latch

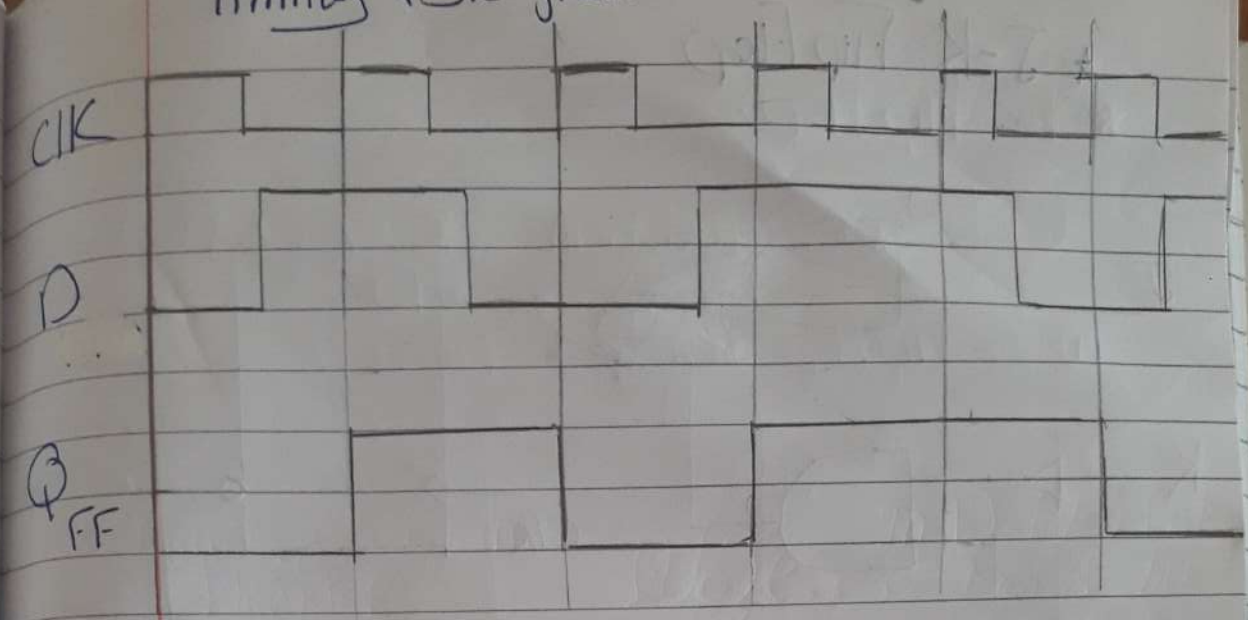
① Disabled when CLK is is High (=1)

② Takes value from Master D-latch on Negative clock (=0)



D	CLK	Q
0	↑ 1	0
1	↑ 1	1

Timing Diagram.



★ J-K Flip-Flop

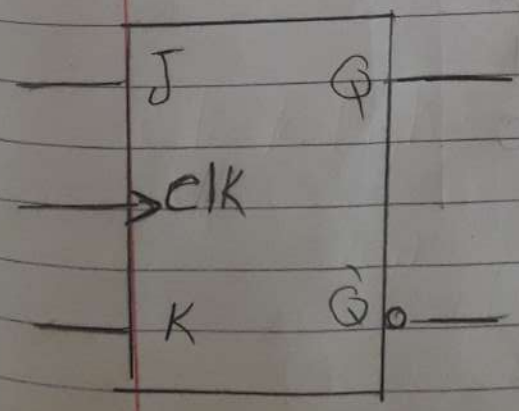
① Construct from D. Flip Flop.

②

J → Reset state

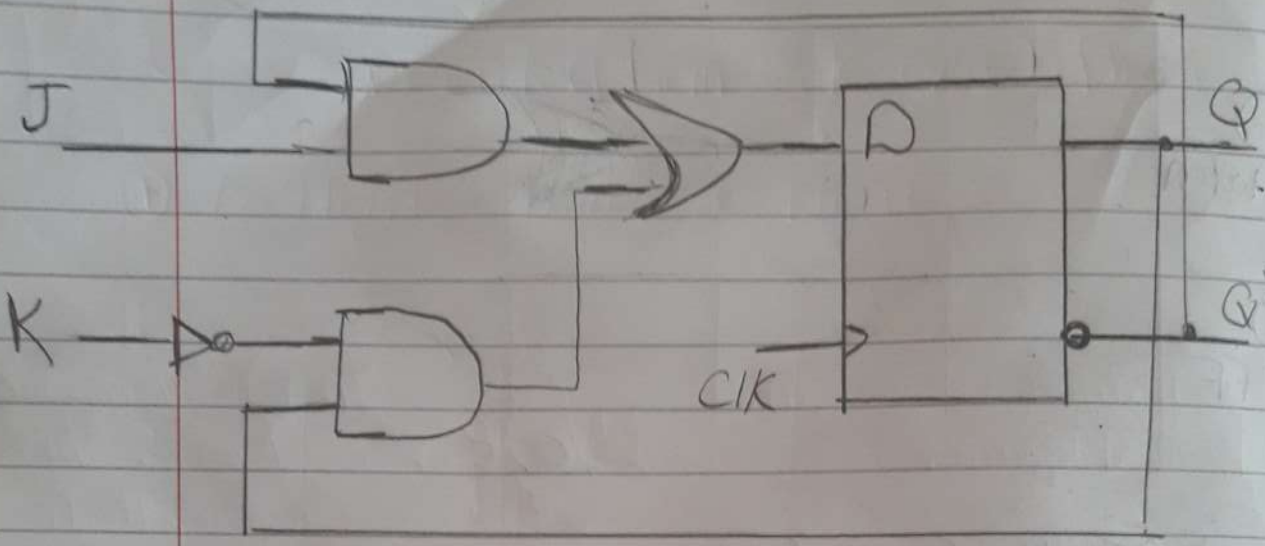
K → Set state.

③ When J=K=1 ⟶ Invert Q'



J	K	Q	Q'
0	0	Q_0	Q_0'
0	1	0	1
1	0	1	0
1	1	Q_0'	Q_0

★ J-K Flip Flop



J	K	CLK	Q	Q'
0	0		Q_0	Q'_0
0	1		0	1
1	0		1	0
1	1		Q'_0	Q_0

في الحالتين دول متوقف على D. FlipFlop

★ D. Flip Flop

D	CLK	Q	Q'
0	↑ = 1	0	1
1	↑ = 1	1	0

ReSet

Preset

J	K	Clk	Q	
0	0	↑	Q_0 (No change)	لا يتم تغيير الاشارة
1	0	↑	1	
0	1	↑	0	
1	1	↑	$\bar{Q_0}$ (Toggle)	تعاكس الاشارة

* Timing Diagram