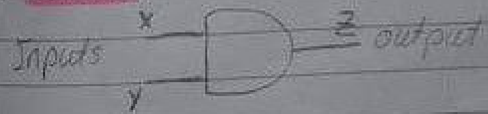
Logic Gates

* Definition!
- logic Gates are electronics Circuit that operate one or more inputs to produce one output The output is simple boolean operation of its ~~ou~~ inputs & any Boolean Function can Represent by logic Gates.

* logic Gates:

1) And	1) Gate shap
2) OR	2) Truth Table
3) Not	3) Expression
4) Nand	4) Expression Diagram
5) NoR	5) Timing Diagram
6) Xor	
7) XNor	

* AND

[1] 

[2] Truth Table:

عدد الاحتمالات :

2^n ← عدد الـ Inputs

$2^2 = 4$

X	y	X • y
0	0	0
0	1	0
1	0	0
1	1	1

★ NOT Gate Truth Table.

X	$Y = X'$
0	1
1	0

★ NOT Representation using NAND.

X	X	$Y = (X.X)'$
0	0	1
1	1	0

=

X	$Y = X'$
0	1
1	0

2) AND

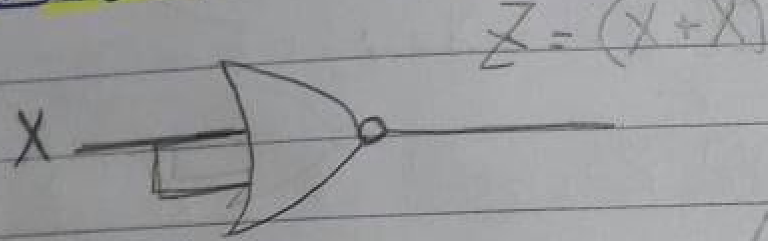
1) AND Truth Table.

X	X	$Z = (X.Y)$
0	0	0
0	1	0
1	0	0
1	1	1

'1'

* NOR

1 NOT



NOT using NOR

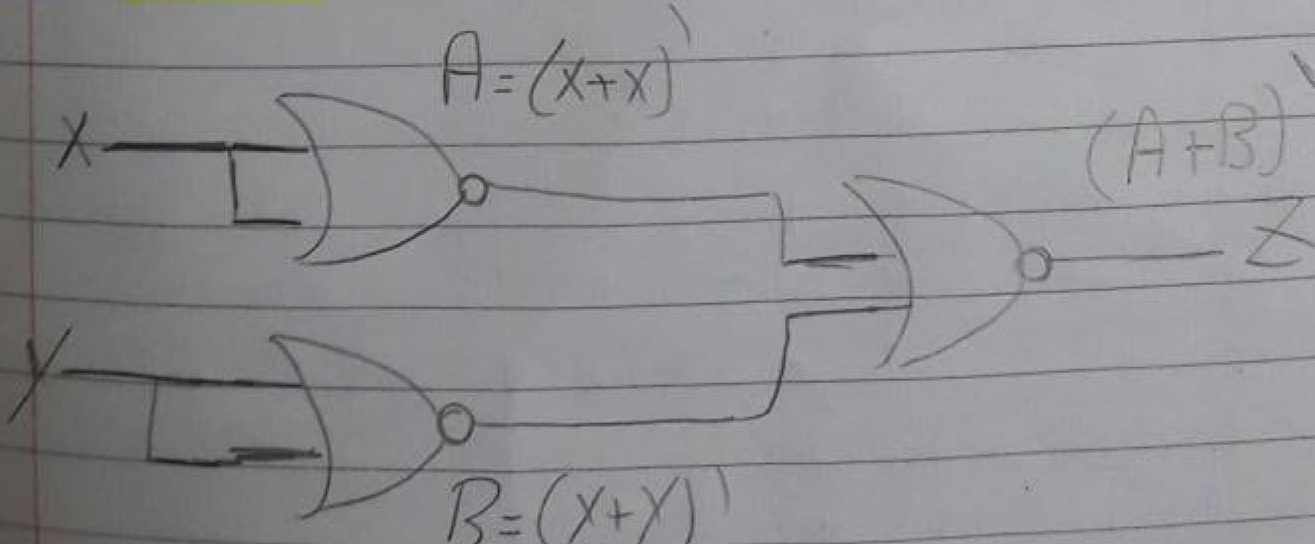
X	$Z = (X+X)'$
0	$(0+0)' = 1$
1	$(1+1)' = 0$

=

NOT

X	$Z = X'$
0	1
1	0

2 AND



AND using Nor

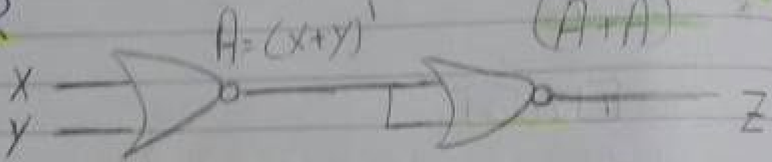
X	Y	A = (X+X)'	B = (Y+Y)'	Z = (A+B)'
0	0	(0+0)' = 1	(0+0)' = 1	(1+1)' = 0
0	1	(0+0)' = 1	(1+1)' = 0	(1+0)' = 0
1	0	(1+1)' = 0	(0+0)' = 1	(0+1)' = 0
1	1	(1+1)' = 0	(1+1)' = 0	(0+0)' = 1

=

AND

X	Y	Z=
0	0	0
0	1	0
1	0	0
1	1	1

3) OR



OR using Nor.

X	Y	A = (X+Y)'	Z = (A+A)'
0	0	(0+0)' = 1	(1+1)' = 0
0	1	(0+1)' = 0	(0+0)' = 1
1	0	(1+0)' = 0	(0+0)' = 1
1	1	(1+1)' = 0	(0+0)' = 1

=

OR

X	Y	Z = X+Y
0	0	0
0	1	1
1	0	1
1	1	1

1

★ NOT Gate Truth Table.

X	Y = X'
0	1
1	0

★ NOT Representation using NAND.

X	X	Y = (X.X)'
0	0	1
1	1	0

=

X	Y = X'
0	1
1	0

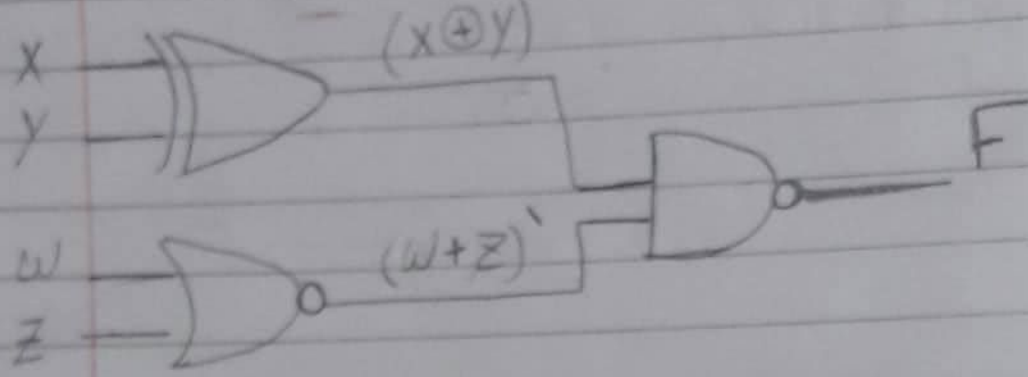
2) AND

1) AND Truth Table.

X	Y	Z = (X.Y)
0	0	0
0	1	0
1	0	0
1	1	1

'4'

[2] Find The Expression & Truth Table For The Circuit in The Fig 1



1) Expression:

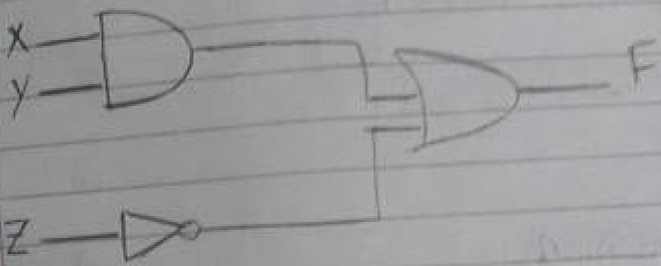
$$F = \left((X \oplus Y) \cdot (W+Z)'\right)'$$

2) Truth Table:

X	Y	W	Z	$(X \oplus Y)$	$(W+Z)'$	$F = ((X \oplus Y) \cdot (W+Z)')'$
0	0	0	0	0	1	1
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	1	0
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	1	1	0
1	0	0	1	1	0	1
1	0	1	0	1	0	1
1	0	1	1	1	0	1

Examples:

[1] Find The The Expression & The Truth Table For The Circuits in The Fig



[1] Expression:

$$F = (XY) + Z'$$

*عدد الاحتمالات

2^n ← عدد الـ Inputs

$n = 3$

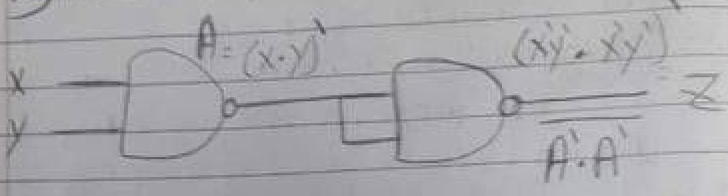
$= 2^3 = \underline{8}$

$(0 \to 7)$

[2] Truth Table:

X	y	Z	X·Y	Z'	F = (XY) + Z'
0	0	0	0	1	1
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	0	1	1
1	0	1	0	0	0
1	1	0	1	1	1
1	1	1	1	0	1

2) AND Representation using NAND.



x	y	A = (x.y)'	Z = $\overline{A'.A'}$
0	0	(0.0)' = 1	(1.1)' = 0
0	1	(0.1)' = 1	(1.1)' = 0
1	0	(1.0)' = 1	(1.1)' = 0
1	1	(1.1)' = 0	(0.0)' = 1

=

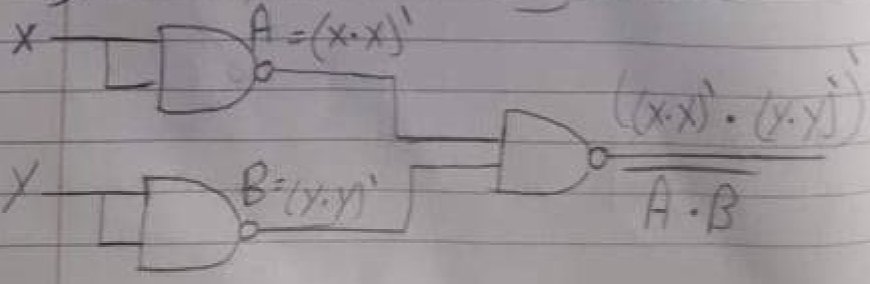
x	y	Z = x.y
0	0	0
0	1	0
1	0	0
1	1	1

$\boxed{3}$ OR

1) OR Truth Table:

x	y	Z = x+y
0	0	0
0	1	1
1	0	1
1	1	1

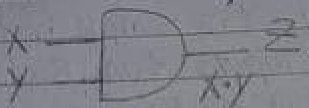
2) OR Representation using NAND



[3] Expression:

$X \cdot y$ OR $X \wedge y$ OR Xy

[4] $X \cdot y = Z$ $\quad$ $X \wedge y = Z$

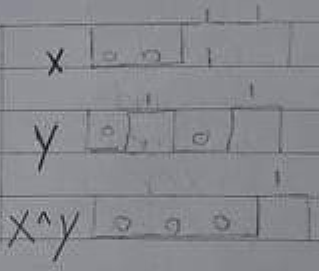


[5] Timing Diagram:

لرسم Timing Diagram لازم

Truth Table:

X	Y	X^y
0	0	0
0	1	0
1	0	0
1	1	1



* OR

[1]

[2] Truth Table:

$2^2 = 4$

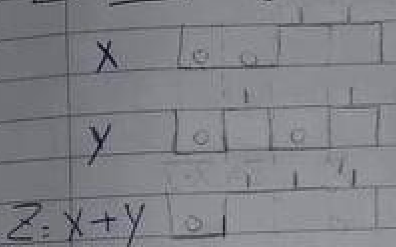
X	y	Z = X + y
0	0	0
0	1	1
1	0	1
1	1	1

3 Expression:

$x + y$ OR $x \vee y$

4 $x + y = z$ $\quad x \vee y = z$,

5 Timing Diagram:



x	y	Z = x+y
0	0	0
0	1	1
1	0	1
1	1	1

* NOT

1 

2 Truth Table:

عدد الاحتمالات

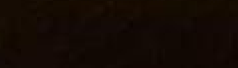
$2^n = 2^1 = 2$

x	y = x'
0	1
1	0

3 Expression:

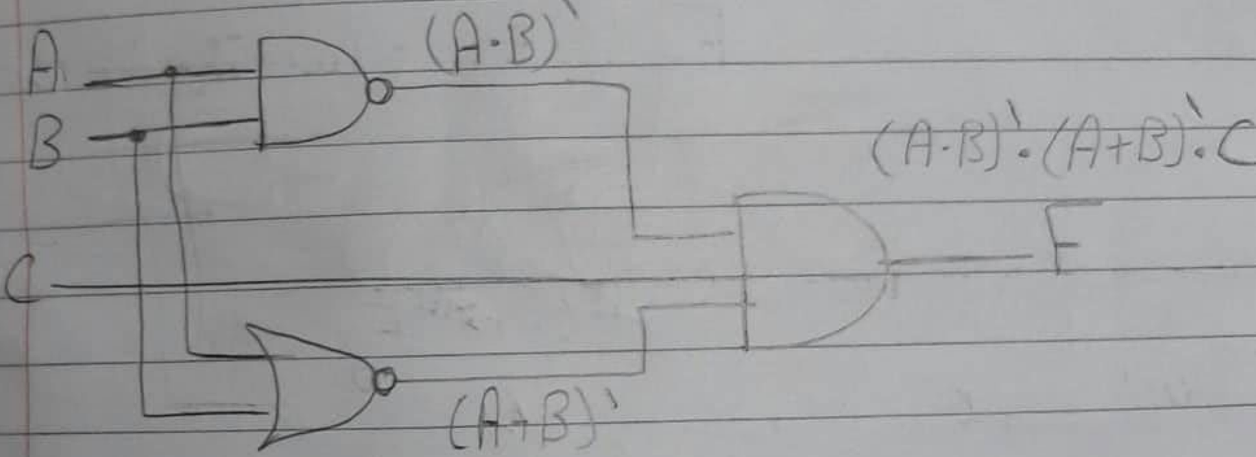
x' OR $\overline{x}$

4 $y = x'$ $\quad y = \overline{x}$



X	Y	W	Z	$(X \oplus Y)$	$(W+Z)'$	$F = ((X \oplus Y) \cdot (W+Z)')'$
1	0	0	0	1	1	0
1	0	0	1	1	0	1
1	0	1	0	1	0	1
1	0	1	1	1	0	1

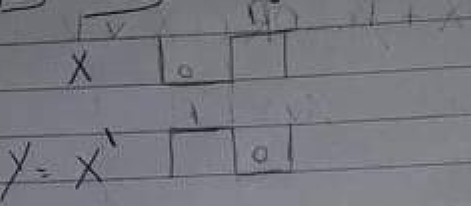
[3] Find The Expression & The Truth Table For The Circuit in The Fig



$$F = [(AB)' \cdot (A+B)' \cdot C]$$

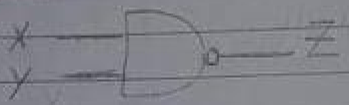
A	B	C	$(AB)'$	$(A+B)'$	$F = [(AB)'(A+B)'C]$
0	0	0	1	1	0
0	0	1	1	1	1
0	1	0	1	0	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	0	0

[5] Timing Diagram.



* NAND

[1]



[2] Truth Table.

$2^2 = 4$

* بتعكس عمل ال AND بس
بتعمل ال Not لل
Result (output).

X	Y	$Z = \overline{X \cdot Y}$
0	0	1
0	1	1
1	0	1
1	1	0

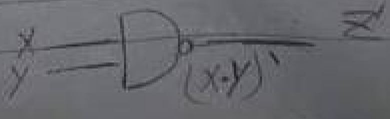
1110

بتسمى ال NAND Gate إنها بتكون
universal Gate
يعني بنقدر نمثل بيها ال AND، OR، Not

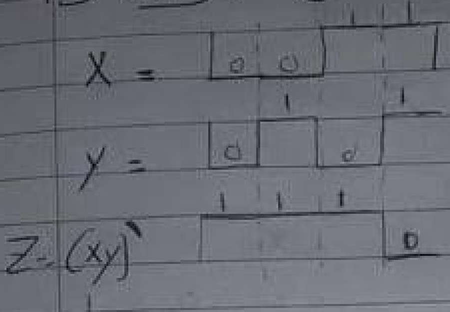
[3] Expression.

$Z = (X \cdot Y)'$ $\quad Z = (XY)'$ $\quad Z = (X \wedge Y)'$

[4]



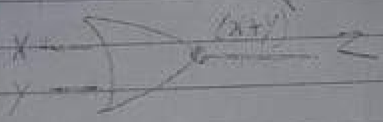
5) Timing Diagram:



X	Y	Z = (xy)`
0	0	1
0	1	1
1	0	1
1	1	0

* NOR

1)



2) Truth Table:

★ نفس عمل ال OR بس
عكس ال Not
output.

X	Y	Z = (X+Y)`
0	0	1
0	1	0
1	0	0
1	1	0

★ NOR Gate تسمى Universal Gate.

3) Expression:

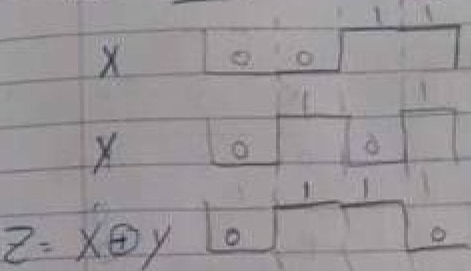
$Z = \overline{(X+Y)}$ $\quad Z = (X+Y)'$

$Z = (X \vee Y)'$

[4] Expression → Diagram

$Z = X \oplus Y$

[5] Timing ~~Table~~ Diagram



X	Y	$Z = X \oplus Y$
0	0	0
0	1	1
1	0	1
1	1	0

* XNOR

[1]

[2] Truth Table

نفس جدول ال Xor بس
نعمل ال Not الـ
Result (output)

X	Y	$(X \oplus Y)'$
0	0	1
0	1	0
1	0	0
1	1	1

[3] Expression

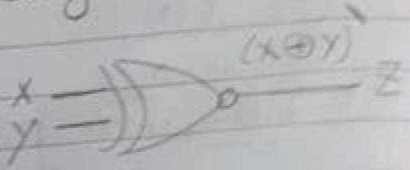
$Z = (X \oplus Y)'$ OR $\overline{(X \oplus Y)}$

$Z = XY + X'Y'$

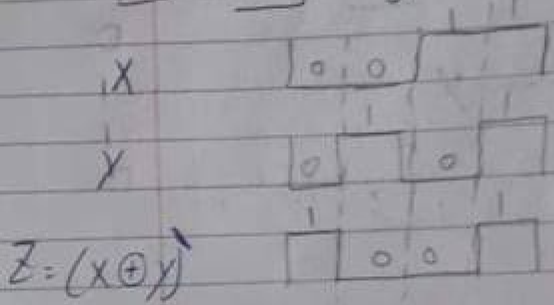
4 Expression → Diagram:

$Z = (x \oplus y)'$

OR $Z = xy + x'y'$



5 Timing Diagram:



X	Y	Z=(x⊕
0	0	1
0	1	0
1	0	0
1	1	1

★ **Universal Gates**

1) NAND
2) NOR

يعني الـ NAND / Nor أقدر أمثل بيهم Not & OR & AND.

★ **NAND**

1 Not

إزاي هنقدر نمثل الـ Not Gates من الـ NAND Gate

OR (using NAND)

X	Y	$A = (X \cdot X)'$	$B = (Y \cdot Y)'$	$Z = (A \cdot B)'$
0	0	$(0 \cdot 0)' = 1$	$(0 \cdot 0)' = 1$	$(1 \cdot 1)' = 0$
0	1	$(0 \cdot 0)' = 1$	$(1 \cdot 1)' = 0$	$(1 \cdot 0)' = 1$
1	0	$(1 \cdot 1)' = 0$	$(0 \cdot 0)' = 1$	$(0 \cdot 1)' = 1$
1	1	$(1 \cdot 1)' = 0$	$(1 \cdot 1)' = 0$	$(0 \cdot 0)' = 1$

=

OR

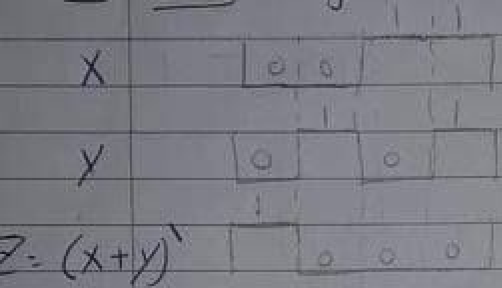
X	Y	$Z = X \vee Y$
0	0	0
0	1	1
1	0	1
1	1	1

* NOR

1 NOT

4 Expression → Diagram

5 Timing Diagram



X	Y	Z = (X+Y)'
0	0	1
0	1	0
1	0	0
1	1	0

★ XOR

1 Ⅰ

2 Truth Table

$2^2 = 4$ عدد الحالات

X	Y	Z = X ⊕ Y
0	0	0
0	1	1
1	0	1
1	1	0

3 Expression

$Z = X \oplus Y$ OR $Z = XY' + X'Y$