

## **FINAL REPORT**

### **Development of Electrical Power Subsystem's Control Board for a Cubesat 1U**

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# **Scope**

This report gives a description of the EPS and Panel boards belonging to the electrical power subsystem (EPS), its function and performance, in support of the preliminary design review of EPS for 1U Cubesat. The technical data of the batteries and solar array provided in this document are to set the maximum operating points of the EPS and Panel board as a multi-mission configuration for Cubesat 1U, and with small changes for Cubesat 3U.

## **Applicable Documents**

- Cal Poly: Cubesat Design Specification
  - Revision 13
- CubeSat Subsystem Interface Definition. UNISEC
  - Version 0.4 - 21.07.2015
- ESA: ECSS-E-ST-20C - Space engineering: Electrical and electronic
- NASA: GSFC-STD-7000 - General Environmental Verification Standard (GEVS)
  - April 2005
- IPC
  - IPC J-STD-001ES
  - IPC-A-610E
- NASA-STD 7002A - Payload Test Requirements
- NASA-STD-7001A - Payload Vibroacoustic Test Criteria
- NASA-HDBK-7004B - Force Limited Vibration Testing
- NASA-STD-5002 - Load Analyses of Spacecraft and Payloads
- Delta II - Payload Planners Guide
  - December 2006, 06H0214

- Space Laucher System DNEPR - User's Guide
  - Issue 2, NOv. 2001
- Vega User's Manual
  - Issue 3, Rev.0, March 2006
- Polar Satellite Launch Vehicle - User's Manual
  - Issue 4, March 2005

## General Description

The control boards for the electrical power subsystem consists of all necessary hardware to store, condition and distribute the electrical power required by all on-board equipments of the nanosatellite during all phases of the spacecraft mission. This design is divided in two main cards, a EPS card and a Panel card.

The electrical power subsystem (EPS), is based on a sunlight regulated bus with a double supply of 5V/3.3V plus a battery bus in the range 6.2V~8.26V, being this within the commercial ranges of the available systems in the market.

The EPS control board has a configuration comprising of:

- Power Condition Converter (PCC) of 5V in a hot redundant mode configuration of 2:1
- Power Condition Converter (PCC) of 3.3V in a hot redundant mode configuration of 2:1
- Ultra small and low-power consumption microcontroller to performance analog-to-digital conversion, I<sup>2</sup>C master/slave operations
- Load switch to connect/disconnect the battery bus and grounds
- Current limit switches to supervise battery bus
- Interface of 50-pin connector (Right Angle Type of 25-pin in two rows) following the CubeSat Subsystem Interface Definition of UNISEC.
- 2-to-1 I<sup>2</sup>C-bus master selector.

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- Bus Capacitance

The Panel board board has a configuration comprising of:

- Synchronous switch-mode battery charge regulator (BCR) for solar power with maximum power point tracking (MPPT).
- General purpose Input/Output (GPIO) I<sup>2</sup>C device to enable/disable the battery charger.
- Quad I<sup>2</sup>C Voltage, Current and Temperature Monitor to monitor the solar array.
- Ideal diode
- Interface of 12-pin connector following the CubeSat Subsystem Interface Definition of UNISEC.

The power supply is received from two (02) small solar arrays incorporated into the "unused " panels by the payload. The energy of the solar arrays is transmitted into the nanosat via connection wires. The output of the solar array is passed through a battery charger with maximum power point tracker (MPPT) capable to operate within the range of 3.5V~6V. The output of the battery charger is configured to operate with two (02) Li-Ion batteries in series, providing an output within the range of 6.2V~8.26V. Using a common interface, the power output coming from the BCR is delivered from the Panel board to EPS board through a backplane of 50-pin connectors. The power received from the Panel board is passed through step down converters employing a Buck configuration for the 5V/3.3V buses.

During the launch the batteries are fully charged but disconnected, according to the " Specification Cubesat Desgin " standard. During periods of eclipse power is provided by 02 -cell Lithium- Ion.

The EPS and Panel boards provides the following features :

- Power bus that allows on-board equipment be used with high efficiency and low mass inverters, achieving a high power / mass ratio at the system level.

- Provides safety and reliability for the satellite due to is tested according to degradation and cases of major faults with low occurrence (high impact/low occurrence).
- Not present single point failures that made it impossible to meet the load requirements.
- The design of the batteries has an arrangement of 02 cells.
- Enough telemetry to allow proper assessment of the status of EPS, health data and the satellite operation to handle safely during all phases of the mission.
- In normal operation, EPS can operate autonomously without the need for telecommands sent from the ground control station.

## Main Technical Features

### **Life**

Length of Service: 06 months

### **Reliability**

0.xxx (in launch and orbit transfer, 40h)

0.xxx (in orbit test 120h)

0.xxx (in orbit to 06 months)

### **LEO Lighting Conditions**

Time of maximum eclipse: 40 min

Maximum angle of incidence of the sun: 90.0 °

Targeting Accuracy of solar panels to the sun: <4 °

## Absolute Maximum Ratings <sup>(1) (2)</sup>

		BCR	Value	Unit
Input Voltage	SA +X, -X	BCR A	10	V
	SA +Y, -Y	BCR B	10	V
	SA +Z, -Z	BCR C	10	V
	Battery		8.3	V
	5V Bus		5.05	V
	3.3V Bus		3.33	V
		Notes	Value	Unit
Input Current	SA +X, -X	@6V	750	mA
	SA +Y, -Y	@6V	750	mA
	SA +Z, -Z	@6V	750	mA
		Notes	Value	Unit
Charge Limits	Voltage	max	8.4	V
	Current	max	1.25	A
	Current Rate	max	C	Fraction of Capacity
		Notes	Value	Unit
Discharge Limits	Voltage	min	6.0	V
	Current	max	1.25	A
	Current Rate	max	C	Fraction of Capacity
		Notes	Value	Unit
Output Current	Battery Bus	@8.26V	6	A
	5V Bus	@5V	4	A
	3.3V Bus	@3.3V	4	A
			Value	Unit
Operating Temperature			-40 to 85	°C
Storage Temperature			-50 to 100	°C
Vacuum			TBC	
Radiation Tolerance			TBC	
Shock			TBC	

Table 1: Absolute Maximum Ratings

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground pin.

# Recommended Operating Conditions

Description	Notes	Min	Nominal	Max	Unit
<b>BCR</b>					
Input Voltage		3.65	--	8	V
Output Voltage		6.2	--	8.26	V
Output Current		0	--	0.5	A
Operating Frequency		510	600	690	kHz
Efficiency	@8.26V Output, Full Load	89.5%	90.00%	90.5%	
<b>Battery Charge Conditions</b>					
EoC Voltage		8.22	8.26	8.30	V
Charge Current	Recommended maximum C/2	--	0.65	--	A
<b>Battery Discharge Conditions</b>					
Full Discharge Voltage		6.16	6.2	6.24	V
Discharge Current	Recommended max C/2	--	--	0.625	A
<b>Battery Capacity</b>					
	@discharge rate C/5, 20°C		1.276		Ah
<b>Unregulated Battery Bus</b>					
Output Voltage		6.2	--	8.26	V
Output Current		--	--	4	A
Efficiency	@8.26V input, Full Load	98.5%	99%	99.5%	
<b>5V Bus</b>					
Output Voltage		4.95	5.00	5.05	V
Output Current		--	--	2	A
Operating Frequency			500		kHz
Efficiency	@5V input, Half Load	--	94.5%	--	
<b>3.3V Bus</b>					
Output Voltage		3.27	3.30	3.33	V
Output Current		--	--	2	A
Operating Frequency		--	500	--	kHz
Efficiency	@3.3V input, Half Load	--	92.5%	--	
<b>Communications</b>					
Protocol		--	I <sup>2</sup> C	--	
Transmission speed		--	100	400	Kbps

Table 2: Recommended Operating Conditions

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# **Configuration of the Electrical Power Subsystem (EPS)**

## **Configuration**

The configuration selected for this design comprises of two boards: a Panel Board and a Subsystem board. This setup allows a less dense Subsystem Board due to the battery charge regulator (BCR) is allocated in the Panel Board, and also the telemetry in the Panel Board is transmitted using I<sup>2</sup>C protocol to the Subsystem Board, deriving in an ADC with less channels.

The electrical power system (EPS) is based on the CubeSat Subsystem Interface Definition - CSID (Proposal) of UNISEC [1], which employs redundant power paths for the storage, generation and conversion. The architecture selected uses a maximum power point tracking function to operate as a sun regulated topology. The power generation block of the EPS is located on the satellite side panels which are connected to the panel bus in order to supply the unregulated battery bus. The power storage block is located on a dedicated subsystem attached to the subsystem bus. A master low side switch allows for global deactivation of all electrical components in order to comply with CDS. The figure 1, shows the general block diagram of this architecture.

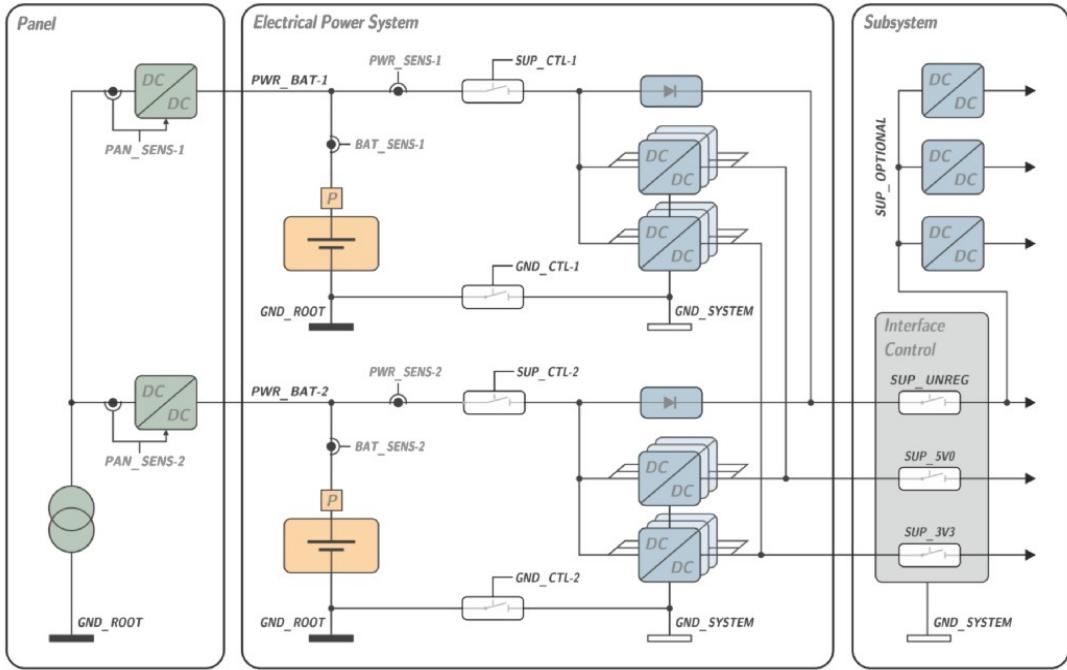


Figure 1: Distributed Electrical Power Concept \*\*

\*\* CubeSat Subsystem Interface Definition - CSID (Proposal) of UNISEC

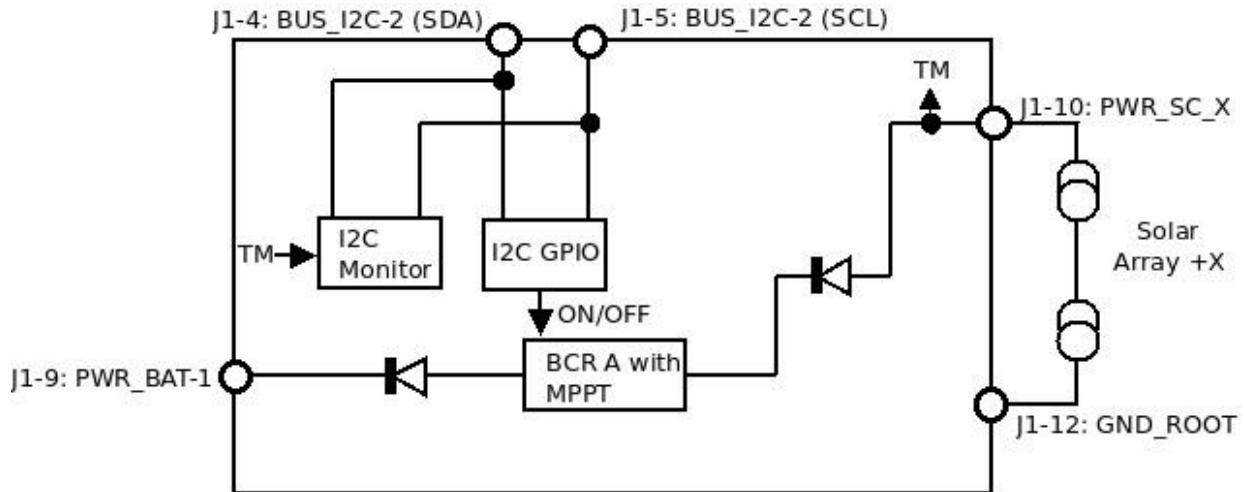
## Panel Board

The configuration employed for the panel board include the BCR, I<sup>2</sup>C telemetry, I<sup>2</sup>C General Purpose Input/Output (GPIO), ideal diodes and a panel interface connector. The figure 2, shows the block diagram of the design developed.

## Battery Charge Regulator (BCR)

The BCR is a highly integrated switch-mode battery charge controller. It provides input voltage regulation, which reduces charge current when input voltage falls below a programmed level. The input regulation loop lowers the charge current so that the solar panel can provide maximum power output.

The BCR offers a constant-frequency synchronous PWM controller with high accuracy current and voltage regulation, charge preconditioning, charge termination, and charge status monitoring.



The BCR charges the battery in three phases: pre-conditioning, constant current, and constant voltage. Charge is terminated when the current reaches 1/10 of the fast charge rate. The pre-charge timer is fixed at 30 minutes. The BCR automatically restarts the charge cycle if the battery voltage falls below an internal threshold and enters a low quiescent current sleep mode when the input voltage falls below the battery voltage.

The BCR controller, can be easily configured with very small hardware changes to support any battery within the range of 2.1V to 26V with VFB set to a 2.1V feedback reference. The charge current is programmed by selecting an appropriate sense resistor. The output of the BCR is named as PWR\_BAT-1.

## I<sup>2</sup>C Telemetry

The I<sup>2</sup>C Telemetry device is used to monitor solar array temperatures, voltages and currents. Through the I<sup>2</sup>C serial interface, the device is configured to constantly measure temperature of the solar array on

the panel through special sensors located directly below the cells. The output voltage and current are measured using special sense amplifiers. The device fits well in the panel board, because provides a sub-millivolt voltage resolution, 1% current measurement and 1°C temperature accuracy.

## I<sup>2</sup>C General Purpose Input/Output (GPIO)

General Purpose parallel Input/Output (GPIO) provide a simple solution for turning ON/OFF the BCR using the I<sup>2</sup>C bus. The microcontroller of EPS or directly from OBC can enable the I/Os by writing to the I/O configuration bits.

## Ideal Diode

The ideal diode is an IC, capable of supplying up to 2.6A from the solar array. The diode contains a 140mΩ P-channel MOSFET connecting IN to OUT. During normal forward operation, the drop across the MOSFET is regulated to as low as 28mV. Quiescent current is less than 40µA for load currents up to 100mA. If the output voltage exceeds the input voltage, the MOSFET is turned off and less than 1µA of reverse current flows from OUT to IN. Maximum forward current is limited to a constant 2.6A (typical) and internal thermal limiting circuits protect the part during fault conditions.

## Panel Interface Connector

The panel bus is in principle a subset of the subsystem bus. The panel interface foresees single row high precision PCB connectors in the standard grid pattern 2.00mm (SMT) with 12 pins.

GND_SYSTEM	1
SUP_5V0	2
NC	3
BUS_I2C-2 (SDA)	4
BUS_I2C-2 (SCL)	5
SUP_UNREG	6
SUP_3V3	7
NC	8
PWR_BAT-1	9
reserved (PWR_SC)	10
NC	11
GND_ROOT	12

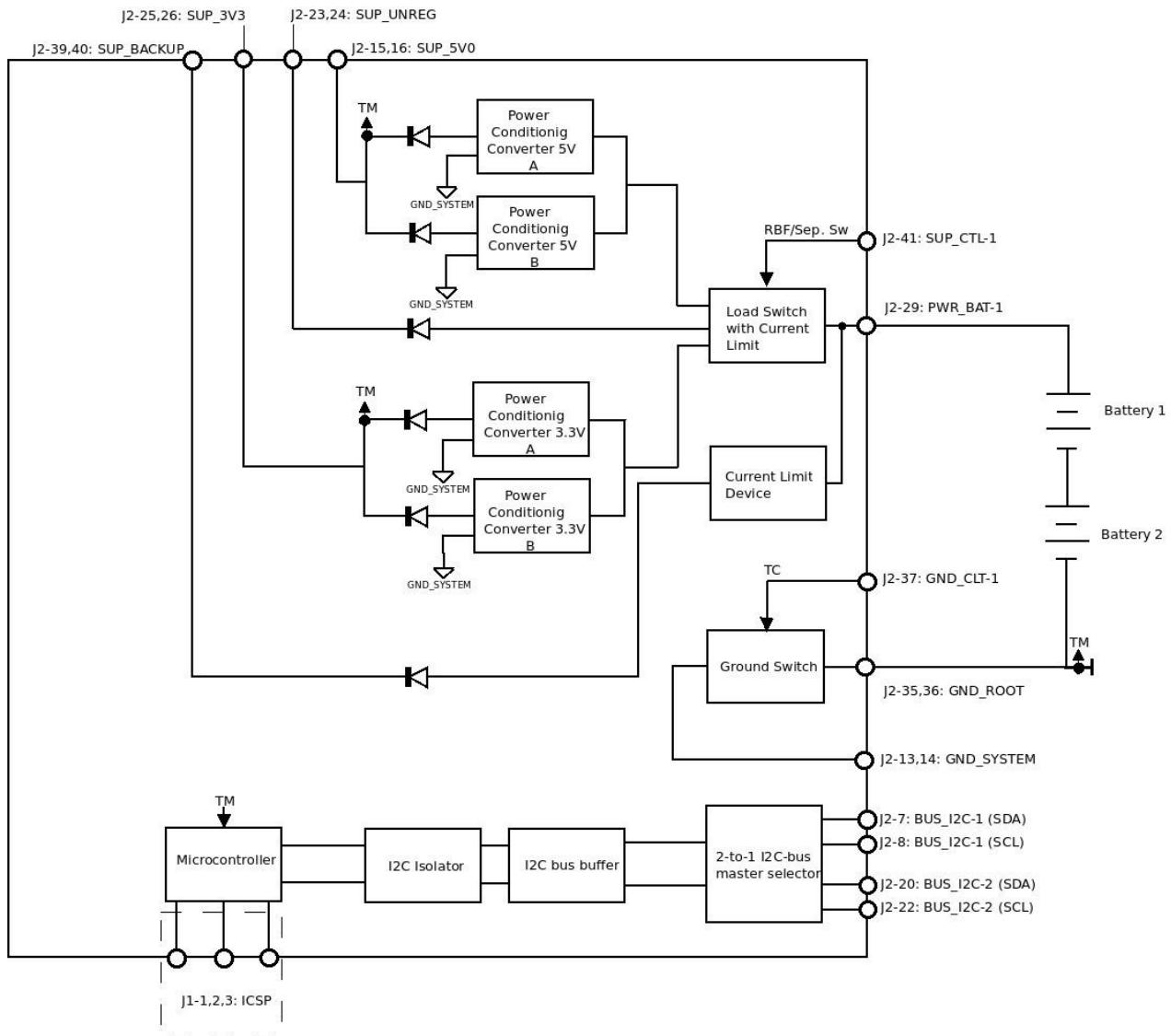
## EPS Board

The EPS board is the main card of the electrical power subsystem, and is connected to the backplane of the satellite. This board has an ultra-small microcontroller to operate the I<sup>2</sup>C and ADC tasks, a 2-to-1 I<sup>2</sup>C-bus master selector, an I<sup>2</sup>C Dual bidirectional bus buffer, a I<sup>2</sup>C Digital Logic Gate Optocoupler, a Power Condition Converter (PCC) of 5V/3.3V in a hot redundant mode configuration of 2:1, an ideal diodes, three load switches with current limit protection and an subsystem interface connector. The figure 4, displays the block diagram of this architecture.

## Microcontroller

The microcontroller used for the EPS board is a PIC of 8-bit devices of Microchip. The main features of this device are:

- Enhanced Mid-range Core with 49 Instruction, 16 Stack Levels
- Flash Program Memory with self read/write capability
- 8-pin ultra small package.
- Internal 32MHz oscillator
- Integrated Capacitive mTouch Sensing Module
- Data Signal Modulator Module



- MI2C, SPI, EUSART w/auto baud
- ECCP (Enhanced/Capture Compare PWM) Module
- Comparator with selectable Voltage Reference
- 4 Channel 10b ADC with Voltage Reference
- 25mA Source/Sink current I/O
- Two 8-bit Timers (TMR0/TMR2)
- One 16-bit Timer (TMR1)

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- Extended Watchdog Timer (EWDT)
- Enhanced Power-On/Off-Reset
- Brown-Out Reset (BOR)
- In Circuit Serial Programming (ICSP)
- On Board In-Circuit Debug
- Wide Operating Voltage (1.8V – 5.5V)
- Standby Current (PIC12LF1840): 20 nA @ 1.8V, typical

In this development, the microcontroller has three main functions, ADC OF 10-bit on 2 channels, I<sup>2</sup>C controller and ICSP for self-programming on the same board.

## 2-to-1 I<sup>2</sup>C-bus master selector

The I<sup>2</sup>C-bus master selector is designed for high reliability dual master I<sup>2</sup>C-bus applications where system operation is required, even when one master fails. The two masters are located on separate I<sup>2</sup>C-buses that connect to the I<sup>2</sup>C-bus of the EPS board devices. I<sup>2</sup>C-bus commands are sent by either I<sup>2</sup>C-bus master and are used to select one master at a time. Either master at any time can gain control of the slave devices if the other master is disabled or removed from the system. The failed master is isolated from the system and does not affect communication between the on-line master and the slave devices on the I<sup>2</sup>C-bus of the EPS board. The device has channel 0 selected at start-up.

## I<sup>2</sup>C Dual bidirectional bus buffer

The device is a bipolar IC that creates a non-latching, bidirectional, logic interface between the normal I<sup>2</sup>C-bus and a range of other bus configurations. It can interface I<sup>2</sup>C-bus logic signals to similar buses having different voltage and current levels.

It achieves this interface without any restrictions on the normal I<sup>2</sup>C-bus protocols or clock speed. The device adds minimal loading to the I<sup>2</sup>C-bus node, and loadings of the remote I<sup>2</sup>C-bus nodes are not transmitted or transformed to the local node. Restrictions on the number of I<sup>2</sup>C-bus devices in a system,

or the physical separation between them, are virtually eliminated. Transmitting SDA and SCL signals via balanced transmission lines with galvanic isolation (opto-coupling) is simple because separate directional Tx and Rx signals are provided. The Tx and Rx signals may be directly connected, without causing latching, to provide an alternative bidirectional signal line with I<sup>2</sup>C-bus properties.

## I<sup>2</sup>C Digital Logic Gate Optocoupler

The device is a truly isolated, multi-channel and bi-directional, high-speed optocouplers. The device provides full duplex and bi-directional isolated data transfer and communication capability in compact package.

These high channel density make them ideally suited to isolating data conversion devices, parallel buses and peripheral interfaces, as I<sup>2</sup>C protocol employed in the EPS board.

## Power Condition Converter (PCC) of 5V/3.3V

These regulators are synchronous step-down DC-DC converters capable of driving up to 2 A of load current from an input voltage ranging from 6 V to 9 V (42V abs max). The LM43603 provides exceptional efficiency, output accuracy and dropout voltage in a very small solution size. Peak current mode control is employed to achieve simple control loop compensation and cycle-by-cycle current limiting.

Discontinuous conduction and automatic frequency modulation at light loads improve light load efficiency. The device requires few external components and pin arrangement allows simple, optimum PCB layout. Protection features include thermal shutdown, VCC under-voltage lockout, cycle-by-cycle current limit, and output short circuit protection.

Both converters, 5V and 3.3V, are configured in a 2-1 hot redundancy, which provides protection

against a failure on the regulators. The outputs for the 5V and 3.3 buses are named as SUP\_5V0, and SUP\_3V3, respectively.

## Ideal Diode

There are two ideal diodes devices used in the EPS board. First, a device that controls an external P-channel MOSFET to create a near ideal diode function for load sharing of the supply of unregulated and backup power (SUP\_UNREG and SUP\_BACKUP). This permits highly efficient OR'ing of multiple power sources for extended battery life. When conducting, the voltage drop across the MOSFET is typically 20mV.

A second configuration used in the EPS board for the PCC 5V/3.3V, which is a dual ideal diodes, each capable of supplying up to 2.6A from input voltages between 2.5V and 5.5V. The ideal diodes use a 100mΩ P-channel MOSFET to independently connect INA to OUTA and INB to OUTB. During normal forward operation, the voltage drops across each of these diodes are regulated to as low as 18mV. Quiescent current is less than 80µA for diode currents up to 1A. If either of the output voltages exceeds its respective input voltage, that MOSFET is turned off and less than 1µA of reverse current flows from OUT to IN. Maximum forward current in each MOSFET is limited to a constant 2.6A and internal thermal limiting circuits protect the part during fault conditions.

## Load switches with current limit protection

The EPS board has three switches with current limit protection, one being used for the ground separation, other for the battery bus isolation and a third for the battery backup bus that is always connected and used as current limit protection.

- A device is used for the battery bus and battery backup (SUP\_UNREG and SUP\_BACKUP), which is a load switch that integrates multiple control features that simplify the design and

increase the reliability of the circuitry connected to the switch. The device contains 56 mΩ switches designed to operate in the 6V to 9V range. An internally generated gate drive voltage ensures good R<sub>ON</sub> linearity over the input voltage operating range. An over-current protection circuit (OCP) continuously monitors the current through the load switch, and controls the switch impedance to limit the current to the level programmed by an external resistor. If the over-current condition persists for more than 7 ms, the switch shuts off automatically. The device also has an over temperature protection circuit (OTP) which will shut the switch off if the junction temperature exceeds about 135 °C. The OTP circuit will release the switch when the temperature has decreased by about 40 °C of hysteresis. In the case of the switch used for SUP\_UNREG, the on/off signal SUP\_CLT-1 is generated by the Remove-before-flight pin and the separation switch arrangement of the satellite structure.

- A device is used for the ground separation of GND\_ROOT from GDN\_SYSTEM. It is a single channel load switch that provides configurable rise time to minimize inrush current. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.8V to 5.7V and can support a maximum continuous current of 6 A. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. This signal is named GND\_CTL-1, and it's controlled by OBC.

## Subsystem Interface Connector

The subsystem interface foresees double row high precision PCB connectors in the standard grid pattern 2.00mm (THT) with 50 pins. The figure 5, shows the arrangement for the EPS board.

NC	1	2	NC
NC	3	4	NC
NC	5	6	NC
BUS_I2C-1 (SDA)	7	8	BUS_I2C-1 (SCL)
NC	9	10	NC
NC	11	12	NC
GND_SYSTEM	13	14	GND_SYSTEM
SUP_5V0	15	16	SUP_5V0
NC	17	18	NC
NC	19	20	BUS_I2C-2 (SDA)
NC	21	22	BUS_I2C-2 (SCL)
SUP_UNREG	23	24	SUP_UNREG
SUP_3V3	25	26	SUP_3V3
PWR_BAT-1	27	28	PWR_BAT-1
NC	29	30	NC
reserved (PWR_SC_Y)	31	32	reserved (PWR_SC_X)
reserved (PWR_SC_Z)	33	34	NC
GND_ROOT	35	36	GND_ROOT
GND_CTL-1	37	38	NC
SUP_BACKUP	39	40	SUP_BACKUP
SUP_CTL-1	41	42	NC
NC	43	44	NC
NC	45	46	NC
NC	47	48	NC
NC	49	50	NC

## Description of Operation of the Panel Board

The main function inside of the panel board is to performance the battery charge regulation. Also, the report of the telemetry of solar array is an important task incorporated in this board.

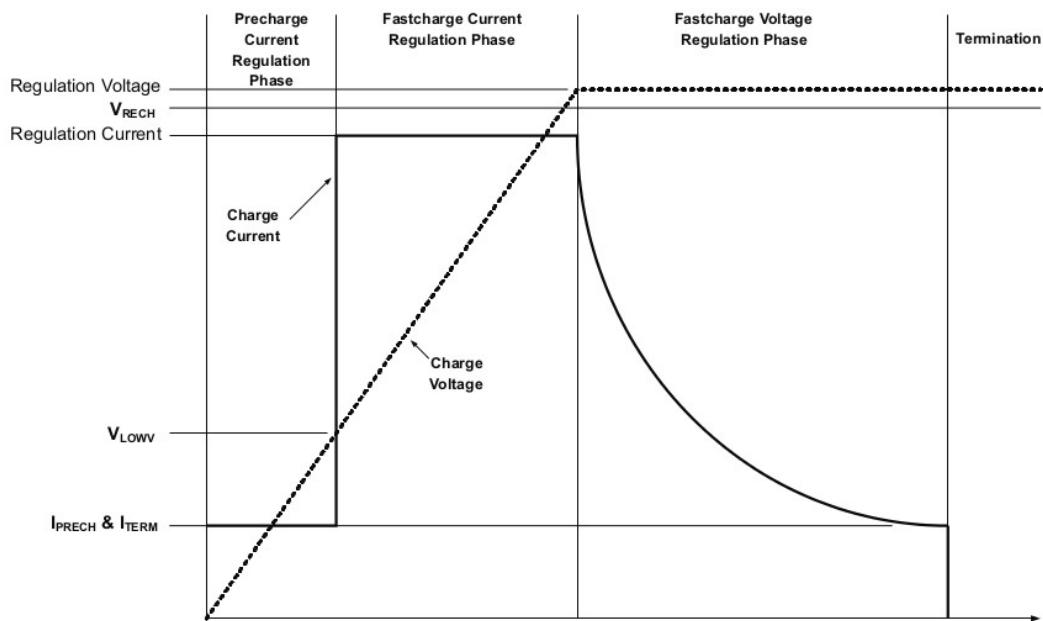
## Battery Charge Regulator (BCR) Operation

The functions of the battery voltage regulation, input voltage regulation, battery current regulation, battery pre-charge, charge termination and pre-charge, enable and disable charging, cycle-by-cycle charge under current, input under-voltage lock out (UVLO), battery over-voltage protection, cycle-by-cycle charge over-current protection is reported.

## Battery Voltage Regulation

The BCR uses a high accuracy voltage regulator for the charging voltage. The charge voltage is programmed via a resistor divider from the battery to ground.

Most commercial Li-ion cells can now be charged to 4.2V/cell. The charge profile of both Li-Ion is preconditioning, constant current, and constant voltage. For maximum cycle life, the end-of-charge voltage threshold could be lowered to 4.1V/cell, in this design fixed to 8.26V (2 cell in series). The figure 6, shows the charging profile.



## Input Voltage Regulation

A solar panel has a unique point on the V-I or V-P curve, called the Maximum Power Point (MPP), at which the entire photovoltaic (PV) system operates with maximum efficiency and produces its maximum output power. The constant voltage algorithm is the simplest Maximum Power Point Tracking (MPPT) method. The BCR automatically reduces charge current so the maximum power

point is maintained for maximum efficiency.

If the solar panel cannot provide the total power of the system and BCR, the input voltage drops. Once the voltage sensed drops below a predefined level, MPPSET of 1.2V, the charger maintains the input voltage by reducing the charge current. If the MPPSET voltage is forced below 1.2V, the BCR stays in the input voltage regulation loop while the output current is zero.

The MPPSET voltage is also used as charge enable control. If the voltage on MPPSET is pulled down below 75mV, charge is disabled. Charge resumes if the voltage on MPPSET goes back above 175mV. In this function is used the I2C GPIO to enable/disable the BCR through a telecommand from OBC.

## Battery Current Regulation

Battery current is sensed by resistor R4 connected between SRP and SRN (see appendix for the schematics of panel board). The full-scale differential voltage between SRP and SRN is fixed at 40mV. Thus, for a 62-m $\Omega$  sense resistor, the charging current is 650mA.

## Battery Precharge

On power-up, if the battery voltage is below the  $V_{LOWV}$  threshold, the BCR applies the precharge current to the battery. This feature is intended to revive deeply discharged cells. If the  $V_{LOWV}$  threshold is not reached within 30 minutes of initiating precharge, the charger turns off. The precharge current is determined as 1/10 of the fast charge current, in this configuration is 65mA.

## Charge Termination and Recharge

The BCR monitors the charging current during the voltage regulation phase. Termination is detected while the voltage on the VFB pin (see appendix for the schematics of panel board) is higher than the

$V_{RECH}$  threshold and the charge current is less than the  $I_{TERM}$  threshold (1/10 of fast charge current), in this configuration is 65mA.

A new charge cycle is initiated when one of the following conditions occurs:

- The battery voltage falls below the recharge threshold
- A power-on-reset (POR) event occurs
- MPPSET falls below 75mV to reset charge enable

## Enable and Disable Charging

The following conditions have to be valid before charging is enabled:

- Charge is allowed ( $MPPSET > 175mV$ )
- Device is not in Under-Voltage-Lock-Out (UVLO) mode and VCC is above the  $VCC_{LOWV}$  threshold
- Device is not in SLEEP mode
- 30ms delay is complete after initial power-up

One of the following conditions stops on-going charging:

- Charge is disabled ( $MPPSET < 75mV$ )
- SLEEP mode

## Cycle-by-Cycle Charge Under Current Protection

In the BCR, if the SRP-SRN voltage decreases below 5mV, the low side FET is turned off for the remainder of the switching cycle to prevent negative inductor current. During DCM, the low-side FET only turns on when the bootstrap capacitor voltage drops below 8.4V to provide refresh charge for the bootstrap capacitor. This is important to prevent negative inductor current from causing a boost effect

in which the input voltage increases as power is transferred from the battery to the input capacitors and lead to an over-voltage stress on the VCC node and potentially cause damage to the system.

## Input Under-Voltage Lock Out (UVLO)

The system must have a minimum VCC voltage to allow proper operation. This VCC voltage come from the solar array. When VCC is below the UVLO threshold, all circuits on the BCR are disabled. Typically, the UVLO is 3.65V.

## Battery Over-Voltage Protection

The converter does not allow the high-side FET to turn on until the BAT voltage goes below 102% of the regulation voltage. This allows one-cycle response to an over-voltage condition – such as occurs when the load is removed or the battery is disconnected. A current sink from SRP to GND is on to discharge the stored energy on the output capacitors.

## Cycle-by-Cycle Charge Over-Current Protection

The charger has a secondary cycle-to-cycle over-current protection. It monitors the charge current and prevents the current from exceeding 200% of the programmed charge current. The high-side gate drive turns off when over-current is detected and automatically resumes when the current falls below the over-current threshold.

## Thermal Shutdown Protection

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junction temperatures low. As an added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the  $T_{SHUT}$  threshold of 145°C. The charger stays off until the junction temperature falls below 130°C.

## I<sup>2</sup>C Telemetry Operation

The I<sup>2</sup>C telemetry device monitors voltage, current and temperature of the solar array. It is configured through an I<sup>2</sup>C interface to measure these parameters. Single or repeated measurements are possible. Remote temperature measurements use a transistor as a temperature sensor, allowing the remote sensor to be a discrete NPN (ex. MMBT3904) in the microcontroller. The internal ADC reference minimizes the number of support components required.

The device communicates through an I<sup>2</sup>C serial interface. The serial interface provides access to control, status and data registers. I<sup>2</sup>C defines a 2-wire open-drain interface supporting multiple slave devices and masters on a single bus. The I<sup>2</sup>C telemetry device supports 100kbit/s in the standard mode and up to 400kbit/s in fast mode. The I<sup>2</sup>C interface is used to trigger single conversions, or start repeated conversions by writing to a dedicated trigger register. The data registers contain a destructive-read status bit (data valid), which is used in repeated mode to determine if the register's contents have been previously read. This bit is set when the register is updated with new data, and cleared when read.

## Description of Operation of the EPS Board

The main operating function on the EPS board are related with the following devices: PCC 5V/3.3V, the load switches with current limit, 2-to-1 I<sup>2</sup>C-bus master selector, I<sup>2</sup>C Dual bidirectional bus buffer, I<sup>2</sup>C Digital Logic Gate Optocoupler and microcontroller.

## Power Condition Converter (PCC) of 5V/3.3V Operation

The PCC is a synchronous Buck converter that employs peak current mode control topology. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the internal high-side switch (HS switch) of the IC and compared to the peak current to control the ON time of the HS switch. The

voltage feedback loop is internally compensated, which allows for fewer external components, and provides stable operation with the output capacitors. The regulator operates with fixed switching frequency in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). At very light load, the PCC will operate in PFM to maintain high efficiency and the switching frequency will decrease with reduced load current.

## Light Load Operation

DCM operation is employed in the PCC when the inductor current valley reaches zero. The PCC will be in DCM when load current is less than half of the peak-to-peak inductor current ripple in CCM. In DCM, the internal LS switch is turned off when the inductor current reaches zero. Switching loss is reduced by turning off the LS FET at zero current and the conduction loss is lowered by not allowing negative current conduction. Power conversion efficiency is higher in DCM than CCM under the same conditions.

In DCM, the HS switch ON time will reduce with lower load current. When either the minimum HS switch ON time ( $t_{ON-MIN}$ ) or the minimum peak inductor current ( $I_{PEAK-MIN}$ ) is reached, the switching frequency will decrease to maintain regulation. At this point, the PCC operates in PFM. In PFM, switching frequency is decreased by the control loop when load current reduces to maintain output voltage regulation. Switching loss is further reduced in PFM operation due to less frequent switching actions.

## Adjustable Output Voltage

The voltage regulation loop in the PCC regulates output voltage by maintaining the voltage on FB pin ( $V_{FB}$ ) to be the same as the internal REF voltage ( $V_{REF}$ ). A resistor divider pair is needed to program the ratio from output voltage  $V_{OUT}$  to  $V_{FB}$ . The resistor divider is connected from the  $V_{OUT}$  of the PCC to ground with the mid-point connecting to the FB pin. The voltage output is set to 5V and 3.3V, for the PCC 5V/3.3V, respectively.

## Under-voltage Lockup

Under voltage lockout (UVLO) prevents the LM43603 from operating until the VCC voltage exceeds 3.1 V (typical). The VCC UVLO threshold has 520 mV of hysteresis (typically) to prevent undesired shutting down due to temporary V IN droops.

## Switching Frequency

The PCC operates at 500 kHz default switching frequency.

## Over Current and Short Circuit Protection

The PCC is protected from over-current conditions by cycle-by-cycle current limiting on both the peak and valley of the inductor current. High-side MOSFET over-current protection is implemented by the nature of the Peak Current Mode control. The HS switch current is sensed when the HS is turned on after a set blanking time. The HS switch current is compared to the output of the internal Error Amplifier (EA) minus slope compensation every switching cycle. The peak current of the HS switch is limited by the maximum EA output voltage minus the slope compensation at every switching cycle. The slope compensation magnitude at the peak current is proportional to the duty cycle.

When the LS switch is turned on, the current going through it is also sensed and monitored. The LS switch will not be turned OFF at the end of a switching cycle if its current is above the LS current limit  $I_{LS-LIMIT}$ . The LS switch will be kept ON so that inductor current keeps ramping down, until the inductor current ramps below the LS current limit. Then the LS switch will be turned OFF and the HS switch will be turned on after a dead time. If the current of the LS switch is higher than the LS current limit for 32 consecutive cycles, hiccup current protection mode will be activated. In hiccup mode, the regulator will be shutdown and kept off for 5.5 ms typically before the PCC tries to start again. If over-current or short-circuit fault condition still exist, hiccup will repeat until the fault condition is removed. Hiccup mode reduces power dissipation under severe over-current conditions, prevents over heating and potential damage to the device.

## Thermal Shutdown

Thermal shutdown is a built-in self protection to limit junction temperature and prevent damage due to over heating. Thermal shutdown turns off the device when the junction temperature exceeds 160°C typically to prevent further power dissipation and temperature rise. Junction temperature will reduce after thermal shutdown. The PCC will attempt to restart when the junction temperature drops to 150°C.

## 2-to-1 I<sup>2</sup>C-bus Master Selector Operation

When a master seeks control of the bus by connecting its I2C-bus channel to the master selector downstream channel on the EPS card, it has to write to the CONTROL register (Reg#01).

Bits MYBUS and BUSON allow the master to take control of the bus.

The MYBUS and the NMYBUS bits determine which master has control of the bus. There is no arbitration. Any master can take control of the bus when it wants regardless of whether the other master is using it or not.

The BUSON and the NBUSON bits determine whether the upstream bus is connected or disconnected to/from the downstream bus. T

Internally, the state machine does the following:

- If the combination of the BUSON and the NBUSON bits causes the upstream to be disconnected from the downstream bus, then that is done. So in this case, the values of the MYBUS and the NMYBUS do not matter.
- If a master was connected to the downstream bus prior to the disconnect, then an interrupt is sent on the respective interrupt output in an attempt to let that master know that it is no longer connected to the downstream bus. This is indicated by setting the BUSLOST bit in the Interrupt Status Register.

- If the combination of the BUSON and the NBUSON bits causes a master to be connected to the downstream bus and if there is no change in the BUSON bits since when the disconnect took effect, then the master requesting the bus is connected to the downstream bus. If it requests a bus initialization sequence, then it is performed.
- If there is no change in the combination of the BUSON and the NBUSON bits and a new master wants the bus, then the downstream bus is disconnected from the old master that was using it and the new master gets control of it. Again, the bus initialization if requested is done. The appropriate interrupt signals are generated.

After a master has sent the bus control request:

1. The previous master is disconnected from the I2C-bus. An interrupt to the previous master is sent through its INT line to let it know that it lost control of the bus. BUSLOST bit in the Interrupt Status Register is set. This interrupt can be masked by setting the BUSLOSTMSK bit to logic 1.
2. A built-in bus initialization/recovery function can take temporary control of the downstream channel to initialize the bus before making the actual switch to the new bus master. This function is activated by setting the BUSINIT to logic 1 by the master during the same write sequence as the one programming MYBUS and BUSON bits. When activated and whether the bus was previously idle or not:
  - 9 clock pulses are sent on the SCL\_SLAVE.
  - SDA\_SLAVE line is released (HIGH) when the clock pulses are sent to SCL\_SLAVE. This is equivalent to sending 8 data bits and a not acknowledge.
  - Finally a STOP condition is sent to the downstream slave channel.

This sequence completes any read transaction which was previously in process and the downstream slave configured as a slave-transmitter should release the SDA line because the master selector did not acknowledge the last byte.

3. When the initialization has been requested and completed, the master selector sends an interrupt

to the new master through its INT line and connects the new master to the downstream channel. BUSINIT bit in the Interrupt Status Register is set. The switch operation occurs after the master asking the bus control has sent a STOP command. This interrupt can be masked by setting the BUSINITMSK bit to logic 1.

4. When the bus initialization/recovery function has not been requested (BUSINIT = 0), the master selector connects the new master to the slave downstream channel. The switch operation occurs after the master asking the bus control has sent a STOP command. If the built-in bus sensor function detects a non-idle condition in the downstream slave channel at the switching time, master selector sends an interrupt to the new master through its INT line. BUSOK bit in the Interrupt Status Register is set. This means that a STOP condition has not been detected in the previous bus communication and that an external bus recovery/initialization must be performed. If an idle condition has been detected at the switching time, no interrupt is sent. This interrupt can be masked by setting the BUSOKMSK bit to logic 1.

## I<sup>2</sup>C Dual Bidirectional Bus Buffer Operation

The device has two identical buffers allowing buffering of both of the I<sup>2</sup>C-bus (SDA and SCL) signals. Each buffer is made up of two logic signal paths, a forward path from the I<sup>2</sup>C-bus interface pin which drives the buffered bus, and a reverse signal path from the buffered bus input to drive the I<sup>2</sup>C-bus interface. Thus these paths are:

- sense the voltage state of the I<sup>2</sup>C-bus pin Sx (or Sy) and transmit this state to the pin Tx (Ty respectively), and
- sense the state of the pin Rx (Ry) and pull the I<sup>2</sup>C-bus pin LOW whenever Rx (Ry) is LOW.

The rest of this discussion will address only the ‘x’ side of the buffer; the ‘y’ side is identical.

The I<sup>2</sup>C-bus pin (Sx) is designed to interface with a normal I<sup>2</sup>C-bus. The logic threshold voltage levels on the I<sup>2</sup>C-bus are independent of the IC supply V<sub>CC</sub>. The maximum I<sup>2</sup>C-bus supply voltage is 15 V and the guaranteed static sink current is 3 mA.

The logic level of Rx is determined from the power supply voltage V<sub>CC</sub> of the chip. Logic LOW is below 42 % of V<sub>CC</sub>, and logic HIGH is above 58 % of V<sub>CC</sub> (with a typical switching threshold of half V<sub>CC</sub>).

Tx is an open-collector output without ESD protection diodes to V<sub>CC</sub>. It may be connected via a pull-up resistor to a supply voltage in excess of V<sub>CC</sub>, as long as the 15 V rating is not exceeded. It has a larger current sinking capability than a normal I<sup>2</sup>C-bus device, being able to sink a static current of greater than 30 mA, and typical 100 mA dynamic pull-down capability as well.

A logic LOW is only transmitted to Tx when the voltage at the I<sup>2</sup>C-bus pin (Sx) is below 0.6 V. A logic LOW at Rx will cause the I<sup>2</sup>C-bus (Sx) to be pulled to a logic LOW level in accordance with I<sup>2</sup>C-bus requirements (maximum 1.5 V in 5 V applications) but not low enough to be looped back to the Tx output and cause the buffer to latch LOW.

The minimum LOW level this chip can achieve on the I<sup>2</sup>C-bus by a LOW at Rx is typically 0.8 V. If the supply voltage V<sub>CC</sub> fails, then neither the I<sup>2</sup>C-bus nor the Tx output will be held LOW. Their open-collector configuration allows them to be pulled up to the rated maximum of 15 V even without V<sub>CC</sub> present. The input configuration on Sx and Rx also present no loading of external signals even when V<sub>CC</sub> is not present.

The effective input capacitance of any signal pin, measured by its effect on bus rise times, is less than 7 pF for all bus voltages and supply voltages including  $V_{CC} = 0$  V.

## I<sup>2</sup>C Digital Logic Gate Optocoupler Operation

The isolator features the GaAsP LEDs with proprietary back emission design. They offer a useful input drive current of 10 mA.

The output detector integrated circuit (IC) in the optocoupler consists of a photodiode at the input of a two-stage amplifier that provides both high gain and high bandwidth. The secondary amplifier stage of the detector IC feeds into an open collector Schottky-clamped transistor.

The entire output circuit is electrically shielded so that any common-mode transient capacitively coupled from the LED side of the optocoupler is diverted from the photodiode to ground. With this electric shield, the optocoupler can withstand transients that slopes up to 10,000V/ $\mu$ s, and amplitudes up to 1,000V.

## Microcontroller Operation

The microcontroller has three specific functions, ADC, I<sup>2</sup>C controller and ICSP.

### ADC Operation

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair).

The ADC voltage reference is software selectable to be either internally generated or externally supplied. In this development, the option of internally generated was selected. The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

The channels AN0 and AN3 are used to measure the 5V and 3.3V bus voltage. Those signals are isolated from the microcontroller using a high-linearity analog optocouplers.

## I<sup>2</sup>C controller

The Inter-Integrated Circuit Bus (I<sup>2</sup>C) is a multi-master serial data communication bus. Devices communicate in a master/slave environment where the master devices initiate the communication. A Slave device is controlled through addressing.

The I<sup>2</sup>C bus specifies two signal connections:

- Serial Clock (SCL)
- Serial Data (SDA)

Both the SCL and SDA connections are bidirectional open-drain lines, each requiring pull-up resistors for the supply voltage. Pulling the line to ground is considered a logical zero and letting the line float is considered a logical one.

The I<sup>2</sup>C bus can operate with one or more master devices and one or more slave devices. There are four potential modes of operation for a given device:

- Master Transmit mode (master is transmitting data to a slave)

- Master Receive mode (master is receiving data from a slave)
- Slave Transmit mode (slave is transmitting data to a master)
- Slave Receive mode (slave is receiving data from the master)

To begin communication, a master device starts out in Master Transmit mode. The master device sends out a Start bit followed by the address byte of the slave it intends to communicate with. This is followed by a single Read/Write bit, which determines whether the master intends to transmit to or receive data from the slave device.

If the requested slave exists on the bus, it will respond with an Acknowledge bit, otherwise known as an ACK. The master then continues in either Transmit mode or Receive mode and the slave continues in the complement, either in Receive mode or Transmit mode, respectively.

A Start bit is indicated by a high-to-low transition of the SDA line while the SCL line is held high. Address and data bytes are sent out, Most Significant bit (MSb) first. The Read/Write bit is sent out as a logical one when the master intends to read data from the slave, and is sent out as a logical zero when it intends to write data to the slave.

The Acknowledge bit (ACK) is an active-low signal, which holds the SDA line low to indicate to the transmitter that the slave device has received the transmitted data and is ready to receive more. The transition of a data bit is always performed while the SCL line is held low. Transitions that occur while the SCL line is held high are used to indicate Start and Stop bits.

If the master intends to write to the slave, then it repeatedly sends out a byte of data, with the slave

responding after each byte with an ACK bit.

If the master intends to read from the slave, then it repeatedly receives a byte of data from the slave, and responds after each byte with an ACK bit.

On the last byte of data communicated, the master device may end the transmission by sending a Stop bit. If the master device is in Receive mode, it sends the Stop bit in place of the last ACK bit. A Stop bit is indicated by a low-to-high transition of the SDA line while the SCL line is held high.

In some cases, the master may want to maintain control of the bus and re-initiate another transmission. If so, the master device may send another Start bit in place of the Stop bit or last ACK bit when it is in receive mode.

The I<sup>2</sup>C bus specifies three message protocols;

- Single message where a master writes data to a slave.
- Single message where a master reads data from a slave.
- Combined message where a master initiates a minimum of two writes, or two reads, or a combination of writes and reads, to one or more slaves.

## ICSP

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:

- ICSPCLK
- ICSPDAT
- $V_{PP}$
- $V_{DD}$
- $V_{SS}$

In Program/Verify mode the program memory, user IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input.

# Simulation Results

The simulation were developed using Pspice, with model provided by the manufacture. It's not possible to simulate all the devices because some models are not available.

## The EPS Board

The main simulation performed in this board were the PCC 5V/3.3V. Using Pspice was possible to tune-in the circuit the voltage drop of 1% of its nominal value for load transient up to 50% of the nominal load.

### Simulation Results of PCC 5V

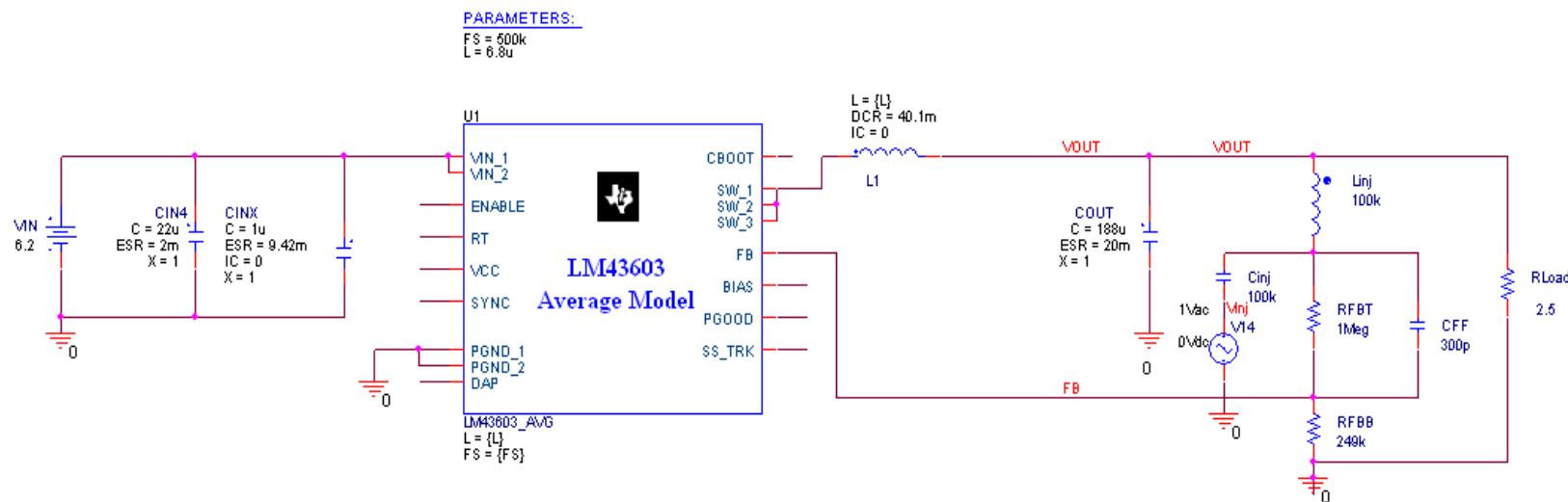
The simulation settings used for this simulation are presented in the table 3.

Description	Value	Unit	SPICE Option
<b>Load Parameters</b>			
Input	6.2 (Lowest Input) 8.26 (Highest Input)	V	
Load	1.0 (half load) 2.0 (full load)	A	
<b>PSPICE Parameters</b>			
Run to time	6m	s	(TSTOP)
Relative accuracy of V's and I's	0.001	-	(RELTOL)
Best accuracy of voltages	1.0u	V	(VNTOL)
Best accuracy of currents	1.0p	A	(ABSTOL)
Best accuracy of charges	0.01p	coulombs	(CHGTOL)
Minimum conductance of any branch	1.0E-12	1/ohm	(GMIN)
DC and bias "blind" iteration limit	150		(ITL1)
DC and bias "best guest" iteration limit	20		(ITL2)
Transient time point iteration limit	45		(ITL4)
Default nominal temperature	27.0	°C	(TNOM)

Table 3: Simulation Settings for the PCC 5V

# Power Condition Converter 5V Loop Response Bode Plot

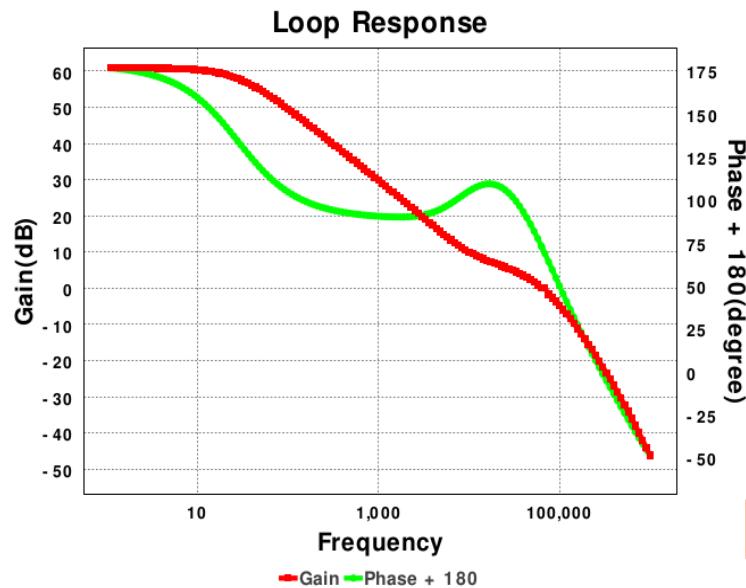
Title Vin: 6.2 - 8.26V Vout: 5V@2A Step-Down Converters		
Size D	Document Number	Rev 1.0
Date: Tuesday, July 14, 2015	Sheet 1 of 1	



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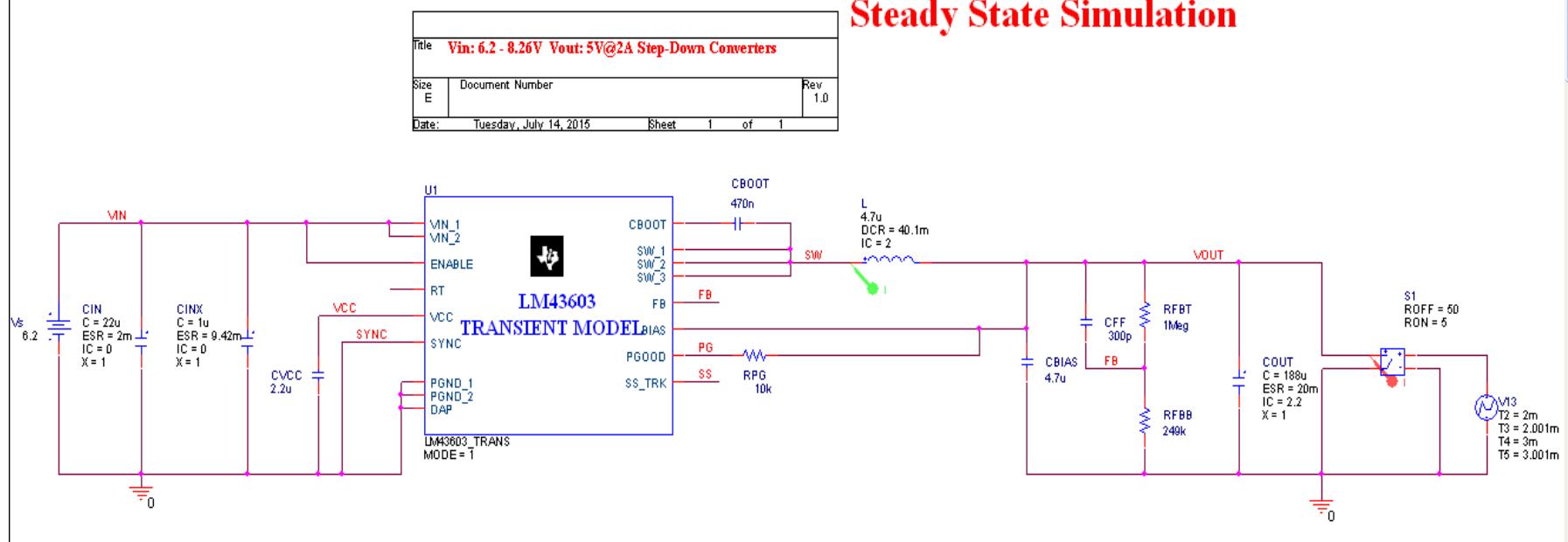
Using Pspice to do the loop stabilization, the phase and gain margin is calculated. The figure 8, shows both responses.

- PM: 73.58°, Gain Margin: -21.71 dB



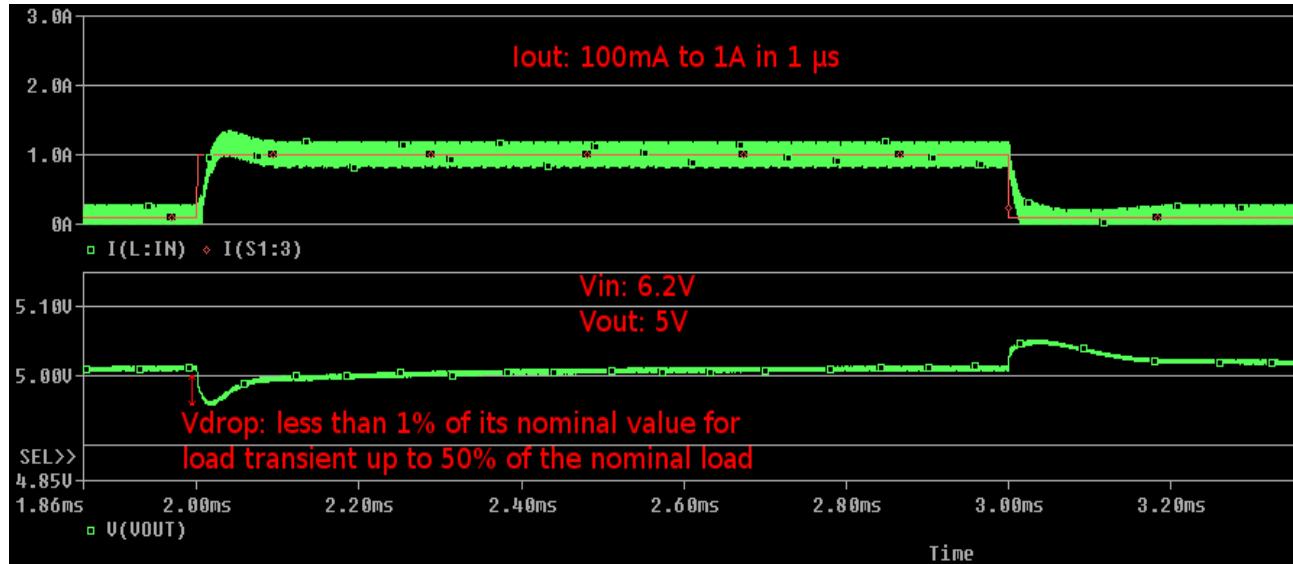
Using a transient model of a current-mode buck converter is obtained the different results. The figure 9, presents the transient model.

## Power Condition Converter 5V Steady State Simulation

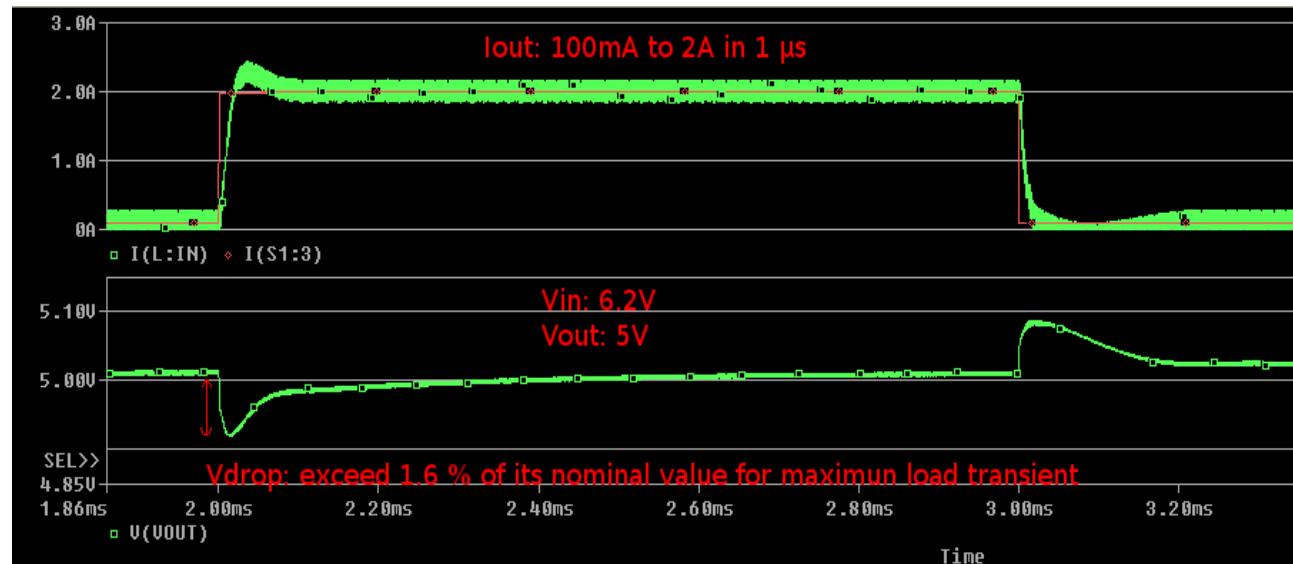


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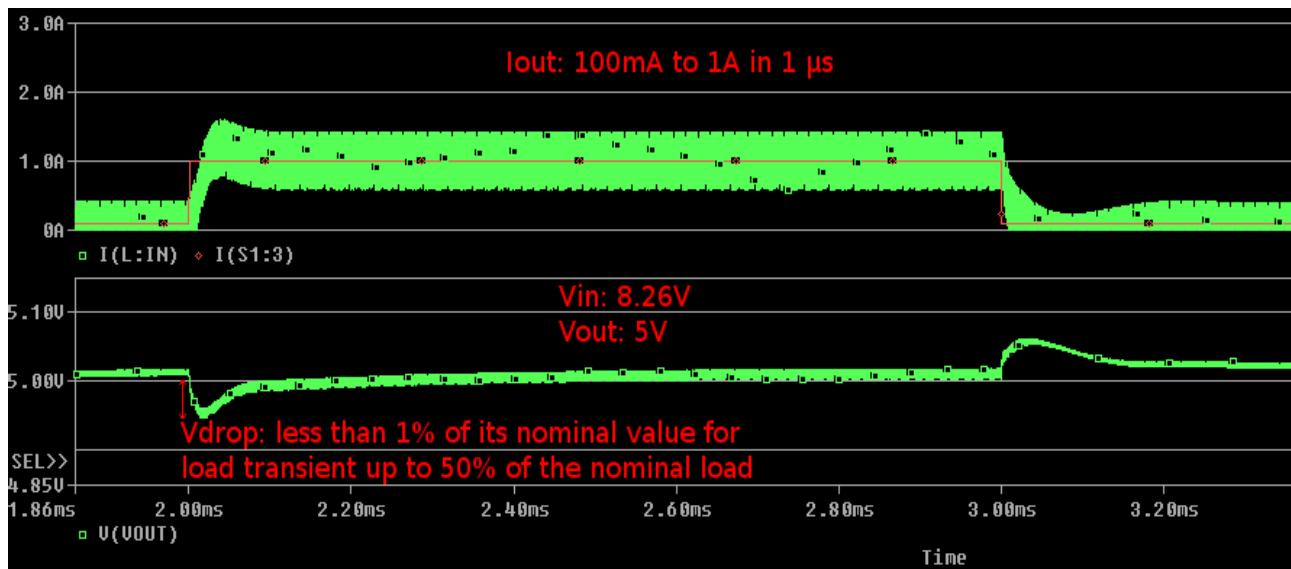
Result: Vin=6.2V / Vout= 5V@0.1A~1A (Half Load) are displayed in the figure 10.



Result: Vin=6.2V / Vout= 5V@0.1A~2A (Full Load) are displayed in the figure 11.



Result: Vin=8.26V / Vout= 5V@0.1A~1A (Half Load) are displayed in the figure 12.



Result: Vin=8.26V / Vout= 5V@0.1A~2A (Full Load) are displayed in the figure 13.

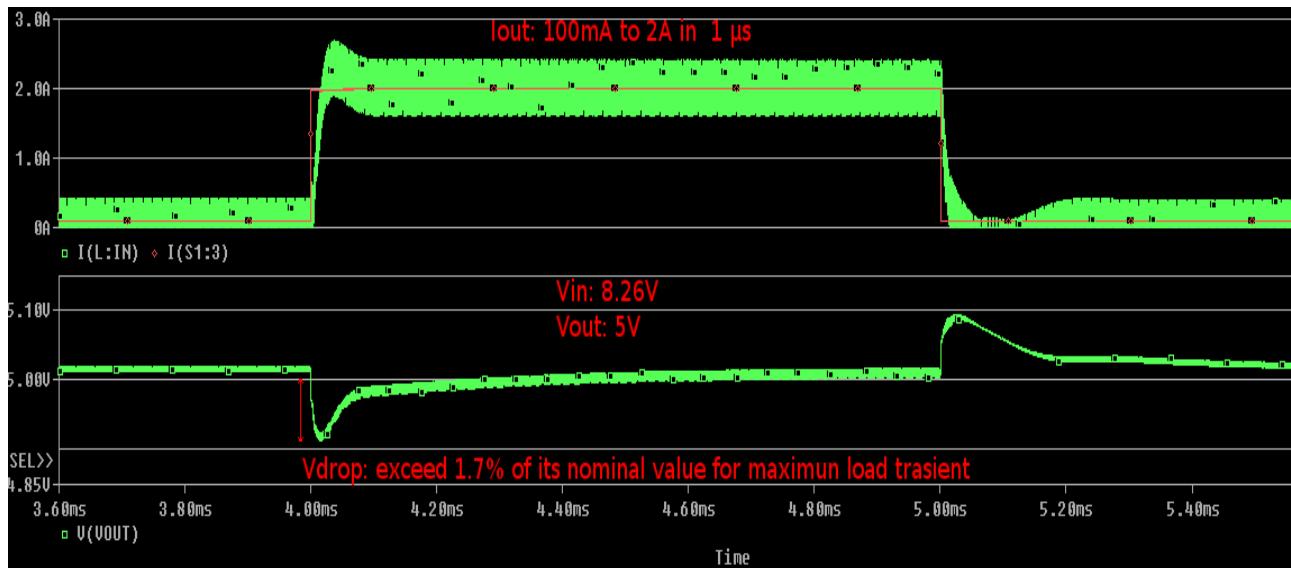
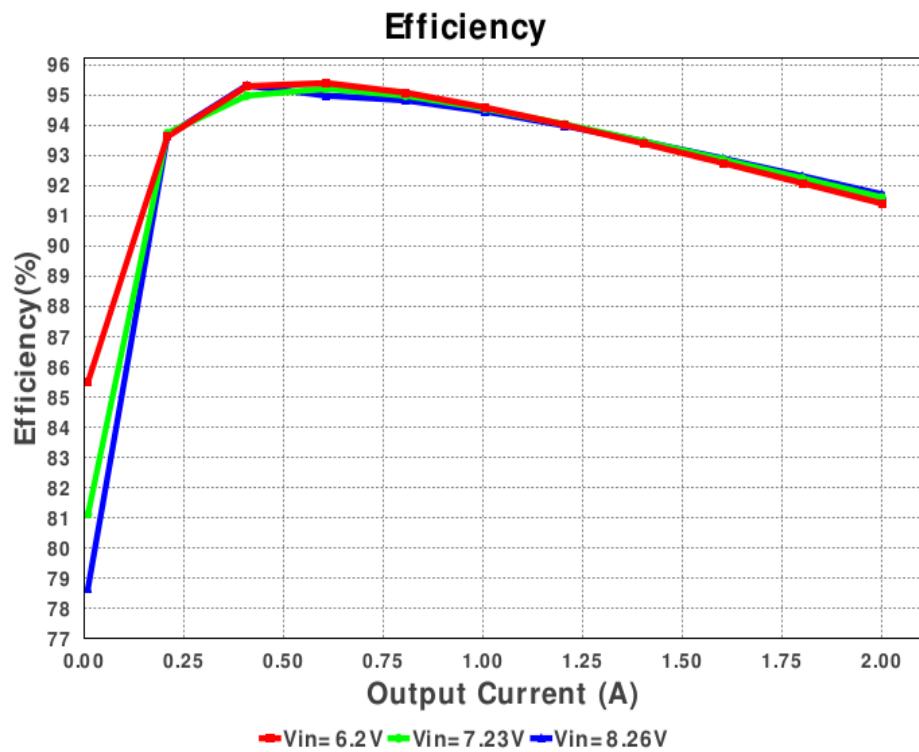


Figure 13: Result: Vin=8.26V / Vout= 5V@0.1A~2A (Full Load)

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Efficiency: ~94.5% at 1A (Half Load)



## Simulation Results of PCC 3.3V

The simulation settings used for this simulation are presented in the table 4.

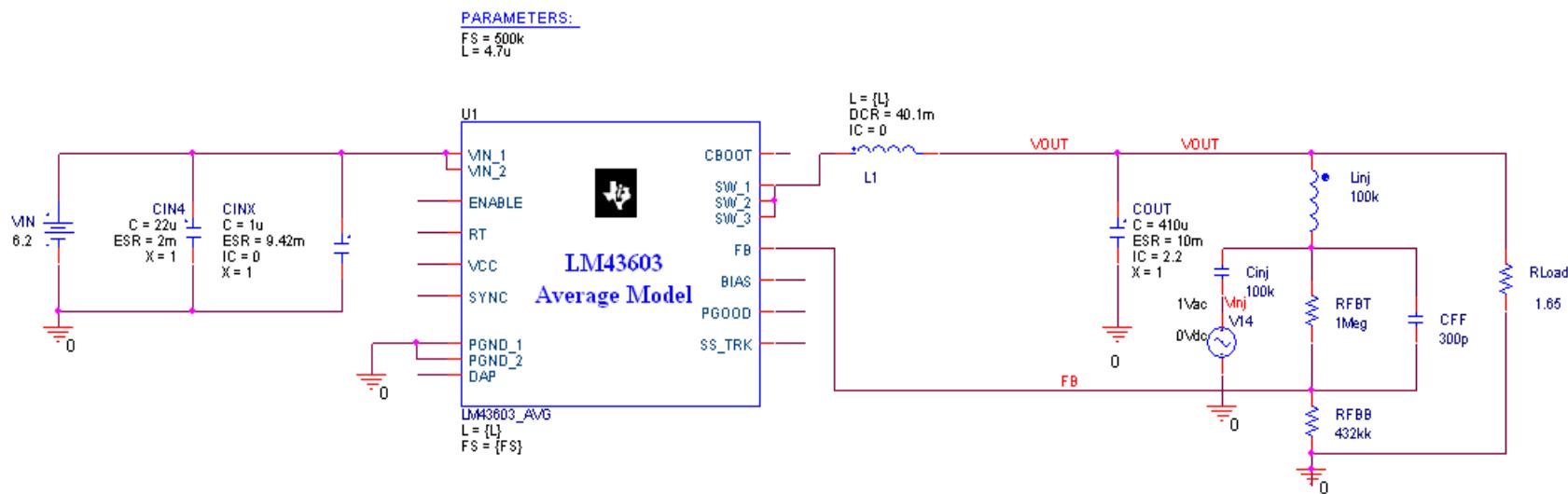
Description	Value	Unit	SPICE Option
<b>Load Parameters</b>			
Input	6.2 (Lowest Input) 8.26 (Highest Input)	V	
Load	1.0 (half load) 2.0 (full load)	A	
<b>PSPICE Parameters</b>			
Run to time	6m	s	(TSTOP)
Relative accuracy of V's and I's	0.001	-	(RELTOL)
Best accuracy of voltages	1.0u	V	(VNTOL)
Best accuracy of currents	1.0p	A	(ABSTOL)
Best accuracy of charges	0.01p	coulombs	(CHGTOL)
Minimum conductance of any branch	1.0E-12	1/ohm	(GMIN)
DC and bias “blind” iteration limit	150		(ITL1)
DC and bias “best guest” iteration limit	20		(ITL2)
Transient time point iteration limit	45		(ITL4)
Default nominal temperature	27.0	°C	(TNOM)

Table 4: Simulation Settings for the PCC 3.3V

The circuit simulated to calculate the loop response is displayed in the figure 15.

# Power Condition Converter 3.3V Loop Response Bode Plot

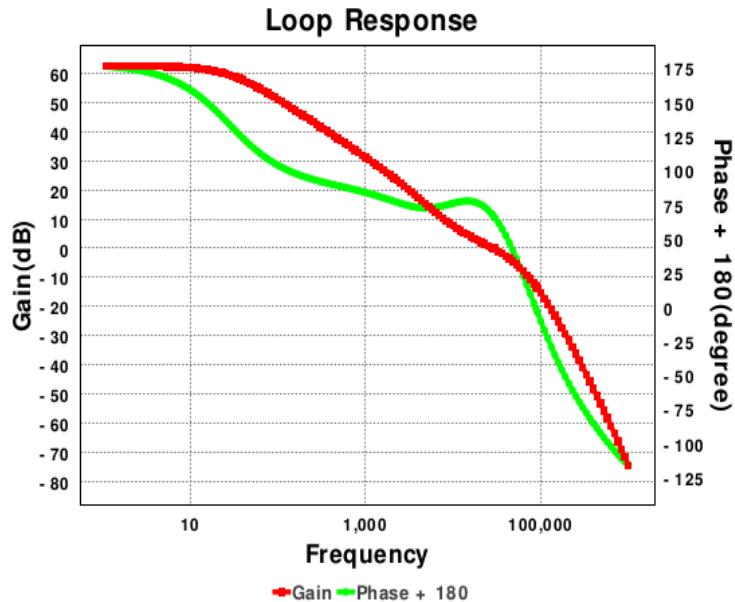
Title Vin: 6.2 - 8.26V Vout: 3.3V@2A Step-Down Converters		
Size D	Document Number	Rev 1.0
Date: Tuesday, July 21, 2015	Sheet 1	of 1



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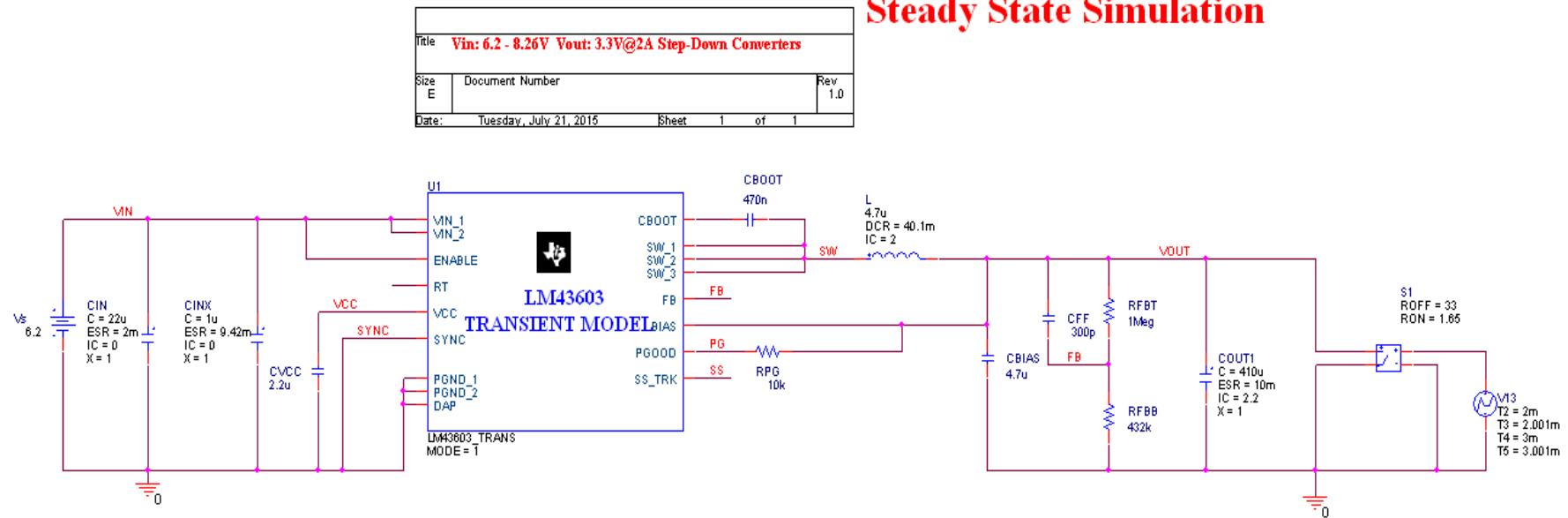
Using Pspice to do the loop stabilization, the phase and gain margin is calculated. The figure 16, shows both responses.

- PM: 68.68°, Gain Margin: -13.04 dB



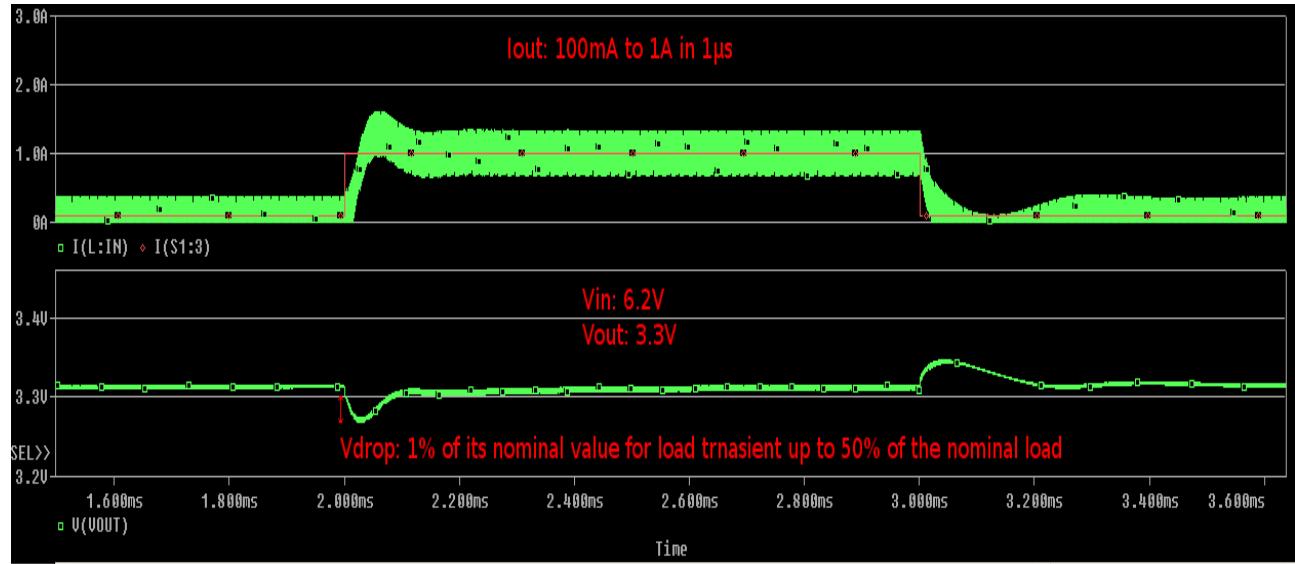
Using a transient model of a current-mode buck converter is obtained the different results. The figure 17, presents the transient model.

## Power Condition Converter 3.3V Steady State Simulation

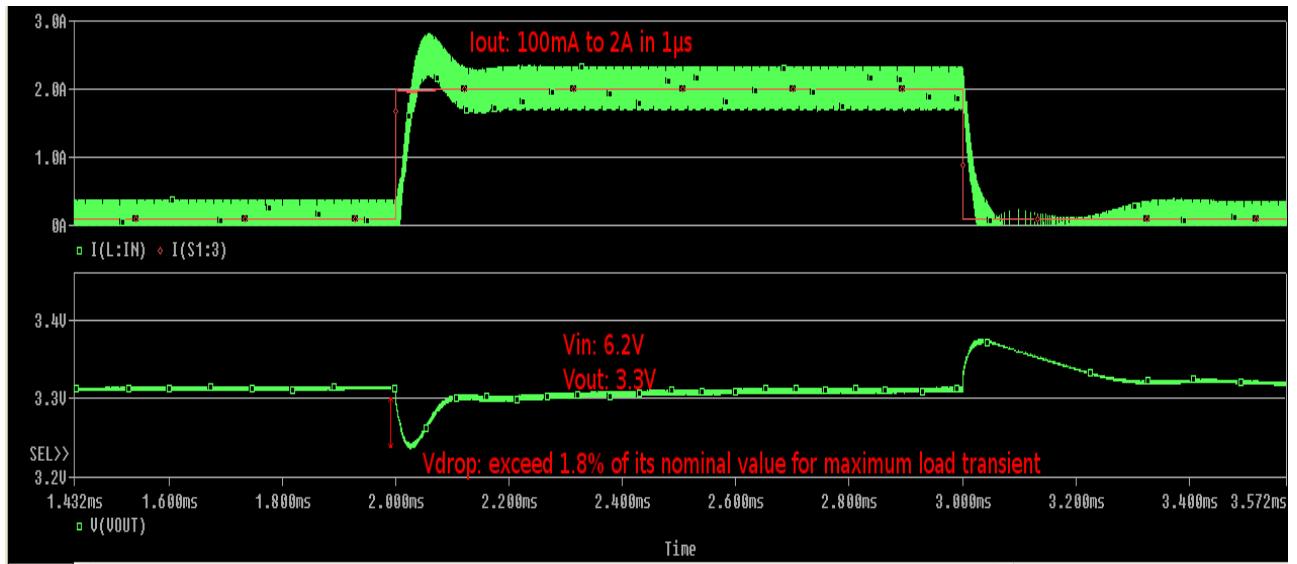


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Result: Vin=6.2V / Vout= 3.3V@0.1A~1A (Half Load) are displayed in the figure 18.

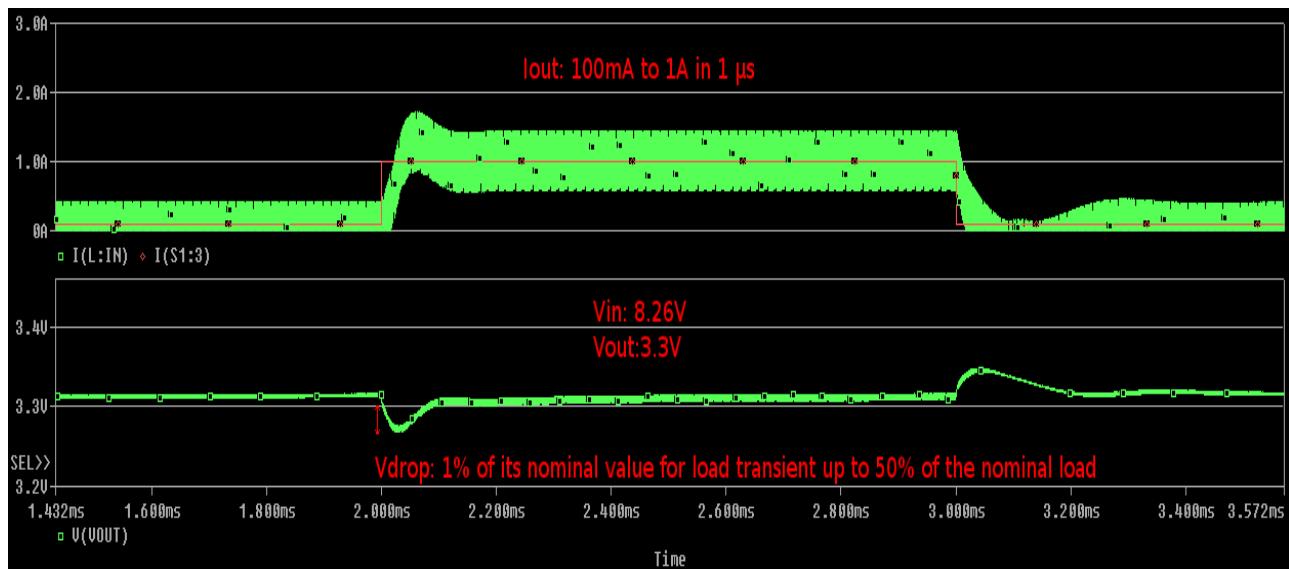


Result: Vin=6.2V / Vout= 3.3V@0.1A~2A (Full Load) are displayed in the figure 19.



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Result: Vin=8.26V / Vout= 3.3V@0.1A~1A (Half Load) are displayed in the figure 20.



Result: Vin=8.26V / Vout= 3.3V@0.1A~2A (Full Load) are displayed in the figure 21.

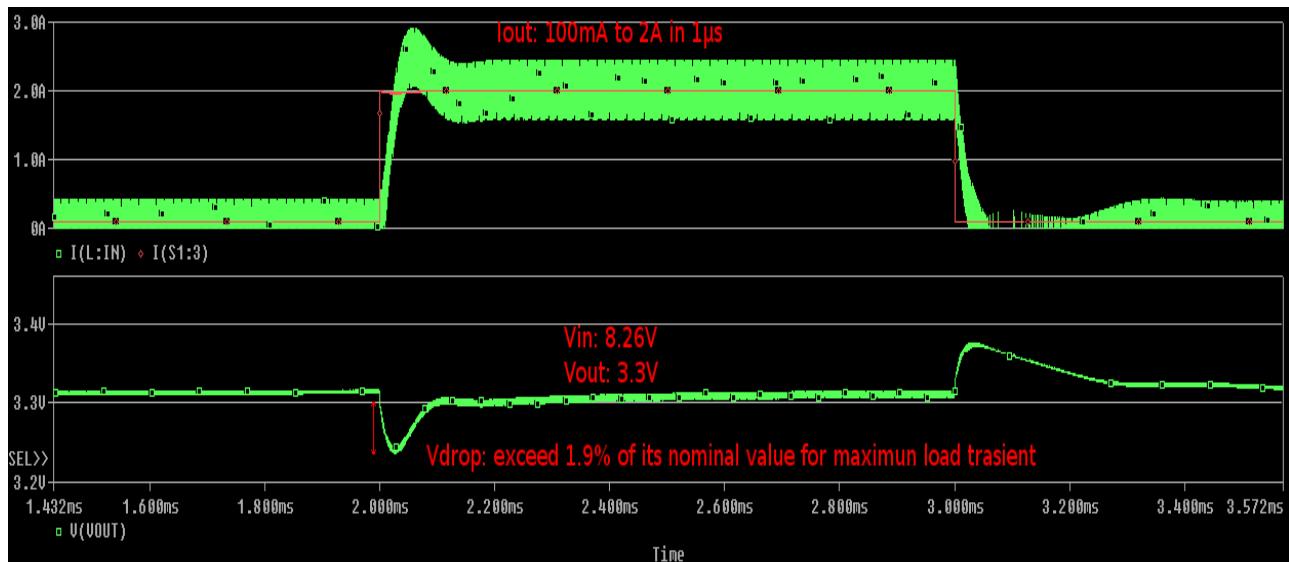
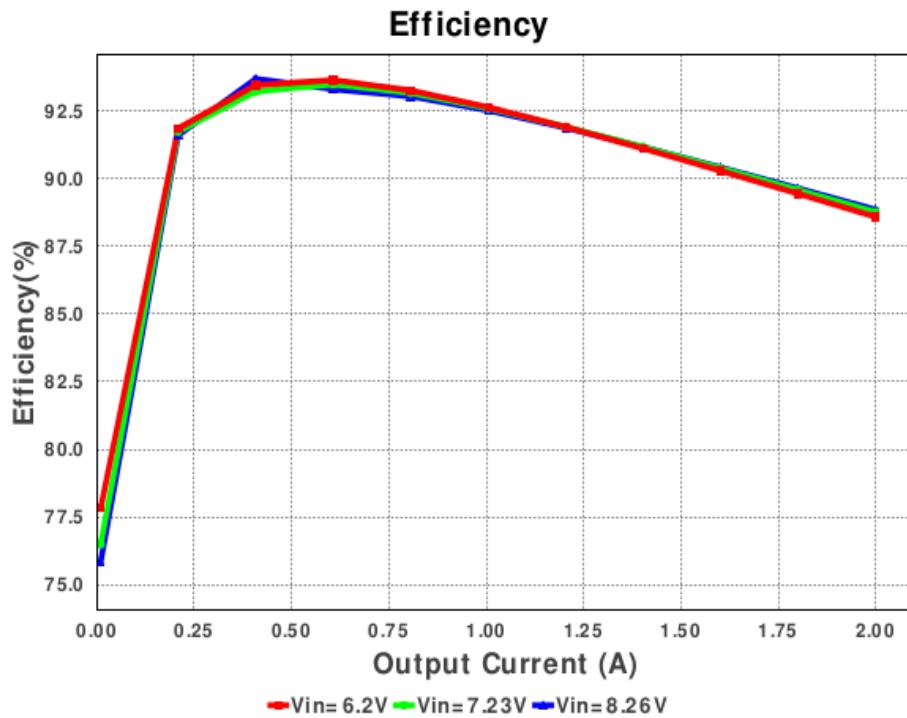


Figure 21: Result: Vin=8.26V / Vout= 3.3V@0.1A~2A (Full Load)

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Efficiency: ~92.52% at 1A (Half Load)



## Conclusion

Preliminary design shows that electrical power subsystem can generate, store, condition and distribute electrical power as necessary for all spacecraft loads to fulfill the mission requirements during all mission phases and expected modes of operation.

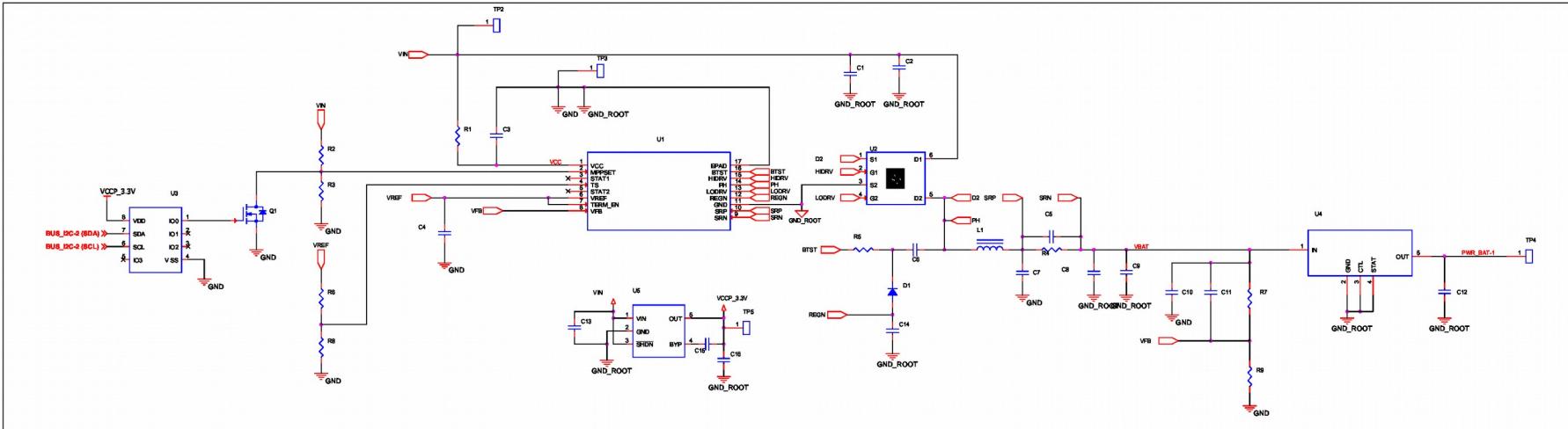
## **Appendix**

---

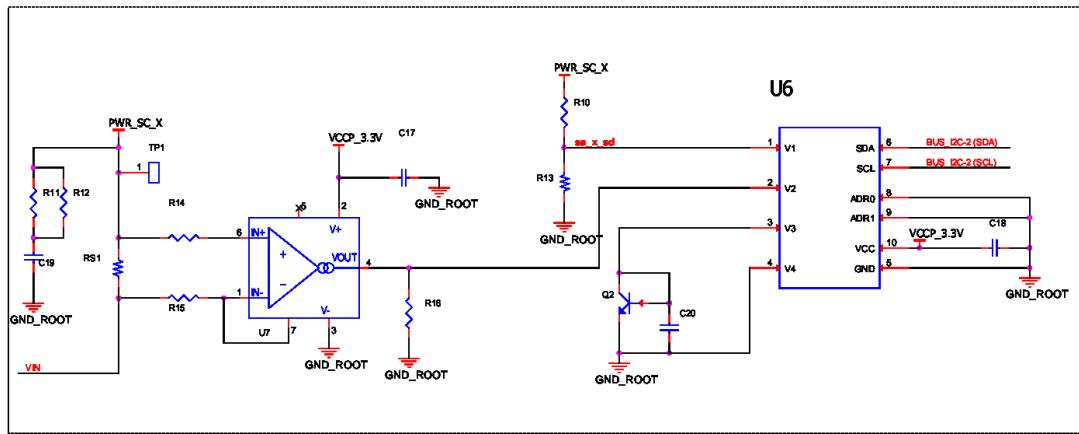
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# Schematics of Panel Board

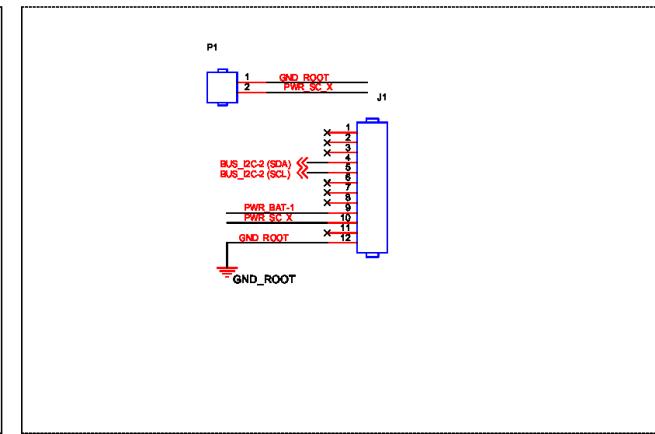
**BCR WITH MPPT CONTROLLER: OUTPUT: 8.26V max.**



**BCR WITH MPPT CONTROLLER**



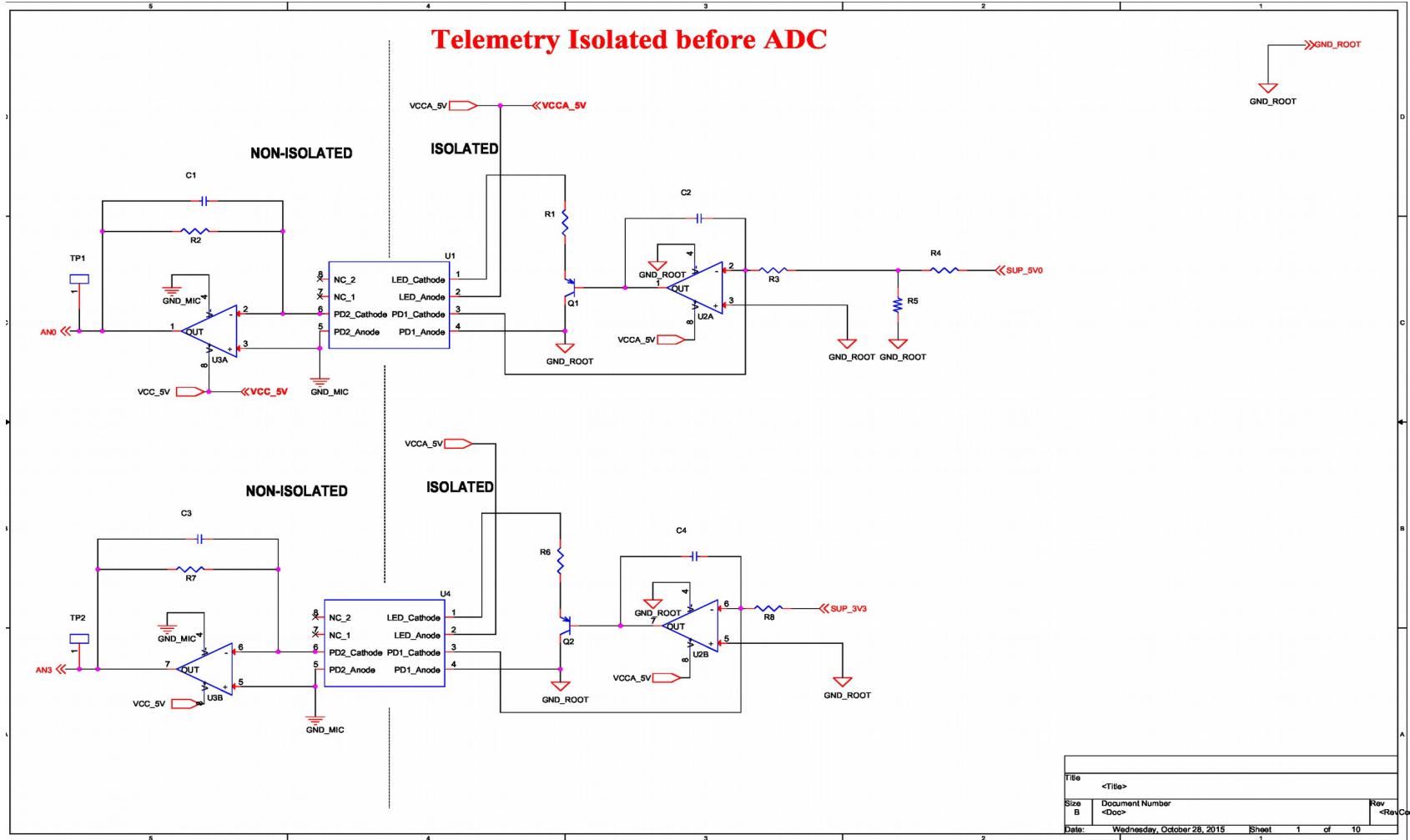
**TELEMETRY**



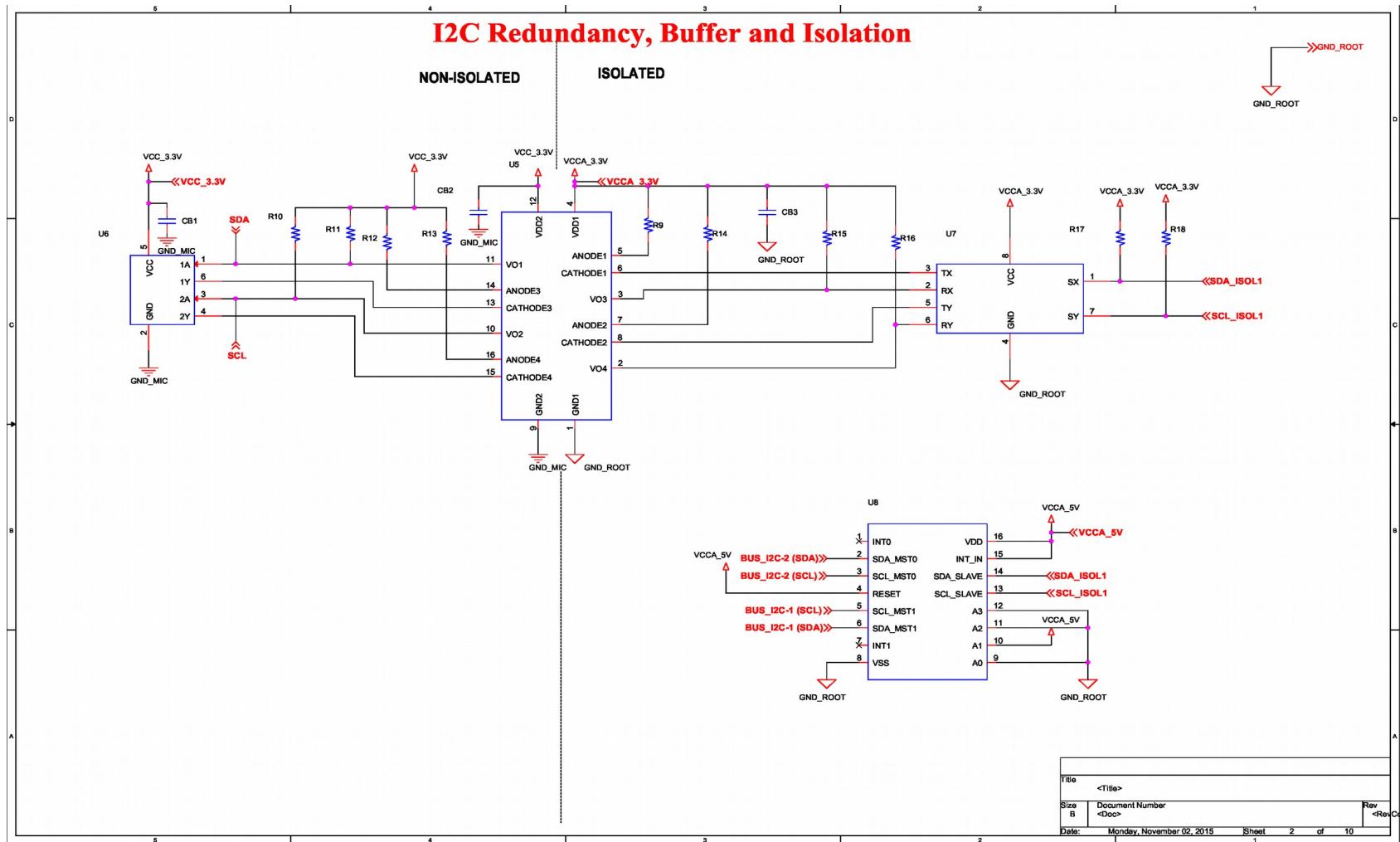
**PANEL INTERFACE CONNECTOR**

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# Schematics of EPS Board

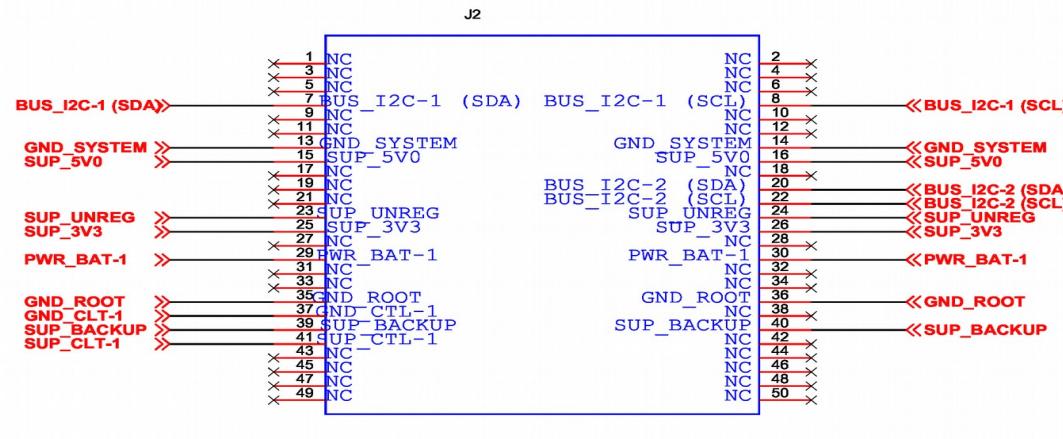


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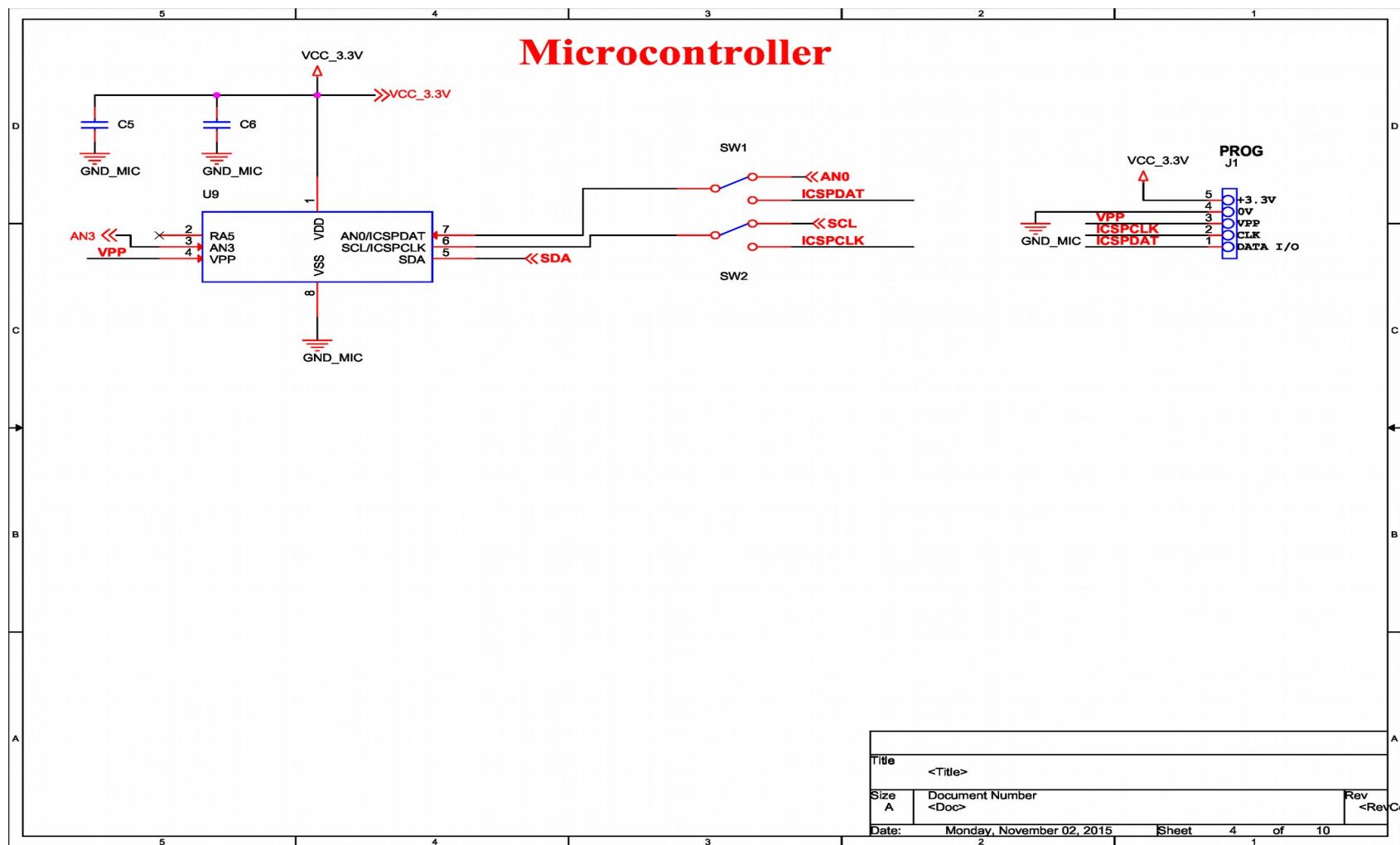
## Subsystem Interface Connector



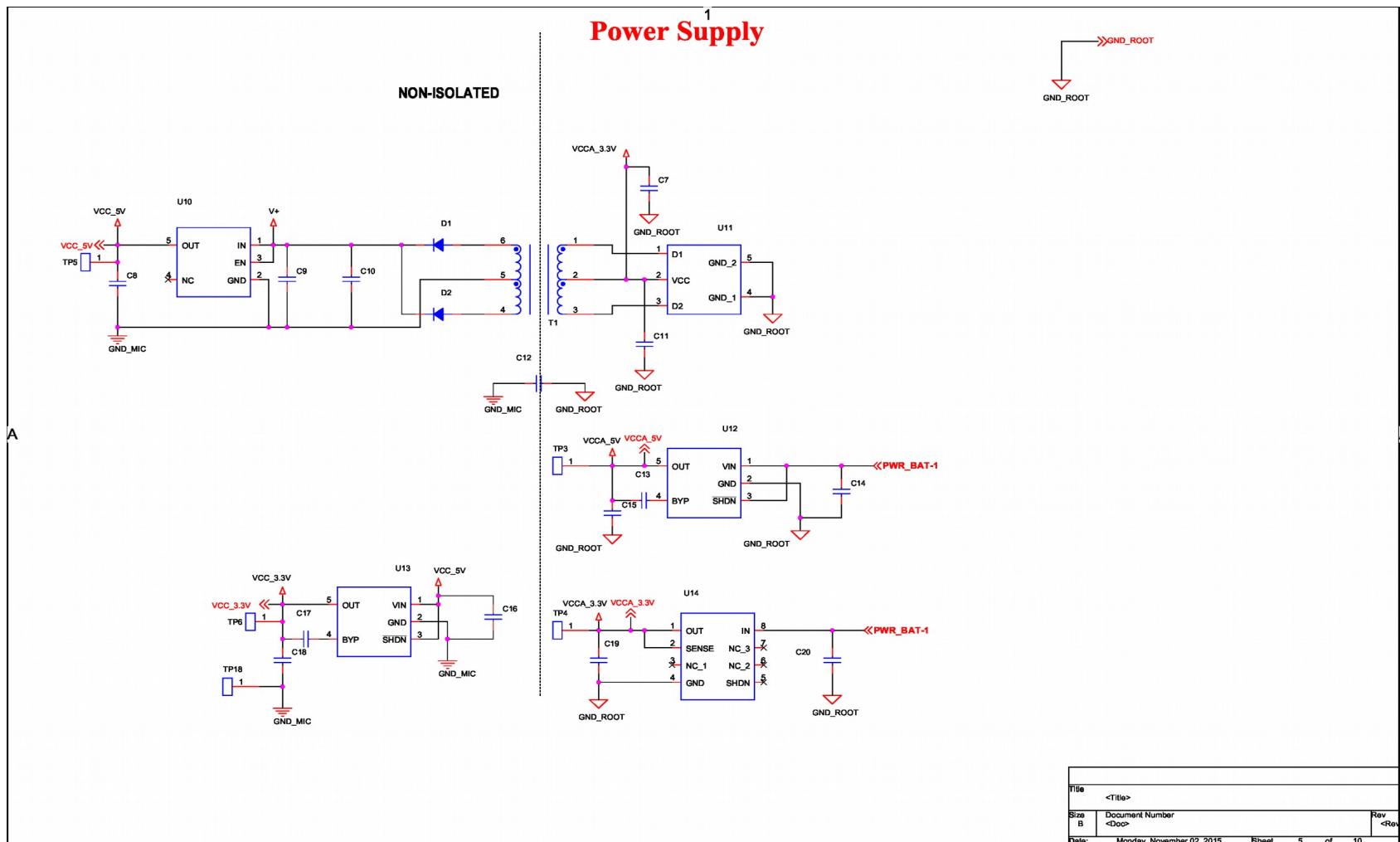
A3B-50PA-2DS

Title <Title>		Rev <RevCo>
Size A	Document Number <Doc>	
Date: Wednesday, October 28, 2015	Sheet 2	of 10

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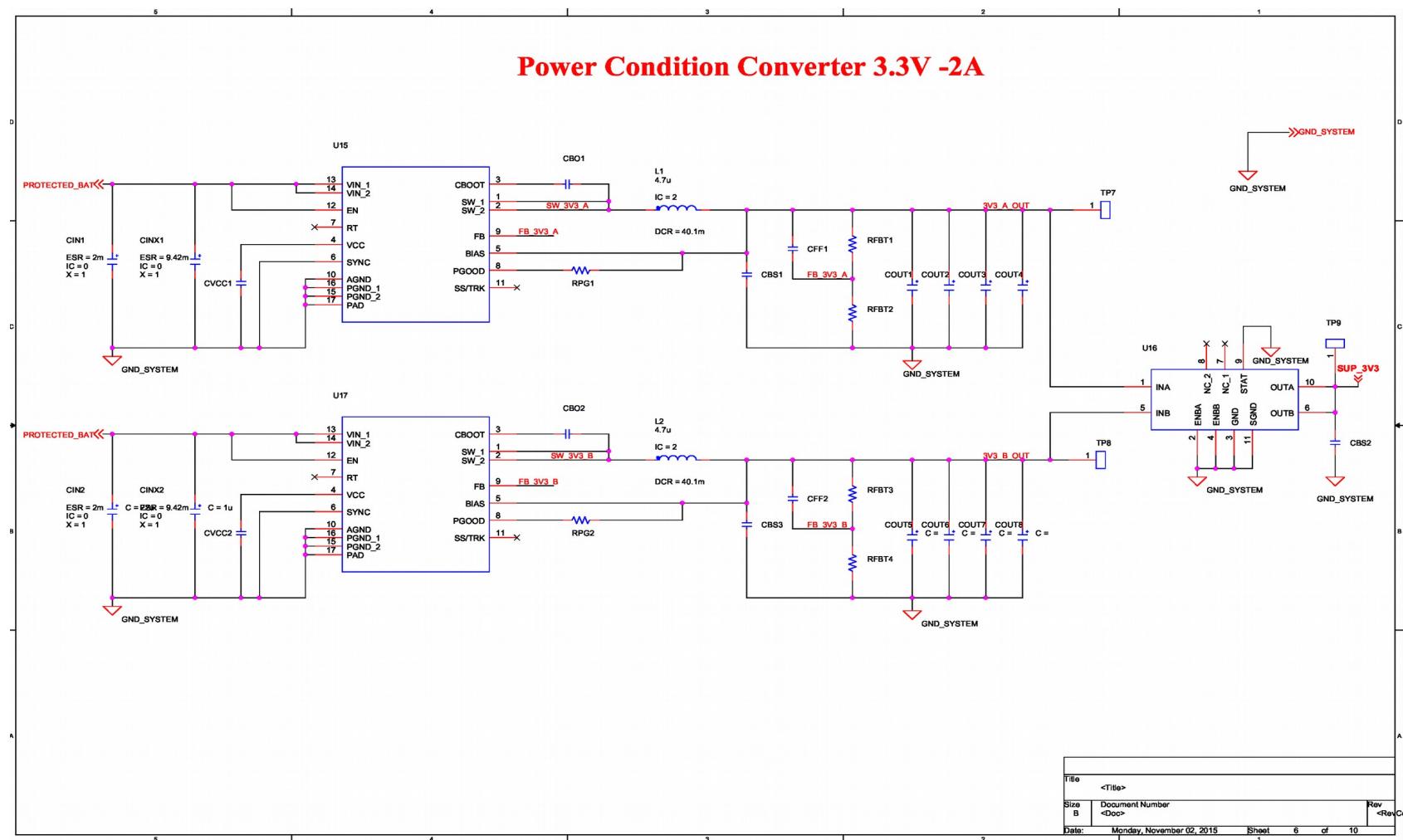


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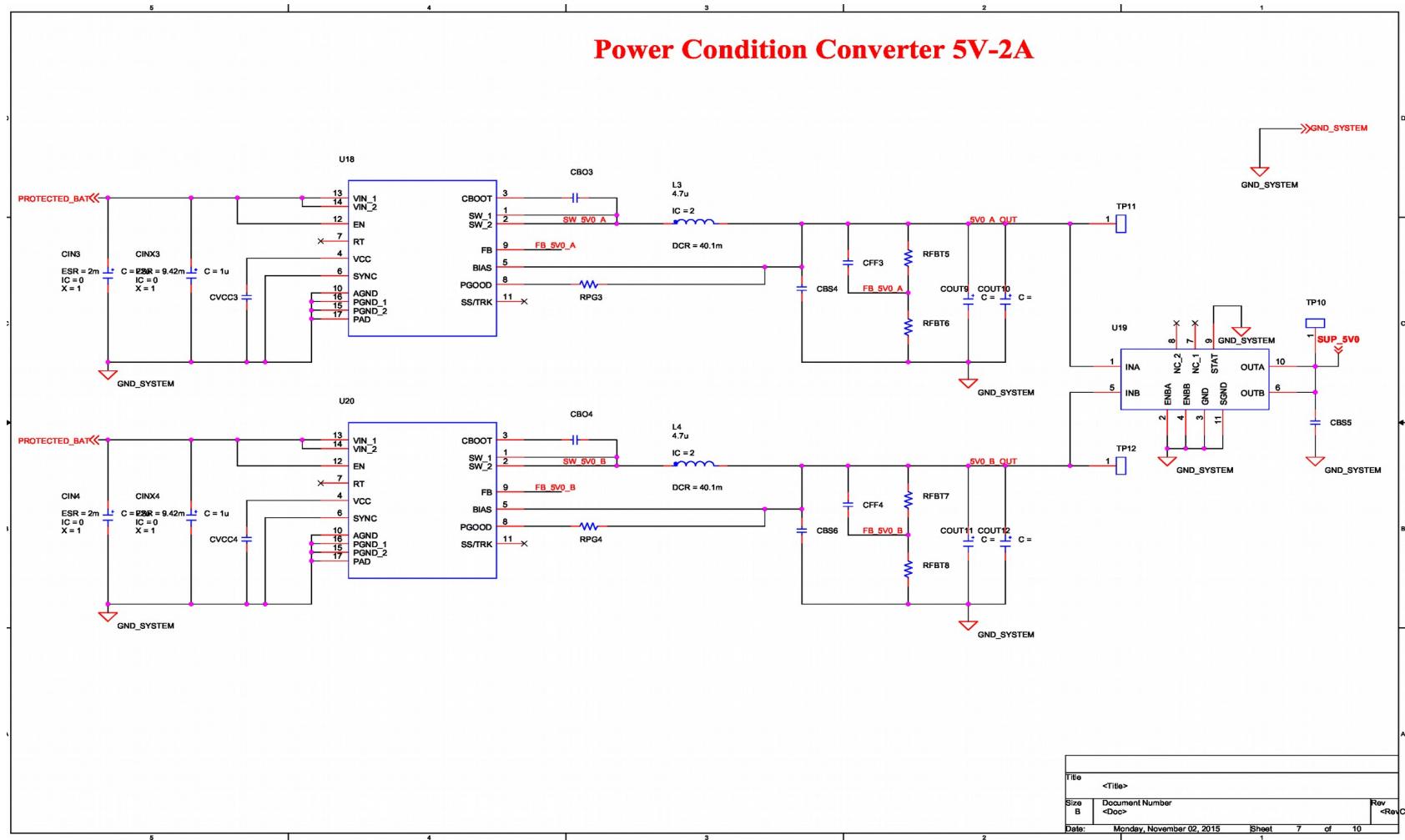
## Power Condition Converter 3.3V -2A



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Date: Monday, November 02, 2015	Sheet 1	of 10

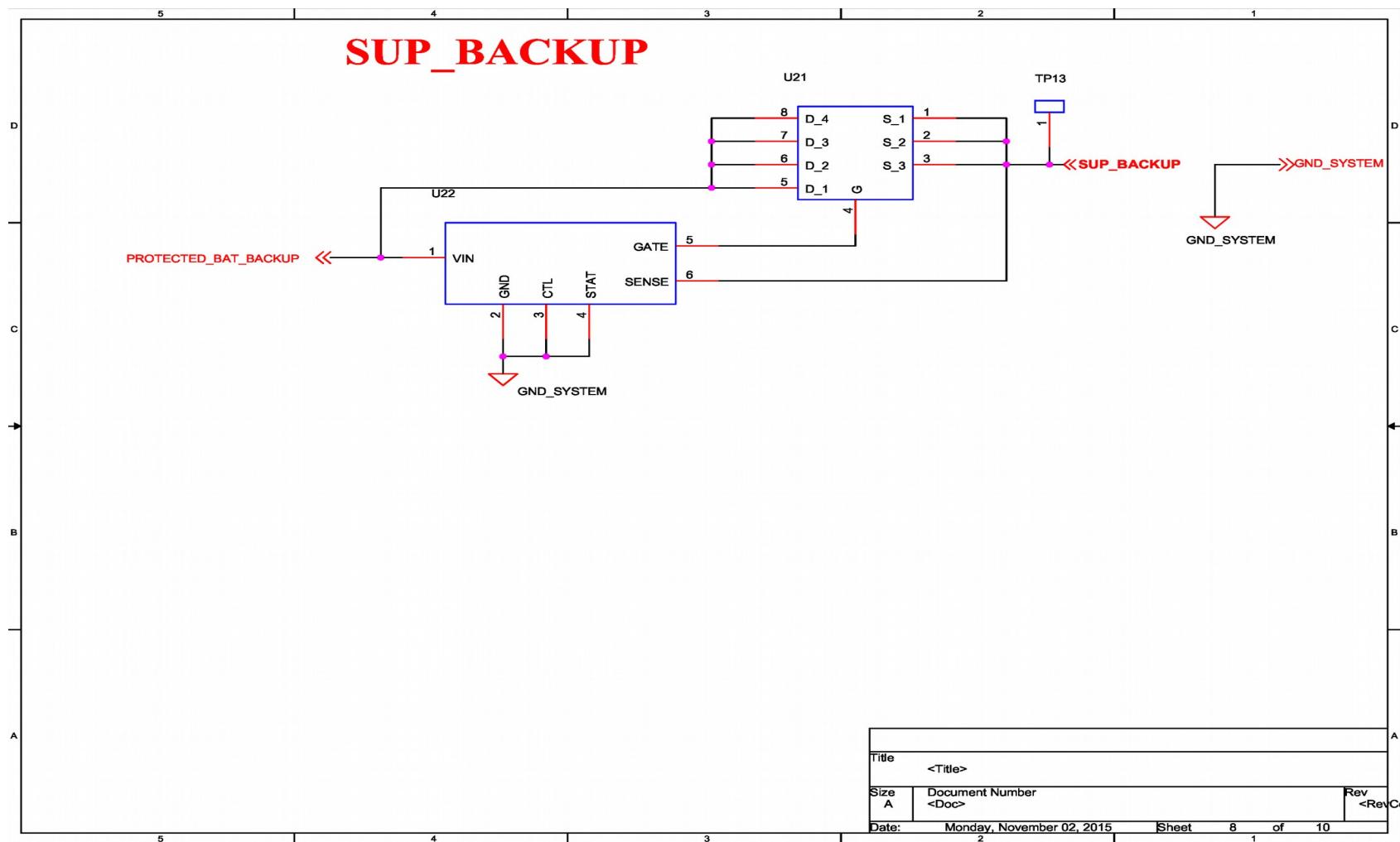
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## Power Condition Converter 5V-2A

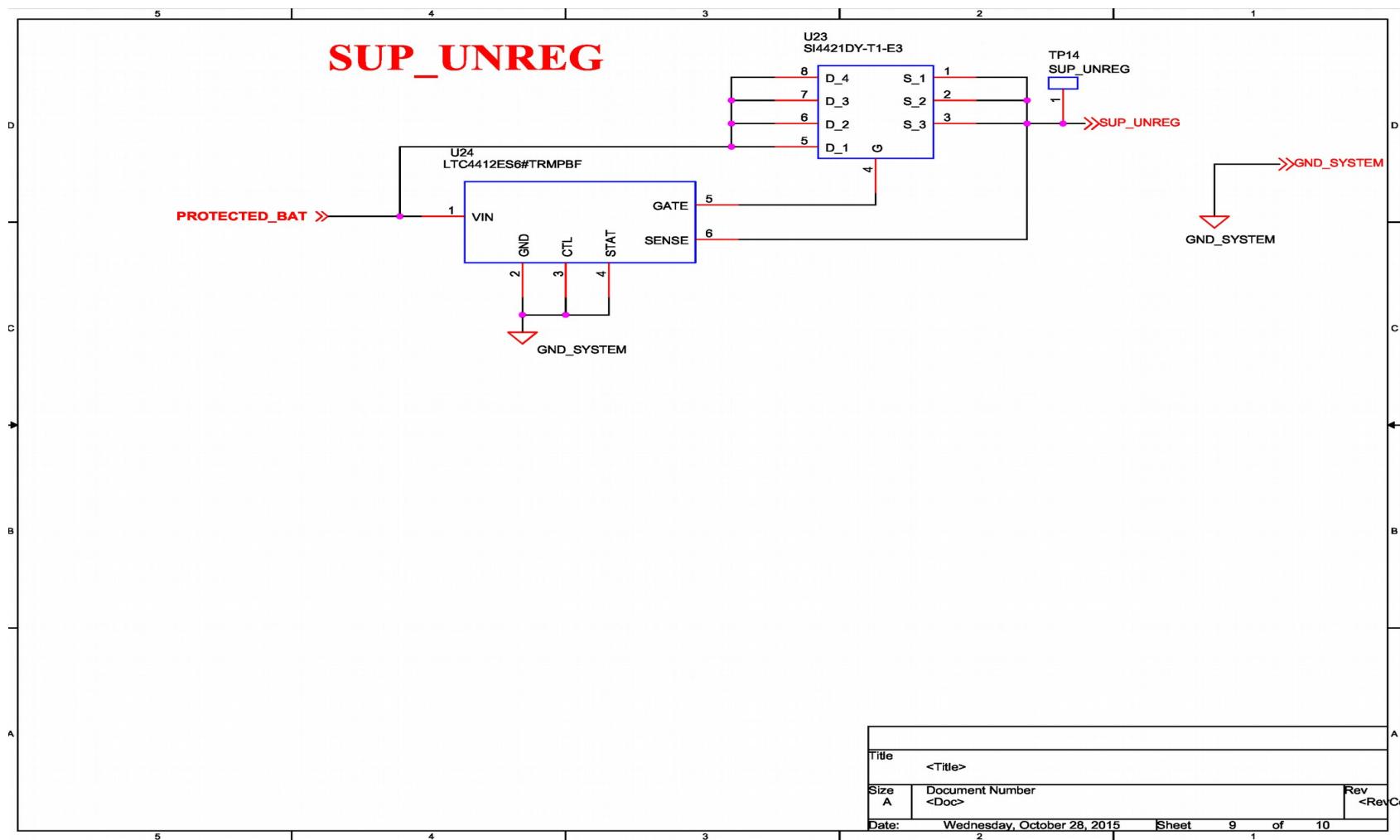


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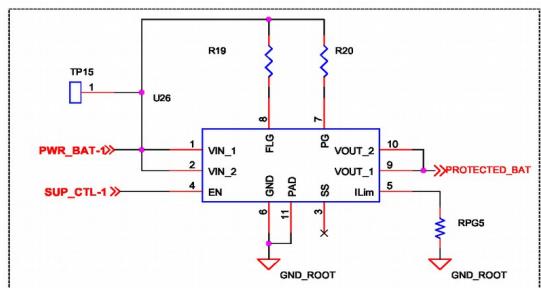


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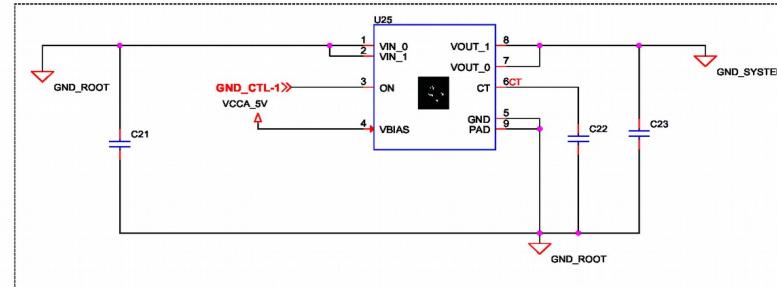
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## SWITCHES



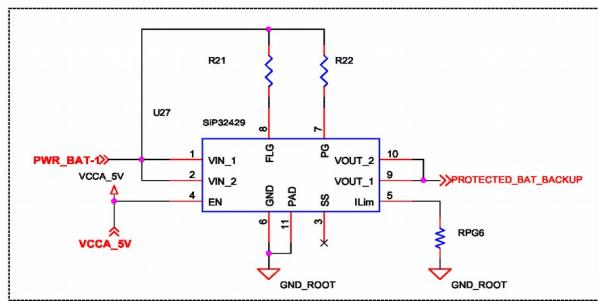
**SWITCH\_SUP\_CTL-1**

SUP\_CTL-1=LOW 0V - HIGH: 5V



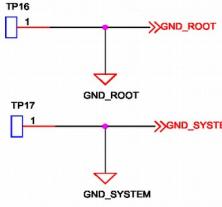
**SWITCH\_GND\_CTL-1**

GND\_CTL-1=OFF 0V - ON:5V



**SWITCH\_SUP\_BACKUP**

ALWAYS ENABLED

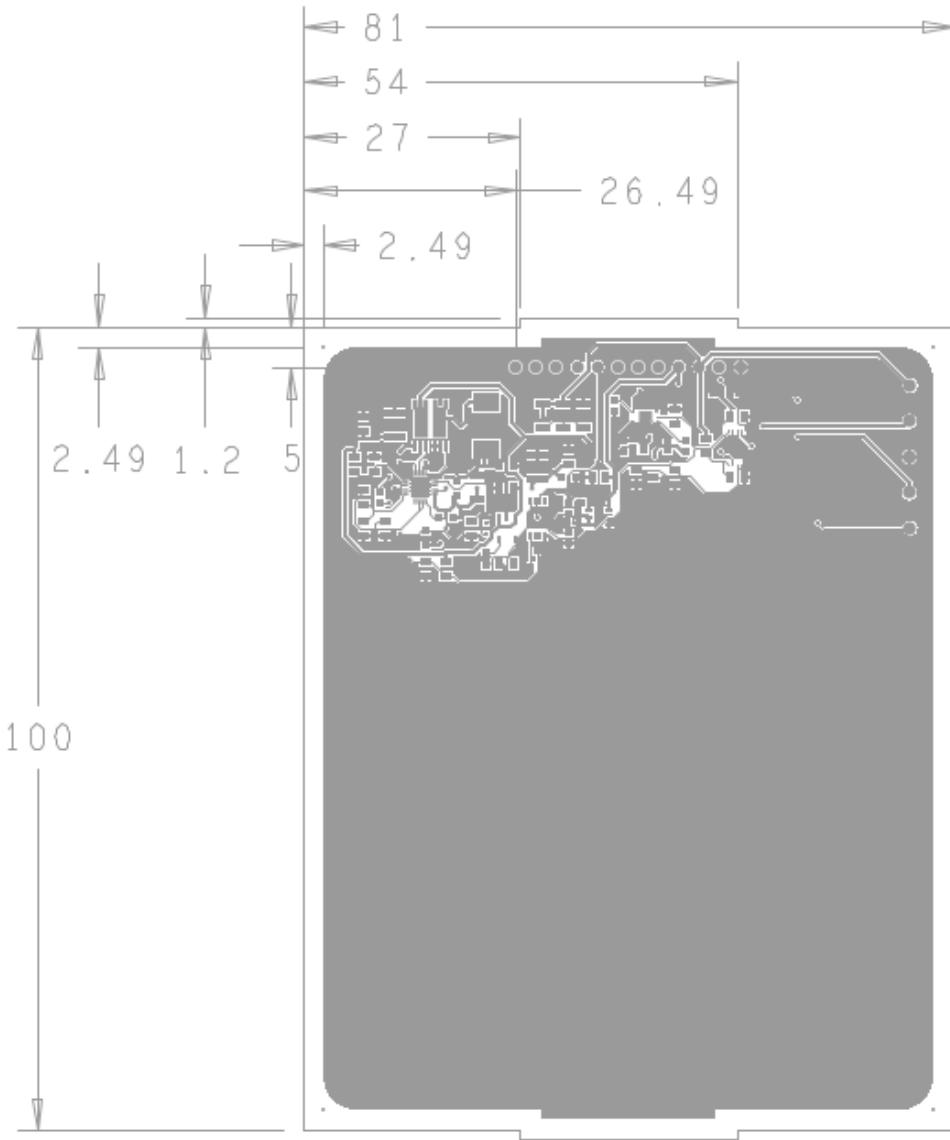


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Date: Monday, November 02, 2015	Sheet 10 of 10	

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# Layout of the Panel Board

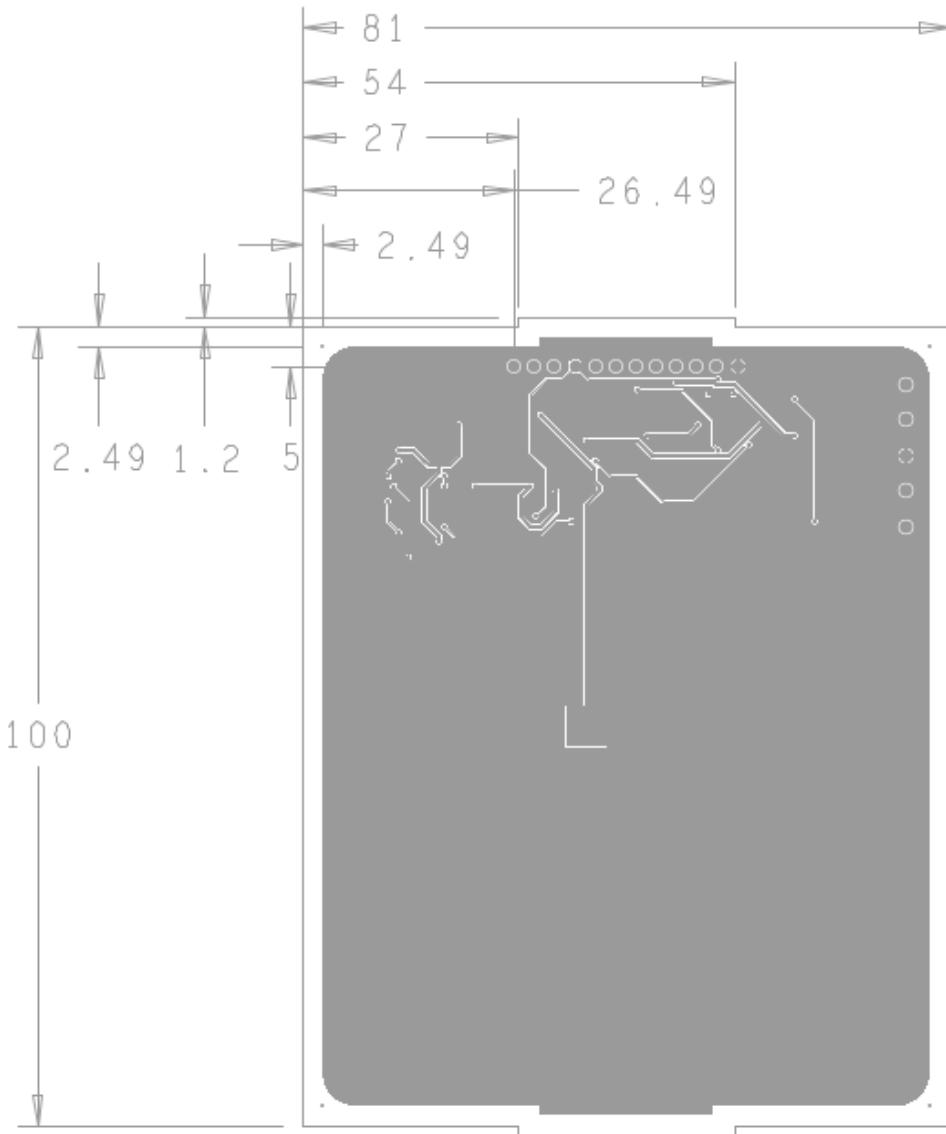
## Top Layer



Kyushu Institute of Technology / La SEINE		Copper Layer Name		Silkscreen		S Mask	P Mask	Assembly	Fab Drawing	
Board No.	Rev.	Top	Internal	Bot	Top	Bot	Top	Bot	Top	Bot
PANEL BOARD	A	L1	X	X					X	
Date: 10/23/2015	File name: panel.brd	Design: C. Salinas	Netlist: C. Salinas	Defined Date: Fri Oct 23, 2015					Time Stamp: 20:50:32	

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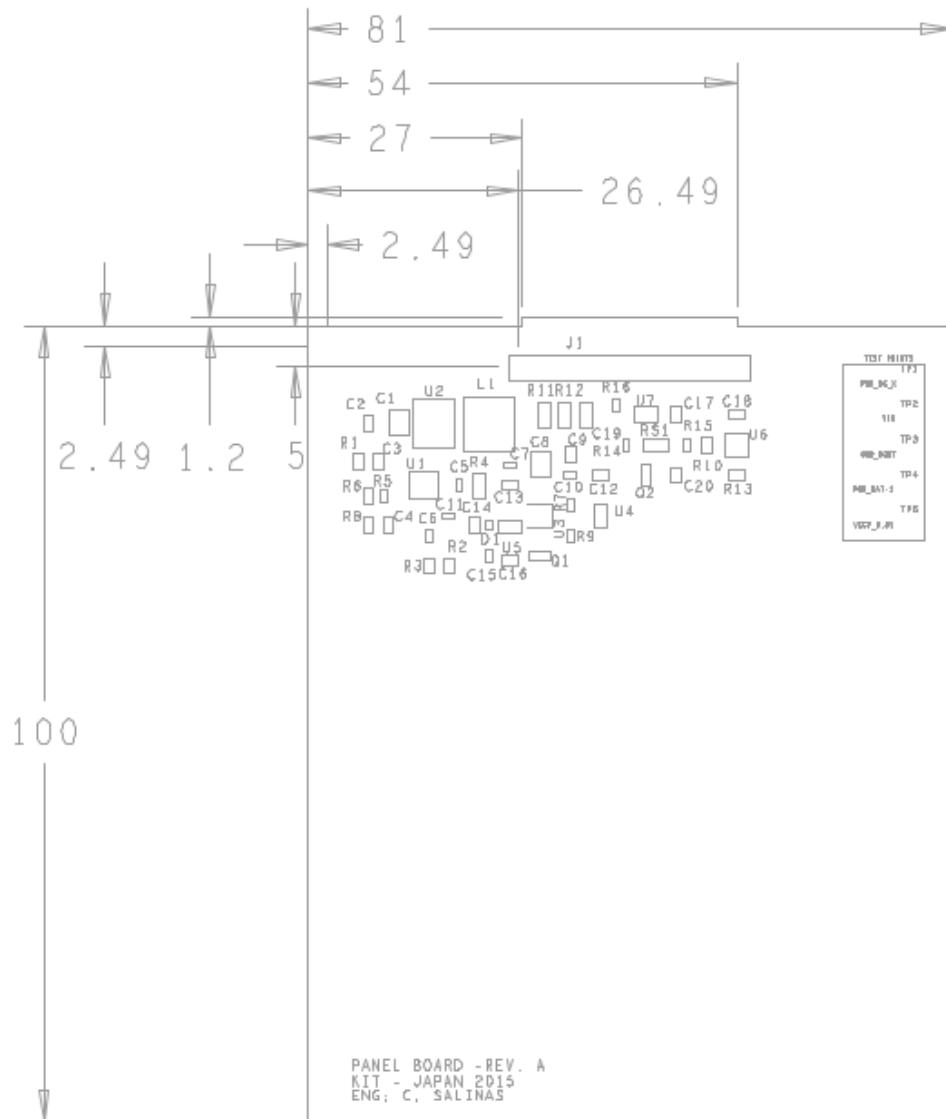
## Bottom Layer



Kyushu Institute of Technology / La SEINE		Copper Layer Name		Silkscreen	S Mask	P Mask	Assembly	Fab Drawing	
Board No.	PANEL BOARD	Top	Internal	Bot	Top	Bot	Top	Bot	
	Ver. A	X	X	L2			X		
Date	10/23/2015	File name	panel.brd	Author	C. Salinas	Print Date	Fri Oct 23, 2015	Time stamp	20:50:32

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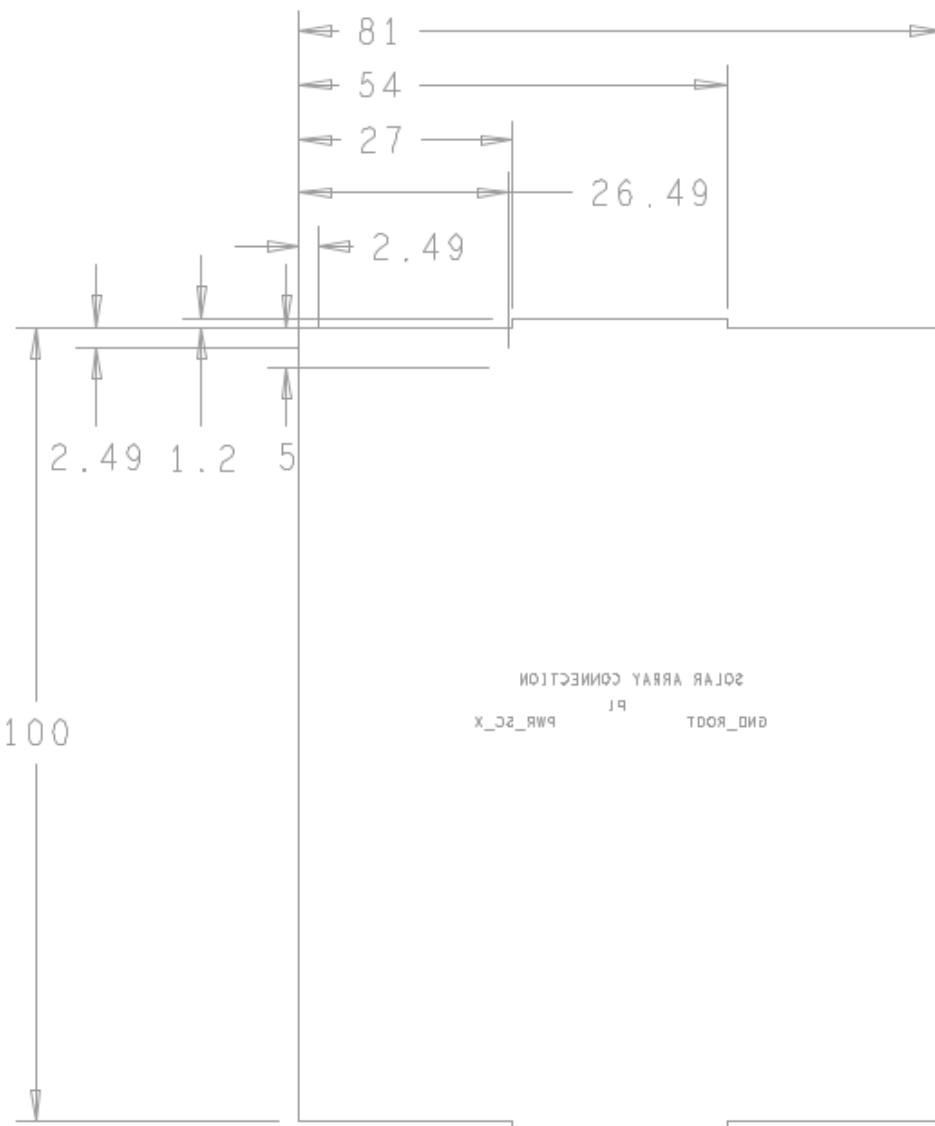
## Silkscreen Top Layer



Kyushu Institute of Technology / La SEINE	Board No. PANEL BOARD	Rev. A	Copper Layer Name		Silkscreen	S Mask	P Mask	Assembly	Fab Drawing
			Top	Internal					
			X	X	SL			X	
Date 10/23/2015	File name panel.brd	Author C. Salinas	Editor C. Salinas	Defined Date Fri Oct 23, 2015					Time stamp 20:50:32

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## Silkscreen Bottom Layer

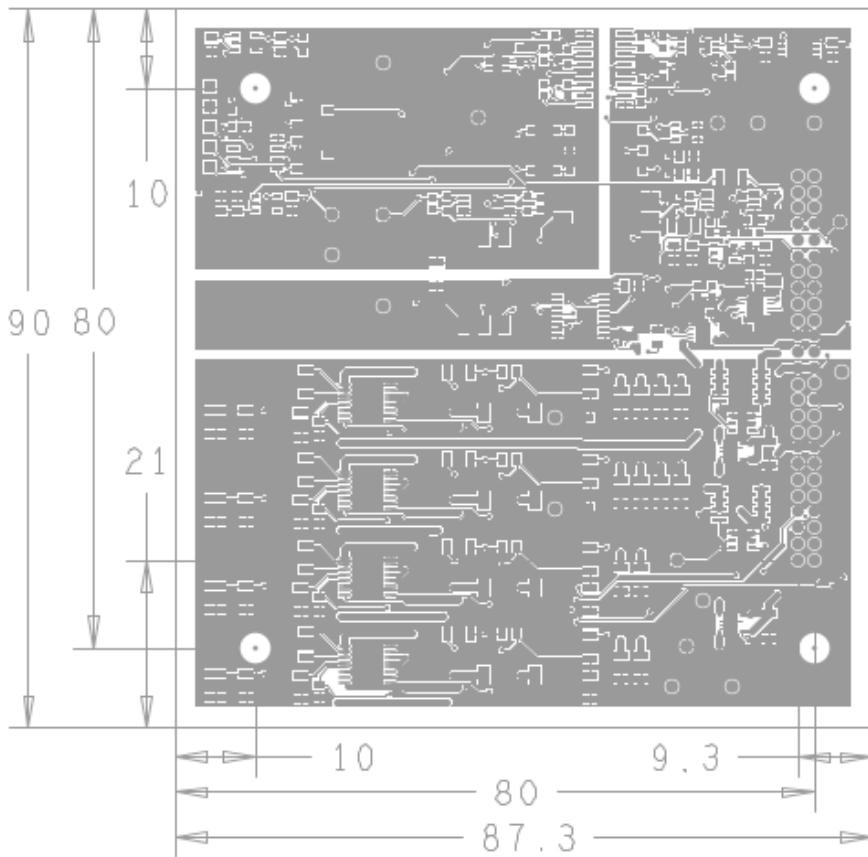


Kyushu Institute of Technology / La SEINE		Copper Layer Name	Silkscreen	S Mask	P Mask	Assembly	Fab Drawing
Board No.	Panel Board	Top Internal	Bot	Top Bot	Top Bot	Top Bot	
	Sur. A	X	X		52		X
Date	10/23/2015	File Name	panel.brd	Author	C. Salinas	Print Date	Fri Oct 23, 2015
						Time	20:50:32

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# Layout of the EPS Board

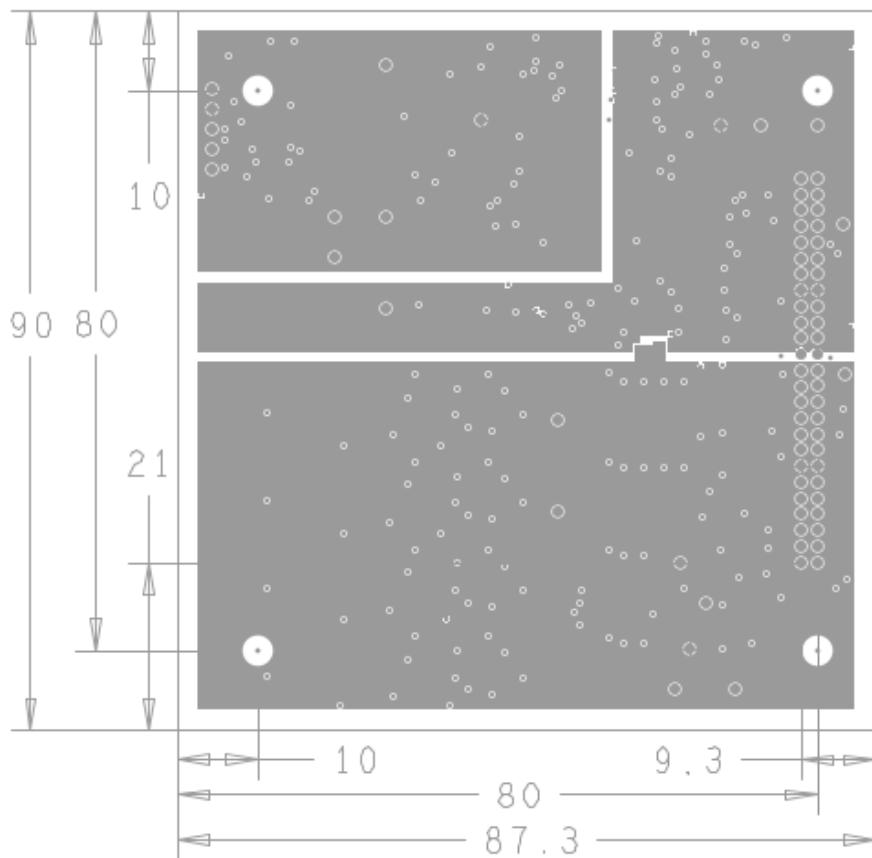
## Top Layer



Kyushu Institute of Technology / La SEINE		Copper Layer Name		Silkscreen		S Mask	P Mask	Assembly	Fab Drawing
Board No.	Rev.	Top	Internal	Bot	Top	Bot	Top	Bot	Top
EPS BOARD	A	LL				X		X	X
Date	10/23/2015	File Name:	eps_board.brd	Engg Mdl:	C_Splines	PCB Mdl:	C_Splines	Modif Pntd:	Fri Oct 23, 2015
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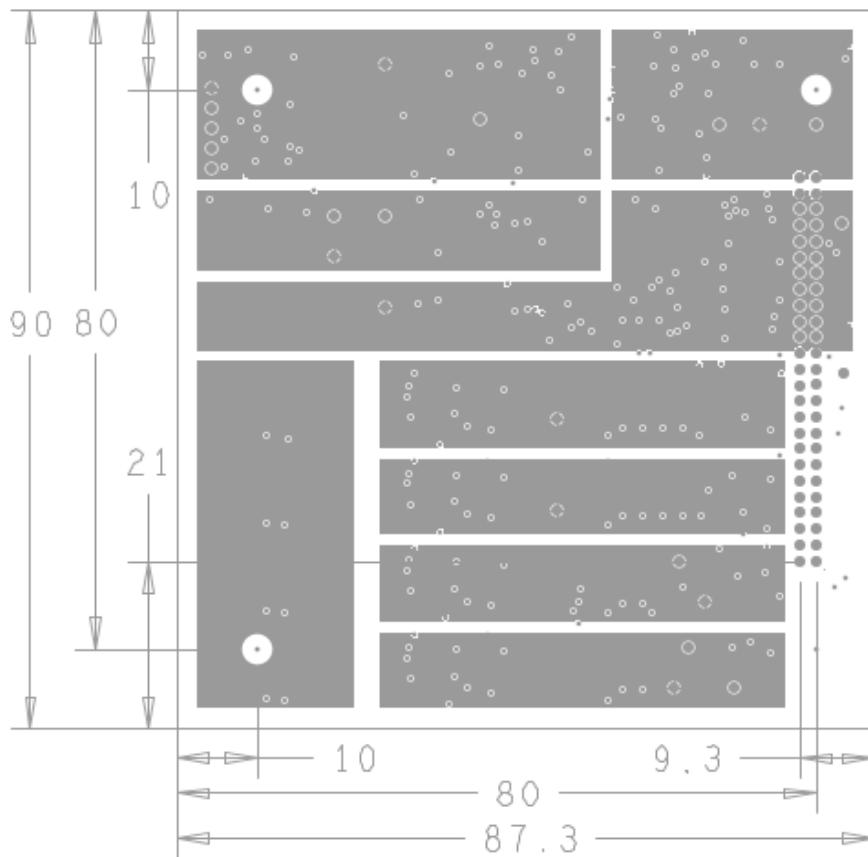
## Second Layer



Kyushu Institute of Technology / La SEINE		Copper Layer Name		Silkscreen		S Mask	P Mask	Assembly	Fab Drawing	
Board No.	EPS BOARD	Top	Internal	Bat	Top	Bot	Top	Bot	Top	Bot
Date	10/23/2015	Rev.	A	L2			X		X	X
File Name:	eps_board.brd	Engines:	C_Salings	PCB Design:	C_Salings	Multiples:	Fri Oct 23, 2015		Time Stamp:	22:21:23

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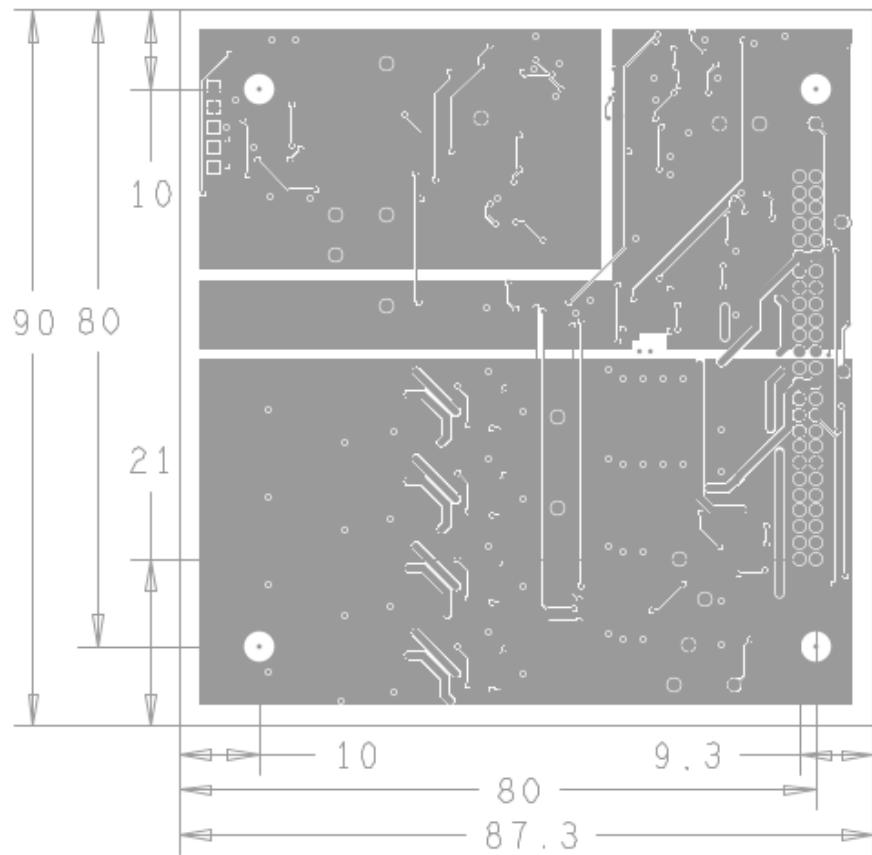
### Third Layer



Kyushu Institute of Technology / La SEINE		Copper Layer Name	Silkscreen	S Mask	P Mask	Assembly	Fab Drawing				
Board No.	EPS BOARD	Top	Internal	Bottom	Top	Bottom	Top	Bottom			
Rev.	A			L8		X		X			
Date	10/23/2015	File Name:	eps_board.brd	Author:	C. Salinas	PCB Design:	C. Salinas	Modified:	Fri Oct 23, 2015	Time Stamp:	22:21:23

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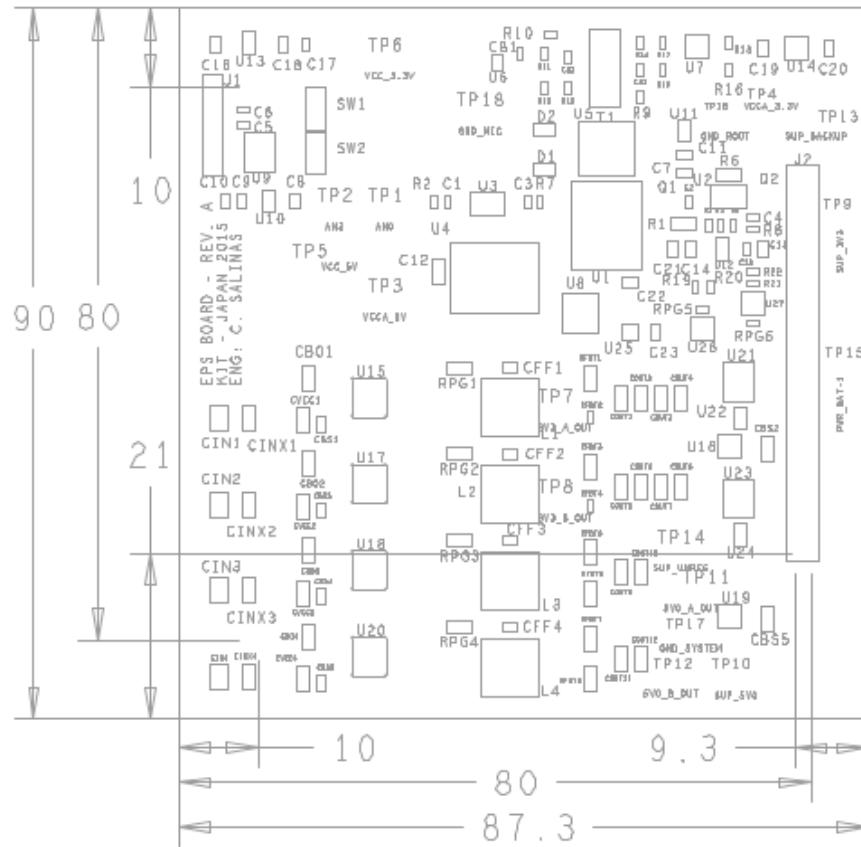
## Bottom Layer



Kyushu Institute of Technology / La SEINE	Copper Layer Name		Silkscreen		S Mask	P Mask	Assembly	Fab Drawing
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Board No. EPS BOARD	Rev. A		L4		X		X	X
Date 10/23/2015	File Name eps_board.brd	Segment C_Splines	PCB Name C_Splines	Multifile Status	Fri Oct 23, 2015			Time Stamp 22:21:23

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## Silkscreen Top



Kyushu Institute of Technology / La SEINE		Copper Layer Name	Silkscreen	S Mask	P Mask	Assembly	Fab Drawing
Board No.	Rev.	Top Internal Bat	Top Bot	Top Bat	Top Bot	Top Bot	Top Bot
EP5 BOARD	A			51	X		X
10/23/2015	PT Model#:	eps_board.brd	Right(MD): C_Salings	PCB Model: C_Salings	Weld Date: 00:00	Fri Oct 23, 2015	TI Date Stamp: 22:21:23

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