Graph Theory Approach for Automatic Test Board Parameter Extraction in Multisite IC Testing

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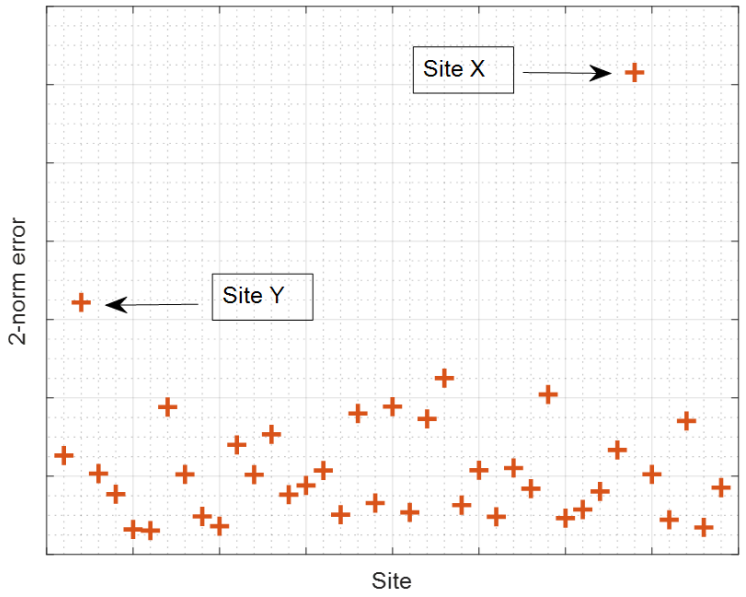
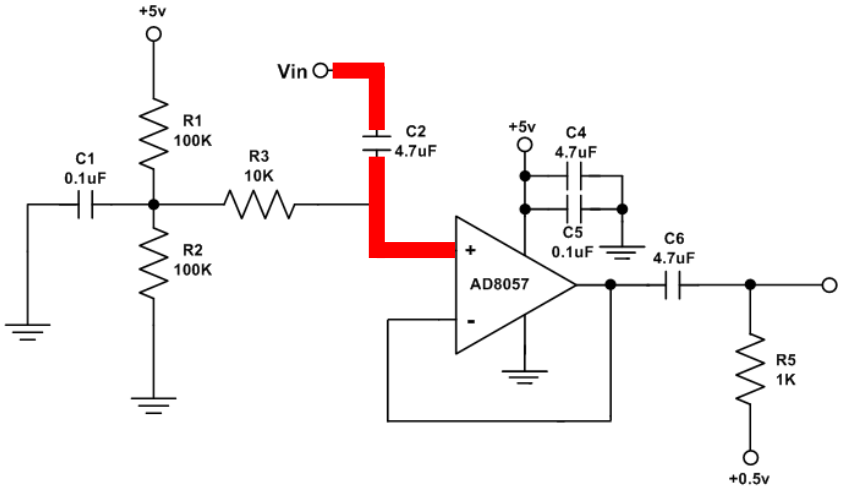
Motivation

- Multisite Testing is proven to save cost and testing time
- Site-to-site (s2s) variation in Multisite testers directly impacts yield loss
- Analysis from test wafers
  - Proven to find some issue sites
  - WBD, CC, QQ algorithms
  - **Can't define root causes with only die data**
- Board Parameter (BP) Analysis
  - Adds level of pre-fabrication verification in ATE development
  - Arduous manual process – requires automation
  - **Root causes for s2s variations come from hardware variations**

NEED BP Extraction Method that…

- Can extract board parameters **relevant to s2s variations**
- Is an **automated** end-to-end solution

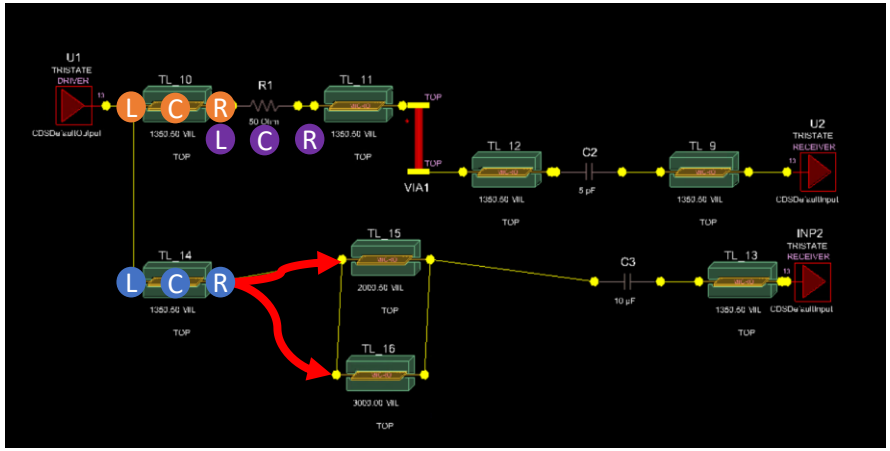




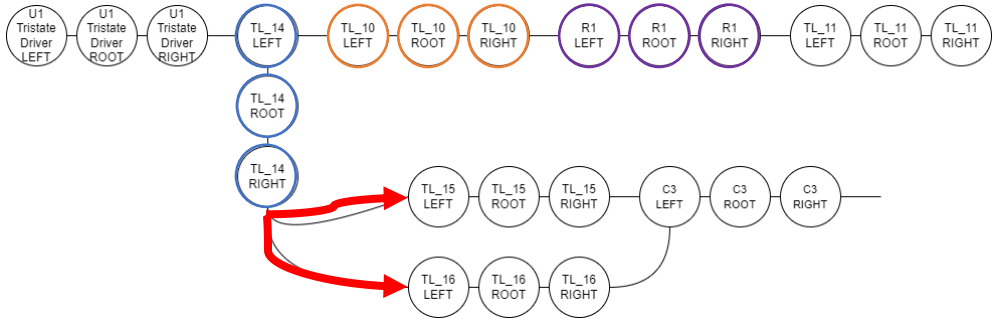
Method

- The “topology” of a testing circuit can be represented as a graph with nodes and edges
  - Topology: physical layout of PCB
  - Nodes: PCB components, traces, vias, etc.
  - Edges: component connections
- **General** – Graph theory is agnostic to Probe Cards and CAD tools
- **Flexible** – Graph traversals open access to information about any path in the topology
- **Automated** – Graph API can be run on any set of topology datafiles
- Multi-path edge case
  - Depth-first search

Circuit Topology



Node Graph Representation



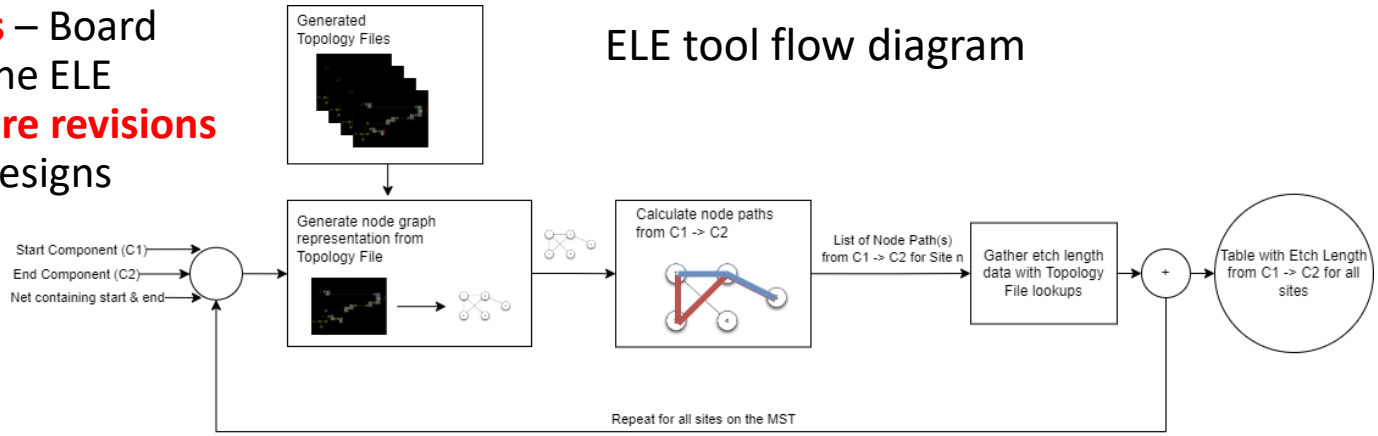
Results

- Etch (trace) length chosen as a parameter to test node graph approach
  - Adaptable to analyze any BP related to PCB topology
- **Automated end-to-end solution** – Etch Length Extractor (ELE) tool applies node graph approach to all sites on TI probe card design
  - Current implementation limited to Cadence Allegro designs (prototype needs standardization)
- **Detect root causes** – Board parameters from the ELE **motivated hardware revisions** on future TI MST designs

Etch length data from TI Multisite Probe Card

	A	B	C
	C1.C2.DIST.1	C1.C2.DIST.2	
	4409.941		
	7755.13		
	4608.838	4608.496	
	5736.229		
	4608.305		
	3617.021	3617.124	
	4647.202	4647.305	
	5372.46	5372.118	

ELE tool flow diagram



Discussion

Summary

- Graph traversal applications opened access to BP's that previously couldn't be obtained
- Automation made extraction feasible and enhanced datasets for WBD, CC, QQ algorithms

Future Work

- Expand graph method to represent **entire site as a single node graph**
  - Graphs are currently limited to groups of discrete components
- **Standardize** graph representation to work for any CAD tool
- Use BP's to **enrich simulation models**