

Graph theory can help detect site-to-site variation in Multisite Testers

Graph Theory Approach for Automatic Test Board Parameter Extraction in Multisite IC Testing

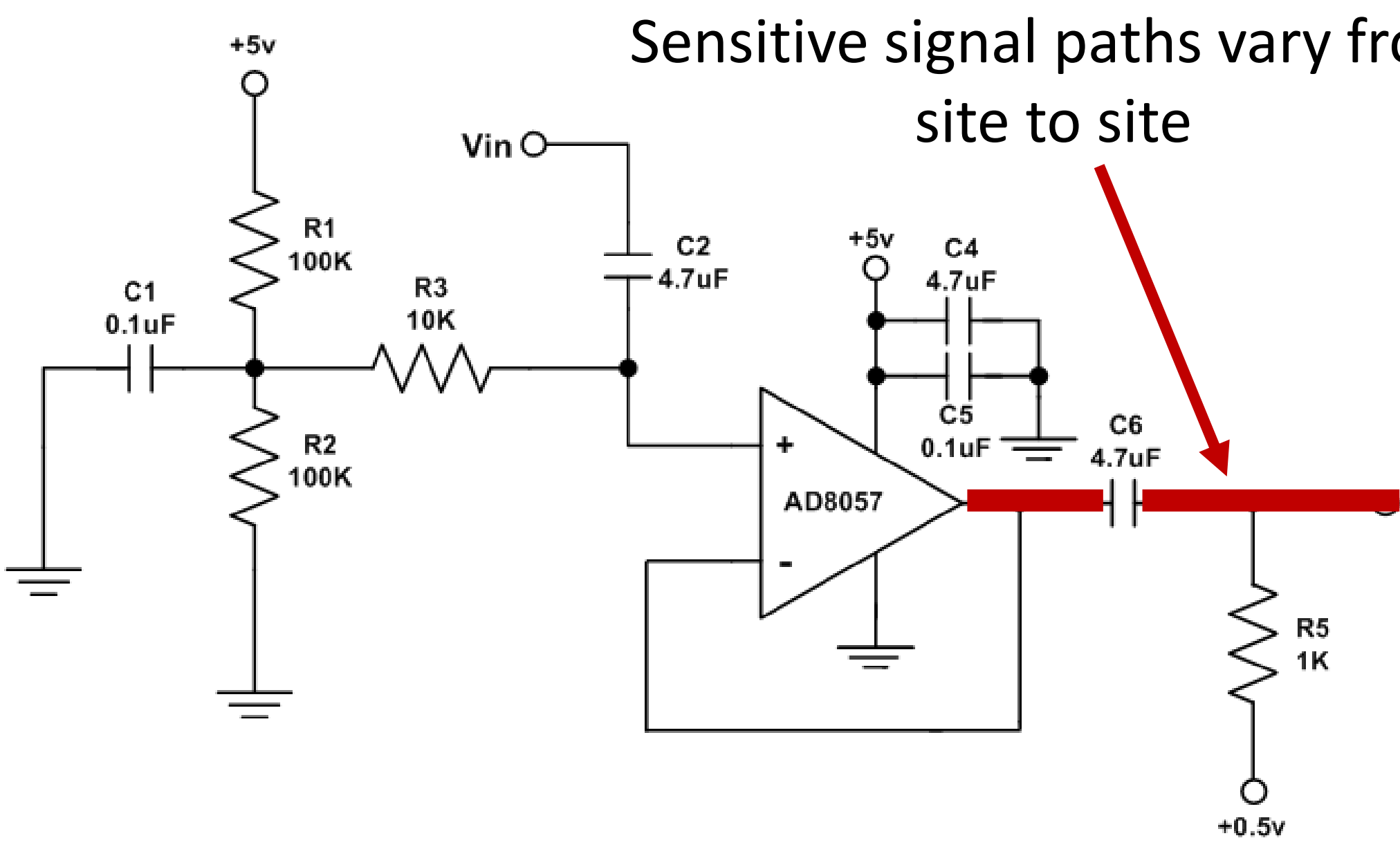
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Take a picture to download the full paper at my ETS 2022 research repository
https://github.com/AbrahamSteenhoek/ETS2022_Research_Repository

MOTIVATION



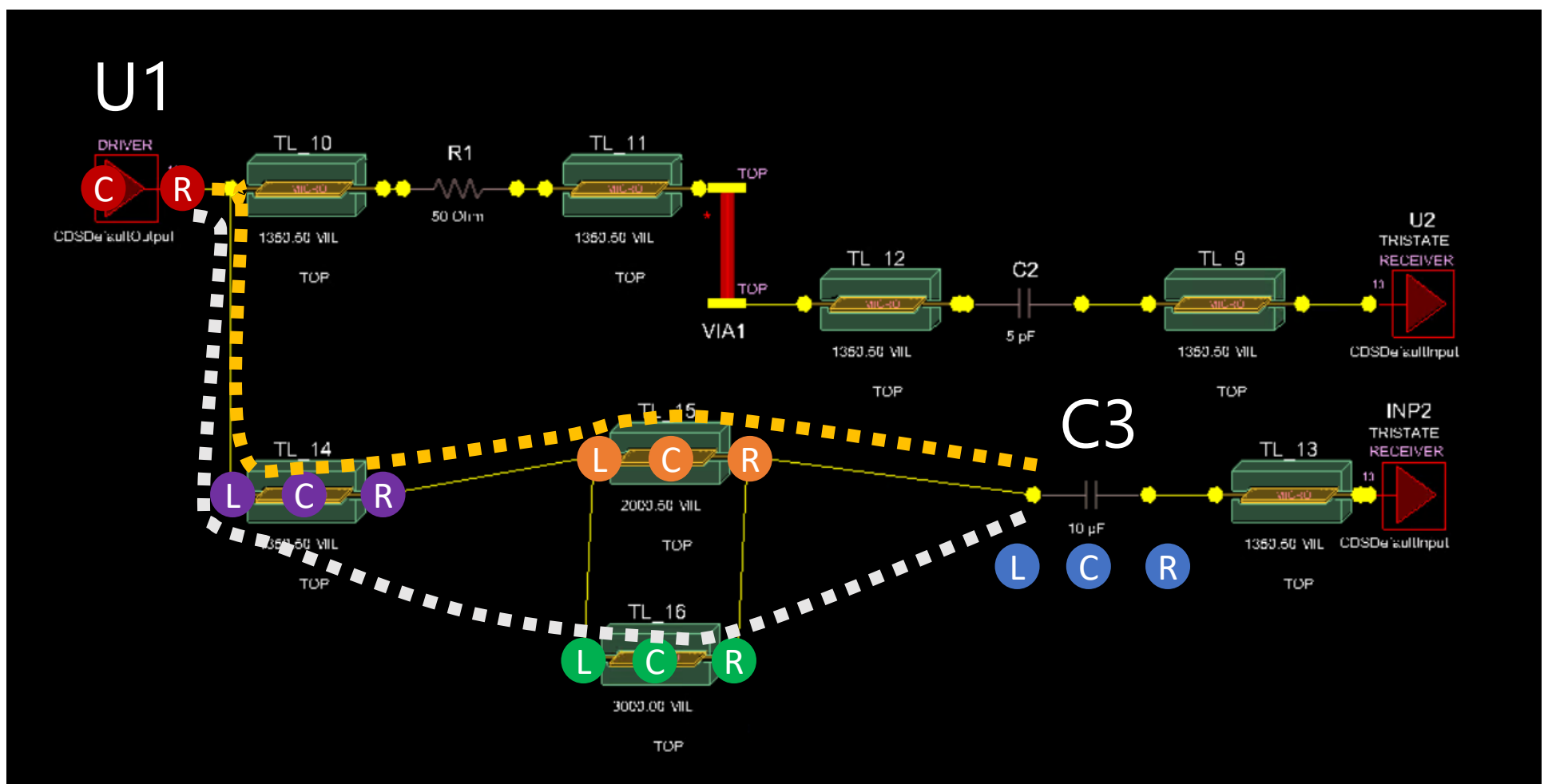
- Site-to-site (s2s) variation in multisite testers negatively impacts yield loss
- Analyzing parameters related to MST hardware can point out root causes for s2s variation
 - Arduous process if parameters are collected manually

NEED a method for extracting hardware parameters that:

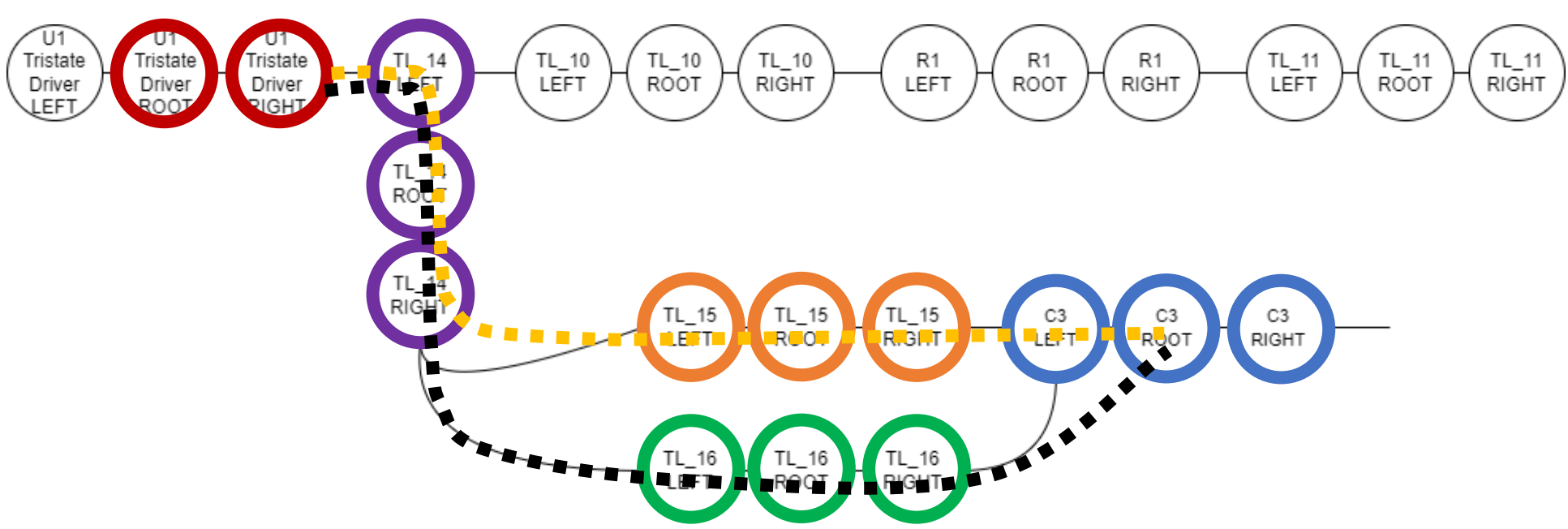
- Can extract params **relevant to s2s variations**
- Is an **automated** end-to-end solution

METHOD

Topology of sample test circuit



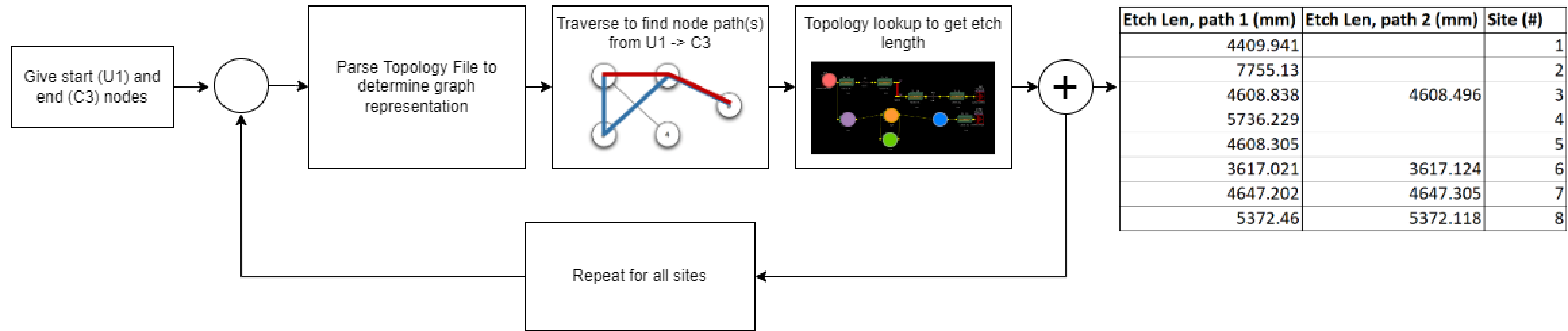
Graph representation of topology



- The “topology” of a testing circuit can be represented as a graph with nodes and edges
 - Topology: physical layout of PCB
 - Nodes: PCB components, traces, vias, etc.
 - Nodes contain metadata (e.g. etch length)
 - Edges: component connections
- **Flexible** – Graph traversals can analyze any parameter related to PCB topology
 - The path U1 → C3 is found with a traversal
- **Automated** – Graph analysis can be run on any set of topology data files
- **General** – Graph theory approach is agnostic to Probe Cards and CAD tools

KEY RESULTS

ELE Tool Flow Diagram



- Etch Length Extractor (ELE) tool applies our approach on real MST designs
- Etch lengths found with ELE match measurements found with manual processes
- **Flexible** – Extracts any parameter related to path between two components
- **Detected root causes** – Board parameters from the ELE motivated hardware revisions on future TI MST designs
- **Automated end-to-end solution** – ELE can be scripted to extract parameters from every site on a MST design automatically