Graph Theory Approach for Multi-site ATE Board Parameter Extraction

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***Abstract*— This paper describes a low-cost technique for extracting parameters of interest for test boards used in multisite automatic test equipment (ATE). In the proposed approach, physical elements and nets on the PCB are represented as a graph with nodes and edges. Graph traversal algorithms are then used to extract data about the connections between specific components on each test site. This approach automates the previously slow and manual process of generating the topology files necessary to extract board parameters. The proposed method is implemented on a multisite test board, and results are presented.**

Keywords—Multisite Testing(MST), Automatic Test Equipment (ATE), Graph Theory, Site to Site (s2s) Variations, Test Board.

I. Introduction

Multisite testing (MST) reduces test costs and time by simultaneously testing integrated circuits (ICs). It can be used both at the wafer probe and final tests, hence its wide acceptance and use. The method reduces all test cost contributors, not only the capital cost of ATE, and has been proven to be significantly cheaper than low-cost sequential ATE [1], [2].

Site-to-site variation (S2S) is one of the demerits of multisite testing. By this, we mean unwanted tester/probe card influence on test results resulting in test site dependency [3]. If not carefully monitored, S2S variations can lead to wrongful labeling of good ICs as "faulty" and loosening of test specifications limits for passed ICs.

Various statistical analysis on multisite volume test data has been successfully used to identify and correct issue test sites (test sites with unacceptable S2S variations) [4]–[6]. Our approach is to analyze hardware characteristics of the MST probe card, referred to in this paper as board parameters (BPs). BPs encompass any parameter related to the physical characteristic of the PCB, including RLC of components, coupling coefficients between traces, trace length & width, number of vias in a trace, and regions on the board that a trace intersects.

Historically, board parameter extraction has been a difficult process because there are not many automated end-to-end solutions. As MST ATE designs increase in complexity, having any kind of manual effort in the data extraction process becomes an exponentially increasing issue.

In this paper, we propose a novel method to extract board parameters from existing MTS ATE designs by applying graph theory methods. Physical elements on the PCB and their interconnects are represented as a graph with nodes and edges. Graph traversal algorithms can then be applied to extract data about the connections between those components on the probe card. This approach allows engineers to automate the collection of board parameters from dense and complex MST designs, and the graph representation provides a rich contextual insight into the connections between components on each site of the MST. In addition, test engineering teams can use this approach to perform test board validation of their probe cards, saving development time and costs.

II. Xnets – Motivation for a Custom Solution

The concept of Xnets is important to understand when evaluating different BP extraction tools. Once a PCB layout is created in Allegro, the software makes a list of nets and Xnets on the PCB. A net is one connection node on a schematic. An Xnet is the result of an automatic process performed by Allegro, where all of the nets that contain only discrete components are lumped together into one summed Xnet. For example, the thick red section highlighted in Fig. 1 is a net, while the net touching the positive side of R1 and C2, and the net touching the negative side of C1, R1, and C2, is one Xnet. Xnets can provide information that nets alone cannot give, such as the length of the path from F1 to C2.

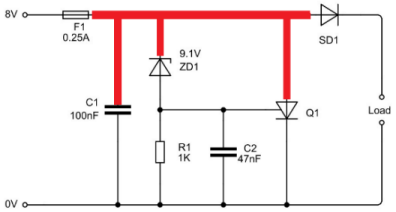

Fig. 1. Quick reports can only extract the etch length of nets(red), but what if we want the etch length of F1 to C2?

We evaluated SigXplorer in addition to Allegro's quick-reporting tools and found out that they both were not satisfactory in automating the extraction and analyzing multiple Xnets. This motivated the development of a custom tool to generate, collect, process, and analyze Xnets to extract BPs.

Allegro stores information about every Xnet in the PCB in its own topology file (TF). As its name implies, the topology file shows the "topology" of the PCB. Allegro's topology file stores the information about all the Xnet's components and their connections in a parsable text-based format. Physical elements like R, C, L, traces are listed in a node/edge graph structure in the file text. Generation of the necessary TFs is automated with a custom script-based approach using Allegro's SKILL language. This script tool is called our TF Generator (TFG).

III. Proposed Method and Implementation

We extract BPs from topology files by analyzing each file as a set of nodes. By representing a section of a PCB as a node graph, we have a very flexible dataset with automated methods of data extraction thanks to graph theory. With tools in graph theory such as traversal and path-finding algorithms, the process of collecting observations that previously would need to be done manually by a test engineer, or possibly even a team, is now automated. In this paper, our custom tool has applied this concept to extract the etch length between any two components in a site. We call this tool the Etch Length Extractor (ELE) for short. The key novelty is in the application of node graphs to MST analysis; the ELE is done to give board parameters as a subject to prove the concept.

The information in each topology file is sufficient to properly translate a topology file into a node graph. Because of this, creating a node graph from an Xnet is a matter of text-parsing. The ELE tool translates each TF into a node graph, which can then be subjected to any classic graph theory algorithm for analysis. With a proper node graph representation, path-finding algorithms can be used to determine the etch length between any two components in the TF. Calculating the etch length between two components involves determining the node path(s) (our dataset contains instances where 2+ traces connect two components) from the start node to the end node, and summing the etch length of all trace segment nodes in the node path(s).

Fig 2. shows the operation of the ELE tool from the user perspective. With the operation of the TFG and ELE tools described, we provide an example of how a test engineer might use them in conjunction.

- Determine a path of interest: e.g., Etch length R1 → C1 for all sites
- Use the TFG to generate topology files for the path from R1 → C1 for all sites on the probe card
- Use the ELE to generate a table of the etch length from R1 -> C1 for all sites, using the TFG-generated files

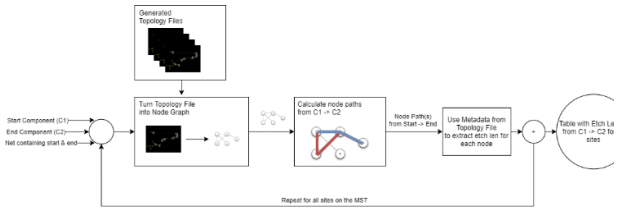

Fig. 2. ELE Tool operation from the user perspective

IV. Results

Fig. 3 shows the output from running the ELE tool on a massive multisite tester from Texas Instruments. The output in Fig. 3 shows that the tool has calculated the trace length from C1 to C2 for all sites on the MST. If there happen to be multiple paths from C1 to C2 on a site, the tool includes the information for both paths. The trace lengths for instances where there are multiple paths from C1->C2 are also calculated independently.

V. Discussion & Future Work

In this paper, the proposed method was proven using the etch length BP. However, the tool can be adapted to analyze other kinds of information with some simple software additions. Because the implementation of this method relies primarily on the concept of representing the topology file as a graph, it is flexible to extracting any kind of information that is available in the source (topology) files from where the graphs are generated.

The entire PCB of a MST is modeled by sets of separate topology files. For future work, The ELE tool can combine node graphs from multiple TFs together. Fig. 4 shows a limitation of the current ELE tool: {R1, R2} to {R3, R4} cannot be extracted because Xnets stop at an active component. Combining node graphs opens the capability to analyze BPs with the context of entire site on the MST, across multiple sites, or *the entire PCB*. Another avenue of future work is to leverage existing simulation engines to extract BPs such as S, Z, ABCD parameters, Johnson Noise, Crosstalk within an Xnet, etc., from the node graphs.

	A	B	C
1	C1.C2.DIST.1	C1.C2.DIST.2	SITE
	4608.838	4608.496	
	5736.229		
	4608.305		
	3617.021	3617.124	
	4647.202	4647.305	

Fig. 3. Crop of output from running ELE tool with the command shown in Figure 15

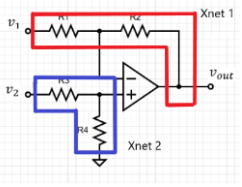

Fig. 4: XNets cannot be used to measure board parameters that span across active components

Acknowledgment

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