Design of a 4 to 2 Binary Encoder

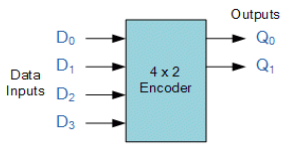
Abrar Adib[1], Mashrife Jaman Radib[2]
Department of Electrical and Electronic Engineering
Chittagong University of Engineering and Technology, Chittagong-4349, Bangladesh
Email: [1]u1802019@student.cuet.ac.bd , [2]u1802007@student.cuet.ac.bd

***Abstract*— This project demonstrates the utilization of VMware Workstation and Cadence Virtuoso Software to create a 4 to2 Binary Encoder. The software enables the generation of a schematic, symbol, and layout for the specified project, building upon insights gained from prior experiments. The goal is to determine the feasibility of fabricating the designed components. The project's outcomes are validated through DRC (Design Rule Check) and LVS (Layout vs. Schematic) tests conducted on each segment of the design. These tests ensure that the project yields optimal results suitable for both its intended functionality and eventual fabrication.**

***Keywords*— 2 input OR Gate, 4 to 2 binary encoder, DRC test, LVS test, Tape out.**

I. Introduction

An Encoder is a type of combinational circuit that executes the opposite function of a Decoder. It is equipped with a maximum of 2n input lines and 'n' output lines. The output it generates is a binary code that corresponds to the active High input [1]. The 4-to-2 Encoder comprises four input lines, namely D3, D2, D1, and D0, along with two outputs Q1 and Q0. The block diagram representing this encoder is depicted in the figure below.



Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x

Fig.01. Block diagram and truth table of 4 to 2 Binary Encoder

For each given instance, only one of the four inputs can have a value of '1' to obtain the corresponding binary code at the output [2].

4 to 2 Binary Encoder can be designed using two 2 input OR gates. The circuit diagram representing this encoder using OR gates is depicted in the figure below.

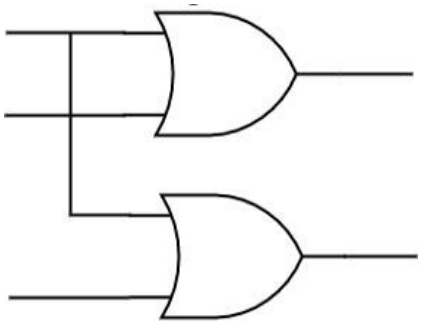


Fig.02. Circuit diagram with 2 input OR GATE

The Truth table for the 4-to-2 encoder using two 2 input OR gates is provided as follows:

Q0=D1+D3
Q1=D2+D3

II. Methodology

In this section,we will discuss about the detailed methodology of the design process of Schematic,Symbol and Layout of a 4 to 2 Binary Encoder.

A. Schematic Design

Schematic design of single OR gate:

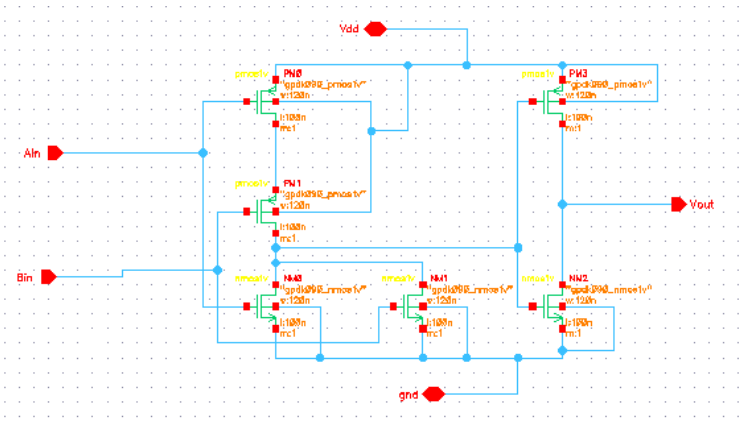


Fig.03. Schematic design of single OR gate

Schematic design for 4 to 2 binary encoder:

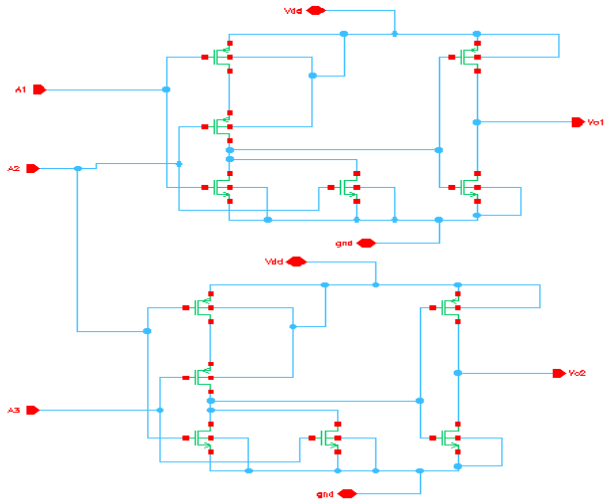


Fig.04. Schematic design for 4-to-2 binary encoder

B. Symbol Design

Symbol design for a single OR gate:

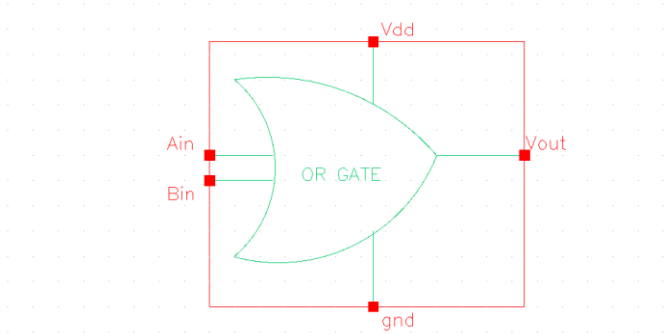


Fig.05. Symbol design for a single OR gate

Symbol design for 4-to-2 binary encoder:

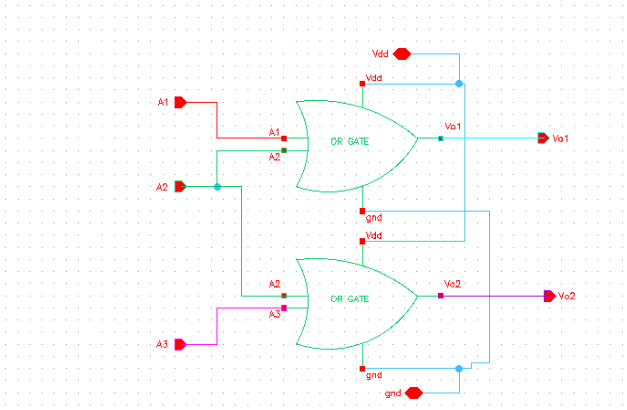


Fig.06. Symbol design for 4-to-2 binary encoder

C. Layout Design

Layout design for 4 to 2 binary encoder:

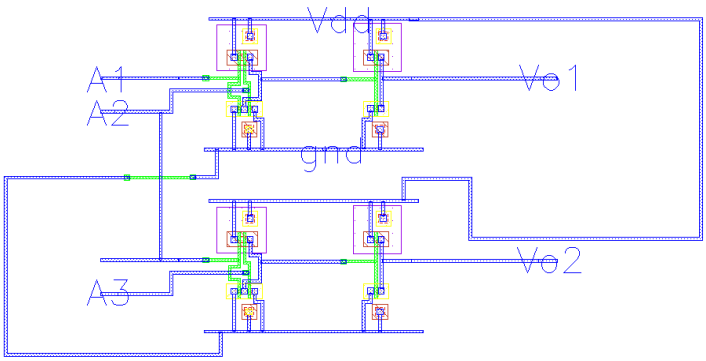


Fig.07. Layout Design for 4 to 2 Encoder Layout

D. DRC test

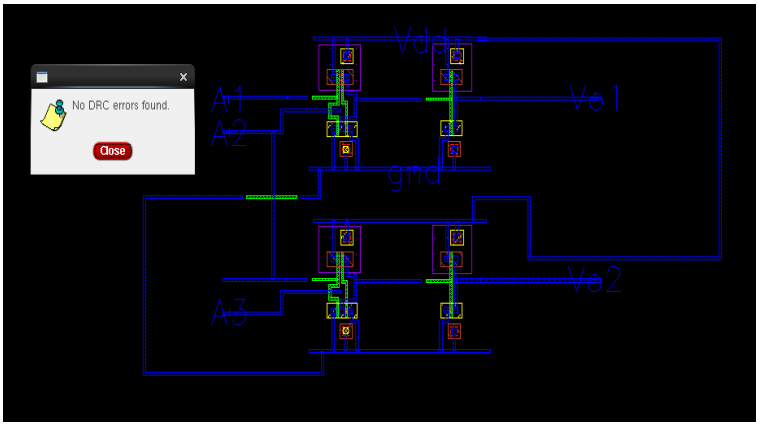


Fig.08. DRC Test

E. LVS test

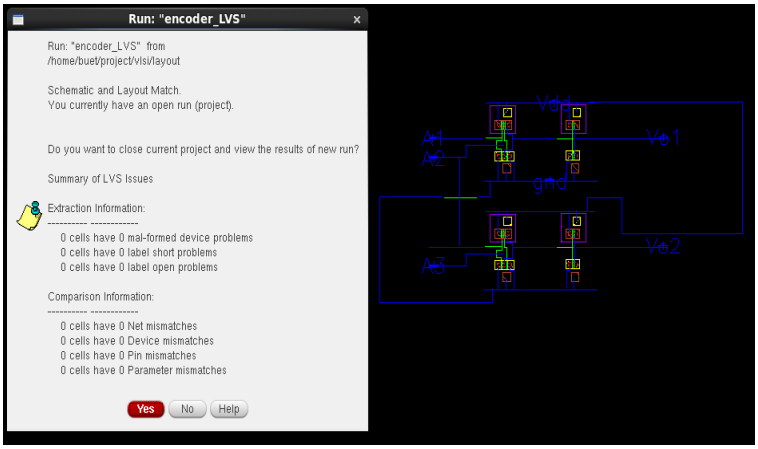


Fig.09. LVS Test

F. RCX run

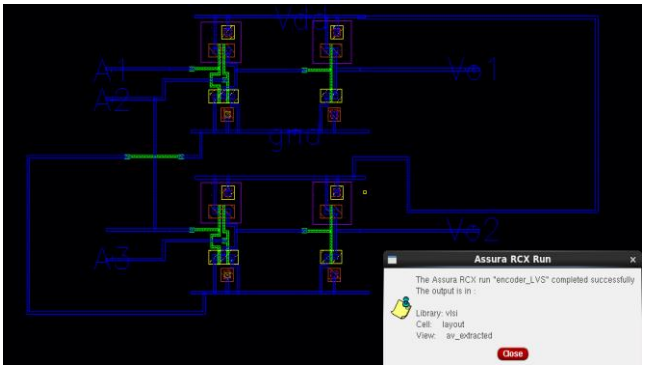
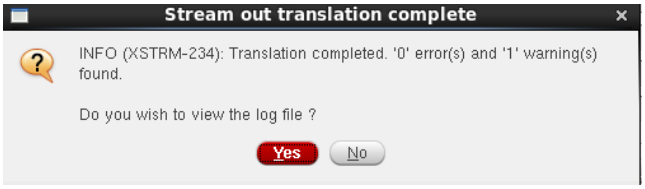


Fig.10. RCX Run

G. Tape out



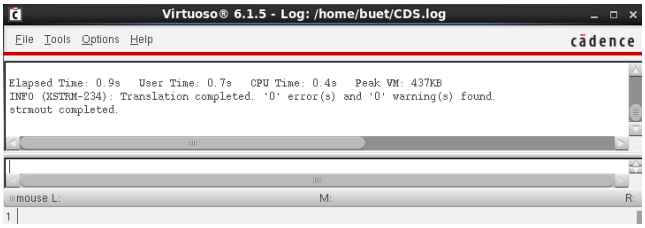


Fig.11. Tape out

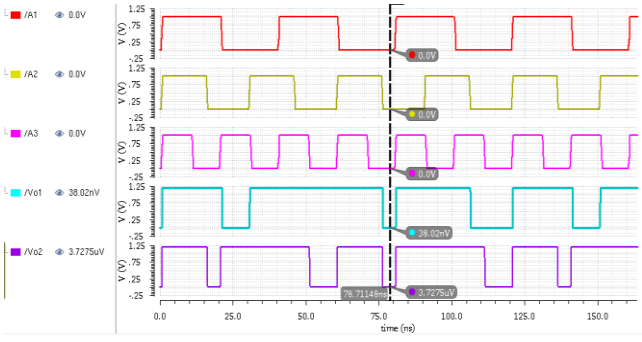
III. Simulation Output

Here,we have analyzed the simulation output for 4 different cases. Furthermore, the theoretical and simulation result have been matched to verify the authentication of the output.

Case 1: When Inputs A1=0, A2=0 & A3=0

i. Theoretical Result :
Vo1= 0, Vo2= 0.

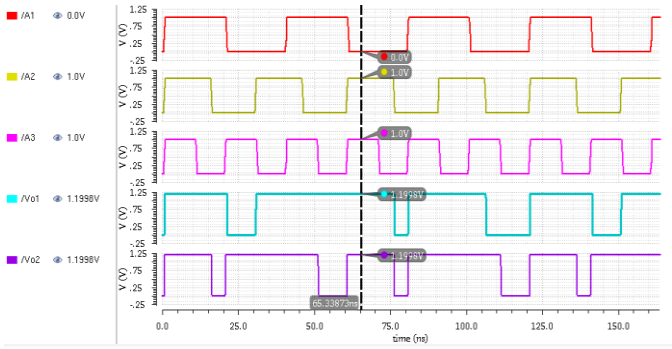
ii. Simulated Result :



Case 2: When Inputs A1=0, A2=1 & A3=1

i. Theoretical Result :
Vo1= 1, Vo2= 1.

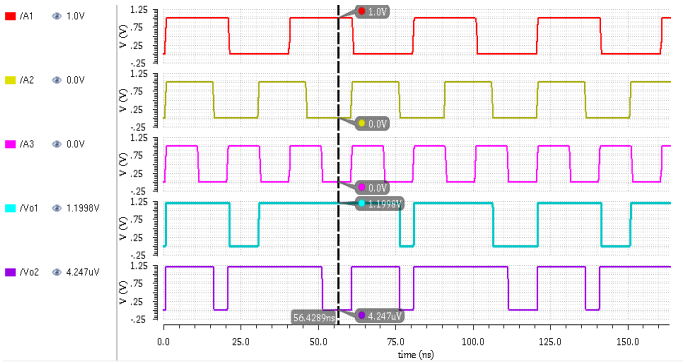
ii. Simulated Result :



Case 3: When Inputs A1=1, A2=0 & A3=0

i. Theoretical Result :
Vo1= 1, Vo2= 0.

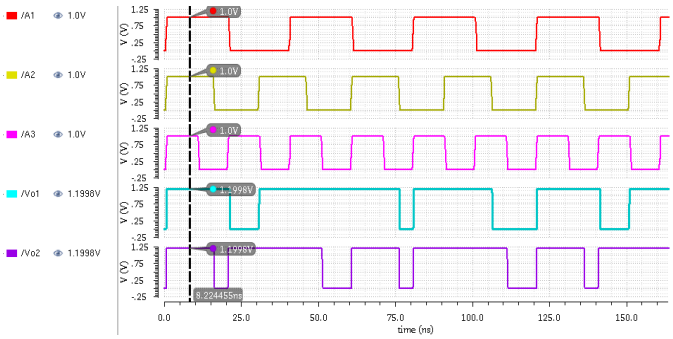
ii. Simulated Result :



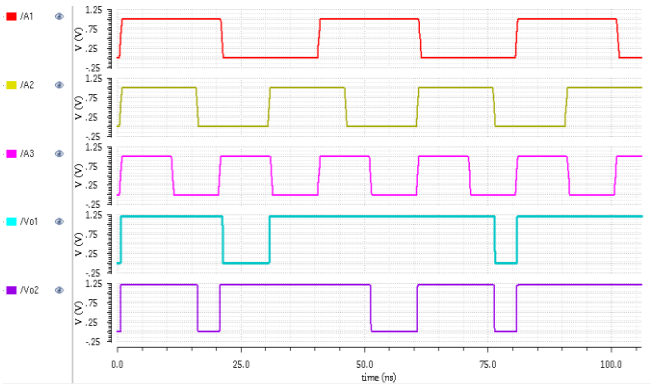
Case 4: When Inputs A1=1, A2=1 & A3=1

i. Theoretical Result :
Vo1= 1, Vo2= 1.

ii. Simulated Result :



Post Simulation Output :



IV. Result Analysis

We observe that the simulation output displayed in both the schematic and layout windows aligns with the expected theoretical values, validating the performance of the chip's functionalities.

V. Conclusion

During this project, we gained proficiency in using Cadence Software. We've successfully created the schematic for a 4-to-2 binary encoder, incorporating a 2-input OR gate. Additionally, we've completed the corresponding Layout design. To ensure the design's correctness, we performed Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification, resolving any errors in the process.

Acknowledgement

The achievement and results of this project were made possible through invaluable guidance and support, and we consider ourselves incredibly fortunate to have received it throughout the completion of our project. We would like to express deep appreciation and gratitude to Mohammad Mahmudul Hasan Tareq, Assistant Professor, as well as all the professors of the Department of Electrical & Electronic Engineering, Chittagong University of Engineering & Technology, for their exceptional mentorship and encouragement during this endeavor.

References:

[1] "tutorialspoint," [Online]. Available: https://www.tutorialspoint.com/digital_circuits/digital_circuits_encoders.htm
[2] https://www.geeksforgeeks.org/encoder-in-digital-logic/