Optimized Double-Stage Common-Source Power Amplifier with Enhanced Linearity and Stability

***Abstract*— This work represents the design and optimization of a CMOS Power Amplifier using Cadence Virtuoso (90 nm technology) Software which operates in the frequency range between the Ku-band and K-band (16.8-18.8 GHz). The amplifier was initially designed as a single stage system, and S-parameter analysis was performed to evaluate its performance. However, the results showed that the single stage PA did not meet the required specifications. To address this, an input matching network and an output matching network were developed utilizing Z-parameter analysis, enhancing its performance in the subsequent S-parameter study. A double stage amplifier was then developed, incorporating an interstage matching network in the form of an LC tank circuit. The final design produced an Gain (S_{21}) of 16.70 dB, S_{11} of -22.32 dB, S_{12} of -26.68 dB, and S_{22} of -17.79 dB at 17.80 GHz. Furthermore, the large signal analysis indicated an output 1dB compression point of about 11.54 dBm along with a saturated power (P_{sat}) of around 12.20 dBm. The stability factor (K) and the noise figure was determined to be about 2.3 and 3.89 dB respectively in the operating region. Finally, the peak power-added efficiency (PAE) was found to be approximately 20%. The design demonstrates an effective implementation of matching networks and cascaded amplifier stages to attain good linearity,stability and overall performance in the inside Ku-band and K-band.**

Keywords— CMOS Power Amplifier, Ku band, K band, Matching network, Tank circuit, Linearity, Stability, Noise figure, Wireless communication.

I. Introduction

Power amplifiers (PAs) are critical elements in Radio Frequency (RF) systems, tasked with amplifying weak signals to elevated power levels for transmission. They are essential in several applications, such as telecommunications, satellite communication, radar systems, and wireless networks. In RF systems, the amplifier must deliver a substantial gain, linearity, and efficiency while reducing distortion, as these elements directly influence signal integrity and total system efficacy [1]. In contemporary RF transmission, excellent linearity is essential to guarantee that the output power correlates with the input, commonly evaluated by the third-order intercept point (IP3). Attaining enhanced linearity mitigates signal distortion and guarantees the amplifier functions efficiently, even at elevated power levels [2]. Power amplifiers are typically engineered to function within a designated frequency range, such as the transition band between the Ku-band and K-band. The amplifier must properly manage the designated frequency range while ensuring stable performance. The Common-Source (CS) arrangement is frequently employed in power amplifiers because of its capacity to provide substantial voltage gain and extensive bandwidth. In this setup, the transistor's source is generally grounded or set at a constant voltage, with the input signal applied to the gate and the output extracted from the drain [3]. Common Source PAs offer significant amplification and is largely used in RF systems due to its simple design, high gain, efficiency linearity and stability specially in applications requiring amplification within the desired frequency range [4].

One of the recent studies have introduced a K-band Common-Drain (CD) power amplifier utilizing 90-nm CMOS technology, attaining remarkable OP_{1dB} and output power through a neutralization strategy to enhance stability and power gain. The CD amplifier design addresses issues of low power gain and inadequate stability via the proposed method [5]. Another work introduces a K-band broadband power amplifier (PA) using 0.13-µm CMOS technology, aimed at 5G and radar applications. The design features asymmetrical Magnetically Coupled Resonators (MCRs) for broadband matching and introduces two novel parameters, α and β, to mitigate gain ripples resulting from transformer loss [6]. Furthermore, an research article introduces a Ka-band CMOS power amplifier (PA) employing a stacked configuration with cascode-like functionality to enhance output power and efficiency. The concept integrates a Common-Source (CS) stage with two Common-Gate (CG) stages to optimize performance [7].

Dual-band amplifiers have become very effective due to their simultaneous impedance matching at different frequencies. Among them, one study examines the design of a dual-band power amplifier for 5G New Radio applications at 28 GHz and 38 GHz, aimed at improving the data speed. The amplifier employs a stacked-FET architecture to reduce gain roll-off and attain comparable performance throughout both the frequency bands. The measurement findings indicate that the suggested power amplifier provides stable output power and efficiency across both bands, rendering it appropriate for 5G inter-band carrier aggregation [8]. Another research focuses on designing a 28/38 GHz dual-band power amplifier for 5G communication, employing a T-topology matching network and an adapted dual-LC tank approach to attain minimal insertion loss and extensive bandwidth performance. This design also effectively reduces gain roll-off and facilitates dual-band operation with decent power-added efficiency (PAE) [9]. Finally, a study outlines the design of a wideband CMOS power amplifier for V-band millimeter-wave transmission, tackling the issues of impedance matching, gain and efficiency for high frequency applications. The two-stage amplifier has a staggered tuning methodology and enhances impedance matching networks to attain high gain and efficiency [10].

However, the discussed studies underscore several limitations in their different power amplifier designs. One study faces difficulties in ensuring power enhancement and stability in the common-drain amplifier, thus requiring careful optimization. Another study encounters challenges related to gain loss and impedance transformation constraints at high frequencies, which impact dual-band performance. One work examines the limited impedance transformation ratio and bandwidth efficiency in the T-topology matching network. The last article emphasizes that impedance matching and parasitic capacitances are constraints on attaining wideband performance and efficiency, especially at higher frequencies [5]-[10].

This work aims to design and optimize a cascode common-source power amplifier with high gain, low noise and power consumption to operate under ku to k frequency band. The PA also exhibits decent linearity performance which makes it suitable to operate within a range of input power. The amplifier can be instrumental in medical devices, telecommunications and wireless sensor networks, ensuring clear signal reception and accurate data interpretation from weak sources.

II. METHODOLOGY

A. Procedure

This study employes a number of techniques for the design and optimization of the two stage power amplifier. A single-stage power amplifier was first built, subsequently followed by an S-parameter analysis to assess its performance. Due to the unsatisfactory initial results, input and output matching networks were developed utilizing Z-parameter analysis to improve impedance matching on the input and output side. A re-evaluation of the S-parameters validated the enhancements. To enhance the amplifier's performance further, a double-stage configuration was employed, integrating an interstage matching network with an LC tank circuit. The conclusive S-parameter analysis revealed substantial enhancements after performing Finite Element Method (FEM). A large-signal study utilizing harmonic balance (hb) analysis in Cadence Virtuoso was conducted to assess the amplifier's linearity, identifying the output 1dB compression point, saturated power, and other essential parameters.

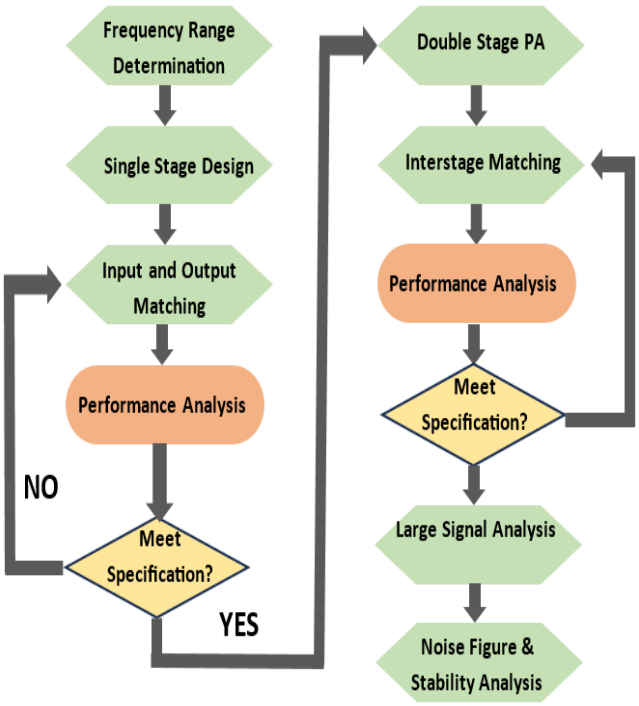

Fig. 1. Flowchart of the proposed power amplifier

After that, the stability of the power amplifier was performed by means of the rollet stability factor, noise figure analysis and linearity consideration. Finally, the power-added efficiency and Figure of Merit (FOM) of the power amplifier were calculated to evaluate the performance of the proposed amplifier compared to the recent works. The conclusive results revealed a satisfactory performance overall.

B. Single Stage Design

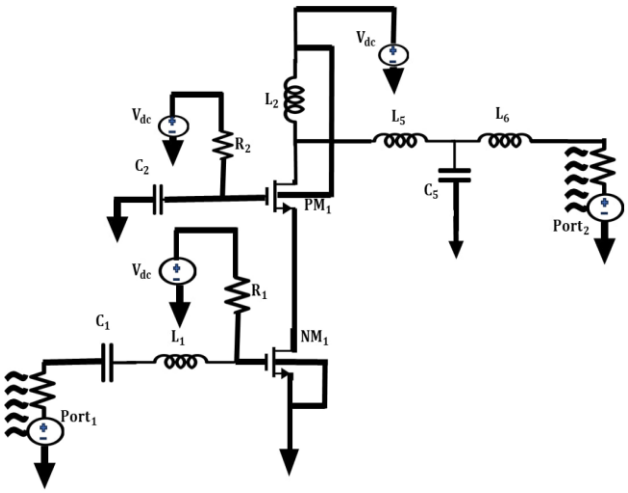

Fig. 2. First stage of the proposed PA

Fig. 2 illustrates the single stage configuration of the proposed Power Amplifier with input and output matching networks. The input signal is applied to the gate of the first transistor (NM_1), and the output is obtained from the drain of the second transistor (PM_1), which serves as the active amplification stage. MOSFETs' operating points are established by biasing resistors R_1 and R_2 to guarantee that the amplifier operates within the appropriate transistor characteristic range. To provide an AC signal path and obstruct DC, the design employs capacitors (C) for coupling and bypassing. The primary objective of the structure is to achieve efficient amplification, which is achieved by delivering moderate gain and low distortion.

C. Biasing Techniques

In power amplifier (PA) design, the biasing approach is essential for ensuring that transistors function within the best performance zone. Appropriate biasing stabilizes the operational point, making sure that the amplifier provides the desired gain, linearity, and efficiency.

This single-stage amplifier uses the voltage divider biasing approach to establish the Gate-to-Source Voltage (V_{gs}) for the PMOS and NMOS transistors. The voltage divider is constructed with resistors (R_1 and R_2) establishing a consistent voltage at the transistors' gate, thus ensuring their operation inside the saturation area. The saturation area is where MOSFETs operate as linear amplifiers, delivering high gain for power amplification. The PMOS transistor, located at the upper section of the circuit, requires a positive gate-to-source voltage for activation, whereas the NMOS transistor at the lower end requires a negative gate-to-source voltage to remain in the active area. The voltage divider guarantees that these parameters are satisfied, enabling both transistors to function correctly without approaching the cutoff or triode regions.

Furthermore, capacitors serve the functions of bypassing and coupling, facilitating the passage of AC signals while obstructing DC components, so safeguarding the biasing against signal fluctuations.

The selected biasing technique guarantees the amplifier functions efficiently, achieving appropriate gain and linearity, while reducing distortion and preserving thermal stability for sustained, reliable performance.

D. Matching Networks Design

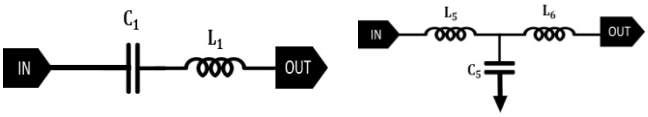

Fig. 3. (a) Input matching network (b) output matching network

Fig. 3 shows the input and output matching networks. The design of the matching network is essential for improving the performance of the power amplifier. This design employs an LC tank circuit to match the amplifier to the 50 Ω source impedance, facilitating impedance matching between the source and the amplifier to reduce reflection and optimize power transfer. The output matching network is configured as a T-network, comprising resistors and capacitors organized in a T-shape to align the load impedance with the amplifier's output port impedance. The integration of the LC input network and T-network output network guarantees effective signal transmission, reduces loss, and improves the overall efficiency of the power amplifier within the specified frequency range.

TABLE I

COMPONENT VALUES OF THE MATCHING NETWORKS

L_1	C_1	L_5	C_5	L_6
2 nH	500 fF	1.38 nH	103.84 fF	1.08 nH

E. Second Stage Addition

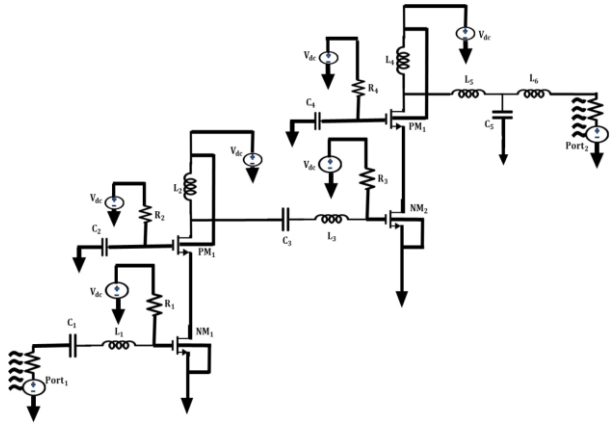

Fig. 4. Two stage configuration of the proposed PA

The incorporation of a second stage in the amplifier design seeks to enhance the overall gain and enhance linearity. The second stage amplifies the signal further by cascading the amplifier stages, while maintaining the performance characteristics of the first stage. An interstage matching network, commonly realized with an LC tank circuit, is employed to achieve excellent impedance matching between stages. This interstage matching enhances power transmission and reduces signal distortion, allowing the second stage to effectively contribute to the overall gain without resulting undesirable losses or performance degradation.

III. Design Parameters

Various parameters were studied to evaluate the performance of the CMOS PA. The output power, power consumption, power gain, linearity, stability and power-added efficiency (PAE) are the most critical elements of a PA design. These factors inherently involve trade-offs, making PA design for CMOS downscaling more challenging. These constituted the primary factors in our design for assessing the overall performance.

A. Output power

The output power (P_{out}) refers to the power supplied to the load, where increased output power frequently leads to diminished efficiency because of thermal losses. To offset this deficit, the device's energy supply must surpass the necessary output power. The output power, intrinsically connected to the efficiency of the power amplifier, is pivotal in ascertaining the overall performance of the PA [11].

$$P_{out} = \frac{V_{out}^{\ 2}}{2R_L} \tag{1}$$

Where V_{out} denotes the output voltage and R_L denotes the load resistance.

B. Power Consumption

The dc power consumption is defined by the sum of dc power consumed by each stage of a power amplifier [12].

$$P_{dc} = 2 \times V_{supply} \times I_{avg} \tag{2}$$

The power consumption of a power amplifier (PA) is vital for portable devices, as it affects battery longevity.

C. Power Gain

Power gain (G) represents the relationship between output and input power, indicating the power amplifier's ability to deliver a significantly amplified power signal to the load. It quantifies the extent to which the amplifier increases the amplitude of a signal [13].

$$G = 10log_{10}\frac{P_{out}}{P_{in}}\ [dB] \tag{3}$$

By enhancing the output power, a power amplifier aims to enhance efficiency and sensitivity.

D. Power Added Efficiency (PAE)

PAE evaluates the PA's ability to convert DC power into an AC signal. PAE is determined by subtracting output power from input power and dividing the result by the DC power consumption [14].

$$PAE = \frac{P_{out}\text{-}P_{in}}{P_{dc}} \tag{4}$$

Increased output power leads to an elevated PAE, signifying enhanced efficiency in the conversion of DC to AC power.

E. Linearity

Linearity denotes the output of a device varying directly in proportion to the input signal. In contemporary RF communication systems, strong linearity is crucial and is generally assessed by 1dB compression point. The term 1 dB compression point (P1dB) of the power amplifier refers to the output power level at which the gain reduces by 1 dB from its constant value.Operating below the compression point is crucial to avoid non-linear behaviors and harmonics [15].

F. *Stability Factor*

The stability factor (K) indicates that the amplifier remains free from oscillation or instability throughout diverse operating conditions.

$$k = \frac{1-|S_{11}|^2 - |S_{22}|^2+|\nabla|^2}{2|S_{12}S_{21}|} \quad (5)$$

$$\nabla = S_{11}S_{22} - S_{12}S_{21} \quad (6)$$

The stability factor, K should be greater than one.

IV. RESULT & DISCUSSION

A. *S-Parameter Analysis*

S_{11}- Input reflection coefficient, S_{12}- Insertion loss, S_{21}- Forward gain, S_{22}- Output reflection coefficient.

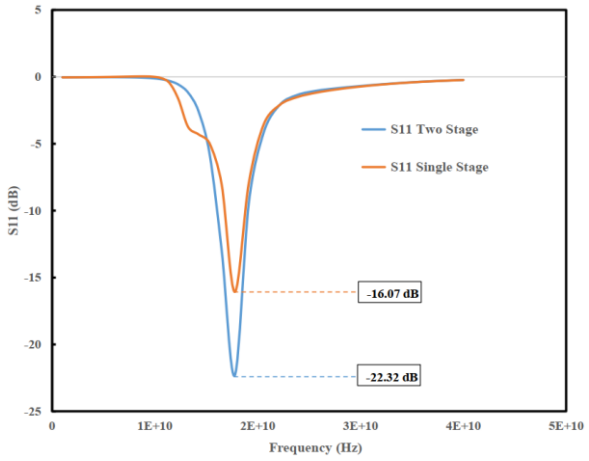

Fig. 5. S_{11} parameter of Single-Stage and Two-Stage Configuration

Fig. 5 represents the comparison between the S_{11} parameter for both single-stage and double stage amplifiers. At the resonant frequency of 17.77 GHz, the double-stage amplifier achieves a significantly better S_{11} value of -22.32 dB, indicating superior impedance matching compared to the single stage amplifier's S_{11} value of -16.07 dB. This demonstrates that the double stage design power transfer efficiency and reduced signal reflection. It is also worth mentioning that the input return loss (S_{11}) is less than -10 dB at frequencies between 16.8-18.8 GHz.

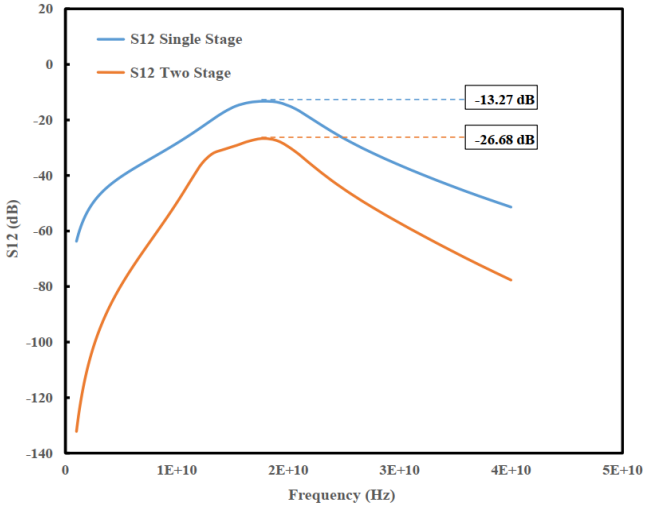

Fig. 6. S_{12} parameter of Single-Stage and Two-Stage Configuration

Fig. 6 compares the S_{12} parameter of single-stage and double-stage amplifiers at the resonance frequency of 17.80 GHz. The S_{12} value for the double-stage amplifier is -26.68 dB, significantly lower than the -13.27 dB of the single-stage amplifier, providing superior reverse isolation and diminished signal feedback in the double-stage configuration. This leads to enhanced stability and overall performance of the double-stage amplifier.

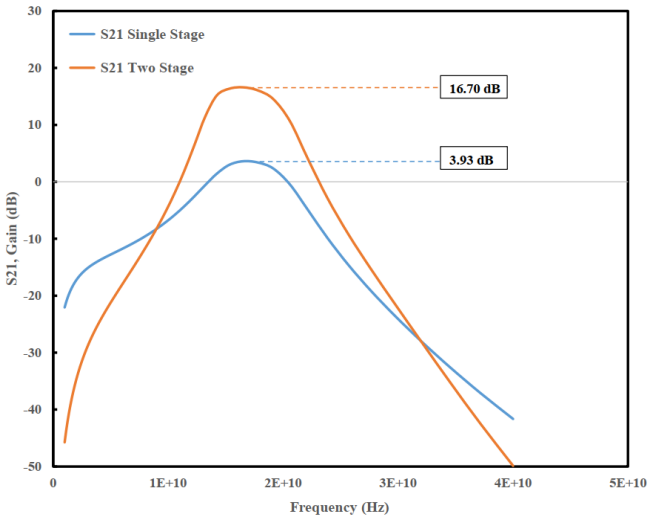

Fig. 7. S_{21} parameter of Single-Stage and Two-Stage Configuration

The graph in fig. 7. indicates that the double-stage amplifier displays a significantly sharper and elevated peak in gain, signifying enhanced amplification capability, whereas the single-stage amplifier presents a lower gain response. At the resonant frequency of 17.80 GHz, the value of S_{21} for the double-stage amplifier is 16.70 dB, significantly higher than the 4.93 dB of the single stage amplifier. This highlights the enhanced amplification capability of the double-stage design.

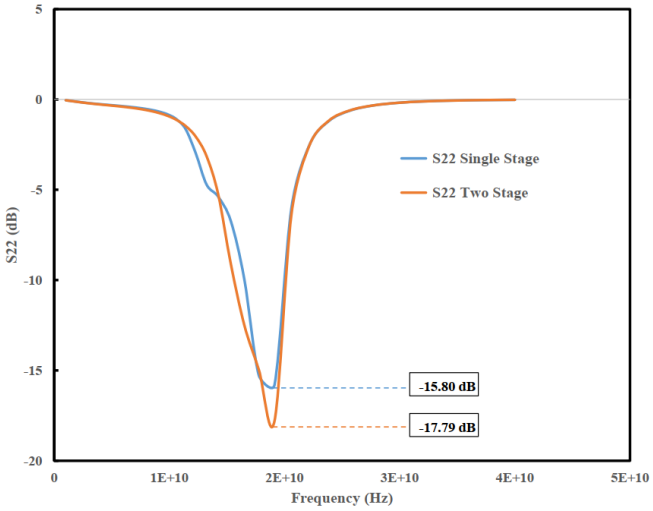

Fig. 8. S_{22} parameter of Single-Stage and Two-Stage Configuration

The graph in fig. 8 indicates that the two-stage setup attains superior output matching relative to the single-stage configuration. The lowest S_{22} value for the two-stage system is roughly –17.79 dB, whereas the single-stage configuration attains about –15.80 dB. A lowered S_{22} value indicates enhanced impedance matching at the output port, resulting in less power being reflected back. The improved output

matching in the two-stage arrangement indicates higher performance regarding stability and power transfer efficiency over the operating frequency range.

B. Stability Analysis

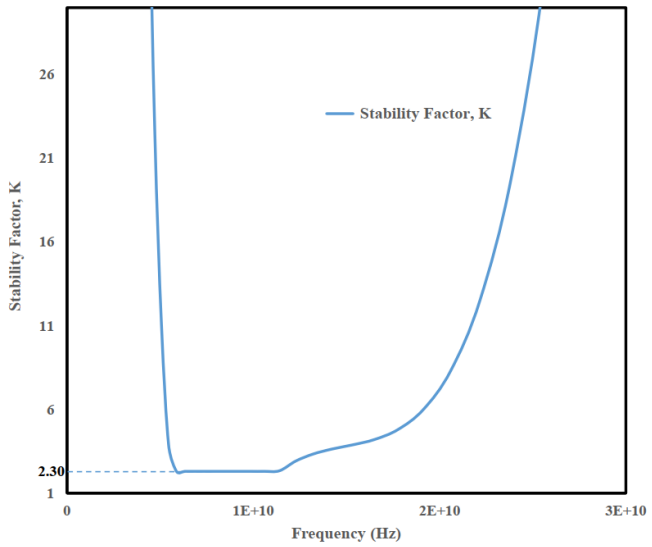

Fig. 9. Stability Factor (K) of the proposed PA

Fig. 9 represents the stability factor (K) of the amplifier across a range of frequencies, which is a vital element in determining the unconditional stability of power amplifiers. For an amplifier to be unconditionally stable, the stability factor K must be greater than 1 at all frequencies of operation. In the plot, K remains above 1 throughout the frequency range, demonstrating that the amplifier maintains stable operation and will not oscillate under any load conditions.

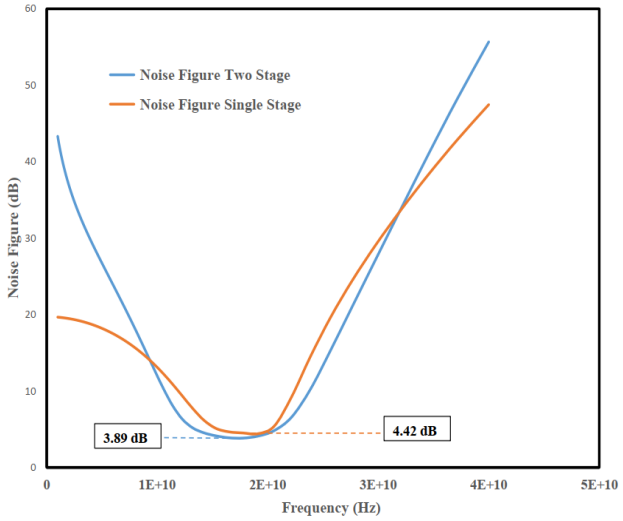

Fig. 10. Noise Figure (NF) of Single-Stage and Two-Stage Configuration

Fig. 10 depicts the noise figure curves for both single-stage and two-stage configurations of the power amplifier. It is observed that the minimum noise figure for the two-stage system is roughly 3.89 dB, whereas the single-stage configuration attains around 4.42 dB, particularly around our desired frequency. Therefore, the NF remains below 5 dB throughout the bandwidth of our amplifier which also makes it appropriate for low noise applications.

C. Linearity Consideration

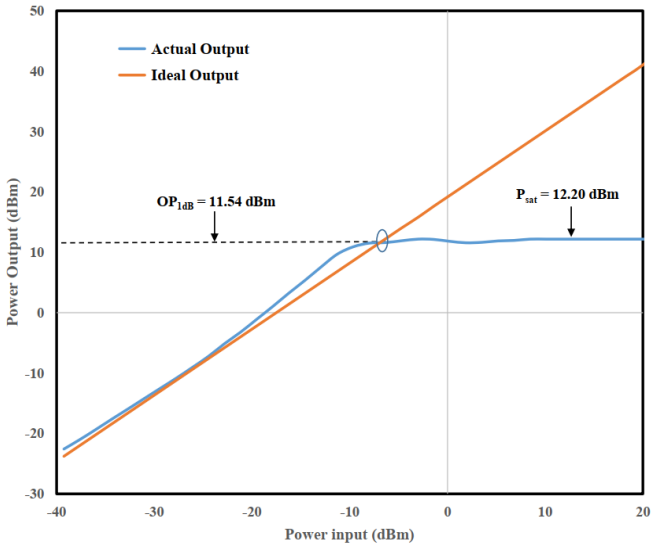

Fig. 11. 1dB Compression Point and Saturated Power

Fig. 11 depicts the output power against input power characteristics of the proposed PA, highlighting two crucial performance metrics, the 1 dB compression point (OP_{1dB}) and the saturated output power (P_{sat}). The ideal output curve represents a linear response, whereas the actual output demonstrates that the amplifier tends to compress as input power increases. The 1dB compression point, shown at 11.54 dBm, represents the point where the output power drops 1 dB below the ideal linear curve, indicating the boundary of nonlinearity. Beyond this, the amplifier reaches its maximum output power at the saturation point (P_{sat} = 12.20 dBm), when further increases in input power will result in insignificant output gain. This curve is critical for measuring the amplifier's linearity and power handling capability.

D. Power Added Efficiency (PAE) Calculation

The DC power consumption of the cascode common source power amplifier was calculated using equation (2) which was found about 83 mW.

Finally, power-added efficiency of the power amplifier was calculated using equation (4). As a result, PAE_{1dB} and $PAE_{max.}$ was around 17.16% and 20% respectively.

E. Figure of Merit (FOM)

The Figure of Merit is a normalized parameter utilized to balance the trade-offs among the characteristics of a Low Noise Amplifier (LNA) in order to enhance efficiency according to specifications.

$$FOM = \frac{Gain \times BW \times node \times Frequency \times V_{dd}}{[NF\text{-}1] \times P_{dc} \times 1000} \qquad (7)$$

The figure of merit (FoM) of the broadband power amplifier (PA) can be determined using maximum gain, bandwidth, noise figure (NF), and power consumption. Using equation (7) , value FoM of the respective circuit was found 26.72 which is significant compared to the other results shown in table II.

TABLE II

COMPARISON WITH PREVIOUSLY ESTABLISHED WORKS

Ref.	Technology	Architecture	BW (GHz)	Freq. (GHz)	S_{11} (dB)	S_{12} (dB)	S_{21} (dB)	S_{22} (dB)	OP_{1dB} (dBm)	PAE_{1dB} (%)	PAE_{max}. (%)	$P_{sat.}$ (dBm)	NF (dB)
[5]	90 nm	2 stage NCD	23-25	23	<-10	-	10.3	<-10	22.5	22.5	24.2	22.9	-
[6]	130 nm	MCR Integrated Cascode	21.3-27.9	24	<-10	<-20	17.5	-	12.1	15.8	30.4	15.7	-
[10]	90 nm	Two-Stage PA	53.5-55	54	-18.77	-16.03	14.34	-12.78	-	-	-	-	15.9
[7]	65 nm	3 Stage Cascode	27.5-31	29	-22.50	-	25.2	-4.50	22.4	25.3	25.8	22.7	-
[8]	150 nm	Stacked-FET		28,38	<-10	-	18.5,18	<-10	25.8,25.7	-	39,36	28.5	-
This work	**90 nm**	**Common Source Cascode**	**16.8-18.8**	**17.8**	**-22.32**	**-26.68**	**16.70**	**-17.80**	**11.54**	**17.16**	**20**	**12.20**	**3.89**

V. CONCLUSION

This work presents the design and optimization of a broadband power amplifier (PA) operating in the transition band between the Ku-band and K-band (16.8-18.8 GHz). The amplifier was initially designed as a single-stage system, with performance evaluated using S-parameters. By incorporating input and output matching networks, the performance improved, but further enhancements were made by cascading a second stage and adding an interstage LC matching network. The proposed two-stage power amplifier achieves exceptional performance metrics, including a power gain of 16.70 dB, an output power at the 1 dB compression (OP_{1dB}) of 11.54 dBm along with a power-added efficiency (PAE_{1dB}) of 17.16%, and a saturation power (P_{sat}) of 12.20 dBm with a peak power-added efficiency ($PAE_{max.}$) of about 20%.

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