Suggested Teaching Guidelines for

System Architecture PG-DVLSI March-2024

Duration: 40 class room hours

Objective: To introduce the various System Architectures Concepts and Communication Protocol.

Prerequisites: Knowledge of Electronics Fundamentals and digital logic design

Evaluation method: CCEE Theory exam – 80% weightage

Internal exam - 20% weightage

List of Books / Other training material

1. Computer organization - V Carl Hamacher, Vranesic, Zaky, Mc-Graw Hill Companies Inc.

Reference:

1. Computer Architecture - Michael J. Finn

Session 1
Lecture: Introduction to programmable logic family

- Basic PLDs
  - ROM
  - PROM
  - PLA
  - CPLD
  - FPGA
- Features of FPGA
  - I/O blocks
  - Logic resources (Memories, processor, DSP, arithmetic etc…)
  - Clocking and Routing resources

Session 2
Lecture: Case Study of Ultra Scale FPGA Architecture

Session 3
Lecture: Case study of Ultra Scale or high-end Architecture

Session 4
Lecture: Comparison between various FPGA Families

- Comparison of Architecture Differences as well as Resource Differences of FPGAs from Different Vendors
- AMD -Xilinx : Virtex, Zynq, Ultrascale
- Intel (Formerly Altera) – Stratix devices
- Achronics – Speedcore eFPGA
- Introduction to Timesharing FPGAs and Structured ASICs

Session 5
Lecture: Ethernet

- Basic of Networking (LAN, WAN, MAN)
- Ethernet- standard 802.3, Frame format, MAC Functionality, Layering structure, Physical media options, Difference b/w half and full Duplex mode, difference b/w 10/100/1000

operations, cabling, auto negotiation, Design with Media Independent interface (MII), management through MDIO/MDC

- Coding Technique- Manchester coding, 4B/5B, 8B/10B, 64B/66B etc…
- Equipments **Architecture-** Hub, Switch, NIC, Future architectural upgrades to the standard (10G, 40G, 100G, 400G).

Session 6
Lecture: PCI-Express

Session 7
Lecture: Introduction to PC Architecture

- History of the PC Architecture
- 8085 to 80486
- Pentium family
- CISC
- RISC
- Instruction Set Architecture

Session 8
Lecture: Introduction to PC Architecture

- Instruction Level Parallel processor
- Superscalar approach
- VLIW approach
- CISC superscalar
- Parallel Decoding
- Superscalar Instruction Issue
- Parallel Execution
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Session 9
Lecture: Introduction to PC Architecture

- Process of Control transfer Instruction
- Branch Static
- Branch problem
- Branch prediction Scheme
- Fixed Prediction
- True Prediction

Session 10
Lecture: Introduction to Memory Architecture

- Memory System
- Types of memory
- Application of ROM
- Internal structure of ROM
- Decoding scheme for ROM
- Types of ROM
- Mask ROM

- PROM
- EPROM
- EEPROM
- Flash Memory

Session 11 -13
Lecture: Introduction to Memory Architecture

- Read Write Memory
- Basics of SRAM
- SRAM Timing
- Basics of DRAM
- Internal structure of DRAM

Session 12
Lecture: Introduction to Memory Architecture

- Types of SRAM
- Synchronous SRAM
- SSRAM pipeline
- SSRAM –ZBT
- DRAM Read
- DRAM Write
- Refresh Cycle
- DRAM Timing
- DRAM Controller

Session 13
Lecture: Introduction to Memory Architecture

- DRAM cycles
- Types of DRAM
- Extended Data out DRAM
- Applications of DRAM

Session 14
Lecture: Introduction to Memory Architecture

- Cache Memory
- Terminology related to Cache
- Addressing issues of Cache
- Searching the Cache
- Cache controller issue

Session 15 & 16
Lecture:

- Introduction to peripheral bus
- USB
- SPI
- eSPI
- UART

Session 17 & 18
Lecture: System on Chip (SOC)

- Introduction to Microcontrollers in FPGAs (ARM)
- FPGA vs soft core
- System architecture
- Module Development
- ALU
- Accumulator
- Program counter
- Program memory
- IR
- TCU
- I/O interface
- Hardware/Software requirements
- Cortex – M1 Architecture
- Bus interfacing
- External Interface
- TCM interface
- Processor operating states
- Processor operating modes
- Exceptions
- NVIC
- Clocks and resets
- Software Developments
- System on chip- Use any tool.
- Overview of ASM & TLM
- High Level Synthesis (HLS)
- Requirement analysis
- Architecture
- Implementation constraints
- Partitioning
- Interfacing requirements
- Integration and Verification

Session 19 & 20
Lecture: Multicore Architecture

Assignment (Compulsory):

- Technical Group Presentations related with the advanced topics from the module by studying standard latest datasheets of FPGA Architectures, Microprocessor Architectures or Communication Protocols.

Assignments (Optional):

- Create a design that takes analog input from LTC1407A-1, calculates the gain and displays the output in LCD. Also implement the software A/D communication.
- Create design that detects left and right rotation of a rotary encoder and controls LED. Also create simple VHDL to create synchronous design technique with above program as reference.
- Create design that transforms the Spartan-3E device on Spartan-3E Starter Kit into a NOR FLASH programmer for the Intel StrataFlash memory (IC22). Write terminal program on

HyperTerminal to manually program individual bytes. Also read the memory to verify contents, perform memory ID check and erase operations.

- Create a project with embedded processor, export that design to SDK, and create a simple Hello World application that prints to the UART USB port.
- Create a project in which the processing System (PS) of Zynq-7000 AP SoC interacts with the Programmable Logic (PL) hardware to process inputs and outputs through the GPIO implemented in the programmable fabric.
- Programs implying interactions between processing system and programmable logic via device drivers:
- HDMI display
- OLED display
- Create projects on
- To show VGA output test pattern
- To connect remote ZedBoard Terminal via SSH Session

Case study (Optional):

Experiment with Pulse Width Modulation (PWM) implemented by a PicoBlaze processor. Create a design that allows you to control 12 PWM channels;

- 8 channels control the intensity of the 8 LEDs on the board
- 4 channels are provided to observe should you have access to an oscilloscope.

Also experiment with simple resistor-capacitor (RC) smoothing circuits connected to the header pins to create additional digital to analogue (D/A) converters or experiment with controlling motors via drive transistors.

The PWM implemented has a pulse repetition frequency (PRF) of 1KHz and an 8-bit resolution (256 steps). The duty cycle for Each LED or ‘J4’ output can be set independently using simple commands entered at a simple terminal program on your PC (HyperTerminal is ideal).