*Suggested Teaching Guidelines for*

## *CMOS VLSI and aspects of ASIC Design PG-DVLSI March-2024*

**Duration:** 32 class room hours + 58 Lab hours

**Objective:** Introduction to Design & Simulation of CMOS Digital Integrated circuits.

**Prerequisites:** Knowledge of basic Electronics

**Evaluation method:** CCEE Theory exam – 40% weightage

Lab exam – 40% weightage

Internal exam – 20% weightage

**List of Books / Other training material**

**Courseware:**

- CMOS VLSI Design: A Circuit and Systems Perspective by Ayan Banerjee, Neil H. E. Weste, David Harris / Pearson
- Application Specific Integrated Circuits by Michael John Sebastian Smith Addison, Wesley

**Reference:**

- Design of Analog CMOS Integrated Circuits 1st Edition by RAZAVI /TMH
- VLSI Technologies by SEZ
- Spice for Circuits and Electronics by Md. H. Rashid (PHI Publication)

**Session 1**
**Lecture: Metal Oxide Semiconductors (MOS)**

- Overview of CMOS Module
- Introduction of MOS devices
- n-MOS, p-MOS and CMOS
- MOS operation

**Session 2**
**Lecture: CMOS Gates and Characteristics**

- CMOS Logic Circuits
- CMOS Inverter and I-V Characters

**Session 3**
**Lecture: Design of Complex Functions**

- Design of Complex Functions using CMOS

**Session 4**
**Lecture: MOS Cells**

- Structure of MOS cells
- Threshold Voltage and DC transfer characteristics
- Introduction to IC Design Cycle and layout

**Session 5**
**Lecture: CMOS functioning and parameters**

- CMOS as a switch, estimation of parasitic values
- rise and fall times
- power dissipation
  - Dynamic and Static
  - Low power architecture

**Session 6**
**Lecture: Technology Scaling**

- Device sizing, rationed and non-rationed logic
- Concepts of Interconnect
- Transistor Scaling and interconnect Scaling

**Session 7**
**Lecture: CMOS Logic Circuits**

- Design of logic circuit, fabrication steps
- CMOS Combinational Logic circuits
- Design of NAND and NOR Gates
- Transmission Gates

**Session 8**
**Lecture: IC Fabrication using CMOS Technology**

- CMOS Technology, wafer information photolithography.
- Well and channel information, Silicon dioxide and gate oxide**.**

**Session 9**
**Lecture: Memory using CMOS**

- Design of Complex circuits
- SRAM, DRAM & current Mirror
- Memory cell and their read write operation.

**Session 10**
**Lecture: Advanced Trends in Backend VLSI**

- Overview of CMOS Fabrication Steps
- Sequential CMOS logic
- Circuit Design of Latches and Flip-Flops
- Introduction to FinFET technology

**Session 11**
**Lecture: CMOS Design Issues**

- Design issue like Delays, Cross talk , Velocity saturation,
- Body effect, latch up, electro migration, hot carrier and Channel Length modulation

**Session 12**
**Lecture: Aspects of ASIC Design**

- Introduction of ASIC Design,
- An overview of Backend VLSI Design Flow – Libraries, Floorplanning, Placement, Routing, Verification, Testing.
- Flow Diagram, Specifications and Schematic cell Design.
- Spice simulation. Analysis of analog and digital circuits, Circuits elements, AC and DC analysis.

**Session 13**
**Lecture: Characteristics of Different Technologies**

- Transfer Characteristics, Transient responses, Noise analysis of current and voltage based on different technologies.

**Session 14**
**Lecture: Back-end Processes**

- Fabrication methods of circuit elements, Layout design of different cells.
- Library cell designing, NAND, NOR, NOT, X-OR etc.
- Circuit Extraction, Electrical rule check, LVS, Post layout Simulation and parasitic extraction.

**Session 15 & 16**
**Lecture: Back-end Designing and Analysis**

- Design format, timing analysis, back annotation and post layout simulation of silicon circuit
- Study of design Issues Antenna effect, Electro migration effect body effect, Inductive and capacitive cross talk, Drain punch through, etc.
- Placement of cells, placing of I/O blocks, Initialization of floor planning, routing and creating design data base
- DFT Guidelines, Test Pattern and BIST
- ASIC design implementation

## Assignment - Lab Sessions:

1. Draw the schematic and simulate the following gate and Do it transient Analysis.
   - Two input OR gate
   - Two input AND gate
   - Two input XOR gate

2. Draw the Layout and Schematic of CMOS inverter.
3. Draw the Layout and Schematic of two input Nand gate. Also Do its LVS and ERC.
4. Construct the Layout and Schematic of 2 input XOR gate and Simulate the dynamic behavior of the xor gate using the layout-extracted net list.
5. Draw the Schematic and Layout of Half adder. Simulate the dynamic behavior of the half adder using extracted netlist.
6. Draw the Schematic and Layout of Full adder. Do its LVS and ERC. Simulate the dynamic behavior of the full adder using extracted netlist.
7. Draw the layout of 4-bit full adder. Simulate the Behavior of 4-bit full adder using the layout extracted netlist.
8. Draw the schematic and layout of 6T-SRAM using EDA tool. Do its DRC, ERC and LVS.