Suggested Teaching Guidelines for

HDL Simulation and Synthesis PG-DVLSI March2024

Duration: 32 class room hours and 78 Hrs Lab

Objective: To introduce Synthesis and timing issues.

Prerequisites: Knowledge of FPGA and timings

Evaluation method: CCEE Theory exam – 40% weightage

Lab exam – 40% weightage

Internal exam – 20% weightage

List of Books / Other training material

Text Book:

No specific courseware for modules, faculty may share some course materials.

Reference:

J. Bhasker and Rakesh Chadha, "Static Timing Analysis for Nanometer Designs – a Practical Approach", (1st Edition, Springer Publications)

Session 1 & 2
Lecture:

- HDL FLOW
- Synthesis Flow
- Simulation and Modeling concepts
  - Modeling
  - Simulation
  - Delays in simulation
  - Race conditions in simulation and their resolving using zero delays
- Simulators and their types
  - Event Based Simulation Vs. Cycle Based Simulation
- Event Scheduling in Verilog
- Concurrency

Session 3
Lecture:

- Partitioning Design
- Design Units
- Synthesis of sequential and Concurrent Statements
- Synchronous Vs Asynchronous Designs

Session 4
Lecture:

- Clock and Reset Designs

Session 5 & 6
Lecture:

- Difference between synthesis and simulation result
- If-else Vs Case

- Incomplete assignments
- Functions
- Blocking Vs Non-Blocking in Verilog
- Sensitivity List

Session 7 & 8
Lecture:

- Arithmetic Operators
- Propagating constants
- Sharing resources
- Pipelining
- Fan-out control
- Logic duplication

Session 9
Lecture:

- Low power designing – Understanding of different types of power reducing and power consumption techniques
- Power Dissipation in State machines
- Advanced concepts

Session 10
Lecture:

- Timing Fundamentals
- Timing Issues

Session 11
Lecture:

- Clock Skew
- Timing issues in Pipelining
- Latency

Session 12
Lecture:

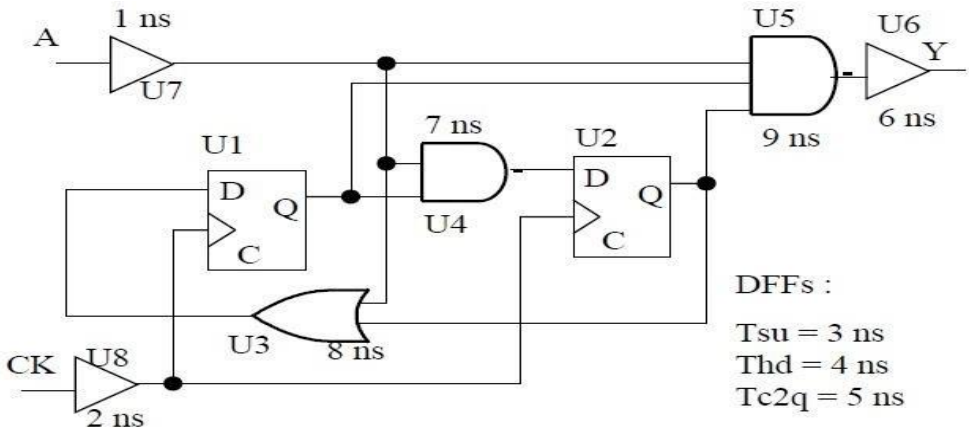
- Timing Constraints
- Timing on Board

Session 13
Lecture:

- Timing Problem solving

Session 14
Lecture:

- Case Study on setup and hold slack using following diagram.



Session 15
Lecture:

- Case Studies to Determine Synthesis Results on complex Verilog codes.

Session 16
Lecture:

- FPGA synthesis and its implementation
- Technological Library
- IP Core

Lab Assignments:

Software Labs:
The following codes should be simulated, synthesised and the results should be observed as well as documented carefully:

1. Multiplexers using Tri-state buffers.
2. Simulation vs. Synthesis of different timing statements in Verilog.
3. Truncation cases of output bits.
4. Synthesis of any code: with and without using pipeling.
5. Synthesis of “if” and “case” statements for 32:1 Multiplexer using primitive and advanced PLDs.
6. Implementation of any code: with and without register duplication.
7. Design 4-bit counter with asynchronous reset and Synchronous Load.
8. Synthesis of FSM using different state encoding styles: Binary, Gray, One-Hot.
9. Generate and observe coverage report for any test bench.
10. Implementation of Reset Synchronized and instantiation of the same in 4-Bit PIPO Shift Register.
11. Observing and obtaining minimum and maximum delays of a given logical circuit.
12. (a) Designing of D-latch. (b) Designing of D Flip-Flop using D- Latch. (c) Designing of 3-bit counter using The D Flip-Flop designed in (b) part. (d) Check for setup and hold violation for first DFF and observe the output of remaining flip flops, where setup time is 4ns and hold time is 3ns.

Requirements of Software Labs –

Mentor Graphics ModelSim / QuestaSim, Xilinx ISE Design Suite (Version 14 or higher), Xilinx Vivado (Version 2014.1 or higher)

Hardware Labs:

The following codes should be simulated, synthesised and implemented on the target hardware:

1. At least three Combinational Logic Designs
2. At least three Sequential Logic Designs
3. At least one IP based Design
4. At least one FSM Based Design
5. At least one simple communication protocol

Requirements of Hardware Labs –

Xilinx FPGA Trainer Kit (Virtex-4 or higher), ZedBoard.