Verification Environment using System Verilog

Outline

- What & why verification environment
- Model checking
- Fault checking
- Types of testing
- Basic components of SV based verification environment
- Case study: memory model

- is a standardized approach of verifying integrated circuit designs, targeting a Coverage-Driven Verification (CDV).
- It combines automatic test generation, self-checking test-benches, and coverage metrics to indicate progress in the design verification.

- Reduced Design cycle time
- Increased design complexity
- Market demand
- Reusability

Checking techniques

Fault checking:

It involves applying tests to failed chips and analyzing the test results to determine the nature of the fault.

model checking:

A method for checking whether a design or system meets a given specification with some reference model

Testing approach

- **Black box testing:**

A form of testing that is performed with no knowledge of a system's internals

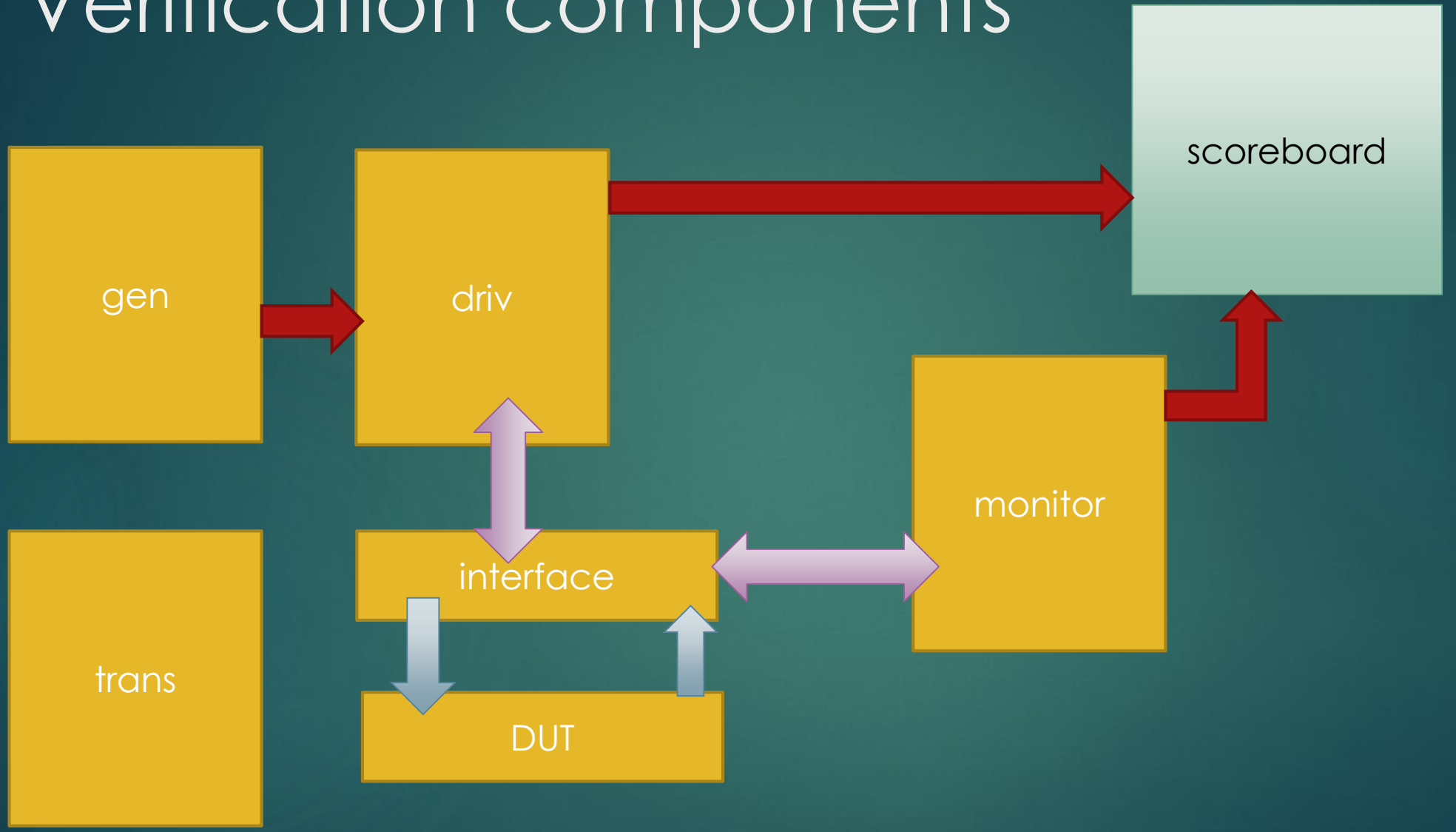
- **White box testing:**

A form of application testing that provides the tester with complete knowledge of the application being tested, including access to source code and design documents.

- **Gray box testing:**

The grey box technique is the blend of white box and black box testing.

Verification components



Case study

- Memory model