CMOS VLSI and Aspects of ASIC Design

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Session 8

Lecture: IC Fabrication using CMOS Technology

- ✓ CMOS Technology, wafer formation, photolithography
- ✓ Well and channel formation, Silicon dioxide and gate oxide
- ✓ Overview of CMOS Fabrication Steps

IC Fabrication using CMOS Technology

- ✓ Well-established CMOS fabrication technology depends upon both n-channel (nMOS) and p-channel (pMOS) transistors be built on the same chip substrate.

- ✓ To accommodate both nMOS and pMOS devices, special regions must be created in which the semiconductor type is opposite to the substrate type.

- ✓ These regions are called **wells or tubs**.

- ✓ A p-well is created in an n-type substrate or, alternatively, an n-well is created in a p-type substrate

Simplified process sequence for the fabrication of CMOS integrated circuits on a p-type silicon substrate

IC Fabrication using CMOS Technology

CMOS Technology:

- CMOS processing steps can be broadly divided into two parts.
- Transistors are formed in the Front-End-of-Line (FEOL) phase, while wires are built in the Back-End-of-Line (BEOL) phase.

Wafer Formation:

- The basic raw material used in CMOS fabs is a *wafer* or disk of silicon, roughly 75 mm to 300 mm (12”–a dinner plate!) in diameter and less than 1 mm thick.
- Wafers are cut from *boules*, cylindrical ingots of single-crystal silicon, that have been pulled from a crucible of pure molten silicon. This is known as the *Czochralski* method and is currently the most common method for producing single-crystal material

IC Fabrication Flow: Basic Steps

- The integrated circuit may be viewed as a set of patterned layers of doped silicon, polysilicon, metal, and insulating silicon dioxide.
- In general, a layer must be patterned before the next layer of material is applied on the chip. The process used to transfer a pattern to a layer on the chip is called **lithography.**
- In areas where the mask is absent, the implantation can occur, or dielectric or metal could be etched away. The patterning is achieved by a process called photolithography, from the Greek photo (light), lithos (stone), and graphe (picture), which literally means "carving pictures in stone using light."
- The sequence starts with the **thermal oxidation** of the silicon surface (a), by which an **oxide layer** of about 1 mm thickness (b).
- The entire oxide surface is then covered with a layer of **photoresist**, which is essentially a light-sensitive, acid-resistant organic polymer, initially insoluble in the developing solution (c).

IC Fabrication Flow: Basic Steps

- If the photoresist material is exposed to ultraviolet (UV) light, the exposed areas become soluble so that they are no longer resistant to etching solvents.
- To selectively expose the photoresist, we have to cover some of the areas on the surface with a mask during exposure. Thus, when the structure with the mask on top is exposed to UV light, areas which are covered by the opaque features on the mask are shielded (d).
- In the areas where the UV light can pass through, on the other hand, the photoresist is exposed and becomes soluble. The type of photoresist which is initially insoluble and becomes soluble after exposure to UV light is called **positive photoresist** and opposite is the **negative photoresist**.
- Negative photoresists are more sensitive to light, but their photolithographic resolution is not as high as that of the positive photoresists. Therefore, negative photoresists are-used less commonly in the manufacturing of high-density integrated circuits.

IC Fabrication Flow: Basic Steps

IC Fabrication Flow: Basic Steps

- Following the UV exposure step, the unexposed portions of the photoresist can be removed by a solvent. Now, the silicon dioxide regions which are not covered by hardened photoresist can be etched away either by using a chemical solvent (HF acid) or by using a dry etch (plasma etch) process (e).
- Note that at the end of this step, we obtain an oxide window that reaches down to the silicon surface (f). The remaining photoresist can now be stripped from the silicon dioxide surface by using another solvent, leaving the patterned silicon dioxide feature on the surface (g).

Fabrication of The nMOS Transistor

- The process starts with the oxidation of silicon substrate (a), in which a relatively silicon thick dioxide layer, also called field oxide, is created on the surface (b).

- Then, the field oxide is selectively etched to expose the silicon surface on which the MOS transistor will be created (c).

- Following this step, the surface is covered with a thin, high-quality oxide layer, which will eventually form the gate oxide of the MOS transistor (d).

Fabrication of The nMOS Transistor

Fabrication of The nMOS Transistor

- On top of the thin oxide layer, a layer of polysilicon (polycrystalline silicon) is deposited (e). Polysilicon is used both as gate electrode material for MOS transistors and also as an interconnect medium in silicon integrated circuits.

- After deposition, the polysilicon layer is patterned and etched to form the interconnects and the MOS transistor gates (f).

- The thin gate oxide not covered by polysilicon is also etched away, which exposes the bare silicon surface on which the source and drain junctions are to be formed (g).

- The entire silicon surface is then doped with a high concentration of impurities, either through diffusion or ion implantation (in this case with donor atoms to produce n-type doping.

Fabrication of The nMOS Transistor

Fabrication of The nMOS Transistor

- Then the doping penetrates the exposed areas on the silicon surface, ultimately creating two n type regions (source and drain junctions) in the p-type substrate (h).

- The impurity doping also penetrates the polysilicon on the surface, reducing its resistivity. Note that the polysilicon gate, which is patterned before doping, actually defines the precise location of the channel region and, hence, the location of the source and the drain regions. Since this procedure allows very precise positioning of the two regions relative to the gate, it is also called the self-aligned process.

- Once the source and drain regions are completed, the entire surface is again covered with an insulating layer of silicon dioxide (i).

- The insulating oxide layer is then patterned in order to provide contact windows for the drain and source junctions (j).

Fabrication of The nMOS Transistor

Fabrication of The nMOS Transistor

- The surface is covered with evaporated aluminium which will form the interconnects (k).
- Finally, the metal layer is patterned and etched, completing the interconnection of the MOS transistors on the surface (l). Usually, a second (and third) layer of metallic interconnect can also be added on top of this structure by creating another insulating oxide layer, cutting contact (via) holes, depositing, and patterning the metal.

Well and Channel Formation

The following are main CMOS technologies:

- n-well process
- p-well process
- twin-well process
- triple-well process

- In a n-well process, the pMOS transistors are built in a n-well and the nMOS transistor is placed in the p-type substrate and p-well process is reverse one.
- p-well processes were used to optimize the pMOS transistor performance.
- Twin-well processes accompanied the emergence of n-well processes. A twin-well process allows the optimization of each transistor type.
- A third well can be added to create a triple-well process. The triple-well process has emerged to provide good isolation between analog and digital blocks in mixed-signal chips; it is also used to isolate high-density dynamic memory from logic. Most fabrication lines provide a baseline twin-well process that can be upgraded to a triple-well process with the addition of a single mask level.

Overview of CMOS n-Well Fabrication Steps

- The n-well CMOS process starts with a moderately doped (with impurity concentration typically less than 10^{15} cm^{-3}) p-type silicon substrate.

- Then, an initial oxide layer is grown on the entire surface. The first lithographic mask defines the n-well region.

- Donor atoms, usually phosphorus, are implanted through this window in the oxide.

- Once the n-well is created, the active areas of the nMOS and pMOS transistors can be defined.

Overview of CMOS n-Well Fabrication Steps

Creation of the n-well region, a thick field oxide is grown in the areas surrounding the transistor's active regions, and a thin gate oxide is grown on top of the active regions

Overview of CMOS n-Well Fabrication Steps

The polysilicon layer is deposited using chemical vapor deposition (CVD) and patterned by dry (plasma) etching. The created polysilicon lines will function as the gate electrodes of the nMOS and the pMOS transistors and their interconnects

Overview of CMOS n-Well Fabrication Steps

Using a set of two masks, the n+ and p+ regions are implanted into the substrate and into the n-well, respectively

Overview of CMOS n-Well Fabrication Steps

An insulating silicon dioxide layer is deposited over the entire wafer using CVD. Then, the contacts are defined and etched away to expose the silicon or polysilicon contact windows

Overview of CMOS n-Well Fabrication Steps

Metal (aluminium) is deposited over the entire chip surface using metal evaporation, and the metal lines are patterned through etching

Overview of CMOS n-Well Fabrication Steps

The resulting cross-sectional view of the chip, showing one nMOS and one pMOS transistor (in the n-well), and the polysilicon and metal interconnections. The final step is to deposit the passivation layer (for protection) over the chip, except over wire-bonding pad areas

Session 9

Lecture: Memory using CMOS

- Design of Complex circuits
- SRAM, DRAM & Current Mirror
- Memory cell and their read write operation.

Memory using CMOS

Design of Complex circuits:

- Designing complex circuits involves several stages, methodologies, and tools to ensure the final product meets performance, power, and area (PPA) specifications.
- We have already discussed in session 3.

$$Z = \overline{a\,b + c\,(d + e)}$$

Memory using CMOS

CMOS Memories:

- Random access memory is commonly classified as read-only memory (ROM) or read/write memory (RAM).
- Volatile memory (RAM) retains its data as long as power is applied, while nonvolatile memory (ROM) will hold data indefinitely.

Memory using CMOS

CMOS Memories:

SRAM:

- ✓ Data stored as long as supply is applied
- ✓ Large (6 transistors/cell)
- ✓ faster and less troublesome, but require more area per bit

DRAM:

- ✓ Periodic refresh required (use charge stored on a floating capacitor)
- ✓ Small (1-3 transistors/cell)
- ✓ Slower and more troublesome, but require less area per bit

Memory Cell and Their Read Write Operation

6T SRAM Cell:

- A SRAM cell needs to be able to read and write data and to hold the data as long as the power is applied.
- An ordinary flip-flop could accomplish this requirement, but the size is quite large.

- Cross Coupled Inverters Stores data
- Bit Lines: True & Complementary data
- M5, M6 Access Transistors
- Word Line asserted to Read/Write cell

Memory Cell and Their Read Write Operation

4x4 6T SRAM Cell:

Memory Cell and Their Read Write Operation

DRAM Cell:

- Very high density & low cost
- Charge stored on a capacitor (logic level)
- Needs refreshing
  - Stored charge leaks-out due to leakage current
  - Typically 2 ms
- 3 Transistor cells
  - Now 1-T cell
- Periphery circuitry also in CMOS
  - decoders, selectors, sense amplifier, out-drivers

- Like SRAM, the cell is accessed by asserting the wordline to connect the capacitor to the bitline. On a read, the bitline is first precharged to *VDD*/2.
- When the wordline rises, the capacitor shares its charge with the bitline, causing a voltage change ΔV that can be sensed.
- The read disturbs the cell contents at *x*, so the cell must be rewritten after each read.
- On a write, the bitline is driven high or low and the voltage is forced onto the capacitor.

Memory Cell and Their Read Write Operation

Techniques for building DRAM capacitors:

Stacked capacitor process: capacitor is stacked on top of the transistor. The capacitor is built as a parallel plate capacitor using two poly layers as the two plates, separated by a SiO2 layer as a dielectric.

Trench capacitor process: capacitor is built by etching a deep vertical groove into the silicon, followed by growing a SiO2 layer, followed by a poly layer.

- Both of these techniques help reduce the cell size, and hence increase the density of the DRAM. The value of the capacitor is around 25fF.

Current Mirror Circuit

Current Mirror Circuit:

- A current mirror circuit is a fundamental building block in electronics used to replicate or mirror a current flowing in one branch to another branch of the circuit.
- It typically consists of two or more transistors where one transistor (called the reference transistor) sets the desired current and another transistor (the mirrored transistor) replicates this current.

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2,$$

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}.$$

- The key property of this topology is that it allows precise copying of the current with no dependence on process and temperature.

Session 10

Lecture: Advanced Trends in Backend VLSI

- Sequential CMOS logic
- Circuit Design of Latches and Flip-Flops
- Introduction to FinFET technology

Sequential CMOS Logic

Sequential CMOS Logic:

- Here, the output is determined by the current inputs as well as the previously applied input variables.
- Bistable circuits have two stable states or operation modes, each of which can be attained under certain input and output conditions. Ex: latch and flip-flop, registers.
- Monostable circuits, have only one stable operating point (state).
- Astable circuits have no stable operating point or state which the circuit can preserve for a certain time period.

Circuit Design of Latches and Flip-Flops

Latches and Flip-Flops:

- Latches and flip-flops are both used for memory elements, data storage in digital circuits.

Latches:

- A latch is a basic storage element that stores one bit of data.
- Latches are level-sensitive devices, meaning they maintain their output state as long as the enable signal (clock or control signal) is active.
- Example: SR (Set-Reset) latch, D (Data) latch, and JK latch.

Flip-Flops:

- A flip-flop is a more sophisticated sequential logic circuit that can store one bit of data and toggle between two states (0 or 1) based on a clock signal.
- Flip-flops are edge-triggered devices, meaning they change state (output) only on a clock edge (rising or falling).
- Example: SR (Set-Reset) flip-flop, D (Data) flip-flop, JK flip-flop, and T (Toggle) flip-flop.

Circuit Design of CMOS SR Latch

Design of CMOS SR latch circuit based on NOR2 gates:

- One of the input terminals of each NOR gate is used to cross-couple to the output of the other NOR gate, while the second input enables triggering of the circuit.
- The SR latch circuit has two complementary outputs, Q and Q'.

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	Q_n	$\overline{Q_n}$	hold
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

Truth table of the NOR-based SR latch circuit

Circuit Design of CMOS SR Latch

Design of CMOS SR latch circuit based on NOR2 gates:

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
V_{OH}	V_{OL}	V_{OH}	V_{OL}	M1 and M2 on, M3 and M4 off
V_{OL}	V_{OH}	V_{OL}	V_{OH}	M1 and M2 off, M3 and M4 on
V_{OL}	V_{OL}	V_{OH}	V_{OL}	*M*1 and M4 off, M2 on, or
V_{OL}	V_{OL}	V_{OL}	V_{OH}	M1 and M4 off, M3 on

Operation modes of the transistors in the NOR-based CMOS SR latch circuit

Circuit Design of CMOS SR Latch

Design of CMOS SR latch circuit based on NAND2 gates:

- A close inspection of the NAND-based SR latch circuit reveals that in order to hold (preserve) a state, both of the external trigger inputs must be equal to logic "1".

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	1	1	not allowed
0	1	1	0	set
1	0	0	1	reset
1	1	Q_n	$\overline{Q_n}$	hold

Truth table of the NAND-based SR latch circuit

Circuit Design of CMOS SR Latch

Design of CMOS SR latch circuit based on NAND2 gates:

Circuit Design of CMOS SR Flip-Flop

Design of CMOS SR Flip-flop circuit based on NOR2 gates:

Circuit Design of CMOS SR Flip-Flop

Design of CMOS SR Flip-flop circuit based on NAND2 gates:

Circuit Design of CMOS JK Flip-Flop

Design of CMOS JK Flip-flop circuit based on NAND2 gates:

J	K	Q_n	$\overline{Q_n}$	S	R	Q_{n+1}	$\overline{Q_{n+1}}$	*Operation*
0	0	0	1	1	1	0	1	*hold*
		1	0	1	1	1	0	
0	1	0	1	1	1	0	1	*reset*
		1	0	1	0	0	1	
1	0	0	1	0	1	1	0	*set*
		1	0	1	1	1	0	
1	1	0	1	0	1	1	0	*toggle*
		1	0	1	0	0	1	

Circuit Design of CMOS JK Flip-Flop

Design of CMOS JK Flip-flop circuit based on NOR2 gates:

Introduction to FinFET Technology

FinFET Technology:

- ✓ FinFET technology represents a significant advancement in semiconductor device fabrication, especially in the realm of modern integrated circuits (ICs).
- ✓ FinFET technology has seen several generations of refinement (e.g., 22nm, 14nm, 10nm, 7nm, and beyond), with each new node offering improved performance, reduced power consumption, and increased transistor density.

FinFET:

- ✓ FinFET (Fin Field-Effect Transistor) is a type of transistor architecture that differs from the traditional planar MOSFET.
- ✓ Instead of a planar channel, FinFETs have a thin vertical fin-like structure that protrudes from the substrate.
- ✓ Field Effect Transistor with Fins having 3D structure.
  - ✓ Better control over current (by implementing a gate on each of the three sides of a fin)
  - ✓ Gate is wrapped around the channel

Introduction to FinFET Technology

FinFET:

- ✓ The fin structure provides multiple surfaces for the control of current flow, allowing better control over the transistor's behavior compared to planar transistors. This results in improved performance and energy efficiency.

Planer

Ultra Thin-body SOI

DoubleGate

TriGate
(Oxide thickness same around Fin)

FinFET (Oxide thickness more at top than side)

Introduction to FinFET Technology

FinFET Advantages:

- **Improved Control**: FinFETs offer better electrostatic control of the channel, reducing leakage currents and improving overall energy efficiency. This is crucial for meeting the demands of modern high-performance and low-power electronic devices.
- **Scaling**: FinFET technology enables continued scaling of transistor dimensions, allowing manufacturers to pack more transistors into a given area without compromising performance or increasing power consumption excessively.
- **Performance**: FinFETs typically exhibit higher drive currents and faster switching speeds compared to planar MOSFETs, making them suitable for high-speed digital circuits, processors, and memory devices.

FinFET Applications:

- **Integrated Circuits**: FinFET technology is predominantly used in the fabrication of modern ICs, including microprocessors, system-on-chips (SoCs), graphics processors, and memory devices.
- **Mobile Devices**: Due to their energy efficiency and performance benefits, FinFETs are widely adopted in mobile devices such as smartphones and tablets to extend battery life and improve processing capabilities.

Future Devices

Session 11

Lecture: CMOS Design Issues

- Design issue like Delays, Cross talk, Velocity saturation,
- Body effect, latch up, electro migration, hot carrier and Channel Length modulation

CMOS Design Issues

- CMOS design faces several challenges that engineers must address to ensure reliable and efficient circuit operation.

Delays:

- Delay is a critical issue that affects the overall performance and speed of the circuit.
- Delay refers to the time it takes for a signal to propagate through a logic gate or a series of gates from input to output.
- Several factors contribute to delay in CMOS circuits are
  - Load Capacitance
  - Parasitic Capacitance and Resistance
  - Gate Length Reduction
  - Setup and Hold Times
  - Clock Distribution
  - Intrinsic Delay
  - Process variations

CMOS Design Issues

Crosstalk:

- Crosstalk refers to undesired or unintentional effects, which can cause functional failure in the chips.
- This functional failure refers to either change in the value of the signal voltage or change in timing.
- It is the unwanted signal due to coupling capacitance between two nets.
- It refers to unintentional coupling of activity between two or more signals.

Avoid crosstalk by:

a. Spacing between nets
b. Shielding
c. Increase the drive strength of cell
d. Layer jumping
e. Maintain the stable supply.

CMOS Design Issues

Velocity Saturation:

- Velocity saturation is a phenomenon that occurs in semiconductor devices, particularly when operated at high electric fields or under strong inversion conditions.

- It limits the maximum achievable current (saturation current) in the transistor because the carriers no longer accelerate linearly with the applied electric field.

- Instead, their velocity saturates, leading to a gradual increase in current with voltage rather than a linear rise.

- Velocity saturation affects the maximum drain current (Idsat) that a transistor can deliver under high voltage conditions. It impacts the speed and efficiency of CMOS circuits, especially in applications requiring high-speed operation.

- Velocity saturation can also impact the effective threshold voltage (Vth) of the transistor, affecting its switching characteristics and overall performance.

CMOS Design Issues

Body Effect:

- The "body effect," also known as the "substrate bias effect," is a phenomenon that affects the threshold voltage (Vth) of MOSFET.
- It arises due to the interaction between the substrate (body) of the transistor and the channel region under different biasing conditions.
- The body effect can also vary with temperature due to changes in carrier concentration and mobility in the substrate, influencing transistor performance in temperature-sensitive applications.
- In some advanced CMOS designs, body biasing techniques (forward or reverse biasing of the substrate) are used to dynamically adjust Vth to optimize transistor performance, reduce leakage currents, or improve speed.

latch up:

- Latch up is a condition where a low impedance path is created between a supply pin and ground.
- This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present.
- Latch up reduction includes putting a high resistance in the path so as to limit the current through supply.

CMOS Design Issues

Electro migration:

- Electron migration is the movement of atoms based on the flow of current through a material. If the current density is high enough, the heat dissipated within the material will repeatedly break atoms from the structure and move them.
- Displacement of the atoms as a result of current flowing through a conductor which causes voids and failures in a device.
- Electromigration (EM) analysis in VLSI design refers to optimizing IC interconnects to prevent electrochemical growth.
- EM can reduce by wire widening, frequency reduction, lower the supply voltage, short wire length and cell sizing.

Voids/ Open

Hillocks/ Short

Short in Metal layer

Open in Metal layer

Open in Via

CMOS Design Issues

Hot Carrier:

- Hot carrier effects refer to phenomena that occur in MOSFET, when carriers (electrons or holes) gain sufficient kinetic energy due to high electric fields within the transistor structure.
- These effects can impact the device reliability and performance over time.
- Hot carrier effects are critical considerations in advanced MOSFET design, impacting transistor performance, reliability, and longevity.
- Effective mitigation strategies involve a combination of design optimization, process improvements, and simulation techniques to minimize the adverse effects of hot carriers on semiconductor devices.

Channel Length Modulation:

- It is a phenomenon in MOSFET, where the effective channel length varies with the drain-source voltage (Vds).
- This effect occurs due to the electric field extending the depletion region into the channel region near the drain as Vds increases, which reduces the effective channel length (Leff) (Early effect).
- This reduction in effective channel length leads to a decrease in channel resistance, allowing a higher drain current (Ids) to flow for a given Vds.

THANK YOU