

Suggested Teaching Guidelines for

Advanced Digital Design PG-DVLSI March-2024

Duration: 50 class room hours

Objective: To introduce Digital Design and Advance Digital Design Issues

Prerequisites: Knowledge of Digital Fundamentals

Evaluation method: CCEE Theory exam – 80% weightage

Internal exam – 20% weightage

List of Books / Other training material

Text Book:

1. Digital Design - Principles and Practices by John F Wakerly

Reference:

1. An Engineering Approach to Digital Design by Fletcher

Session 1

Lecture: Basic Digital Circuits

- Basic Digital Circuits: Introduction, Principles, Working.
- Usage / Applications.

Session 2

Lecture: Combination Circuits

- Logic Arrays
- NAND-NAND / NOR-NOR circuits
- Encoders and Decoders

Session 3

Lecture: Arithmetic Circuits

- 2's Complement
- Half and Full adders
- RCA,CLA,CSA

Session 4 & 5

Lecture: Logic Minimization

- Introduction to Various Logic Minimization techniques
- Quine McCluskey technique
- Shannon's reduction using relay switches

Session 6

Lecture: Logical Hazards

- Hazards and glitches
- Hazard elimination

Session 7

Lecture: Logic Families

PG-DVLSI Page 1 of 3



- Introduction to different Logic families with their sub-families/types.
- TTL NAND using TTL with working, different types of TTL families with features, usage.
- ECL NAND using ECL with working, different types of ECL families with features, usage.
- CMOS NAND using CMOS with working, Different types of CMOS families with features, usage.
- Comparison of speed and power of different families and sub-families/types.

Session 8

Lecture: Tristate and other circuits

- Tristate
- Muller-C
- AOI (And-Or-Inverter)
- Design of Logic Gates with CMOS technology: NOT, NAND, NOR, XOR.

Session 9

Lecture: Sequential Circuits

- Sequential Circuit Principles
- Types of Sequential Circuits
- Clock jitter, clock skew, timing parameters, propagation delays
- Latches
- Flip-flops

Session 10 & 11

Lecture: Counter Design and Frequency Division

- Counters: Introduction and types
- Designing of Counters using FSM approach: MOD-N, Binary, Decade
- Binary Counter as a Frequency divider
- Frequency division hazards

Session 12

Lecture: Registers

- Registers
- Shift Registers
- LIFO
- FIFO
- LFSR

Session 13 & 14

Lecture: Finite State Machines (FSM)

- Types of FSM
- Problem solving
- State reduction techniques

Session 15 & 16

Lecture: Static Timing Analysis

PG-DVLSI



- Need of Static Timing Analysis of Digital Circuits
- Metastability
- Setup and Hold Violations
- Time Borrowing and Time Stealing

Session 17 & 18

Lecture: Asynchronous Circuits

- Introduction to multiple clock domain circuits
- Working across multiple clock domains
- Handshaking

Session 19 & 20

Lecture: Asynchronous to Synchronous Circuit Interaction

Session 21-24

Lecture: Case studies of Advanced Digital Design Circuits

 Several case studies like complex FSMs, Real life problems and their solutions, Pipelined Approaches for Communication Protocols or Recursive Operations, Design Optimization, Latency reduction, Development of Microporcessor / Microcontroller Design, Circuit Development for Data Encryption / Decryption Algorithms etc.

PG-DVLSI Page 3 of 3