CMOS VLSI and Aspects of ASIC Design

PRESENTED BY:

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CMOS VLSI and Aspects of ASIC Design

Pre-requisites: Knowledge of Basic Electronics

Course Educational Objectives:

- ✓ To make the students familiar with the basic concept of CMOS device and its manufacturing technology
- ✓ Introduction to design & simulation of CMOS digital integrated circuits
- ✓ To have a complete knowledge of aspects of ASIC design

Course Outcomes:

- ❖ To understand and analyse the basics of VLSI Technology including fabrication processes
- ❖ Able to design & demonstrate different combinational logic circuits & sequential logic circuits
- ❖ To understand the aspects of ASIC design flow

SYLLABUS

Session 1
Lecture: Metal Oxide Semiconductors (MOS)
- Overview of CMOS Module
- Introduction of MOS devices
- n-MOS, p-MOS and CMOS
- MOS operation

Session 2
Lecture: CMOS Gates and Characteristics
- CMOS Logic Circuits
- CMOS Inverter and I-V Characters

Session 3
Lecture: Design of Complex Functions
- Design of Complex Functions using CMOS

Session 4
Lecture: MOS Cells
- Structure of MOS cells
- Threshold Voltage and DC transfer characteristics
- Introduction to IC Design Cycle and layout

Session 5
Lecture: CMOS functioning and parameters
- CMOS as a switch, estimation of parasitic values
- rise and fall times
- power dissipation
  - ❖ Dynamic and Static
  - ❖ Low power architecture

Session 6
Lecture: Technology Scaling
- ✓ Device sizing, rationed and non-rationed logic
- ✓ Concepts of Interconnect
- ✓ Transistor Scaling and interconnect Scaling

Session 7
Lecture: CMOS Logic Circuits
- ✓ Design of logic circuit, fabrication steps
- ✓ CMOS Combinational Logic circuits
- ✓ Design of NAND and NOR Gates
- ✓ Transmission Gates

Session 8
Lecture: IC Fabrication using CMOS Technology
- ✓ CMOS Technology, wafer formation, photolithography.
- ✓ Well and channel formation, Silicon dioxide and gate oxide.

Session 9
Lecture: Memory using CMOS
- ✓ Design of Complex circuits
- ✓ SRAM, DRAM & current Mirror
- ✓ Memory cell and their read write operation.

Session 10
Lecture: Advanced Trends in Backend VLSI
- ✓ Overview of CMOS Fabrication Steps
- ✓ Sequential CMOS logic
- ✓ Circuit Design of Latches and Flip-Flops
- ✓ Introduction to FinFET technology

Session 11
Lecture: CMOS Design Issues
- ✓ Design issue like Delays, Cross talk , Velocity saturation,
- ✓ Body effect, latch up, electro migration, hot carrier and Channel Length modulation

Session 12
Lecture: Aspects of ASIC Design
- ❖ Introduction of ASIC Design,
- ❖ An overview of Backend VLSI Design Flow – Libraries, Floorplanning, Placement, Routing, Verification, Testing.
- ❖ Flow Diagram, Specifications and Schematic cell Design.
- ❖ Spice simulation. Analysis of analog and digital circuits, Circuits elements, AC and DC analysis.

Session 13
Lecture: Characteristics of Different Technologies
- ❖ Transfer Characteristics, Transient responses, Noise analysis of current and voltage based on different technologies.

Session 14
Lecture: Back-end Processes
- ❖ Fabrication methods of circuit elements, Layout design of different cells.
- ❖ Library cell designing, NAND, NOR, NOT, X-OR etc.
- ❖ Circuit Extraction, Electrical rule check, LVS, Post layout Simulation and parasitic extraction.

Session 15 & 16
Lecture: Back-end Designing and Analysis
- ❖ Design format, timing analysis, back annotation and post layout simulation of silicon circuit
- ❖ Study of design Issues Antenna effect, Electro migration effect body effect, Inductive and capacitive cross talk, Drain punch through, etc.
- ❖ Placement of cells, placing of I/O blocks, Initialization of floor planning, routing and creating design data base
- ❖ DFT Guidelines, Test Pattern and BIST
- ❖ ASIC design implementation

REFERENCES

Courseware:

1. CMOS VLSI Design: A Circuit and Systems Perspective by Ayan Banerjee, Neil H. E. Weste, David Harris / Pearson
2. Application Specific Integrated Circuits by Michael John Sebastian Smith Addison, Wesley

Reference Books:

1. Design of Analog CMOS Integrated Circuits 1st Edition by RAZAVI /TMH
2. VLSI Technologies by SEZ
3. Spice for Circuits and Electronics by Md. H. Rashid (PHI Publication)
4. Kang Sung M., and Leblebici Y., CMOS Digital Integrated Circuits: Analysis and Design, Tata McGraw-Hill Publishing Company Limited, Third Edition, 2003.

Introduction To VLSI

- VLSI appears to be one of the greatest tech innovations in the modern electronic product and computer manufacturing industry, particularly when discussing integrated circuits, component designing and microchip processors.

- Wireless communication has achieved its heights due to the successful application of VLSI.

- VLSI: Process of integrating billions of transistors to make complex chips.

Major Chips Makers:

✓ Microprocessors: Intel, AMD
✓ Mobile Processors: Qualcomm, Mediatek, Samsung
✓ Microcontrollers: ARM, Texas Instruments, Cypress, Atmel
✓ Networking Chips: Cisco, Juniper Networks, Broardcom
✓ Memory: Rambus, SanDisk, Western Digital
✓ FPGA: Xilinx, Microsemi

Why VLSI?

- VLSI is a booming industry, and job opportunities have been massive throughout the last decade, specifically in Bengaluru, Hyderabad, Pune, Noida, etc.
- With increasing digitalization the necessity of manufacturing advanced ICs is the need of the hour.
- The invention of transistors inspired the underlying principles of VLSI design.

- ❖ Circuit sizes are much smaller if we compare them to their older versions.
- ❖ VLSI circuits are expected to capture relatively low space.
- ❖ VLSI utilizes less power than its active counterpart (discrete components).
- ❖ The overall expense of manufacturing electronic gadgets has become lower due to this technological innovation.
- ❖ Researchers are hopeful of further elevating the VLSI's operating speed and capacity.

Roadmap to Start Career in VLSI

Types of VLSI Companies:

EDA
- Development of tools and provide support of that tools.
- Synopsys, cadence, mentor, etc

DESIGN BASED
- Designing a chip.
- Intel, Qualcomm, NXP, etc.

FOUNDRY
- IC manufacturing and fabrication.
- TSMC, Samsung and Global Foundry, etc.

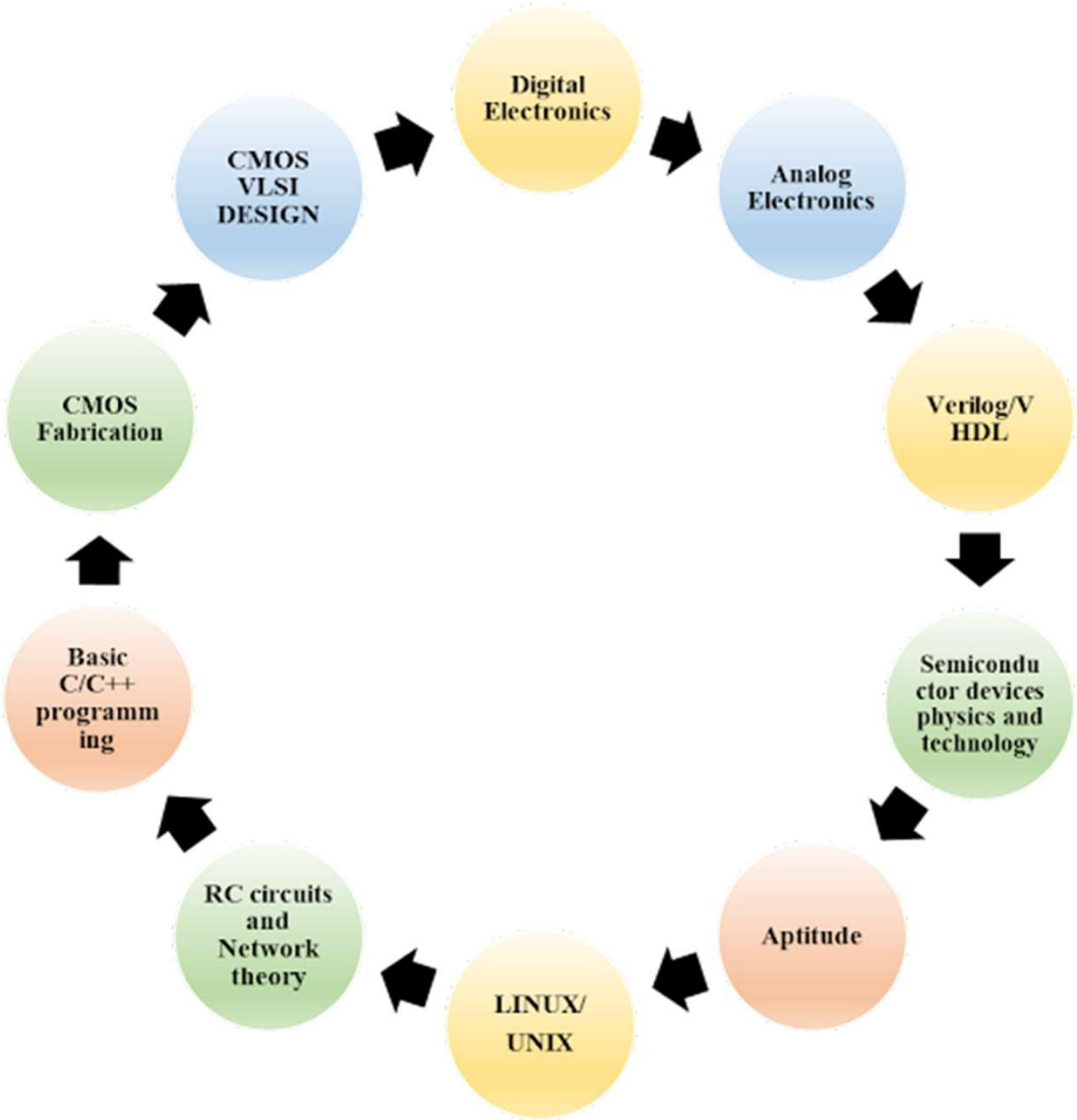
Job Profiles:

Frontend
- RTL Design Engineer
- IP/SOC Design Engineer
- RTL Integration Engineer
- ASIC/IP/SOC Verification Engineer
- Pre Silicon Validation Engineer
- FPGA Design/Prototyping Engineer
- Emulation Engineer
- DFT Engineer
- Formal Verification Engineer
- Post Silicon Validation Engineer

Backend
- Physical Design Engineer
- Synthesis and STA Engineer
- Physical Verification Engineer
- Layout Design Engineer
- Analog and Mixed Signal Circuit Design Engineer

Roadmap to Start Career in VLSI

Fundamental topics for every VLSI profile:



Industry Expectations

VLSI/Semiconductor Companies

- Semiconductor companies in India are broadly categorized into:
    1. Product Based Companies (Qualcomm, Intel, Broadcom, AMD, etc)
    2. Service Based Companies (Sankalp, Moschip, PerfactVIP, Altran, etc)
    3. EDA Companies (Cadence, Mentor Graphics, Synopsys, Aldec, etc)
- All based companies will always be in sync up to meet the technology deliverables with the support of VLSI Engineers.

Product-Based Company	Service-Based Company
These are the companies that have their own products to sell.	These companies may or may not have their products, but their primary business is service.
These hire a very limited number of candidates from top colleges like IITs and NITs.	These are the mass recruiters in campus placements.
These provide high salaries and hikes, also the salary is revised based on the cost of living.	These provide comparatively less salary and hikes.
These conduct more interview rounds, and cracking interviews is a bit more difficult than Service-Based companies.	Cracking interview is relatively easy and has few rounds.
The Learning curve is good, optimized, and efficient. Also, you get to work on the latest technologies.	The learning curve is average. Generally, they put freshers into support projects.
Flexible office timings, all you need to do is finish your work in the given time frame.	Strict office timings, around 7-9 working hours per day.
Relatively high job security.	Relatively low job security.

Career Opportunities in VLSI

Physical Design	ASIC Design & verification	Analog Layout Design
Physical design engineer	ASIC Designer	AMS Layout design
STA engineer	RTL Verification	STD cell Layout design
EM IR Sign off Engineer	IP verification engineer	IO Layout design
DFT Engineer	RTL Designer	Memory Layout design
Methodology & Flow Engineer	ASIC verification engineer	RF Layout design
Physical verification Engineer	UVM verification engineer	PDK/DRC Expert

Session 1 & Session 4

Lecture: Metal Oxide Semiconductors (MOS)

- ✓ Overview of CMOS Module
- ✓ Introduction of MOS devices
- ✓ n-MOS, p-MOS and CMOS
- ✓ MOS operation

Lecture: MOS Cells

- ➢ Structure of MOS cells
- ➢ Threshold Voltage and DC transfer characteristics
- ➢ Introduction to IC Design Cycle and layout

Overview of CMOS Module

- CMOS (Complementary Metal-Oxide-Semiconductor) technology is fundamental in creating integrated circuits (ICs) and digital logic circuits.

- Key Components of a CMOS Module are:
  - ✓ Transistors (n-MOS & p-MOS)
  - ✓ Logic Gates (NOT, NAND, NOR, XOR, etc)
  - ✓ Power Supply (VDD, GND)
  - ✓ Input/Output Ports (Receive/send signals from/to other devices)
  - ✓ Interconnects (Metal connections to form complex circuits)
  - ✓ Capacitors (To form dynamic circuits and storage elements)
  - ✓ Substrate (Silicon base on which the CMOS circuit is built)

- The use of Digital CMOS ICs in high-performance computing, telecommunications and consumer electronics have been growing at a very fast pace.

Overview of CMOS Module

- The monolithic integration of a large number of functions on a single chip usually provides:
  - ✓ Less area/volume and therefore, compactness
  - ✓ Less power consumption
  - ✓ Less testing requirements at system level
  - ✓ Higher speed, due to significantly reduced interconnection length
  - ✓ Significant cost savings

ERA	DATE	COMPLEXITY (# of logic blocks per chip)
Single transistor	1958	< 1
Unit logic (one gate)	1960	1
Multi-function	1962	2 - 4
Complex function	1964	5 - 20
Medium Scale Integration (MSI)	1967	20 - 200
Large Scale Integration (LSI)	1972	200 - 2,000
Very Large Scale Integration (VLSI)	1978	2,000 - 20,000
Ultra Large Scale Integration (ULSI)	1989	20,000 - ?

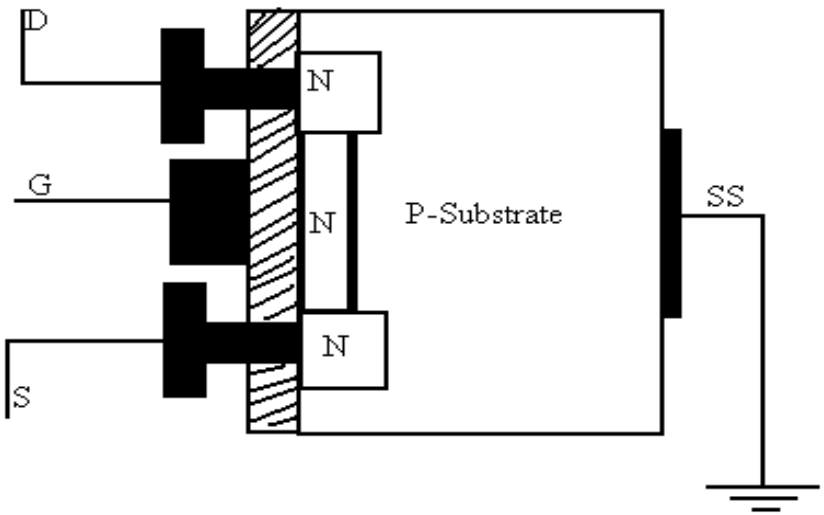
Evolution of logic complexity in integrated circuits

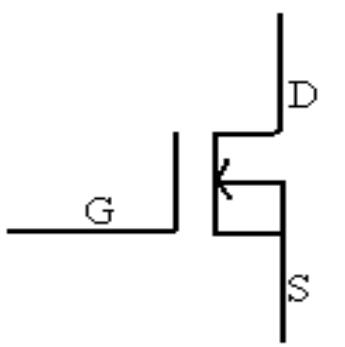
Introduction of MOS devices

- Compared to the bipolar junction transistor (BJT), the MOS transistor occupies a relatively smaller silicon area, and its fabrication involves fewer processing steps.
- There are two types of MOSFETs (Metal Oxide Semiconductor Field Effect Transistor).

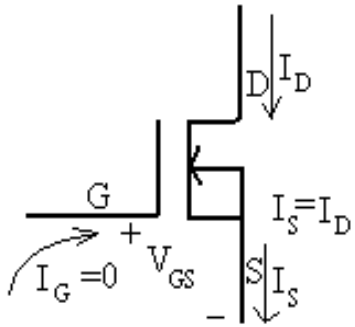
  1. Depletion Type MOSFET (N-channel & P-channel) (In-built channel)
  2. Enhancement Type MOSFET ((N-channel & P-channel) (No channel)

N-Channel Depletion Type MOSFET:





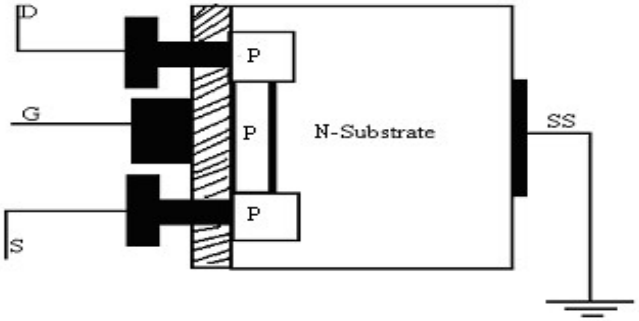
N-Channel Depletion Type MOSFET

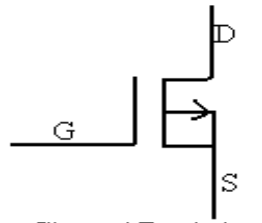


N-Channel Depletion Type MOSFET

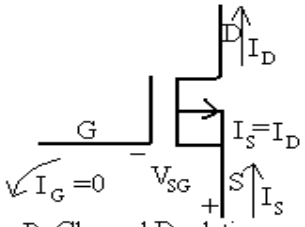
Introduction of MOS devices

P-Channel Depletion Type MOSFET:



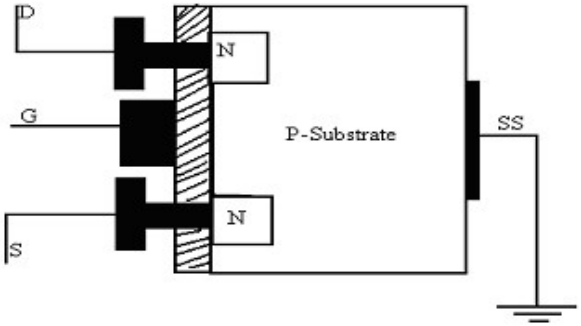


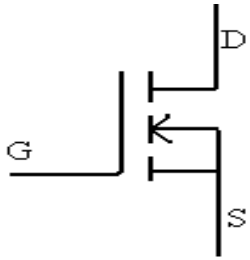
P -Channel Depletion Type MOSFET



P -Channel Depletion Type MOSFET

N-Channel Enhancement Type MOSFET:





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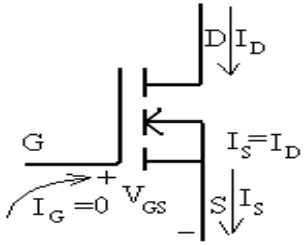

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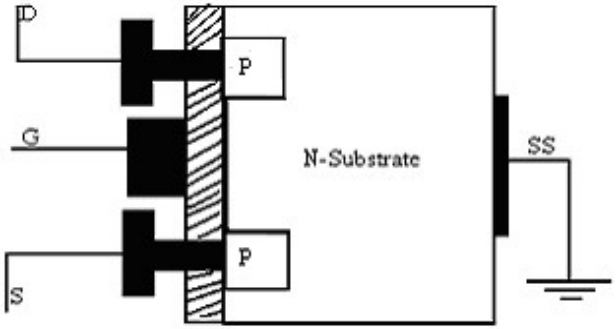
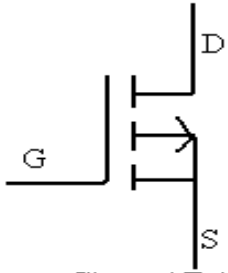
P-Channel Enhancement Type MOSFET:





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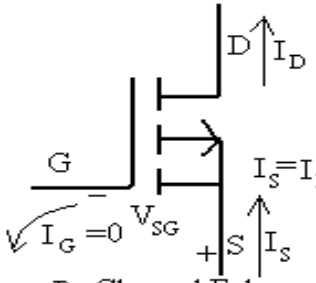


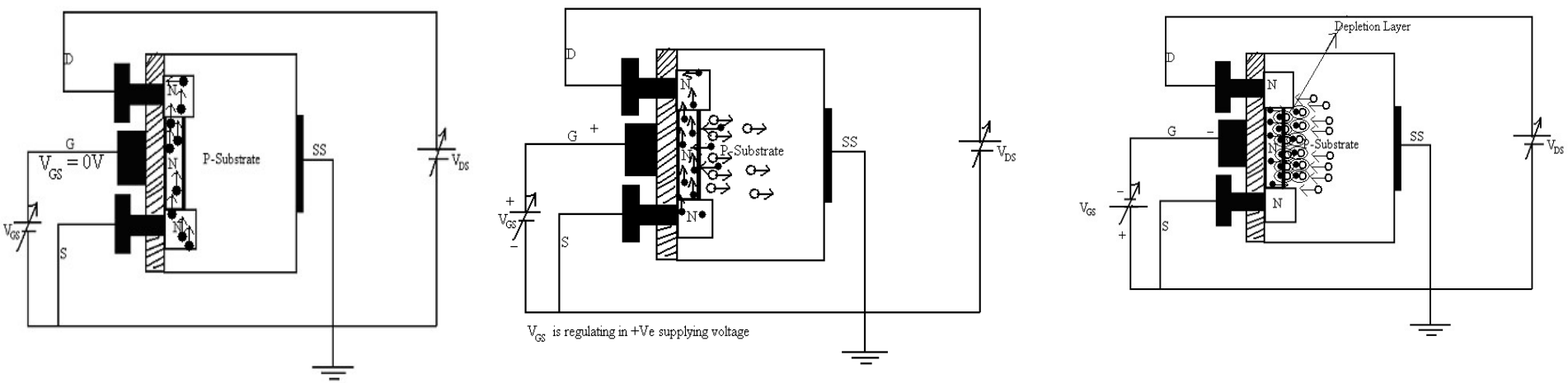
P -Channel Enhancement Type MOSFET

Introduction of MOS devices

N-Channel Depletion Type MOSFET Operation:

- V_{GS} =0V and V_{DS} (+ve) is regulating as the given polarity.
- When V_{GS} = + Ve voltage, the positive polarity at Gate will attract the electrons from the channel towards the insulator and also repel the Holes in P-substrate and attract the minority carriers from P-substrate towards the channel/Insulator. Hence, Carriers density (Electrons) in the N-channel will increase. Therefore, the current will increase.

➢ When V_{GS} = -Ve voltage, The Negative polarity at Gate will Repel the electrons from the N-channel towards the P-Type substrate and also attract the Holes from P-substrate towards the channel and Hence, a depletion layer will be formed at the junction of N-channel and P -substrate. Hence, Carriers density (Electrons) in the N-channel will decrease. Therefore, the current will decrease.



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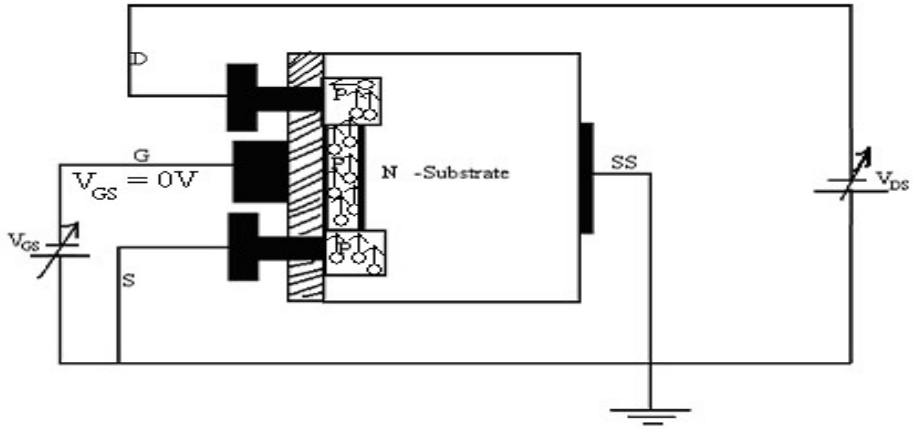

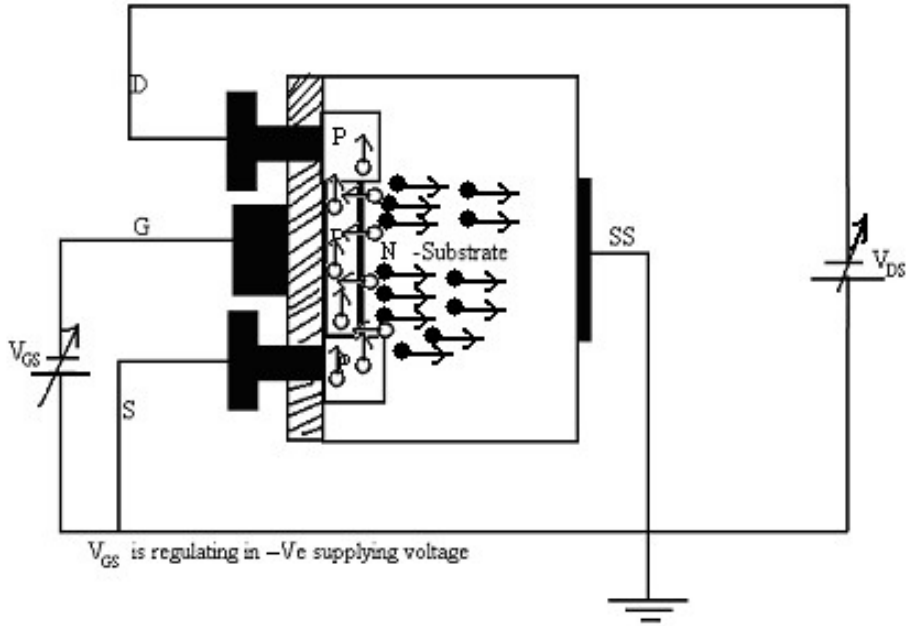

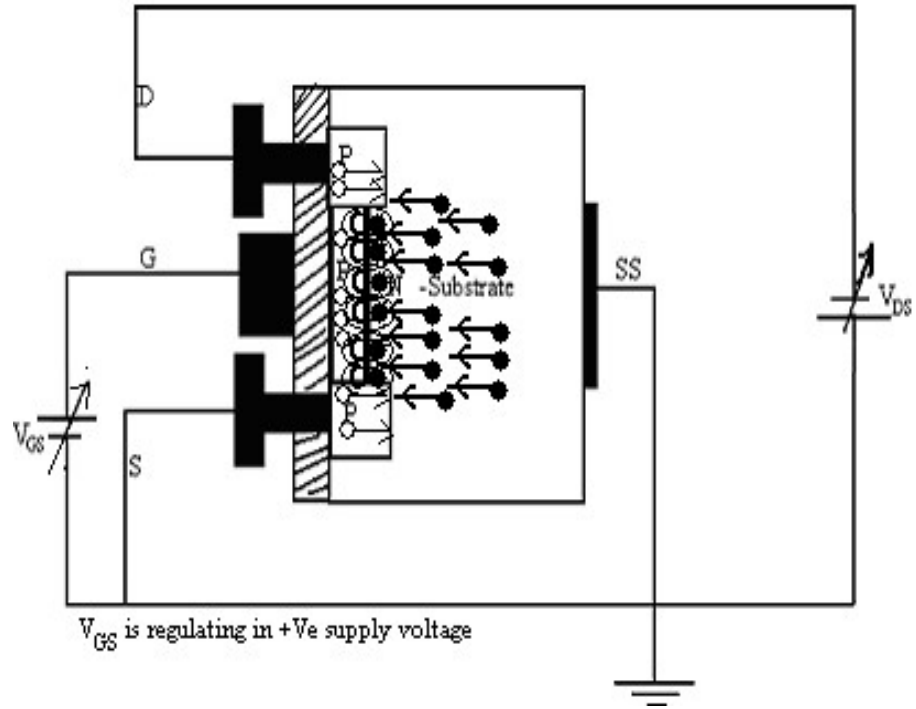

Introduction of MOS devices

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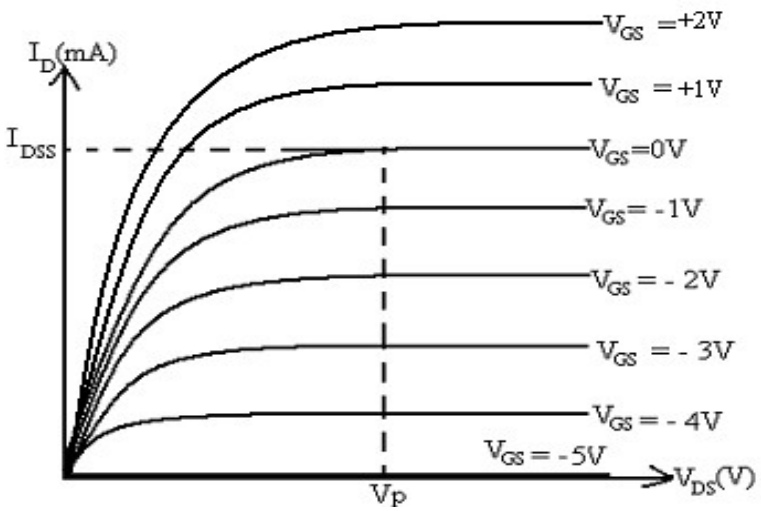

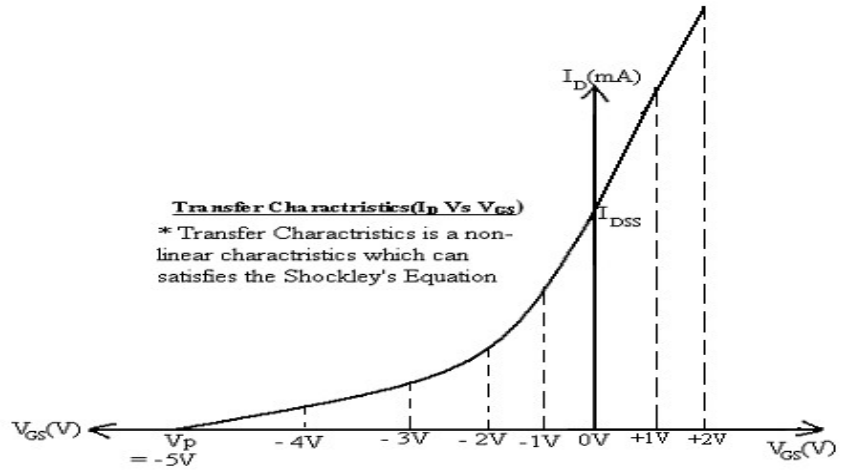

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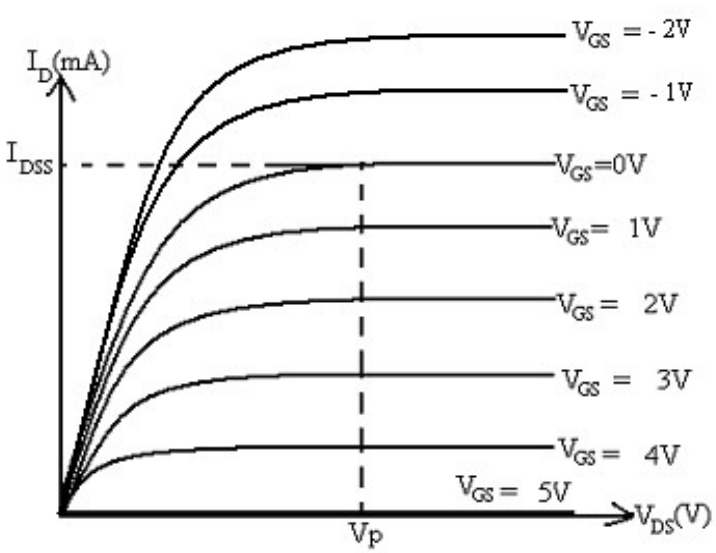

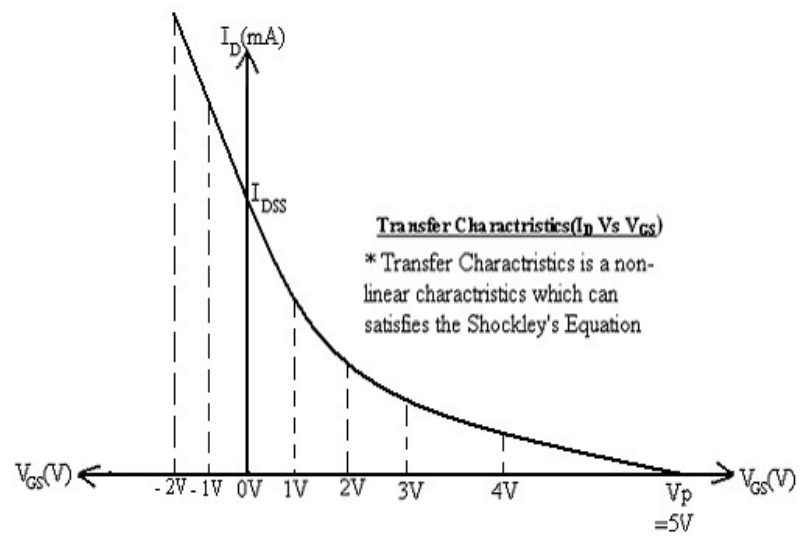

Introduction of MOS devices

N-Channel Enhancement Type MOSFET Operation:

- V_{GS} =0V and V_{DS} (+ve) is regulating as the given polarity. No current flow due to absence of channel.
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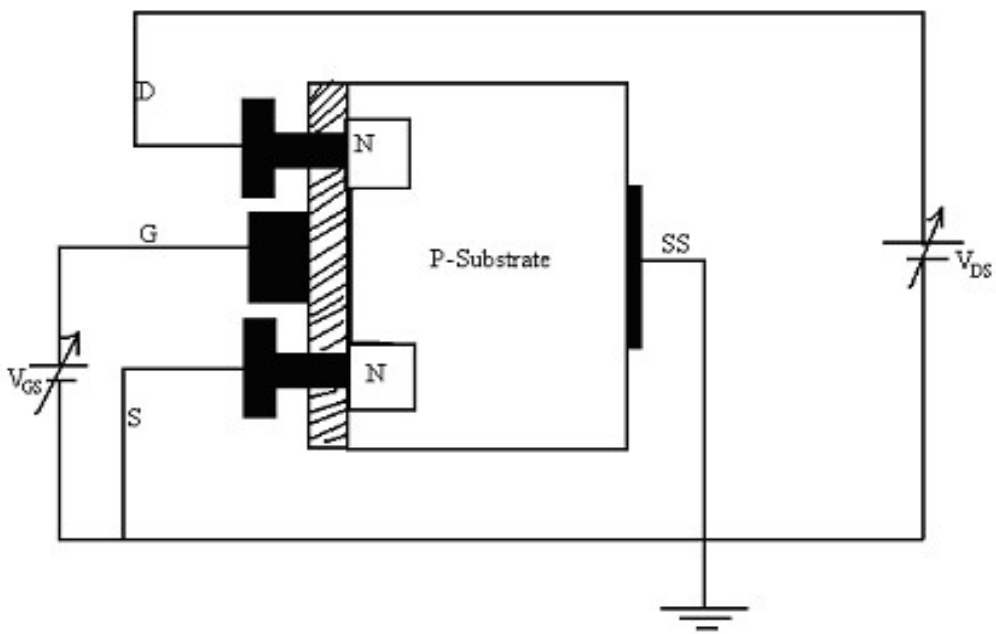

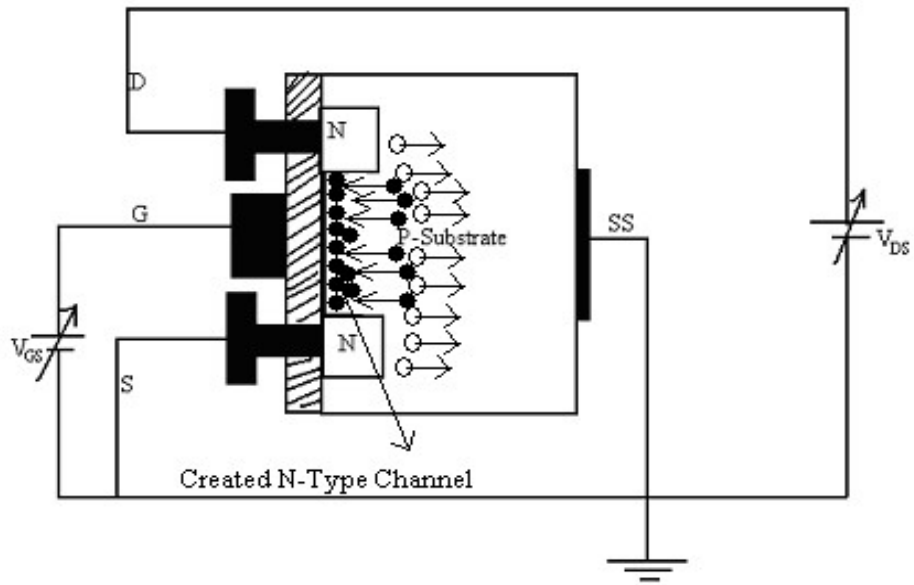

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- V_{GS} =0V and V_{DS} (-ve) is regulating as the given polarity. No current flow due to absence of channel.
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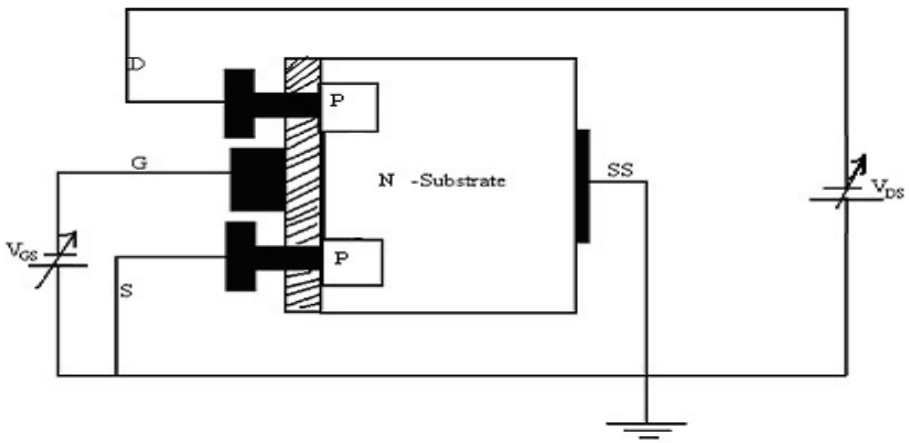
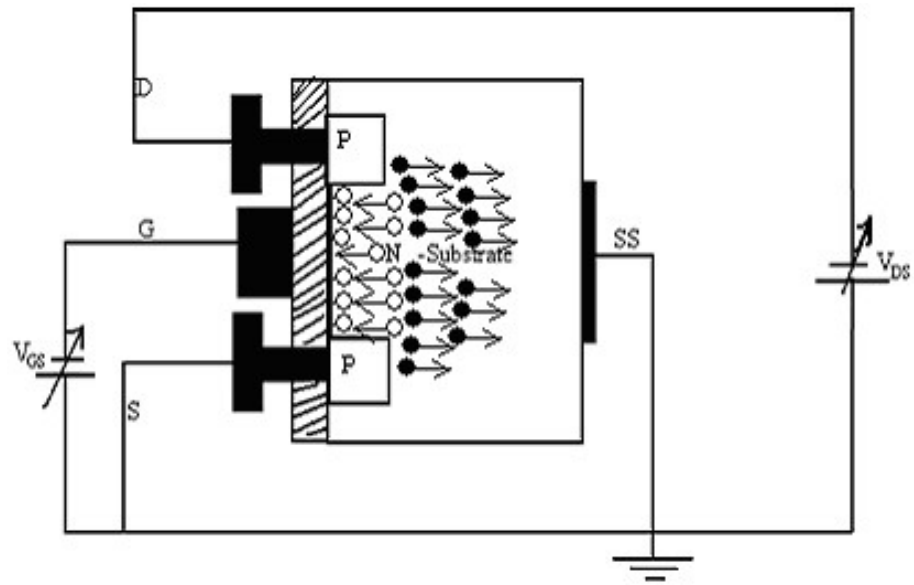
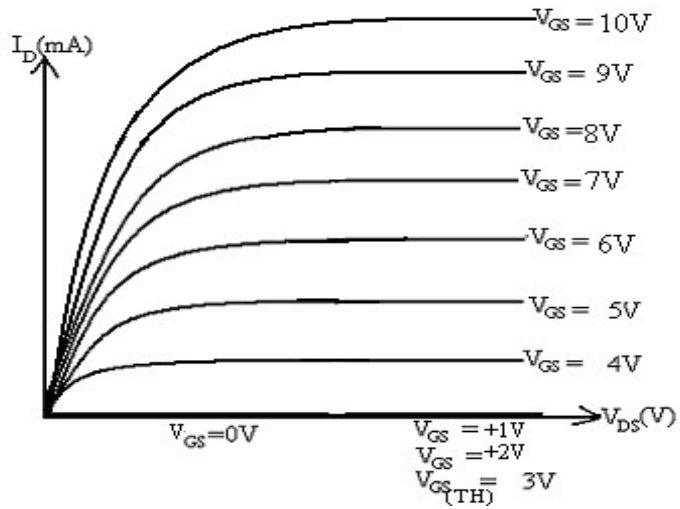
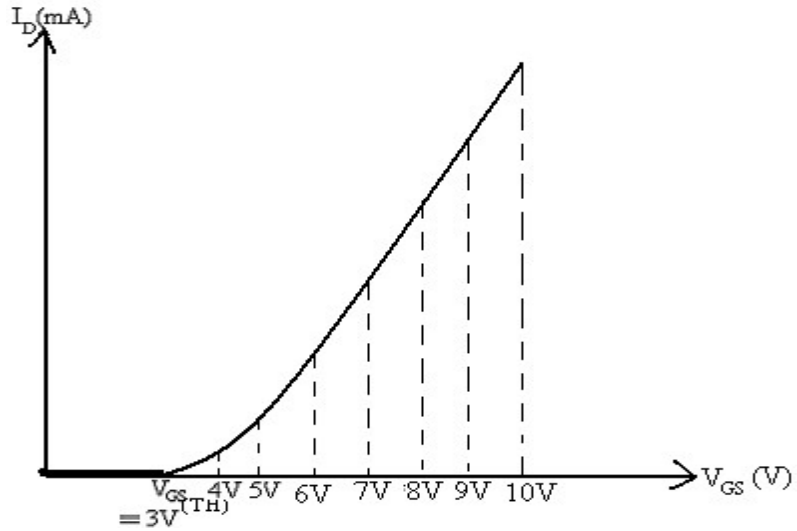




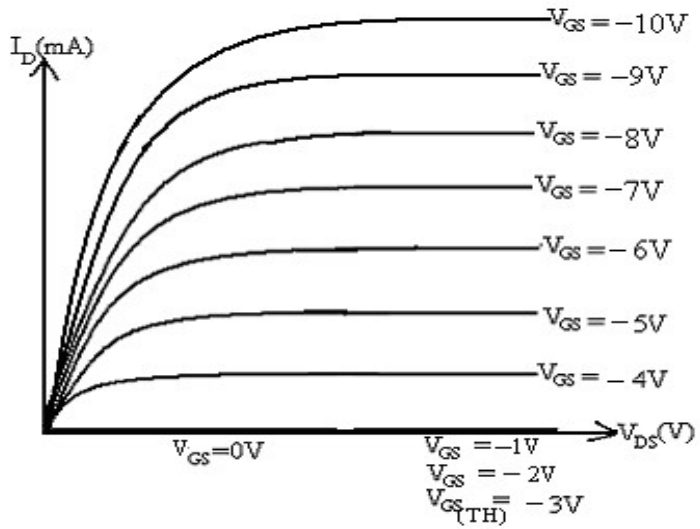
Introduction of MOS devices

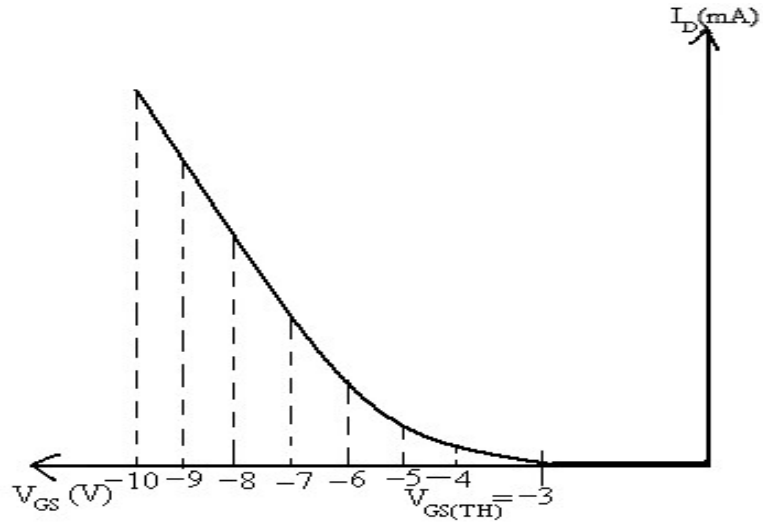
N-Channel Enhancement Type MOSFET:





P-Channel Enhancement Type MOSFET:

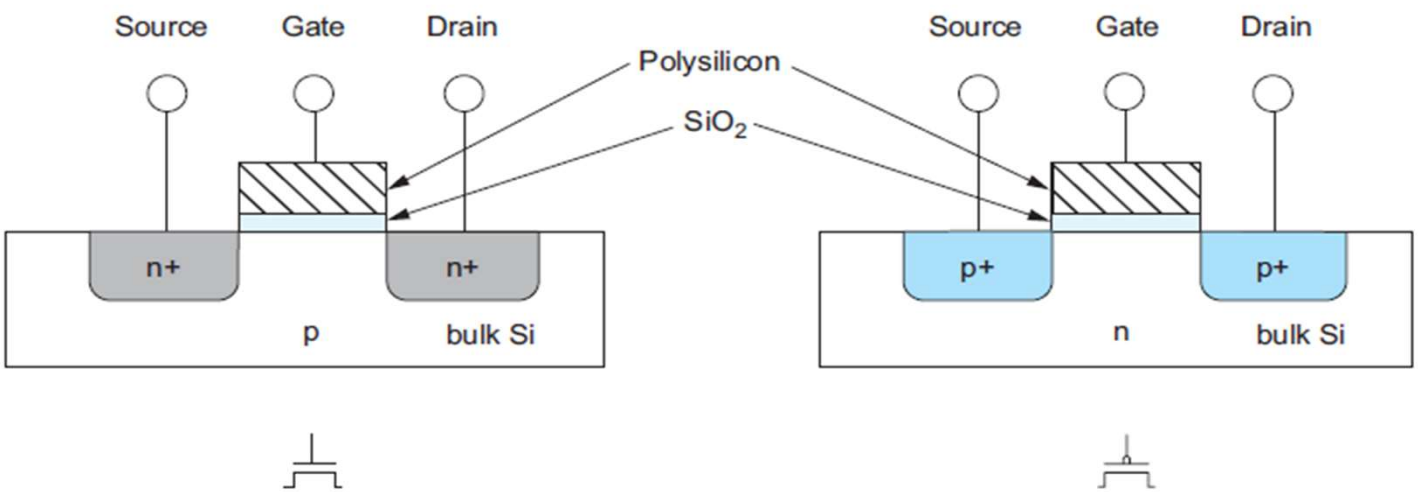




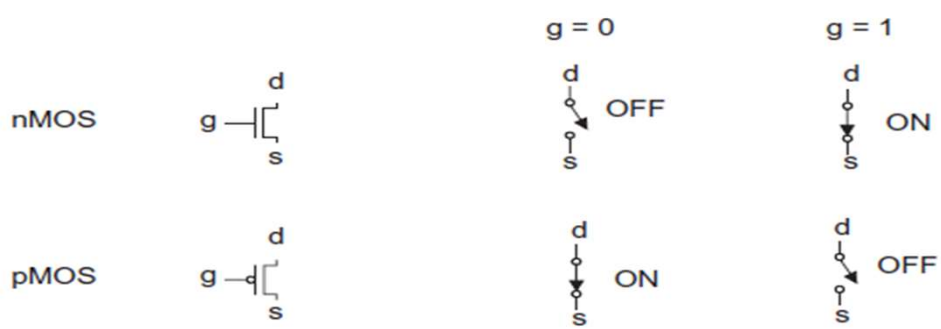
n-MOS, p-MOS and CMOS

- CMOS technology provides two types of transistors (also called devices): an n-type transistor (nMOS) and a p-type transistor (pMOS).
- Transistor operation is controlled by electric fields so the devices are also called Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

n-MOS & p-MOS Transistor:

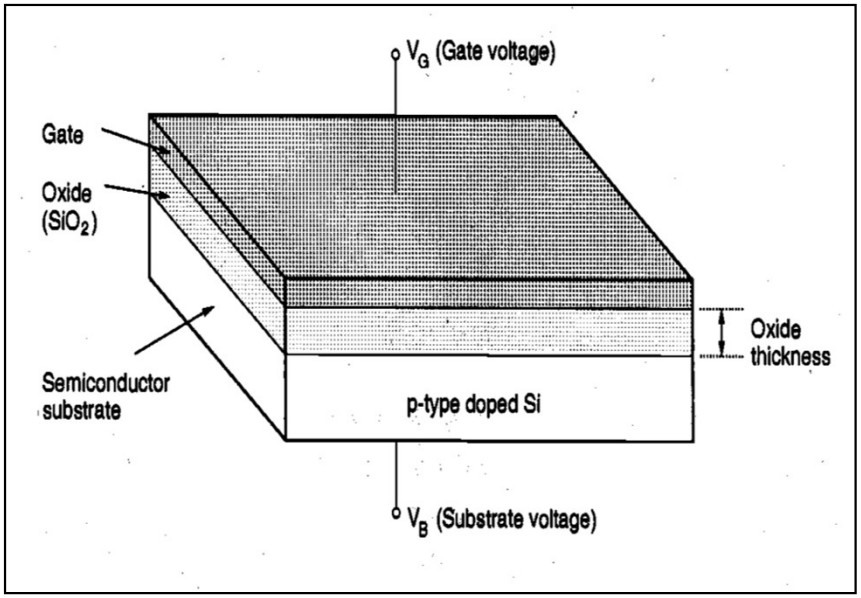


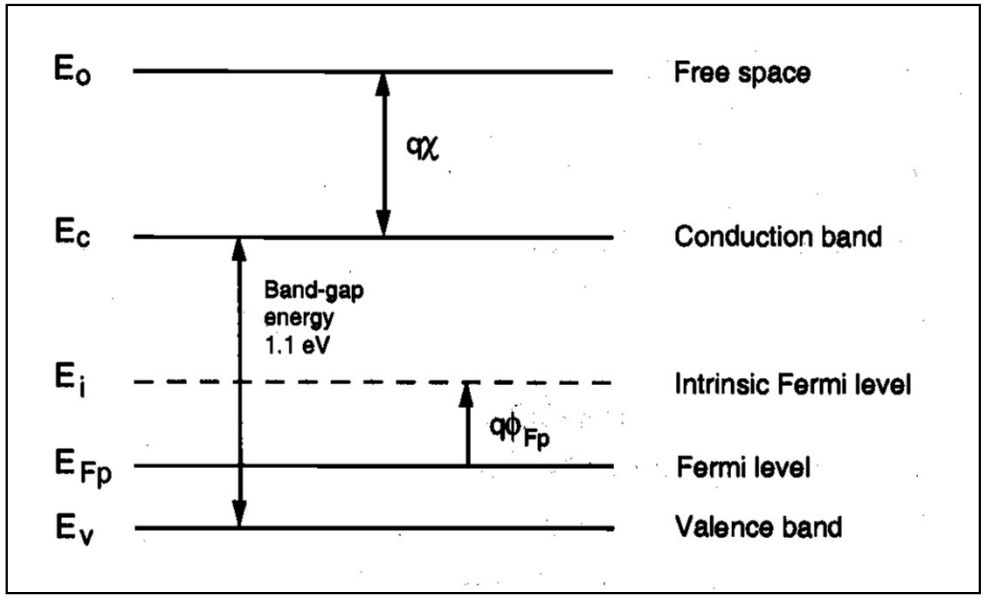
Transistor symbols and switch-level models:



MOS Transistor (Cell)

- MOS structure consists of three layers: **The metal gate electrode, the insulating oxide (SiO_2) layer, and the p-type bulk semiconductor (Si), called the substrate**.
- As such, the MOS structure forms a capacitor, with the gate and the substrate acting as the two terminals (plates) and the oxide layer as the dielectric. The thickness of the silicon dioxide layer is usually between 10 nm and 50 nm.
- The equilibrium concentrations of mobile carriers in a semiconductor always obey the Mass Action Law as $n.p = n_i^2$





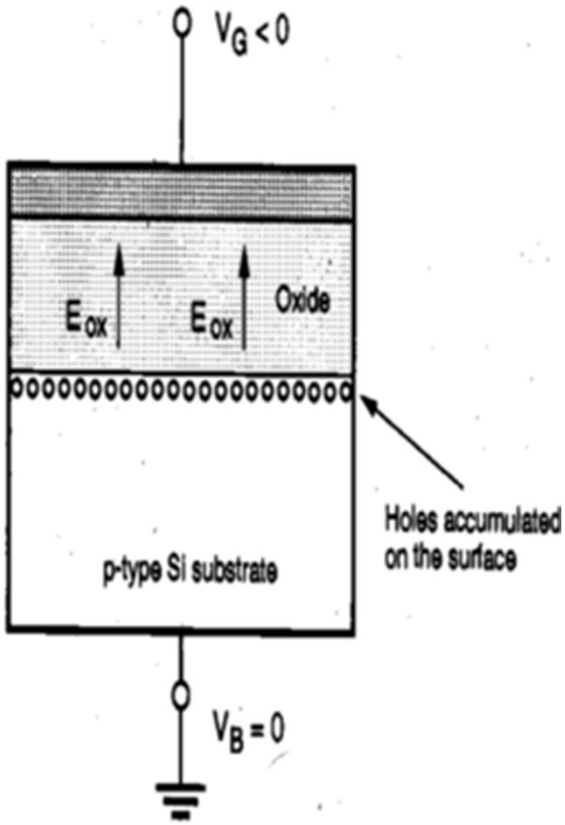
The MOS System under External Bias

- Assume that the substrate voltage is set at $V_B = 0$, and let the gate voltage be the controlling parameter. Depending on the polarity and the magnitude of V_G, three different operating regions can be observed for the MOS system: **accumulation, depletion, and inversion**.

✓ If a **negative voltage V_G** is applied to the gate electrode, the holes in the p-type substrate are attracted to the semiconductor-oxide interface. The majority carrier concentration near the surface becomes larger than the equilibrium hole concentration in the substrate; hence, this condition is called carrier **accumulation** on the surface.

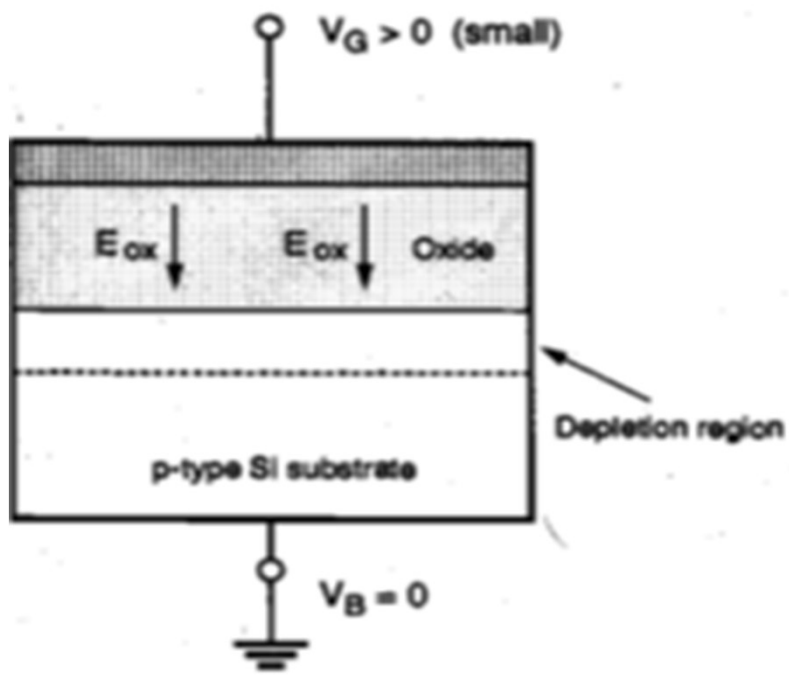
✓ Note that in this case, the oxide electric field is directed towards the gate electrode

✓ While the hole density near the surface increases as a result of the applied negative gate bias, the electron (minority carrier) concentration decreases as the negatively charged electrons are pushed deeper into the substrate.



The MOS System under External Bias

- Now consider a **small positive gate bias V_G** is applied to the gate electrode. Since the substrate bias is zero, the oxide electric field will be directed towards the substrate in this case.
- The majority carriers, i.e., the holes in the substrate, will be repelled back into the substrate as a result of the positive gate bias, and these holes will leave negatively charged fixed acceptor ions behind. Thus, a **depletion region** is created near the surface.

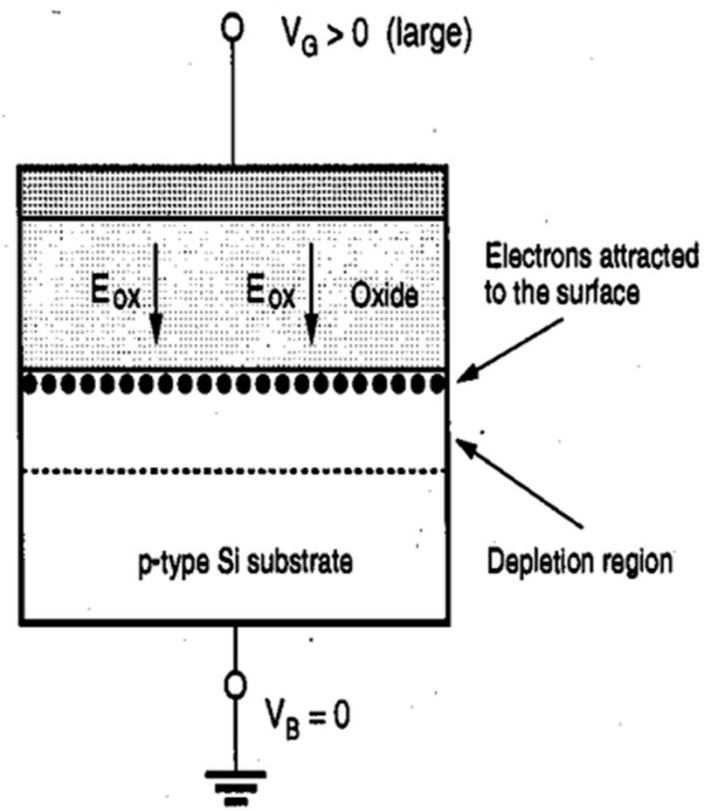


The MOS System under External Bias

- Consider next a **further increase in the positive gate bias**. As a result of the increasing surface potential the substrate semiconductor in this region becomes n-type.
- Within this thin layer, the electron density is larger than the majority hole density, since the positive gate potential attracts additional minority carriers (electrons) from the bulk substrate to the surface.

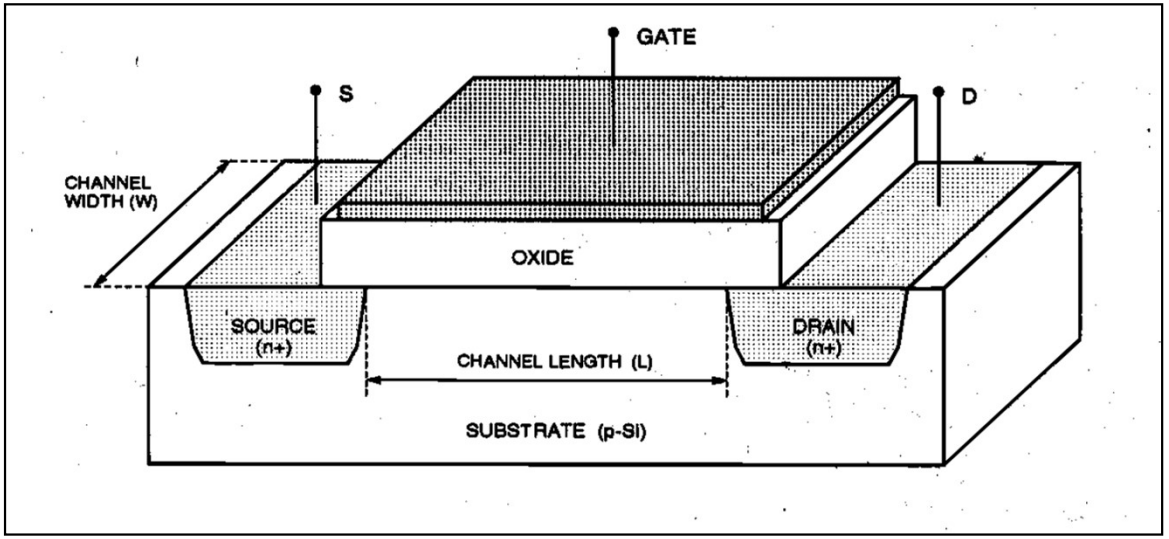
✓ The n-type region created near the surface by the positive gate bias is called the inversion layer, and this condition is called surface **inversion**.

✓ It will be seen that the thin inversion layer on the surface with a large mobile electron concentration can be utilized for conducting current between two terminals of the MOS transistor.



Structure and Operation of MOS Transistor

- This four-terminal device consists of a p-type substrate, in which two n+ diffusion regions, the drain and the source are formed. The surface of the substrate region between the drain and the source is covered with a thin oxide layer, and the metal (or polysilicon) gate is deposited on top of this gate dielectric.
- The two n+ regions will be the current-conducting terminals of this device. Note that the device structure is completely symmetrical with respect to the drain and source regions; the different roles of these two regions will be defined only in conjunction with the applied terminal voltages and the direction of the current flow.



Structure and Operation of MOS Transistor

- A conducting channel will eventually be formed through applied gate voltage in the section of the device between the drain and the source diffusion regions.

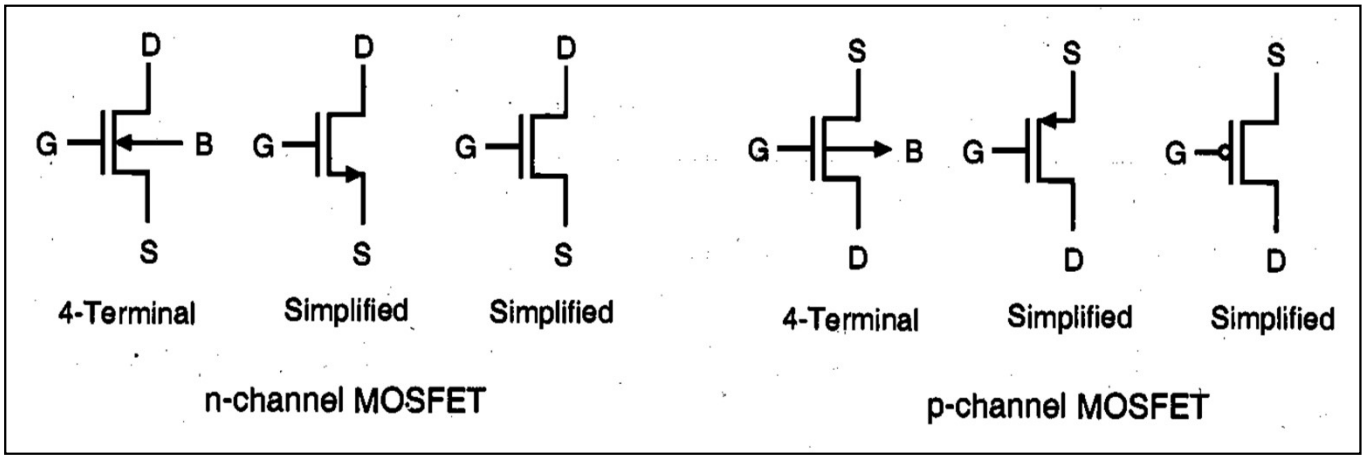
- The distance between the drain and source diffusion regions is the channel length L, and the lateral extent of the channel (perpendicular to the length dimension) is the channel width W.

- Both the channel length and the channel width are important parameters which can be used to control some of the electrical properties of the MOSFET.

- The thickness of the oxide layer covering the channel region, t_{ox} is also an important parameter.

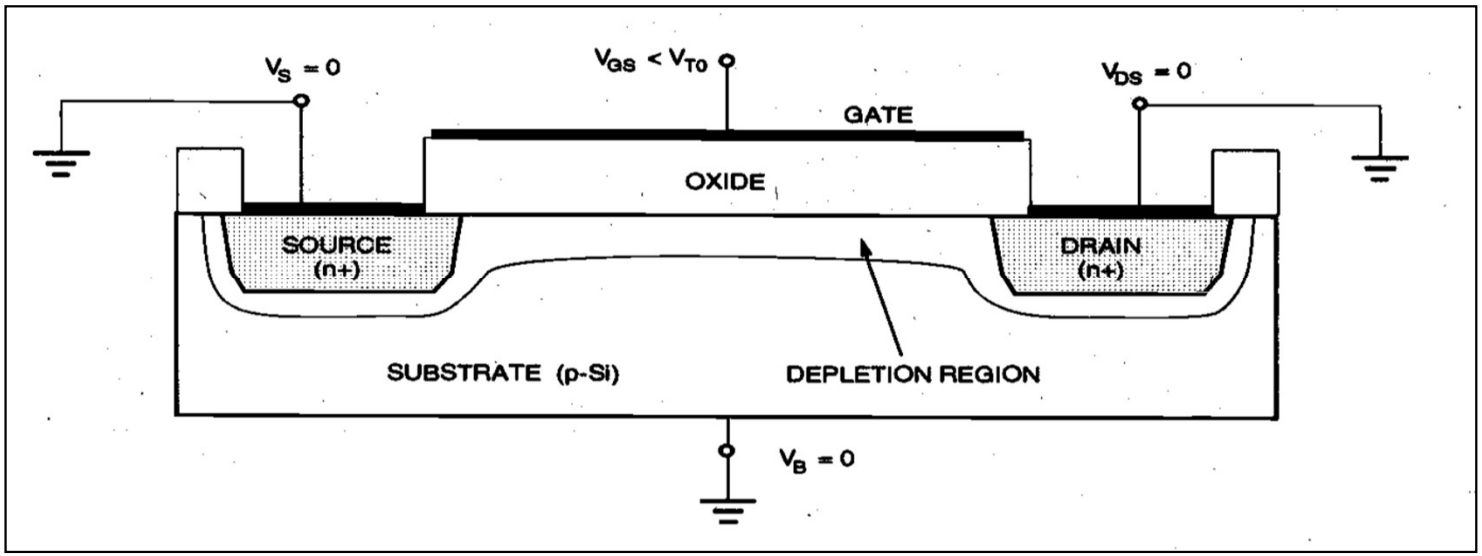
Structure and Operation of MOS Transistor

- A MOS transistor which has no conducting channel region at zero gate bias is called an enhancement-type (or enhancement-mode) MOSFET.
- If a conducting channel already exists at zero gate bias, on the other hand, the device is called a depletion-type (or depletion-mode) MOSFET.
- In a MOSFET with p-type substrate and with n+ source and drain regions, the channel region to be formed on the surface is n-type. Thus, such a device with p-type substrate is called an n-channel MOSFET.
- In a MOSFET with n-type substrate and with p+ source and drain regions, on the other hand, the channel is p-type and the device is called a p-channel MOSFET.



Operation of MOSFET

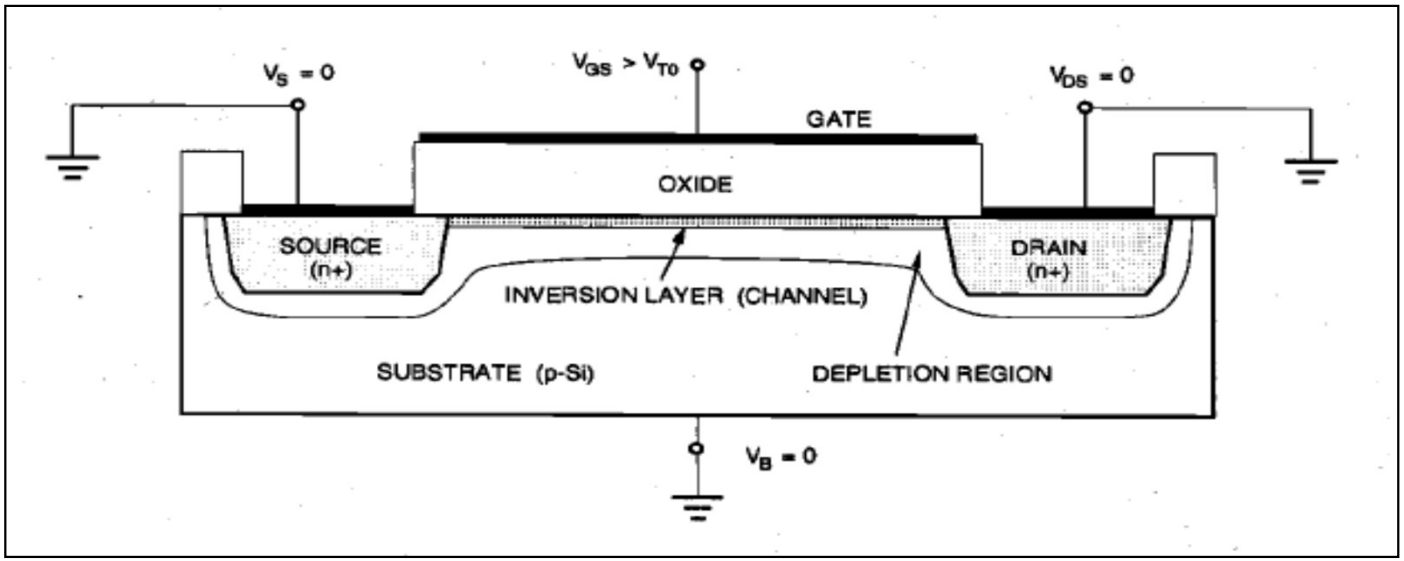
- The source, the drain, and the substrate terminals are all connected to ground. A positive gate-to-source voltage V_{GS} is then applied to the gate in order to create the conducting channel underneath the gate. With this bias arrangement, the channel region between the source and the drain diffusions behaves exactly the same as for the simple MOS structure.
- For small gate voltage levels, the majority carriers (holes) are repelled back into the substrate, and the surface of the p-type substrate is depleted.
- Since the surface is devoid of any mobile carriers, current conduction between the source and the drain is not possible.



Formation of a depletion region in an n-channel enhancement-type MOSFET

Operation of MOSFET

- ✓ Now assume that the gate-to-source voltage is further increased. Here, surface inversion will be established, and a conducting n-type layer will form between the source and the drain diffusion regions as shown in below figure.
- ✓ This channel now provides an electrical connection between the two n+ regions, and it allows current flow, as long as there is a potential difference between the source and the drain terminal voltages. The bias conditions for the onset of surface inversion and for the creation of the conducting channel are therefore very significant for MOSFET operation.



Formation of an inversion layer (channel) in an n-channel E-MOSFET

Operation of MOSFET

- ✓ The value of V_{GS} needed to cause surface inversion (to create the conducting channel) is called the threshold voltage V_{T0}.
- ✓ Any gate-to-source voltage smaller than V_{T0} is not sufficient to establish an inversion layer; thus, the MOSFET can conduct no current between its source and drain terminals unless $V_{GS} > V_{T0}$.
- ✓ For gate-to-source voltages larger than the threshold voltage, on the other hand, a larger number of minority carriers (electrons) are attracted to the surface, which ultimately contributes to channel current conduction.
- ✓ Also note that increasing the gate-to- source voltage above and beyond the threshold voltage will not affect the surface potential and the depletion region depth.
- ✓ Both quantities will remain approximately constant and equal to their values attained at the onset of surface inversion.

The Threshold Voltage

- ✓ For all practical purposes, we can identify four physical components of the threshold voltage:

  (i) The work function difference between the gate and the channel (Φ_{GC})

  (ii) The gate voltage component to change the surface potential

  (iii) The gate voltage component to offset the depletion region charge

  (iv) The voltage component to offset the fixed charges in the gate oxide and in the silicon oxide interface.

$$\Phi_{GC} = \phi_F(substrate) - \phi_M \qquad \text{for metal gate}$$

$$\Phi_{GC} = \phi_F(substrate) - \phi_F(gate) \qquad \text{for polysilicon gate}$$

- The depletion region charge density at surface inversion:

$$Q_{B0} = -\sqrt{2q \cdot N_A \cdot \varepsilon_{Si} \cdot |-2\phi_F|}$$

The Threshold Voltage

- The depletion region charge density can be expressed as a function of the source-to-substrate voltage V_{SB}.

$$Q_B = -\sqrt{2q \cdot N_A \cdot \varepsilon_{Si} \cdot \left|-2\phi_F + V_{SB}\right|}$$

- The component that offsets the depletion region charge is then equal to $-Q_B/C_{ox}$, where C_{ox} is the gate oxide capacitance per unit area.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

- For zero substrate bias, the threshold voltage V_{T0} is expressed as follows:

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

- For nonzero substrate bias, on the other hand, the depletion charge density term must be modified to reflect the influence of V_{SB} upon that charge, resulting in the following generalized threshold voltage expression.

$$V_T = \Phi_{GC} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

The Threshold Voltage

- The generalized form of the threshold voltage can also be written as:

$$V_T = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_B - Q_{B0}}{C_{ox}} = V_{T0} - \frac{Q_B - Q_{B0}}{C_{ox}}$$

$$\frac{Q_B - Q_{B0}}{C_{ox}} = -\frac{\sqrt{2q \cdot N_A \cdot \varepsilon_{Si}}}{C_{ox}} \cdot \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

- Thus, the most general expression of the threshold voltage V_T can be found as follows:

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

- Where, the parameter γ is the substrate-bias (or body-effect) coefficient.

$$\gamma = \frac{\sqrt{2q \cdot N_A \cdot \varepsilon_{Si}}}{C_{ox}}$$

The Threshold Voltage

❖ The threshold voltage expression given above can be used both for n-channel and p-channel MOS transistors with some polarity change in coefficient.

- The substrate Fermi potential ϕ_F is negative in nMOS, positive in pMOS.
- The depletion region charge densities Q_{BO} and Q_B are negative in nMOS, positive in pMOS.
- The substrate bias coefficient γ is positive in nMOS, negative in pMOS.
- The substrate bias voltage V_{SB} is positive in nMOS, negative in pMOS.

❖ Typically, the threshold voltage of an enhancement-type n-channel MOSFET is a positive quantity, whereas the threshold voltage of a p-channel MOSFET is negative.

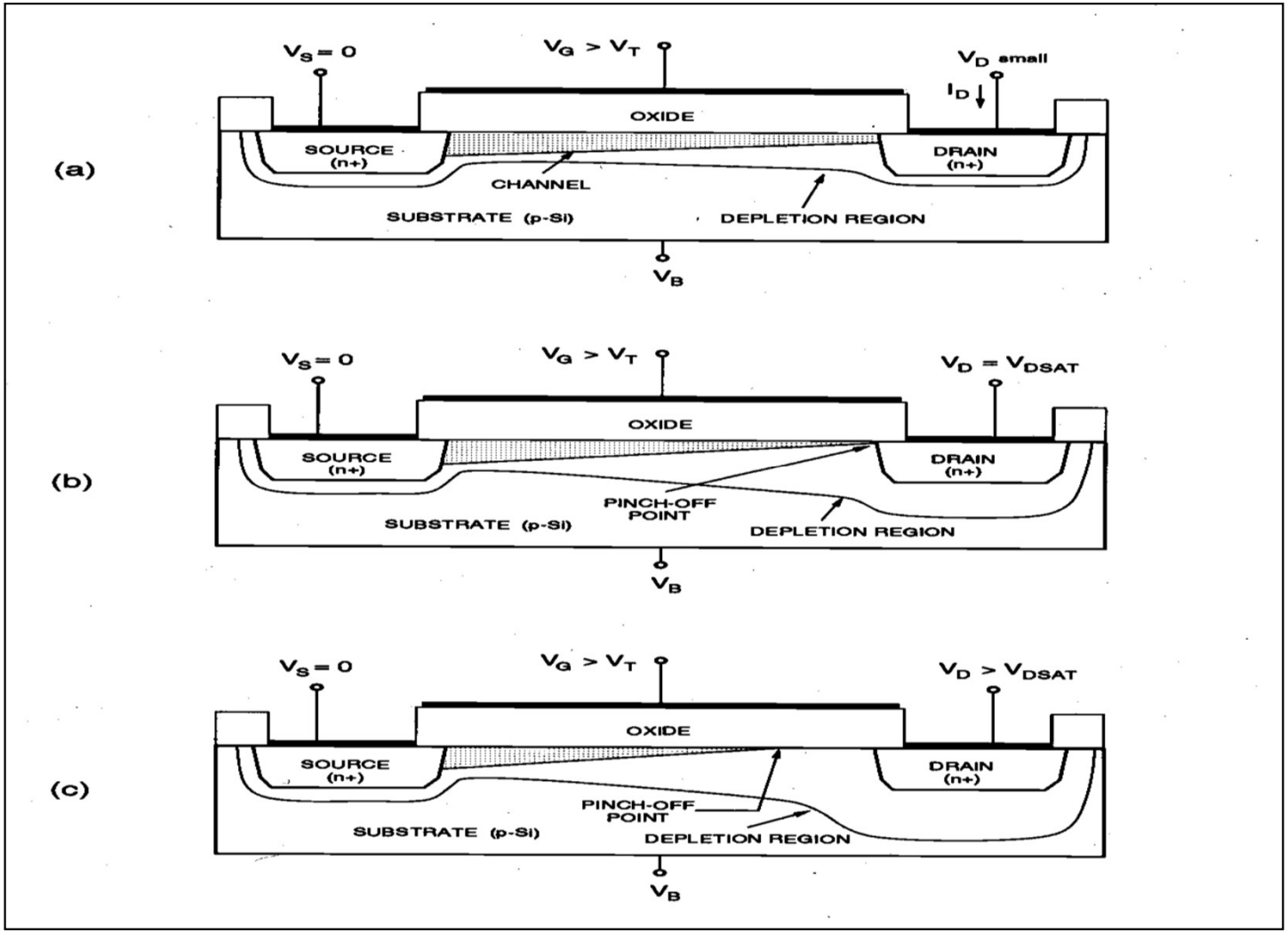
MOSFET Operation: A Qualitative View

- Once the inversion layer is established on the surface, an n-type conducting channel forms between the source and the drain, which is capable of carrying the drain current. Next, the influence of drain-to-source bias V_{DS} and different modes of drain current flow will be examined for an nMOS transistor with $V_{GS} > V_{T0}$.
- At $V_{DS} = 0$, thermal equilibrium exists in the inverted channel region, and the drain current I_D is equal to zero (Fig (a)). If a small drain voltage $V_{DS} > 0$ is applied, a drain current proportional to V_{DS} will flow from the drain to the source through the conducting channel. The inversion layer, i.e., the channel, forms a continuous current path from the drain to the source. This operation mode is called the ***linear mode,*** **or the** ***linear region***.
- Thus, in linear region operation, the channel region acts as a voltage-controlled resistor. The electron velocity, in the channel for this case is usually much lower than the drift velocity limit. Note that as the drain voltage is increased, the inversion layer charge and the channel depth at the drain end start to decrease.

MOSFET Operation: A Qualitative View

- Eventually, for $V_{DS} = V_{DSAT}$, the inversion charge at the drain is reduced to zero, which is called the pinch-off point (Fig. (b)).
- Beyond the pinch-off point, i.e., for $V_{DS} > V_{DSAT}$, a depleted surface region forms adjacent to the drain, and this depletion region grows toward the source with increasing drain voltages. This operation mode of the MOSFET is called the ***saturation mode*** **or the** ***saturation region****;* For a MOSFET operating in the saturation region, the effective channel length is reduced as the inversion layer near the drain vanishes, while the channel-end voltage remains essentially constant and equal to V_{DSAT} (Fig (c)).
- Note that the pinched-off (depleted) section of the channel absorbs most of the excess voltage drop $(V_{DS} - V_{DSAT})$ and a high-field region forms between the channel-end and the drain boundary. Electrons arriving from the source to the channel-end are injected into the drain-depletion region and are accelerated toward the drain in this high electric field, usually reaching the drift velocity limit. The pinch-off event, or the disruption of the continuous channel under high drain bias, characterizes the saturation mode operation of the MOSFET.

MOSFET Operation: A Qualitative View



Cross-sectional view of an n-channel (nMOS) transistor, (a) operating in the linear region, (b) operating at the edge of saturation, and (c) operating beyond saturation

MOSFET Current-Voltage Characteristics

Gradual Channel Approximation

- ✓ To begin with the current-flow analysis, consider the cross-sectional view of the n channel MOSFET operating in the linear mode, as shown in next figure. Here, $Vs = V_B = 0$. The V_{GS} and V_{DS} voltage are the external parameters controlling the drain (channel) current I_D. The gate-to-source voltage is set to be larger than the threshold voltage V_{T0} to create a conducting inversion layer between the source and the drain. We define the coordinate system for this structure such that the x-direction is perpendicular to the surface, pointing down into the substrate, and the *y*-direction is parallel to the surface. The y-coordinate origin (y = 0) is at the source end of the channel. The channel voltage with respect to the source will be denoted by $V_c(y)$. Now assume that the threshold voltage V_{T0} is constant along the entire channel region, between $y = 0$ and $y = L$. Next, assume that the electric field component E_y along the *y*-coordinate is dominant compared to the electric field component E_x along the *x*-coordinate. This assumption will allow us to reduce the current-flow problem in the channel to the *y* dimension only. Note that the boundary conditions for the channel voltage V_C are:

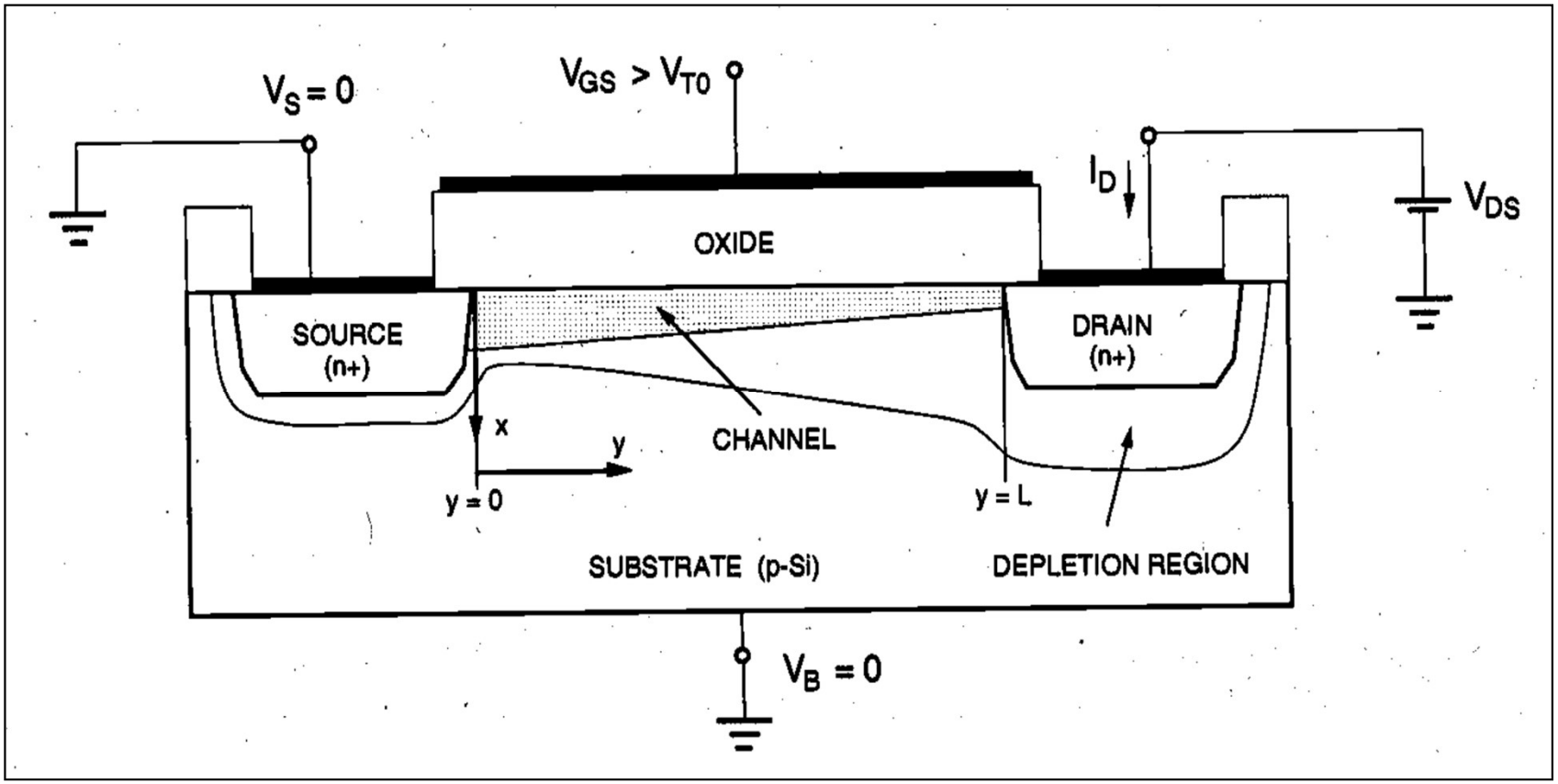
$$V_c(y=0) = V_S = 0$$
$$V_c(y=L) = V_{DS}$$

- ✓ Also, it is assumed that the entire channel region between the source and the drain is inverted:

$$V_{GS} \geq V_{T0}$$
$$V_{GD} = V_{GS} - V_{DS} \geq V_{T0}$$

Gradual Channel Approximation

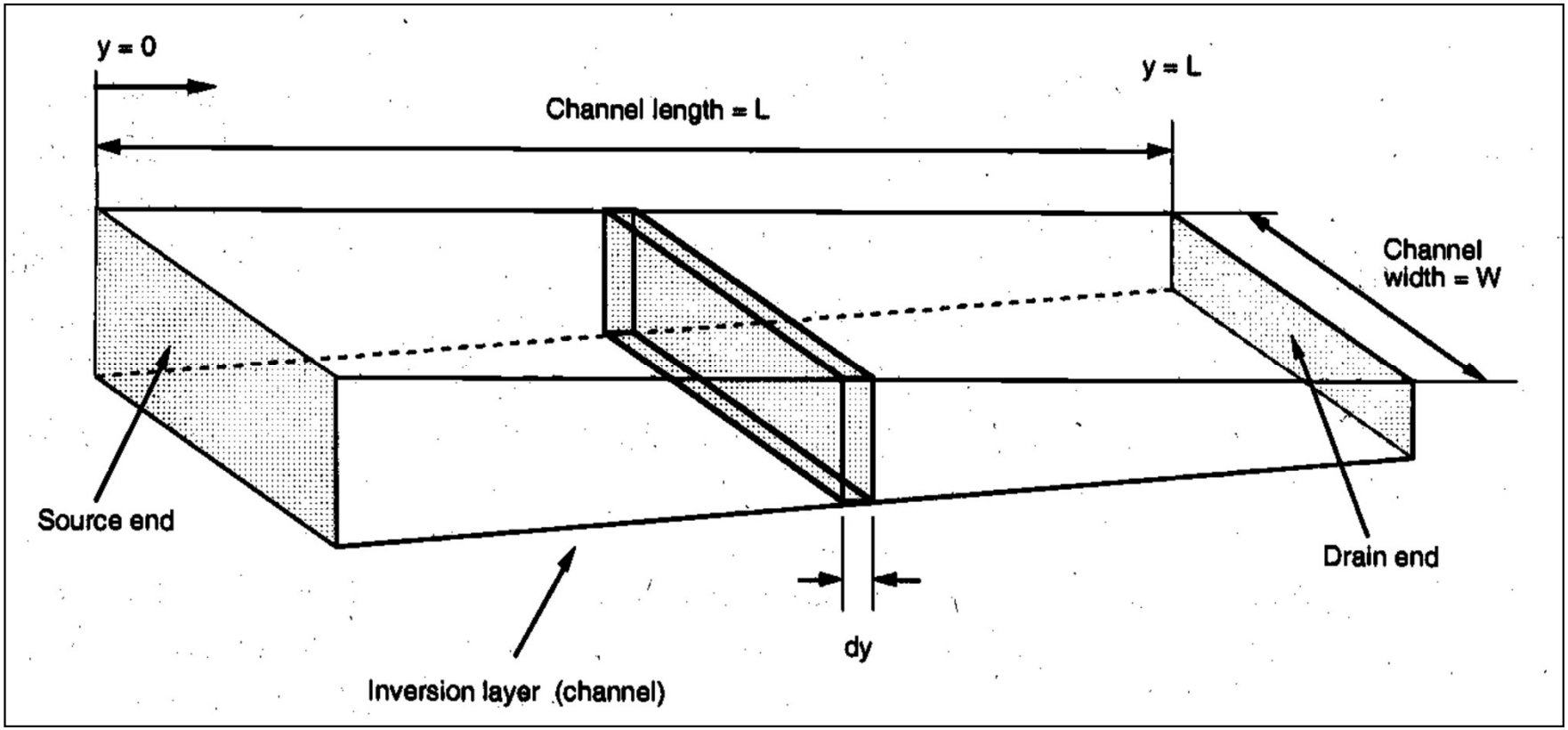
- ✓ The channel current (drain current) I_D is due to the electrons in the channel region travelling from the source to the drain under the influence of the lateral electric field component E_y. Since the current flow in the channel is primarily governed by the lateral drift of the mobile electron charge in the surface inversion layer, we will consider the amount and the bias-voltage dependence of this inversion layer in more detail.



Gradual Channel Approximation

- Let $Q_I(y)$ be the total mobile electron charge in the surface inversion layer. This charge can be expressed as a function of the gate-to-source voltage V_{GS} and of the channel voltage $V_c(y)$ as follows:

$$Q_I(y) = -C_{ox} \cdot \left[V_{GS} - V_c(y) - V_{T0} \right]$$



Simplified geometry of the surface inversion layer (channel region)

Gradual Channel Approximation

- Now consider the incremental resistance *dR* of the differential channel segment as shown in previous figure. Assuming that all mobile electrons in the inversion layer have a constant surface mobility μ_n, the incremental resistance can be expressed as follows. Note that the minus sign is due to the negative polarity of the inversion layer charge Q_I.

$$dR = -\frac{dy}{W \cdot \mu_n \cdot Q_I(y)}$$

- Applying Ohm's law for this segment yields the voltage drop along the incremental segment *dy,* in the *y*-direction.

$$dV_c = I_D \cdot dR = -\frac{I_D}{W \cdot \mu_n \cdot Q_I(y)} \cdot dy$$

- This equation can now be integrated along the channel, i.e., from $y = 0$ to $y = L$, using the boundary conditions.

$$\int_0^L I_D \cdot dy = -W \cdot \mu_n \int_0^{V_{DS}} Q_I(y) \cdot dV_c$$

$$I_D \cdot L = W \cdot \mu_n \cdot C_{ox} \int_0^{V_{DS}} \left(V_{GS} - V_c - V_{T0}\right) \cdot dV_c$$

Gradual Channel Approximation

- Assuming that the channel voltage V_c, is the only variable in above equation that depends on the position y, the drain current is found as follows.

$$I_D = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_{T0}) V_{DS} - V_{DS}^2\right]$$

$$I_D = \frac{k'}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_{T0}) V_{DS} - V_{DS}^2\right] \qquad I_D = \frac{k}{2} \cdot \left[2 \cdot (V_{GS} - V_{T0}) V_{DS} - V_{DS}^2\right]$$

- where the parameters k and k' are defined as:

$$k' = \mu_n \cdot C_{ox} \qquad k = k' \cdot \frac{W}{L}$$

- For saturation condition:

$$V_{DS} \geq V_{DSAT} = V_{GS} - V_{T0}$$

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_{T0}) \cdot (V_{GS} - V_{T0}) - (V_{GS} - V_{T0})^2\right]$$
$$= \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{T0})^2$$

Problem

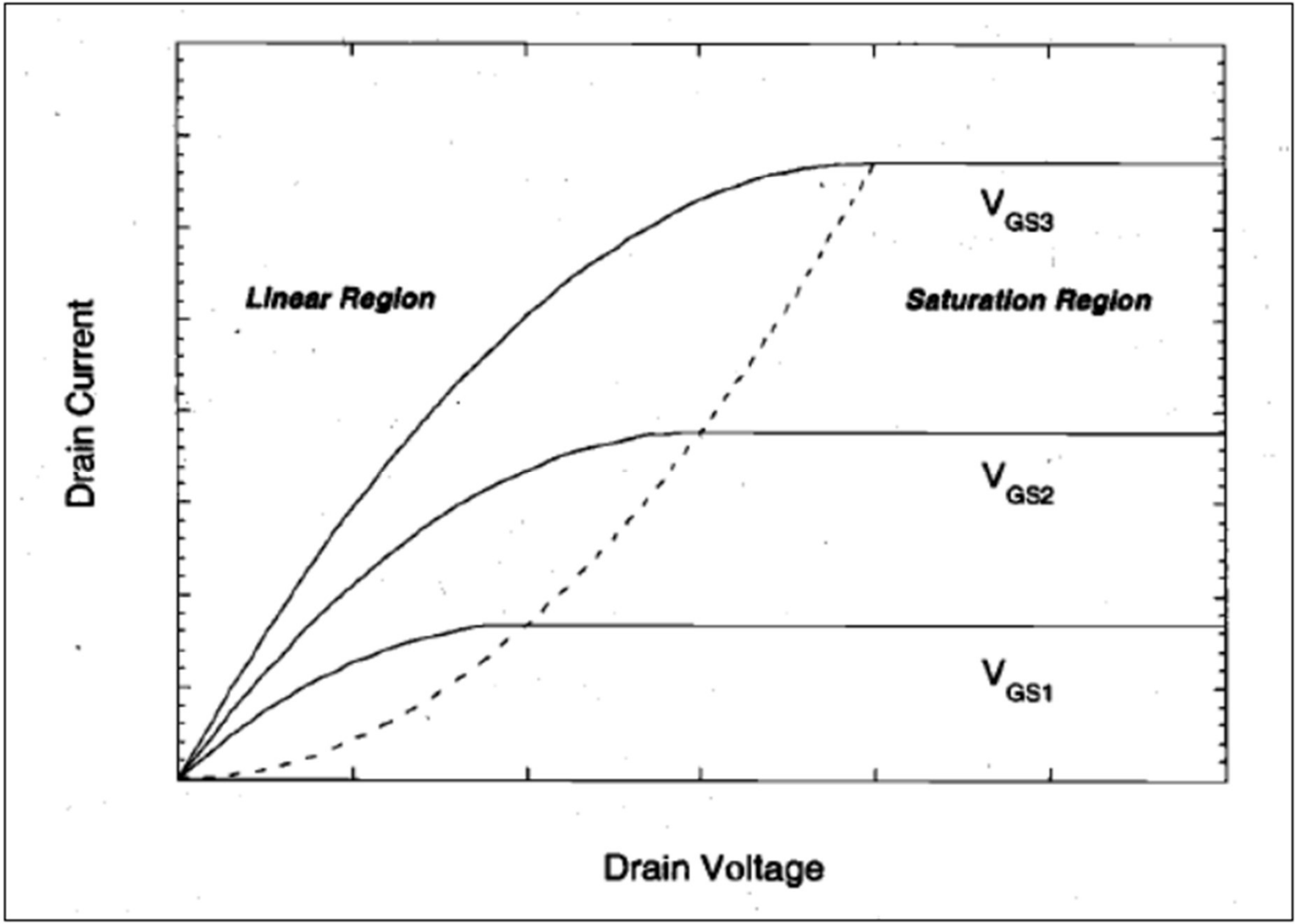
For an n-channel MOS transistor with $\mu_n = 600\ \text{cm}^2/\text{V}\cdot\text{s}$, $C_{ox} = 7\cdot 10^{-8}\ \text{F/cm}^2$, $W = 20\ \mu\text{m}$, $L = 2\ \mu\text{m}$ and $V_{T0} = 1.0$ V, examine the relationship between the drain current and the terminal voltages.

Solution:

$$k = \mu_n \cdot C_{ox} \cdot \frac{W}{L} = 600\ \text{cm}^2/\text{V}\cdot\text{s} \times 7\cdot 10^{-8}\ \text{F/cm}^2 \times \frac{20\ \mu\text{m}}{20\ \mu\text{m}} = 0.42\ \text{mA/V}^2$$

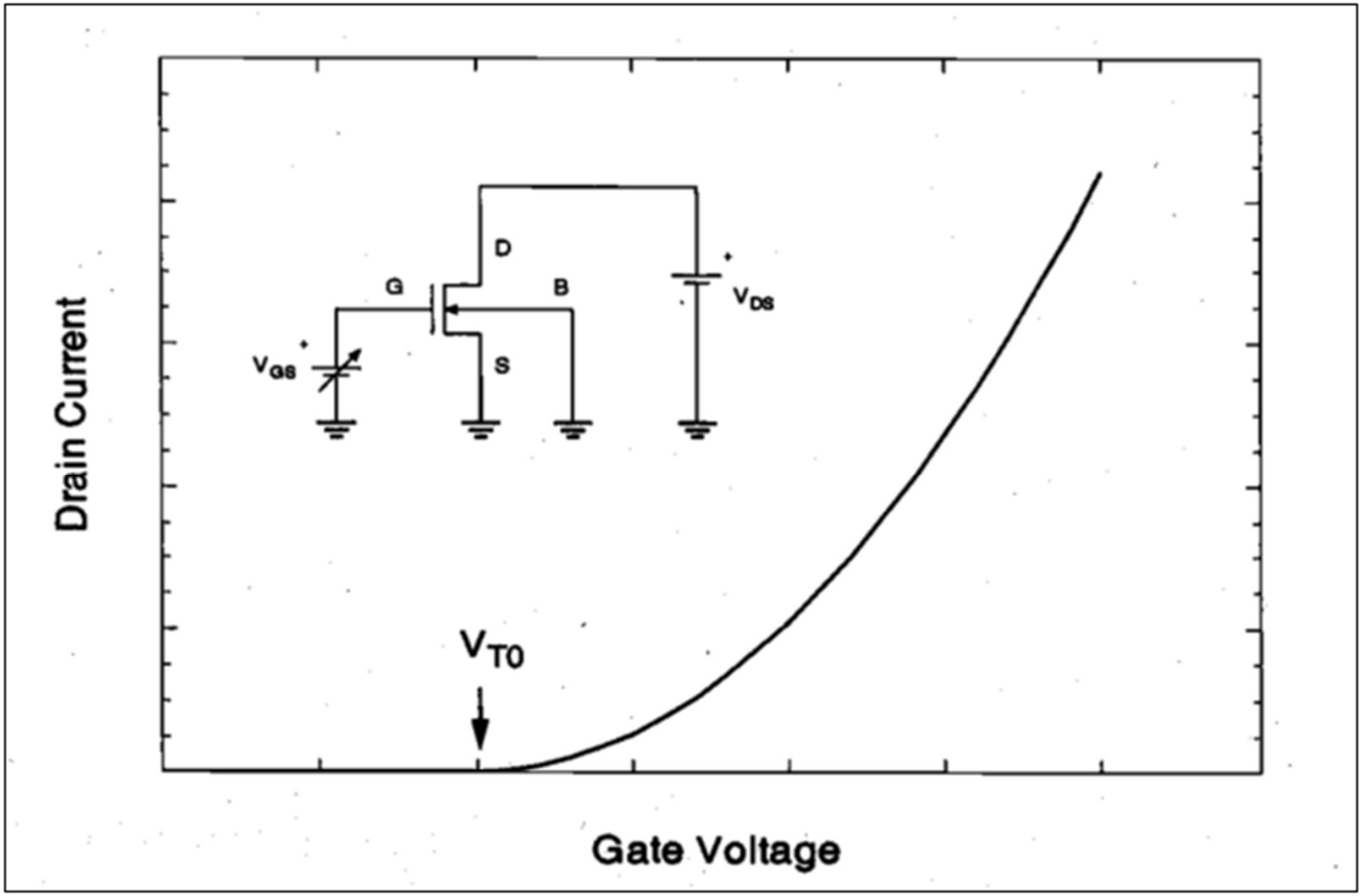
$$I_D = 0.21\ \text{mA/V}^2\left[2\cdot\left(V_{GS} - 1.0\right)\cdot V_{DS} - V_{DS}^2\right]$$

Gradual Channel Approximation



Basic current-voltage characteristics of an n-channel MOS transistor

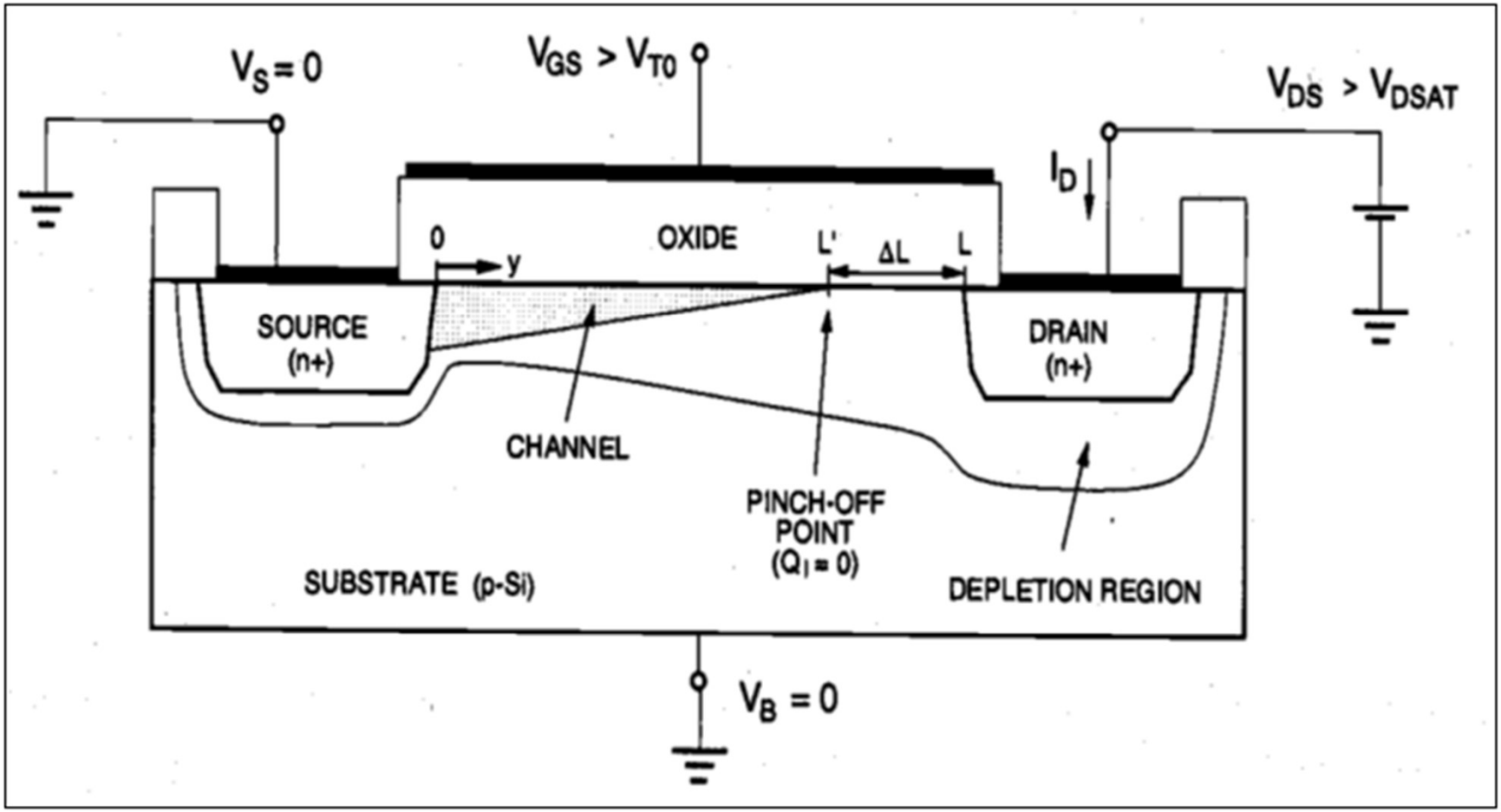
Gradual Channel Approximation



Drain current of the n-channel MOS transistor as a function of the gate to-source voltage V_{GS}, with $V_{DS} > V_{DSAT}$ (transistor in saturation)

Channel Length Modulation

- ✓ If the drain-to-source voltage V_{DS} is increased even further beyond the saturation edge so that $V_{DS} > V_{DSAT}$, an even larger portion of the channel becomes pinched-off.



Channel length modulation in an n-channel MOSFET operation in saturation mode

Channel Length Modulation

- Consequently, the *effective channel length* (the length of the inversion layer where GCA is still valid) is reduced to:

$$L' = L - \Delta L,$$

- where ΔL is the length of the channel segment with $Q_I = 0$. Hence, the pinch-off point moves from the drain end of the channel toward the source with increasing drain-to-source voltages. The remaining portion of the channel between the pinch-off point and the drain will be in depletion mode. Since $Q_I(y) = 0$ for $L' < y < L$, the channel voltage at the pinch-off point remains equal to V_{DSAT}, i.e.,

$$V_c(y = L') = V_{DSAT}$$

- We can represent the inverted portion of the surface by a shortened channel, with a channel-end voltage of V_{DSAT}. The gradual channel approximation is valid in this region; thus, the channel current can be found:

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L'} \cdot \left(V_{GS} - V_{T0}\right)^2$$

Channel Length Modulation

- ✓ This accounts for the actual shortening of the channel, also called *channel length modulation.* Rewriting the saturation current as follows:

$$I_D(sat) = \left(\frac{1}{1 - \frac{\Delta L}{L}} \right) \cdot \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{T0})^2$$

- ✓ The channel length shortening ΔL is actually proportional to the square root of $(V_{DS} - V_{DSAT})$.

$$\Delta L \propto \sqrt{V_{DS} - V_{DSAT}}$$

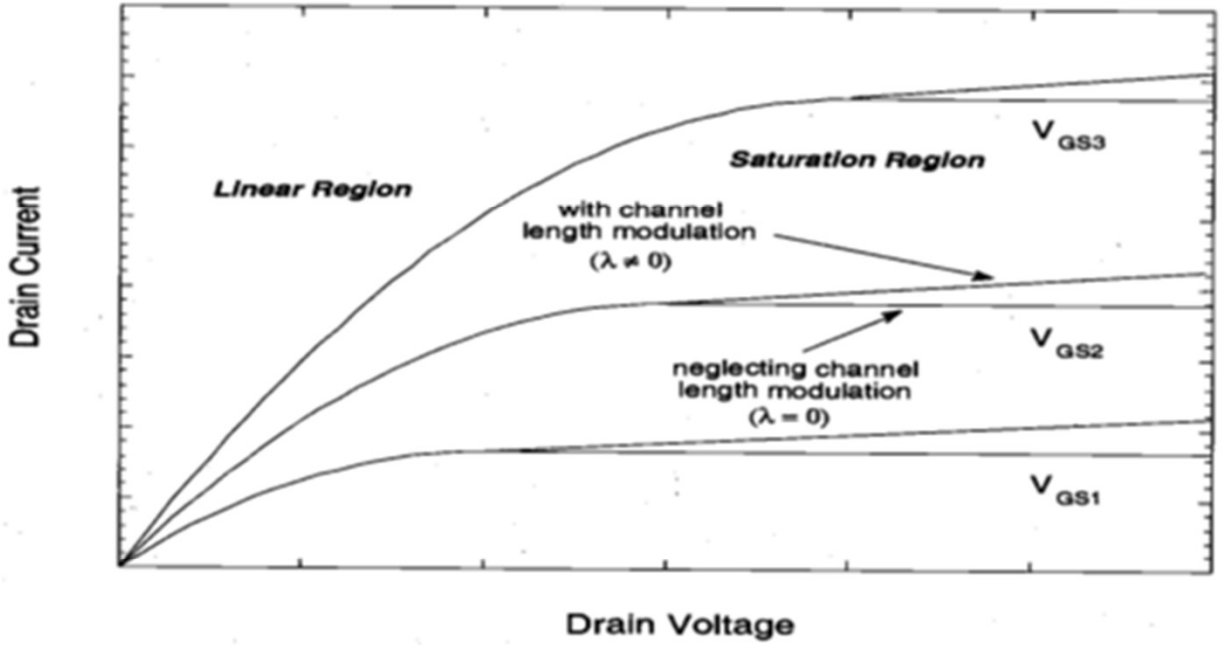
- ✓ To simplify the analysis even further, we will use the following empirical relation between and the drain-to-source voltage instead:

$$1 - \frac{\Delta L}{L} \approx 1 - \lambda \cdot V_{DS}$$

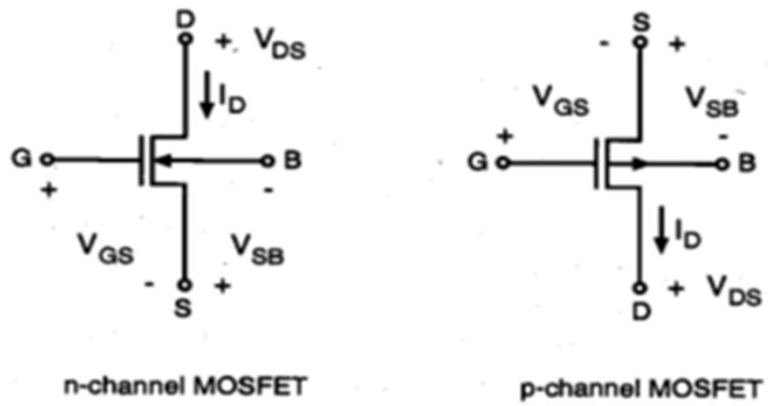
- ✓ Here, λ is an empirical model parameter, and is called the *channel length modulation coefficient.* Assuming that $\lambda V_{DS} << 1$, the saturation current can now be written as:

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{T0})^2 \cdot (1 + \lambda \cdot V_{DS})$$

Channel Length Modulation



Current-voltage characteristics of an n-channel MOS transistor, including the channel length modulation effect



Channel Length Modulation

$$I_D = 0, \quad for \quad V_{GS} < V_T$$

$$I_D(lin) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2\right] \qquad for \quad V_{GS} \geq V_T \quad and \quad V_{DS} < V_{GS} - V_T$$

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \qquad for \quad V_{GS} \geq V_T \quad and \quad V_{DS} \geq V_{GS} - V_T$$

Current-voltage equations of the n-channel MOSFET

$$I_D = 0, \quad for \quad V_{GS} > V_T$$

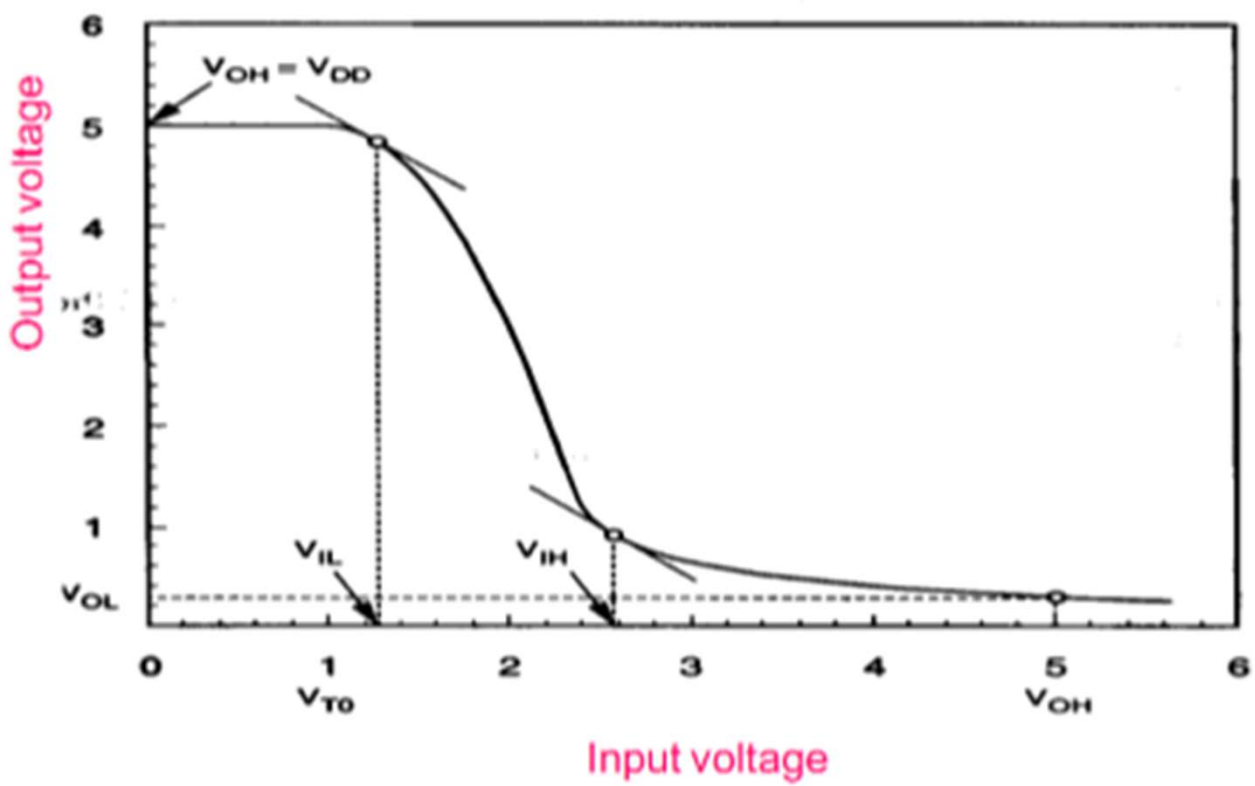
$$I_D(lin) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2\right] \qquad for \quad V_{GS} \leq V_T \quad and \quad V_{DS} > V_{GS} - V_T$$

$$I_D(sat) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \qquad for \quad V_{GS} \leq V_T \quad and \quad V_{DS} \leq V_{GS} - V_T$$

Current-voltage equations of the p-channel MOSFET

MOS DC Transfer Characteristics

- ✓ DC transfer characteristics refer to the relationship between the input voltage and the output voltage of a circuit, typically a logic gate or an amplifier, when a constant (DC) voltage is applied.
- ✓ This characteristic is essential in understanding and analyzing the behavior and performance of electronic circuits, particularly CMOS logic gates.



Introduction to IC Design Cycle and Layout

IC Design Cycle:

- ✓ The Integrated Circuit (IC) design cycle is a comprehensive process that involves several stages, each essential for creating a functional and reliable IC.

- ✓ The cycle encompasses various phases, from initial concept and specification to the final testing and manufacturing of the IC.

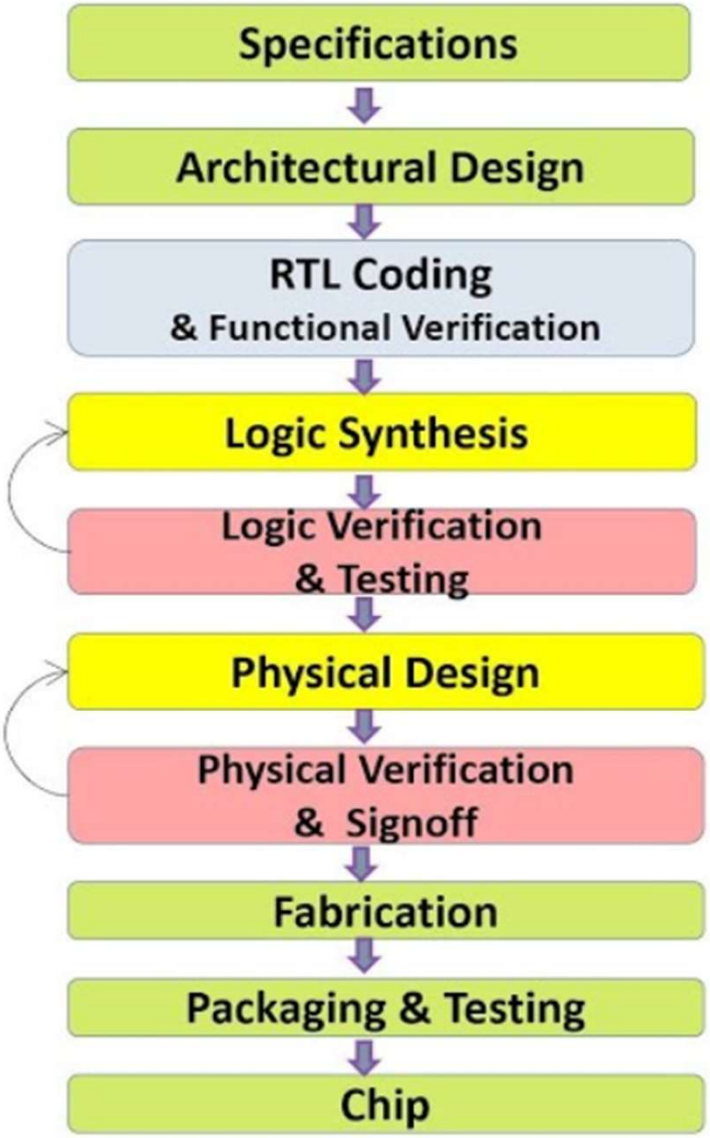
- ✓ From initial concept to final production, each step is critical to ensure that the final IC meets all specifications, performs reliably, and can be produced efficiently.

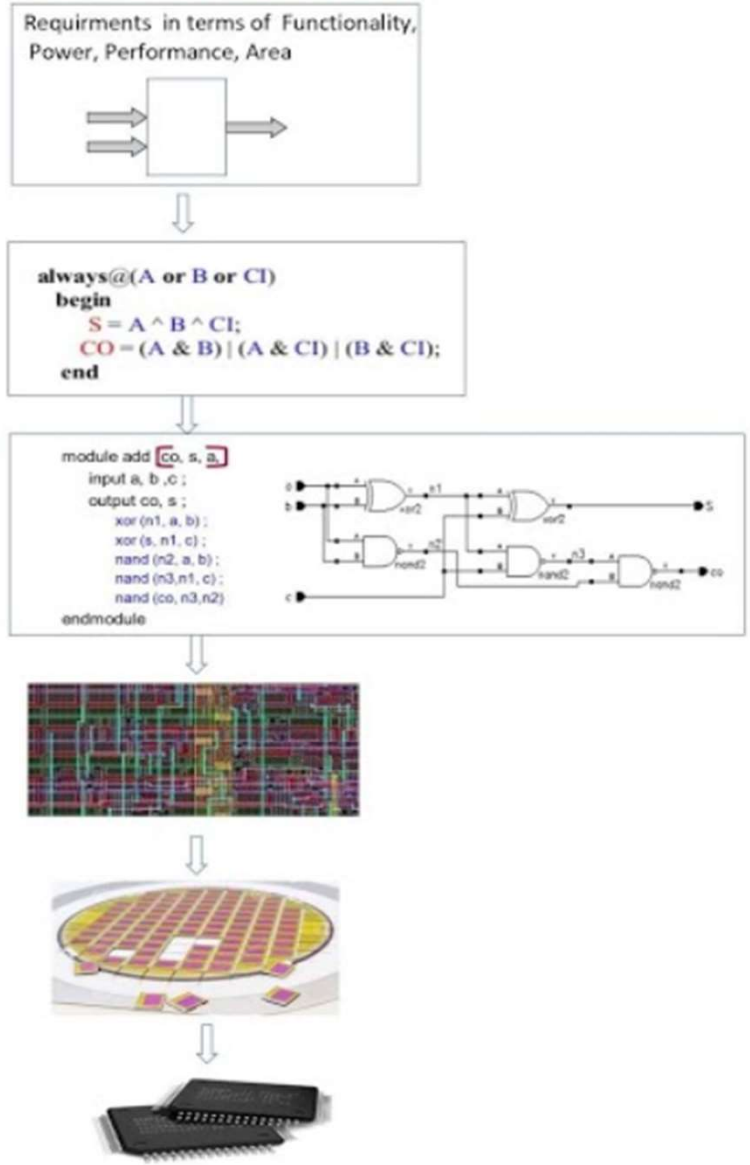
Layout:

- ✓ The physical (mask layout) design of CMOS logic gates is an iterative process which starts with the circuit topology (to realize the desired logic function) and the initial sizing of the transistors (to realize the desired performance specifications).

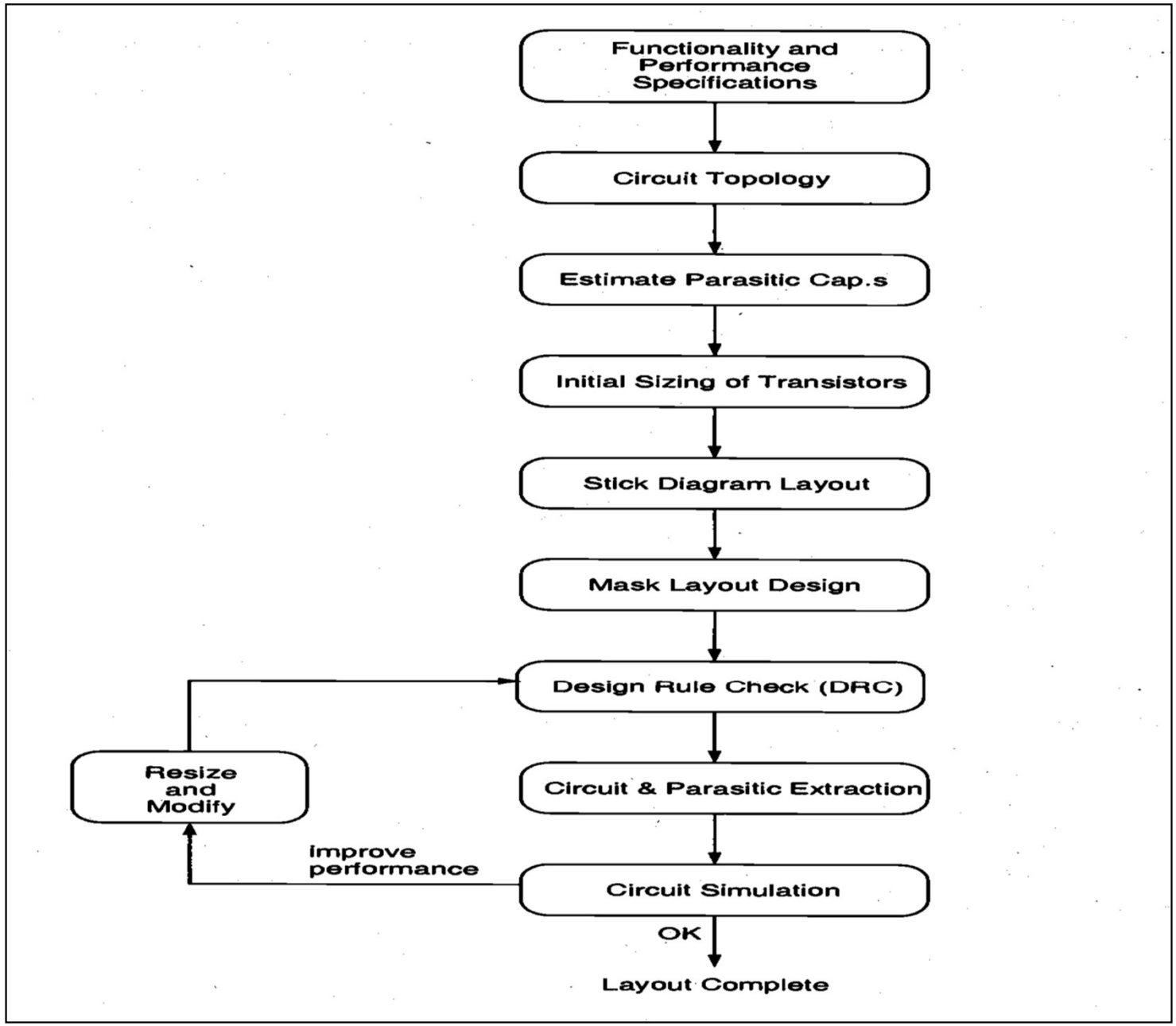
Introduction to IC Design Cycle

VLSI-IC Design Flow / ASIC Flow / RTL to GDS Flow

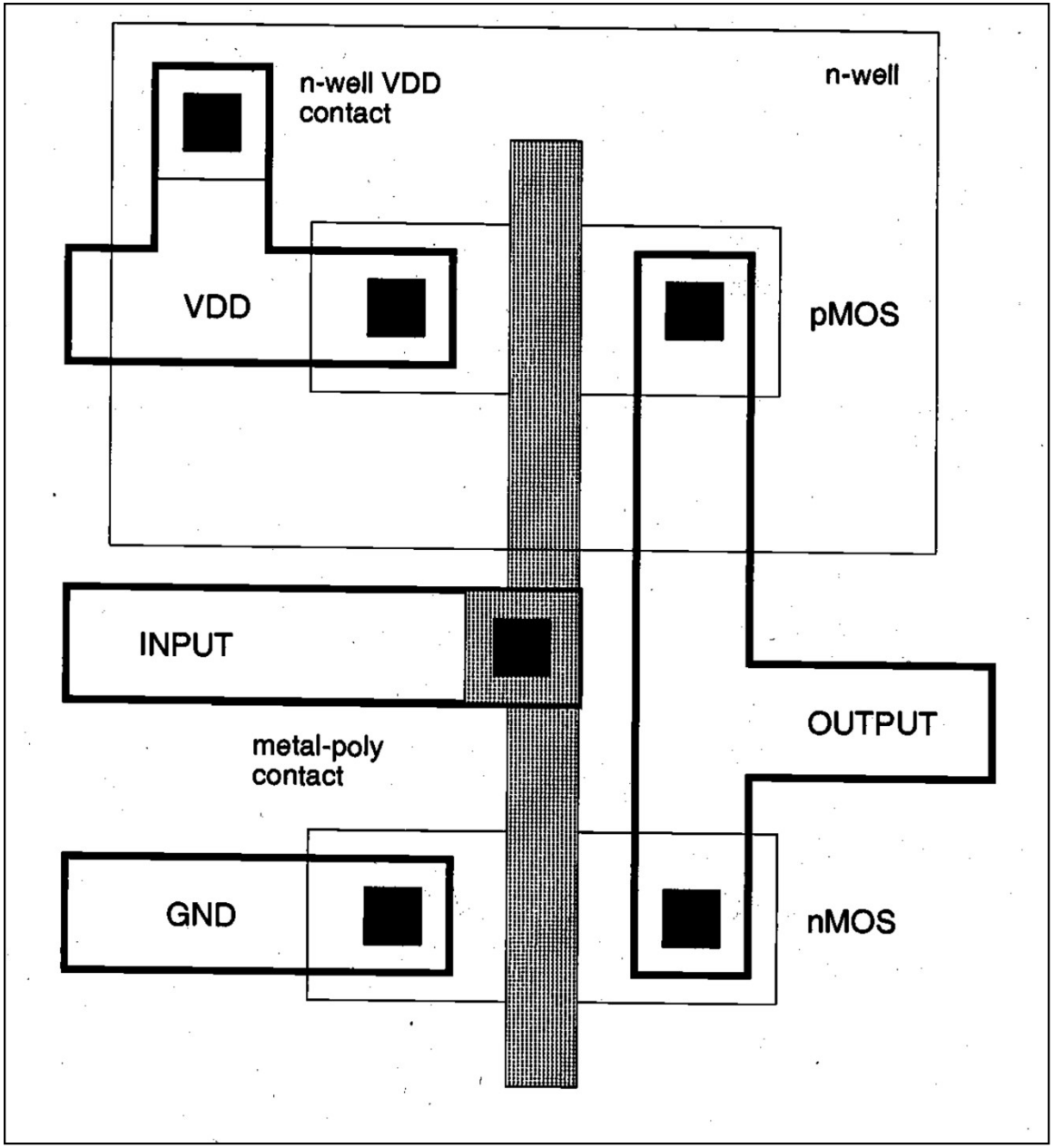


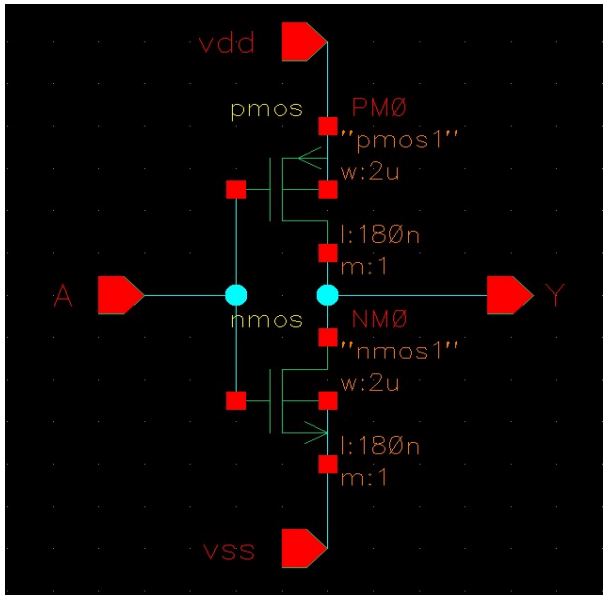


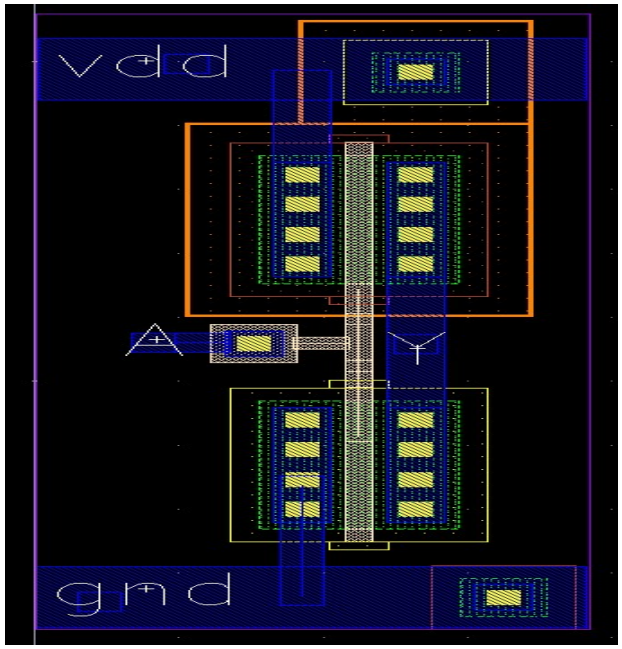
Layout Design Process



Complete mask layout of the CMOS inverter







Session 2

Lecture: CMOS Gates and Characteristics

- CMOS Logic Circuits
- CMOS Inverter and I-V Characters

CMOS Logic Circuits

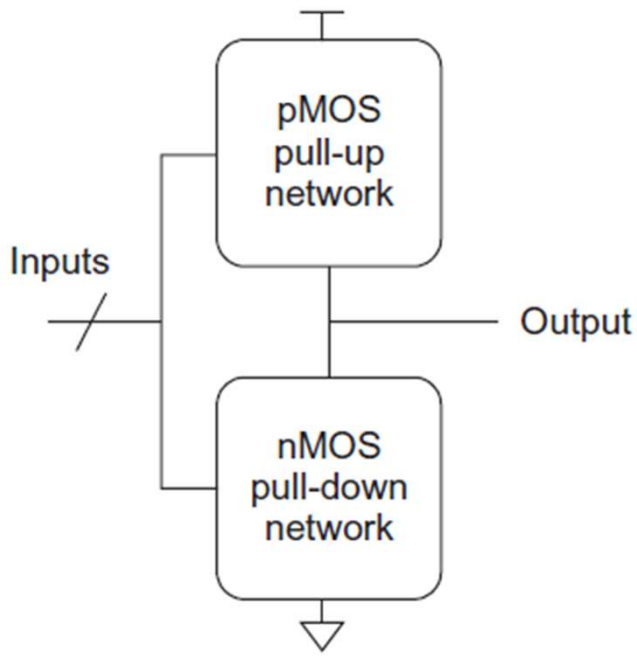
- CMOS logic circuits utilize both NMOS and PMOS transistors to implement various digital logic functions.

CMOS Logic Gates:

✓ The Inverter, NAND, NOR gates are examples of static CMOS logic gates, also called complementary CMOS gates.

✓ In general, a static CMOS gate has an nMOS pull-down network to connect the output to 0 (GND) and pMOS pull-up network to connect the output to 1 (VDD) as shown in below Figure.

✓ The networks are arranged such that one is ON and the other OFF for any input pattern.



CMOS Logic Circuits

CMOS Logic Gates:

✓ The pull-up and pull-down networks in the inverter each consist of a single transistor.

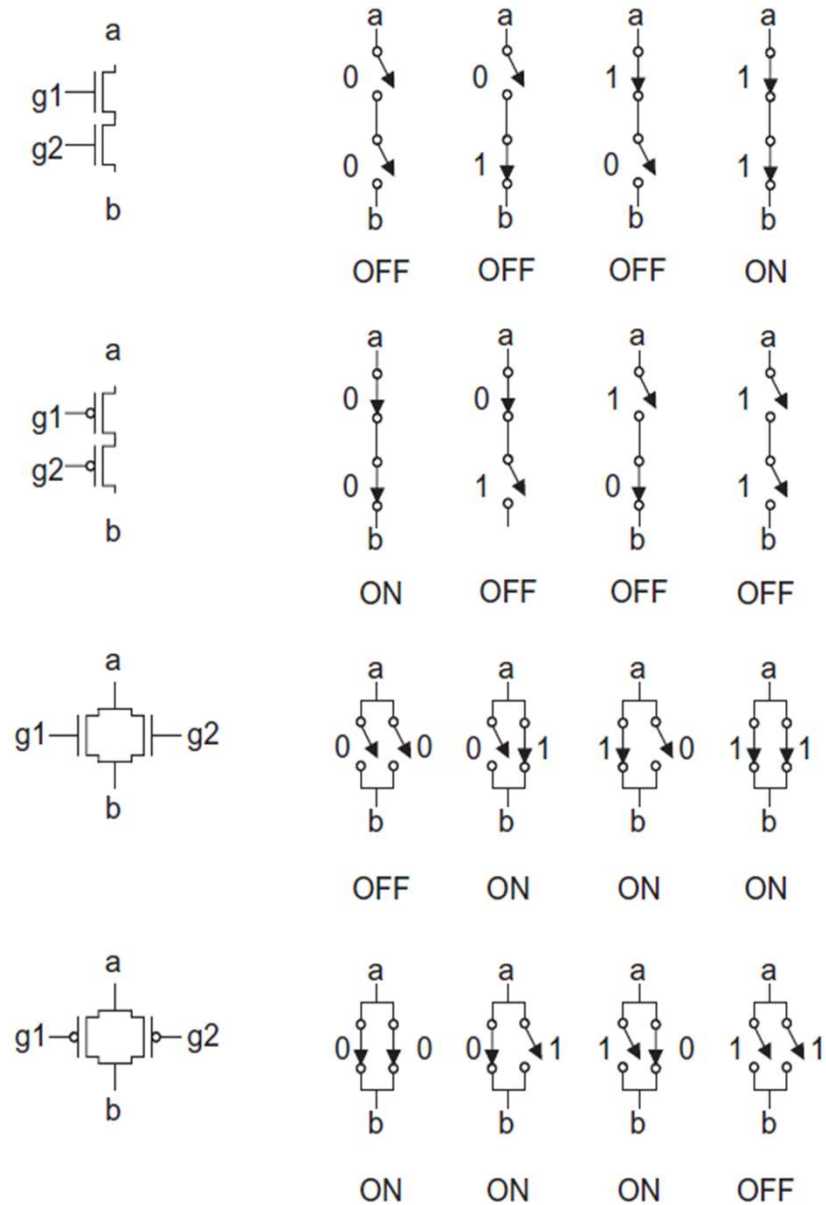
✓ The NAND gate uses a series pull-down network and a parallel pullup network and reverse is in NOR gate.

✓When both pull-up and pull-down are OFF, the high impedance or floating Z output state results. This is of importance in multiplexers, memory elements, and tristate bus drivers.

✓The crowbarred (or contention) X level exists when both pull-up and pull-down are simultaneously turned ON.

✓Contention between the two networks results in an indeterminate output level and dissipates static power. It is usually an unwanted condition.

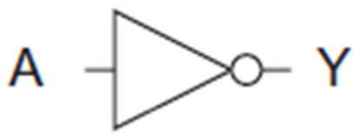
	pull-up OFF	pull-up ON
pull-down OFF	Z	1
pull-down ON	0	crowbarred (X)

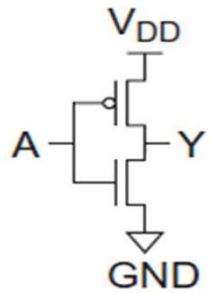


CMOS Logic Circuits

Basic CMOS Logic Gates: NOT (Inverter), NAND, NOR etc

NOT Gate:

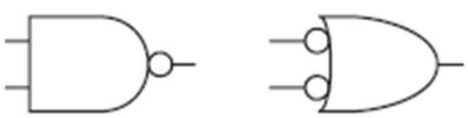


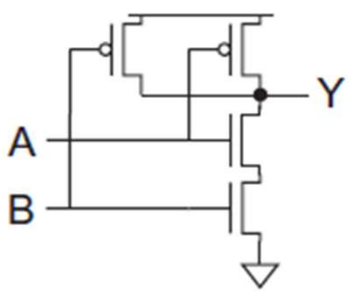


A	Y
0	1
1	0

NAND Gate:

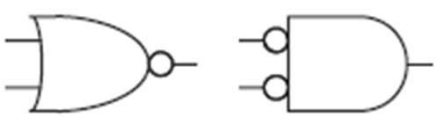
2-input CMOS NAND gate consists of two series nMOS transistors between Y and GND and two parallel pMOS transistors between Y and VDD.

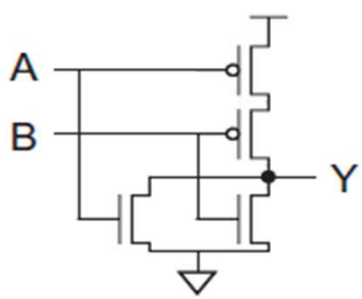




A	B	Pull-Down Network	Pull-Up Network	Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

NOR Gate: Connection of series pMOS and parallel nMOS.





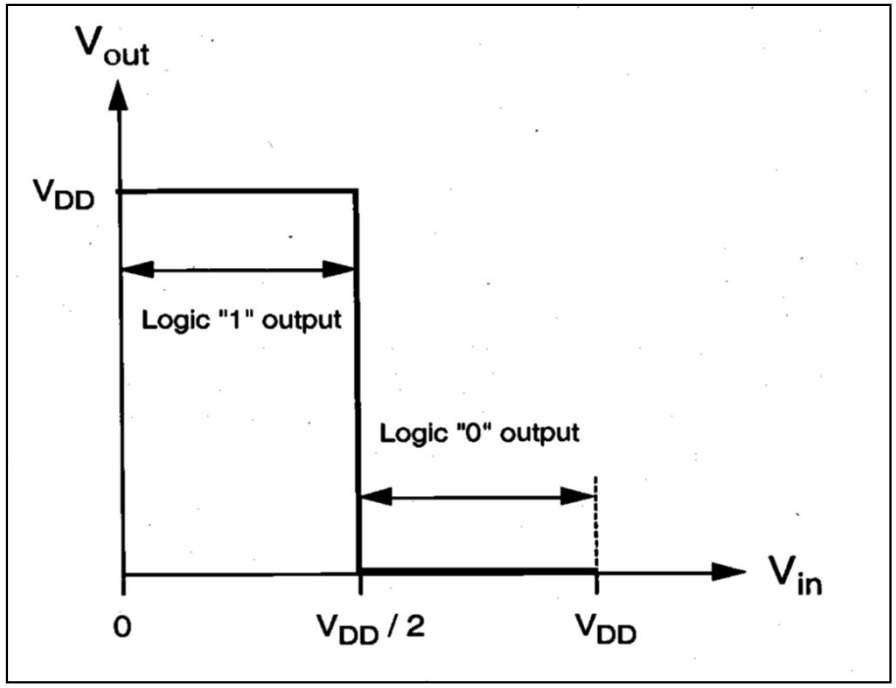
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

CMOS Inverter and I-V Characteristics

CMOS Inverter: The inverter (NOT) is the most fundamental logic gate that performs a Boolean operation on a single input variable.

- The DC voltage transfer characteristic (VTC) (Function of output voltage and input voltage) of the ideal inverter circuit is shown in below figure.
- The voltage V_{th} is called the inverter threshold voltage. Note that for any input voltage between 0 and $V_{th} = V_{DD}/2$, the output voltage is equal to V_{DD} (logic "1").
- For any input voltage between V_{th} and V_{DD}, the output voltage assumes a value of 0 (logic "0").

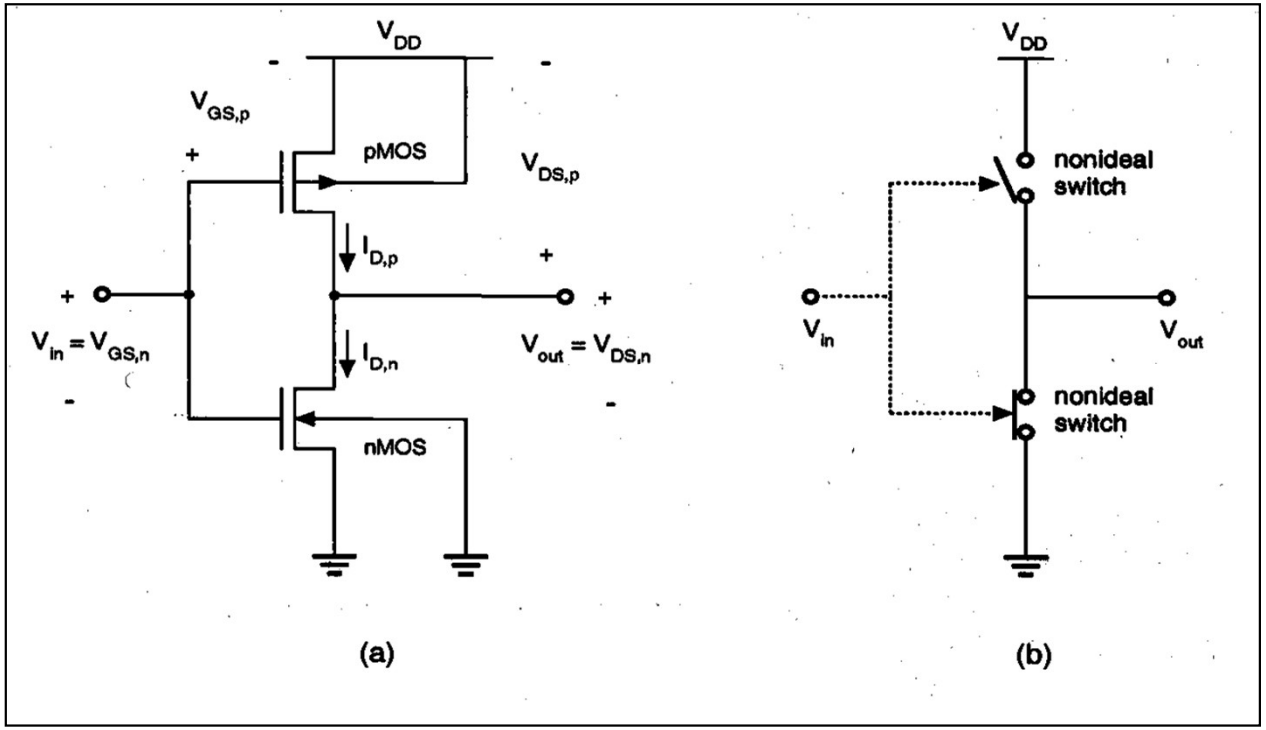
- Thus, an input voltage $0 < V_{in} < V_{th}$ is interpreted by this ideal inverter as a logic "0" while an input voltage $V_{th} < V_{in} < V_{DD}$ *is* interpreted as a logic "1".

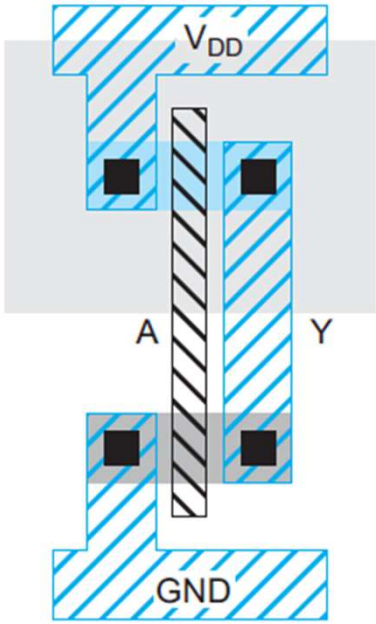


CMOS Inverter and I-V Characteristics

Advantages of CMOS Inverter:

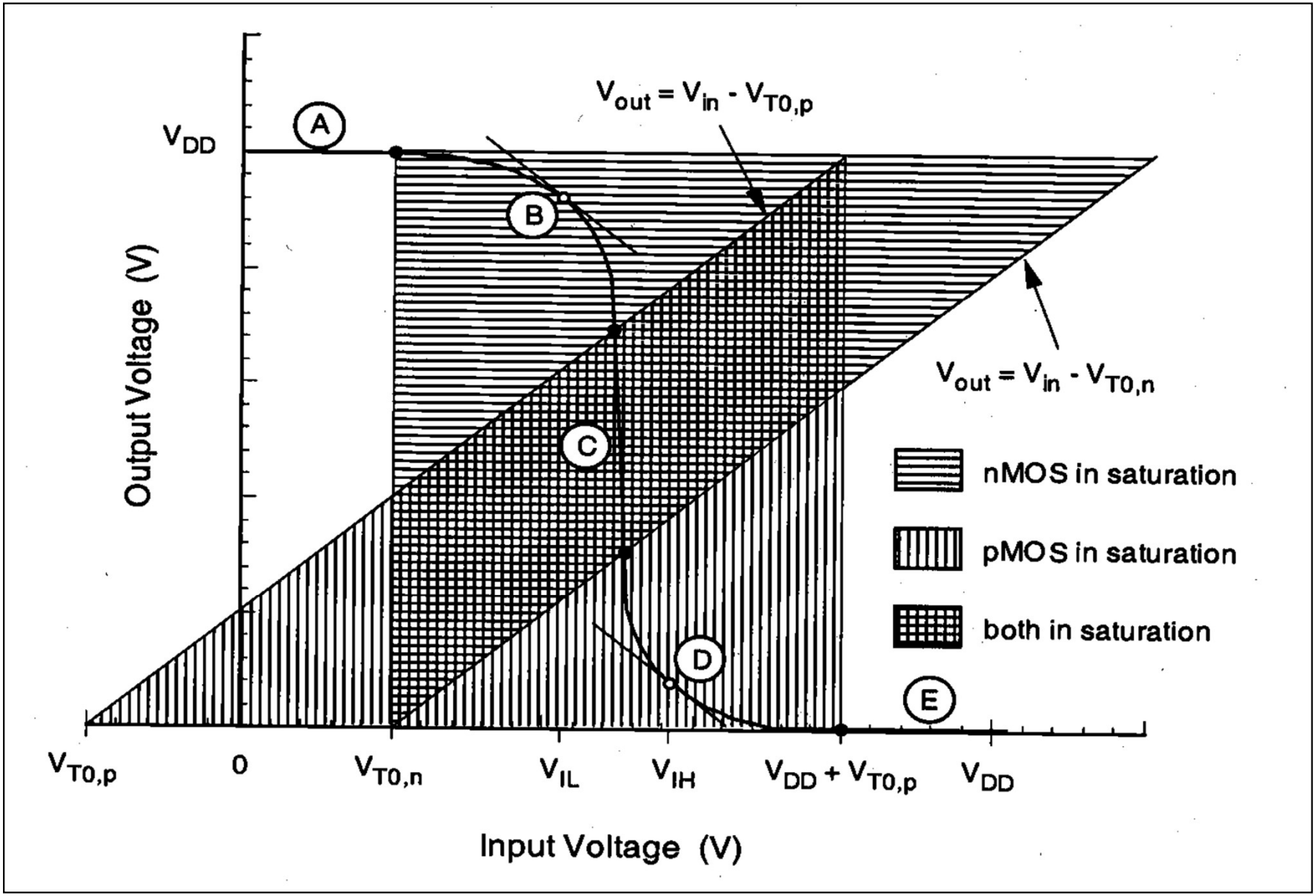
- The steady-state power dissipation of the CMOS inverter circuit is virtually negligible, except for small power dissipation due to leakage currents.
- The voltage transfer characteristic (VTC) exhibits a full output voltage swing between 0 V and V_{DD}.
- The VTC transition is usually very sharp. Thus, the VTC of the CMOS inverter resembles that of an ideal inverter.





CMOS Inverter and I-V Characteristics

Circuit Operation:



CMOS Inverter and I-V Characteristics

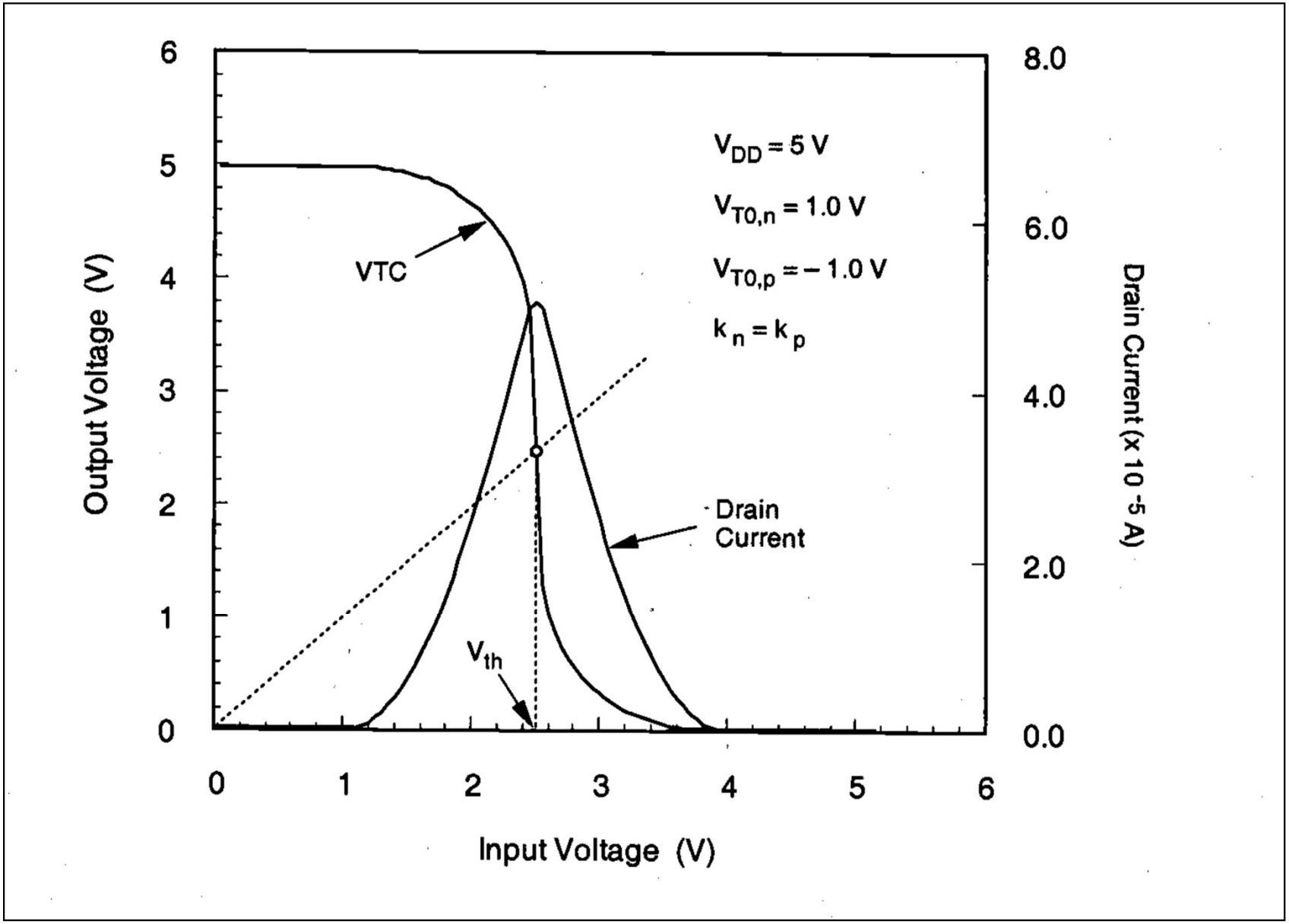
- The table below lists these regions and the corresponding critical input and output voltage levels.

- The critical voltage points on the VTC, where $V_{out} = V_{OH} = V_{DD}$ and $V_{out} = V_{OL} = 0$ for this inverter and others are V_{IL}, V_{IH} and V_{th} .

Region	V_{in}	V_{out}	nMOS	pMOS
A	$< V_{T0,n}$	V_{OH}	cut-off	linear
B	V_{IL}	high $\approx V_{OH}$	saturation	linear
C	V_{th}	V_{th}	saturation	saturation
D	V_{IH}	low $\approx V_{OL}$	linear	saturation
E	$>\left(V_{DD} + V_{T0,p}\right)$	V_{OL}	linear	cut-off

CMOS Inverter and I-V Characteristics

Typical VTC and the power supply current of a CMOS inverter circuit:



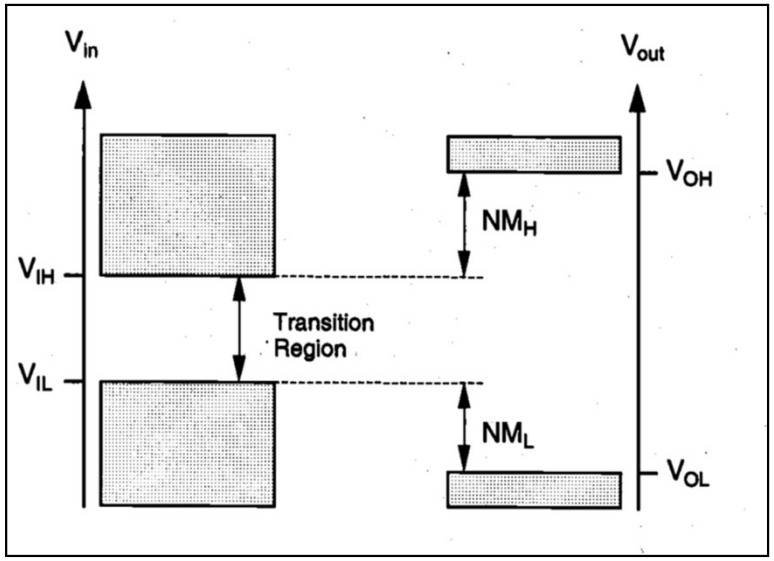
CMOS Inverter and I-V Characteristics

Noise Margins:

- The noise tolerances for digital circuits, called noise margins and denoted by NM.
- The noise immunity of the circuit increases with NM.
- Two noise margins are NM_L and NM_H.

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$



- The noise margins NM_L and NM_H for this symmetric CMOS inverter are now calculated:

$$NM_L = V_{IL} - V_{OL} = V_{IL}$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH}$$

THANK YOU