[CS6250] CN P4 Assignment 1

Team 108

Members

Rohith Sudheer , Simran Gade, Abrar Ahmed Mohammed

Report

Explain each register arrays that have you defined, what is their size and what is their purpose

In this report, we mainly discuss the design choices made. In the topology given to us, each switch has at most 3 interfaces/ports, so we defined the register array as $register < bit < X >> (Y) my\_register$, where $X = 32$ and $Y = 6$, which is 3×2, one for active and the other for an inactive register per port. We define the registers arrays this way for both ingress and egress ports. The purpose of the ingress register arrays keeps count of the packets received at the port and the egress register keeps track of the messages sent from the port.

Explain how you managed your switches to detect failures on all the switch-to-switch links (and not only one)

For each port on the switch we maintain an egress and ingress table to monitor each link between switches. In order to detect failures, we would compare the ingress inactive counter of the receiver switch and egress inactive counter of the sender switch. If the values don't match, then there would be a failure.

Explain which registers does the controller read and write.

The controller reads the inactive registers (ingress and egress) and then sets them to zero (by writing to them) and switches the active and inactive registers. Controller writes to the *active_register* in order to make the swap.

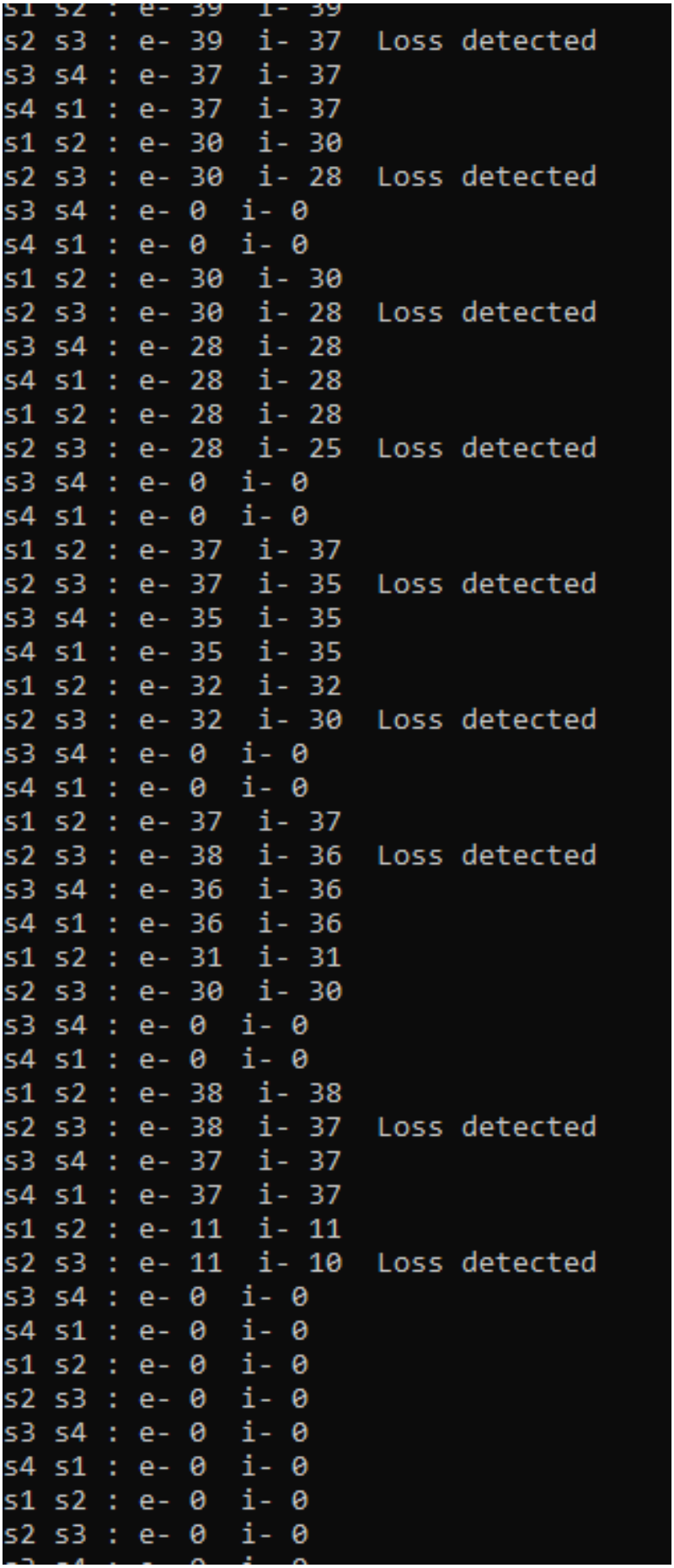

Figure 1: controller.py output when pinging h2 from h1 with 5% loss on s2-eth2