3.3 Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

a. What is the maximum directly addressable memory capacity (in bytes)?

b. Discuss the impact on the system speed if the microprocessor bus has

1. a 32-bit local address bus and a 16-bit local data bus, or

2. a 16-bit local address bus and a 16-bit local data bus.

c. How many bits are needed for the program counter (PC) and the instruction register (IR)?

Solution:

a. Since the first byte (8-bits) contains the opcode, so the bits available for operand address = 32-8=24 bit

Thus, the maximum addressable memory, 2^{24} = 16, 777,216 Bytes = 16 MB

b. (1) If the local address bus is 32 bits, the whole address can be transferred at once and decoded in memory. However, because the local data bus is only 16 bits, it will require 2 cycles to fetch a 32-bit instruction or operand.

(2) The 16 bits of the address placed on the address bus can't access the whole memory. In addition, the microprocessor will need 2 cycles to fetch the 32-bit instruction/operand.

c. The program counter must be at least 24 bits (24-bit addresses). If the instruction register is to contain the whole instruction, it will have to be 32-bits long; if it will contain only the opcode (called the opcode register) then it will have to be 8 bits long.

Problem 3.4.

Consider a hypothetical microprocessor generating a 16-bit address (for example, assume that the program counter and the address registers are 16 bits wide) and having a 16-bit data bus.

a. What is the maximum memory address space that the processor can access directly if it is connected to a "16-bit memory"?

b. What is the maximum memory address space that the processor can access directly if it is connected to an "8-bit memory"?

Answer:

a. The Maximum memory address space = 2^16 = 64 Kbytes.

b. The Maximum memory address space = 2^16 = 64 Kbytes.

Therefore, in (a) and (b), the microprocessor is to access 2^{16} = 64K bytes, but the only difference is that

- With an 8-bit memory each access will transfer 8-bit (a byte) while
- With a 16-bit memory each access may transfer 8-bits (a byte) or 16-bits (a word)

3.5 Consider a 32-bit microprocessor, with a 16-bit external data bus, driven by an 8-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/s?

To increase its performance, would it be better to make its external data bus 32 bits or to double the external clock frequency supplied to the microprocessor? State any other assumptions you make and explain. Hint: Determine the number of bytes that can be transferred per bus cycle.

Solution:

8 MHz = 1sec

8 000000 clock cycles take 1 sec

1 Clock cycle = 1 /8 MHz = 1/8000000 sec =125 ns

So, 1 Bus cycle takes = 4 × 125 ns = 500 ns (1 bus cycle = 4 input clock cycle)

Given External data bus = 16-bit

Thus, 2 bytes of data can be transferred in every 500 ns

In 500 ns data can be transferred 2 bytes

In 1 sec data can be transferred 4 MB

Transfer rate = 4 MBytes/sec

To increase its performance, if external data bus will be 32 bits then

4 bytes can be transferred in every 500 ns

transfer rate = 8 MBytes/sec

To increase its performance, if double the external clock frequency then

Clock cycle = 1 /16 MHz = 62.5 ns

Bus cycle = 4 × 62.5 ns = 250 ns

2 bytes of data can be transferred in every 250 ns

transfer rate = 8 MBytes/sec

In the first case, the word length of the memory will have to double to be able to send or receive 32-bits of data.

In the second case, the speed of the memory chips will also need to double.

3.7 Consider two microprocessors having 8- and 16-bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.

a. Suppose all instructions and operands are two bytes long. By what factor do the maximum data transfer rates differ?

b. Repeat assuming that half of the operands and instructions are one-byte long.

Solution:

a. During a single bus cycle, the 8-bit microprocessor transfers one byte while the 16-bit microprocessor transfers two bytes. The 16-bit microprocessor has twice the data transfer rate.

b. Suppose we do 100 transfers of operands and instructions, of which 50 are one byte long and 50 are two bytes long.

- The 8-bit microprocessor takes 50 x 1 + (50 x 2) = 150 bus cycles for the transfer.
- The 16-bit microprocessor requires 50 + 50 = 100 bus cycles. Thus, the data transfer rates differ by a factor of 150/100=1.5.

3.14 A microprocessor has an increment memory direct instruction, which adds 1 to the value in a memory location. The instruction has five stages: fetch opcode (four bus clock cycles), fetch operand address (three cycles), fetch operand (three cycles), add 1 to operand (three cycles), and store operand (three cycles).

a. By what amount (in percent) will the duration of the instruction increase if we have to insert two bus wait states in each memory read and memory write operation?

b. Repeat assuming that the increment operation takes 13 cycles instead of 3 cycles.

Solution a:

- Without the wait states, the instruction takes 16 bus clock cycles (4+3+3+3+3).
- The instruction requires four memory accesses, resulting in 8 wait states (**fetch opcode: two bus wait states + fetch operand address: two bus wait states + fetch operand: two bus wait states + store operand: two bus wait states)**.
- The instruction, with wait states, takes 24 clock cycles (16+8)
- In 16 clock cycle increasing amount is 8
- In 1 clock cycle ========== = 8/16
- In 100 ---------- =(8*100/16) =50%

b. In this case, the instruction takes 26 bus cycles without wait states and 34 bus cycles with wait states, for an increase of ((34-26)/26)*100% = 30.769%.

3.17 Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 40% are only 8-bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor.

Solution:

- Consider a mix of 100 instructions and operands.
- The number of bus cycles required for the 16-bit microprocessor is:
  = 20x2+ 40x1 + 40x1 = 120.
- The number of bus cycles required for the 32-bit microprocessor is:
  = 20x1+ 40x1 + 40x1 =100.
- The amount of improvement achieved is = (120-100) *100/120 = 16.67%= 17%.