Group No. 1

Course No. : CSE 210N
Course Name : Digital Electronics and Pulse Techniques Sessional

Experiment No. : 2

STUDY OF A TRANSISTORIZED NOT GATE

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Level : 2
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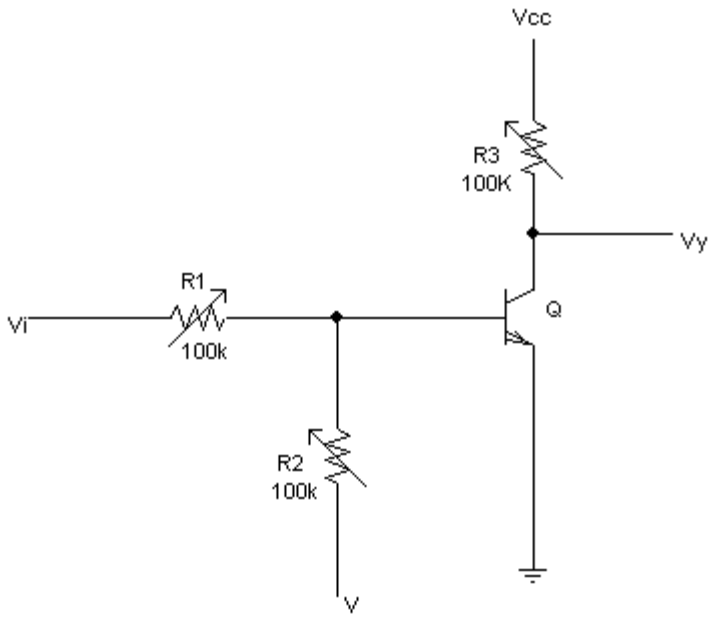
Objective:

The objective of the experiment is to implement the NOT and to observe the effect of changing different circuit parameters on the gate.

Circuit Diagram:



Questions:

1. **Why CE configuration is preferred in switching circuit? Why not others?**

Answer:

The required condition for a 'on' transistor in CE configuration to drive in saturation is,

$$h_{fe} > I_{C(Sat)} / I_B$$

In CE configuration, h_{fe} is sufficient to satisfy the above condition. This is why CE configuration is preferred in switching circuit.

But, in CB configuration, the input current (I_E) almost equals the collector current (I_C). Thus the current gain is almost equal to unity, which is not sufficient for the operation of the transistor in saturation region.

CC configuration is only applicable as a voltage buffer rather than in the switching circuit.

2. **Which factor affect the switching speed of the transistor and how?**

Answer:

The internal capacitive effect of the transistor affects the switching speed of it and it does not switch in zero time. When the input voltage v_1 rises from the negative (zero) level V(0) to the positive level V(1), the collector current does not respond immediately. Rather a delay time t_D elapses before any appreciable collector current begins to flow. This delay time is required mainly for the EBJ depletion capacitance to charge up to the forward-bias voltage V_{BE} (approximately 0.7V). After this charging process is completed, the collector current begins an exponential rise toward a final value of βI_B.

In fact, it is during the interval of the rising edge of I_C that the excess minority carrier charge is being stored in the base region. Since the transistor will saturate, the collector current will be limited to $I_{C(sat)}$. The excess minority charge stored in the base region does contribute in a corresponding collector current component. Rather, this extra charge arises from the forcing of more current into the base than is required to saturate the transistor.

Let us now consider the turn-off process. When the input voltage v_1 returns to the low level V(0), the collector does not respond but remains constant for a time, t_s. This is the time required to remove the saturating charge from the base, known as the storage time. The reverse current I_{B1} helps to "discharge the base" and remove the extra stored charge; in the absence of I_{B1}, the saturating charge has to be removed entirely by recombination. Once the extra charge stored has been removed, the collector current begins to fall exponentially with a time constant determined by the junction capacitances and the output voltage reaches the 1 level, V(1).

Experimental Data:

When R_3 is varied:

R_1 = 35.4 kΩ, R_2 = 50.8 kΩ, V_i = 5.0V, V = -5V

R_3 (kΩ)	V_{BE} (V)	V_O (V)
0.067	0.604	4.41
0.750	0.604	3.69
1.680	0.604	2.70
2.740	0.604	1.59
3.430	0.604	0.84
4.010	0.604	0.28
4.900	0.600	0.13

When R_2 is varied:

R_1 = 35.4 kΩ, R_2 = 73.3 kΩ, V_i = 5.0V, V = -5V

R_2 (kΩ)	V_{BE} (Volts)	V_O (Volts)
41.5	0.299	5.02
44.3	0.480	4.27
45.3	0.503	3.15
45.7	0.512	2.48
46.3	0.536	0.05

When R_1 is varied:

R_2 = 51.1 kΩ, R_3 = 73.3 kΩ, V_i = 5.0V, V = -5V

R_1 (kΩ)	V_{BE} (Volts)	V_O (Volts)
36.9	0.540	0.03
40.0	0.525	0.59
41.0	0.515	2.10
41.3	0.503	3.11
41.9	0.493	3.68
43.0	0.404	4.98

When V is varied:

R_1 = 35.65 kΩ, R_2 = 51.1 kΩ, R_3 = 73.3 kΩ , V_i = 5V

V (Volts)	V_{BE} (Volts)	V_O (Volts)
-4.95	0.546	0.02
-5.81	0.529	0.12
-5.83	0.526	0.40
-5.85	0.520	1.40
-5.87	0.512	2.21
−5.91	0.501	3.25
−6.15	0.411	4.98

Discussion:

- **When R_3 is varied:**

  For higher values of R_3, the circuit operates correctly, because higher value of R_3 ensures smaller collector current. As a result, the transistor drives more into the saturation region. But, when smaller value of R_3 is used, increased I_C causes the circuit to be malfunctioning.

  So, higher value of R_3 is desired.

- **When R_2 is varied:**

  For higher values of R_2, the drop across it becomes also higher. As a result, V_B becomes sufficient to turn the transistor on. Since, V is negative, in case of smaller values of R_2, voltage at the base may even appear negative, which certainly cannot turn the transistor on.

So, higher value of R_2 is desired.

- **When R_1 is varied:**

  Here the resistance of R_1 should be set to a value such that the base of the transistor acquires sufficient voltage to turn the transistor on. This condition can be achieved by keeping the resistance of R_2 low.

- **When V is varied:**

  The output voltages corresponding to V in the experimental data suggest that higher values of V confirm the correct operation of the gate. More negative values of V do not provide sufficient voltage to the base to turn the transistor on.

  So, higher value of V is desired.