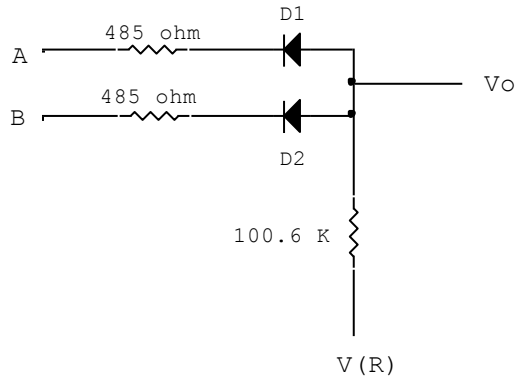
Objective:

Logic gates play the most vital role in designing digital circuits. In this experiment we observed different aspects of DL (Diode Logic) and DTL (Diode Transistor Logic) gates.

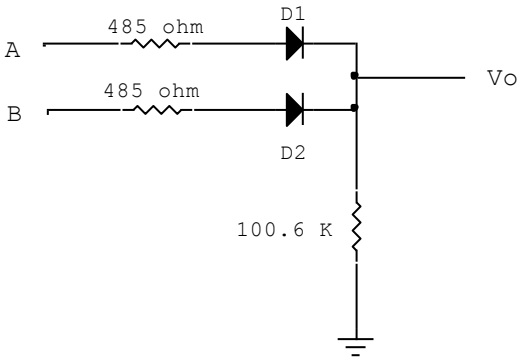
Equipments:

1. Resistors (485 Ω , 2.2 KΩ , 100.6 KΩ)
2. Diodes
3. npn Transistor (BD-135)
4. Trainer Board
5. Wires

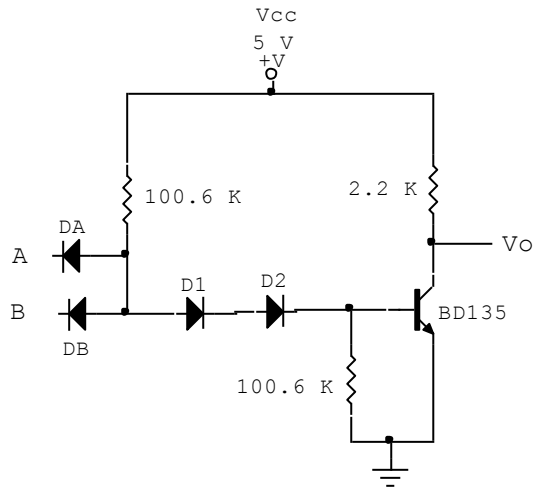
Circuit Diagram:



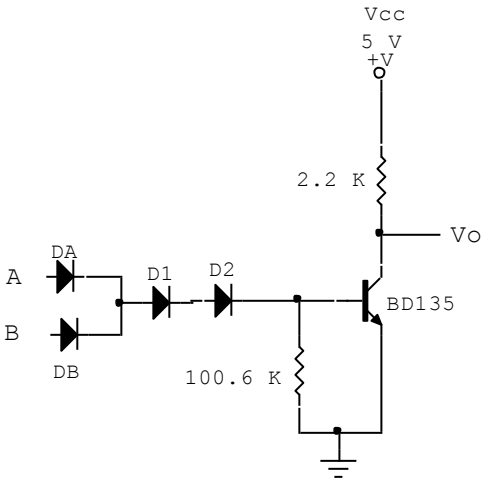
Circuit # 01



Circuit # 02



Circuit # 03



Circuit # 04

Data Collection:

Table for Ckt # 01

V_R = 4.97 V

V_A (Volt)	V_B (Volt)	V_{D1} (Volt)	V_{D2} (Volt)	V_o (Volt)
0.001	0.001	0.402	0.402	0.404
0.001	4.99	0.429	- 4.56	0.42
5.00	0.001	- 4.57	0.429	0.432
4.99	5.00	- 0.04	- 0.04	4.90

Table for Ckt # 02

V_A (Volt)	V_B (Volt)	V_{D1} (Volt)	V_{D2} (Volt)	V_o (Volt)
0.001	0.001	$- 0.2 \times 10^{-3}$	$- 0.4 \times 10^{-3}$	0.001
0.001	4.97	- 4.54	0.42	4.54
4.97	0.001	0.42	- 4.54	4.54
4.99	4.98	0.40	0.40	4.58

Table for Ckt # 03

V_A (V)	V_B (V)	V_{DA} (V)	V_{DB} (V)	V_{D1} (V)	V_{D2} (V)	V_P (V)	V_{CE} (V)	V_o (V)
0.002	0.001	0.402	0.403	0.157	0.227	0.404	4.99	4.99
0.002	4.99	0.43	- 4.56	0.16	0.23	0.436	4.99	5.00
5.0	0.001	- 4.56	0.42	0.16	0.23	0.43	5.00	4.99
5.0	5.0	- 3.59	- 3.59	0.39	0.42	1.4	0.13	0.13

Table for Ckt # 04

V_A (V)	V_B (V)	V_{DA} (V)	V_{DB} (V)	V_{D1} (V)	V_{D2} (V)	V_P (V)	V_{CE} (V)	V_o (V)
0.002	0.0014	- 0.004	- 0.53	0.017	0.027	0.0046	4.9	4.99
0.001	2.58	- 1.93	0.649	0.62	0.63	1.87	0.007	0.008
2.51	0.001	0.63	- 1.87	0.62	0.63	1.87	0.008	0.008
2.59	2.6	0.641	0.649	0.665	0.671	1.964	0.007	0.007

Questions & Answers:

1. Analyze the Ckt # 01 and Ckt # 02 with the help of truth table for both positive and negative logic.

For Ckt # 01:

I_1	I_2	V_o
0	0	0
0	1	0
1	0	0
1	1	1

For Ckt # 01 the above truth table acts as a negative logic NOR and positive logic AND.

For Ckt # 02:

I_1	I_2	V_0
0	0	0
0	1	1
1	0	1
1	1	1

For Ckt # 02 the above truth table acts as a positive logic OR and negative logic NAND.

2. What happens if V_R is more positive than V(1)?

If V_R is more positive than V(1) then for Ckt # 01 all diodes will always be forward biased and hence output will always be low irrespective of input.

Similarly in the Ckt # 02 all the diodes will be reverse biased and hence output will always be high irrespective of input. So both the circuit will not perform the desired logical operation, as they meant to be.

3. What happens if not all inputs have the same upper level?

If for any reason the inputs of the positive logic AND gate do not have the same upper level V(1), then the output of the gate will equal $V(1)_{min}$,i.e. the least positive value of V(1). In this case the diode connected to $V(1)_{min}$ conducts and maintains all other diodes in the reversed biased condition.

For OR gate, under the same condition, the output is equal to the most positive level V(1) i.e. more precisely is smaller than the most positive value of V(1) by V_γ .

4. Why the resistance in the output circuit is so high? Why diode D_2 is used?

High Resistance:

To increase the drop across resistance and make V_o near zero when it is necessary to make V(0) = 0.2. Otherwise, it would show high voltage depending on resistance. Nevertheless, for less current, drop will also be high because of the high resistance, and enabling the circuit to perform the desired logical operation.

Why D_2 is used ?

It is meant to increase noise margin for high output. So, the circuit will work properly for high noise spikes. To achieve higher noise margin for high output three diodes can also be used in the circuit. But we must make sure that V_{CC} must be able to make the circuit operating in the desired logic level, i.e, we must make sure that for output to be low the path along, V_{CC} to the transistor throgh D_1 and D_2 , must be operating and the transistor must go to saturation level.

5. Can Emitter and Collector be interchanged?

Emitter and Collector can be interchanged for saturation state of transistor because in this state both base−emitter and base−collector has to be forward biased. But for other state of transistor operation, if this is done then the transistor may be improperly biased causing malfunction, as resistance between base-emitter and base-collector are not the same. i.e., Collector and Emitter aren't doped in same level. Also the thickness of Emitter and Collector differ. However, if this is done, then the circuit will be common collector and its A_V is not as high as common emitter. We know that common collector voltage gain is almost eual to one. And hence this configuration is known as voltage follwer.

So we will get the output voltage as the input to the base of the transistor. So the digital circuit will not work properly for the desired logical operation.

6. What is the significance of $h_{FE\ (min)}$?

For proper functioning of circuit h_{FE} must be greater than $h_{FE\ (min)}$. If any transistor used whose h_{FE} is less than $h_{FE\ (min)}$ then the circuit won't work as this is the minimum requirement for any transistor to use. For any change in I_B transistor's h_{FE} must be higher than this or it won't switch from cutoff to saturation or from saturation to cutoff. And we will not get the circuit to perform the desired logical operation.

CALCULATIONS:

For Ckt # 03:

$V_{CC} = 5$ V
$V_P = 1.4$ V
$V_o = 0.13$ V
$\therefore I_C = (5 - 0.13) / 2.2 = 2.2136$ mA
Current through 100.6 KΩ, diode D_1 and diode D_2 is,

$$I_2 = (5 - 1.4) / 100.6 = 0.0358 \text{ mA}$$

$V_{BE} = V_P - V_{D1} - V_{D2} = 1.4 - 0.39 - 0.42 = 0.59$ V
then,
$I_1 = 0.59 / 100.6 = 0.005865$ mA
$I_B = I_2 - I_1 = (0.0358 - 0.005865)$ mA
$= 0.029935$ mA
$h_{FE\ (min)} = I_C / I_B = 2.2136 / 0.029935 \approx 73.95$

Noise Margin Calculation:

For Ckt # 03:

- If all the inputs are high and they exceed the permitted logical value of 5 Volt then the diodes at the input will be more reverse biased. So we will have no effect for the output zero, i.e., for NM(0), when the inputs are increasing.

- Now for Negative Spike we get
  $NM(0) = -(5 - V_P + 0.6)$
  $= -(5.6 - 1.4) = -4.2$ V

- We need minimum V_{D1} = 0.6 V, V_{D2} = 0.6 V, and V_{BE} = 0.5 V to make the path along D_1 D_2 to base of transistor to conducting. So, noise margin will be, NM(1) = 0.6 + 0.6 + 0.5 – 0.43 = 1.27 V

For Ckt # 04:

NM(0) = - (V_B – V_P + 0.6) V = - (2.58 – 1.87 + 0.6) = - 1.31 V

- We need minimum V_{D1} = 0.6 V, V_{D2} = 0.6 V, and V_{BE} = 0.5 V to make the path along D_1 D_2 to base of transistor to conducting. So, noise margin will be, NM(1) = 0.6 + 0.6 + 0.5 – 0.0046 = 1.6954 V

Discussion:

In this experiment we came to know how to calculate noise margin of a logic circuit, and also, how to calculate $h_{FE\ (min)}$, and about its significance in switching circuits. From our experiment it was also evident that same circuit can be used for other logic. Such as in first circuit it acted both like a negative logic NOR and positive logic AND gate.

Noise Margin:

AND gate: NM(0)=-0.34 Volt
NM(1)=0.8 Volt

Or gate: NM(0)=-2.1 Volt
NM(1)=2.2 Volt