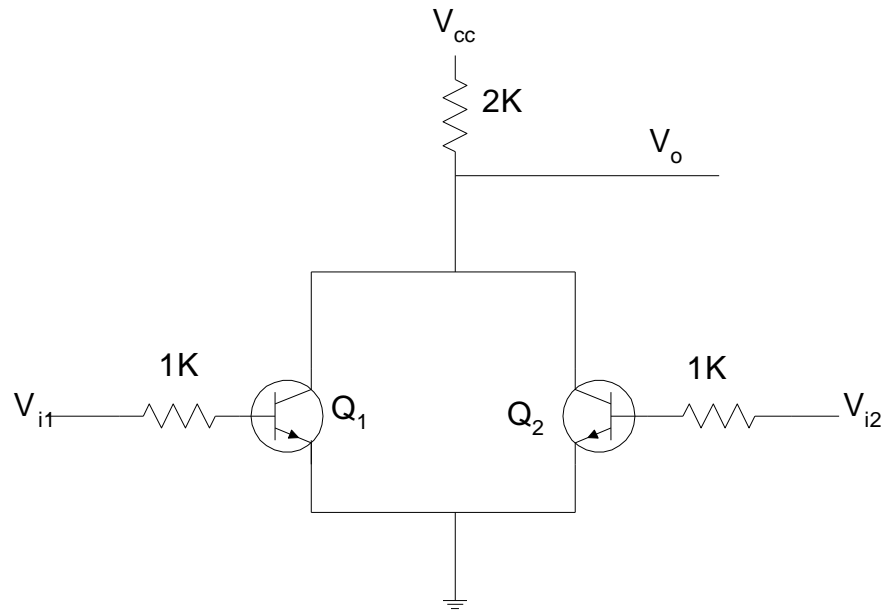Objective:

The main objective of this experiment is to study the characteristics of RTL NOR gate.

Circuit Diagram:

QUESTIONS & ANSWERS:

1. Analyze the operation of RTL NOR gate with the experimental data.

Ans.: As this is a NOR gate so high output will be observed only when all the inputs are low else output will be low. In the table-1 we see that when both the inputs are low the output is high else for all other combinations of input yields a low output.

Also from the table-2, when V_{i1} is grounded (i.e., first input is low) and when second input is at voltage 0.2V the output is high as required. This is because as all the input is low or nearly grounded so both the transistors are in cut-off so almost negligible amount of current is flown through the passive pull up resistor (R_C), resulting in a high output of 5.03 voltage. Same thing is observed in table-3 where V_{i2} is grounded and when first input is 0.2V the output is high.

But if any of the input is nearly 0.6—0.65V the output becomes low. Because, as this amount of applied then this will carry the corresponding transistor to come out of cut-off to active region and further increase in voltage will take it to saturation causing the output to be as low as 0.2V. This is also observed in both the last two tables where when any of the input is about 0.65V or 0.67V the output is 0.66V and 0.08 respectively for table-2 and 3 respectively. So this represents that noise margin is very low for V(1).

2. What is the importance of studying the RTL gate?

Ans.: Importance of studying the RTL gate is delineated below:

❖ This gate is elegantly simple and hence may be used conveniently to develop concepts useful in connection with all types of gates.

❖ RTL gate is historically the first gate to have been used extensively and many installations employing this type of gate are still in operation.

❖ Topologically at least, RTL is a forerunner of IIL (Integrated-Injection-Logic) which at the present wiring is one of the newest of commercially available LSI (Large Scale Integration) logic families.

3. Draw the V_0 vs. V_{I1} and V_{I2} curves.
Ans.: The graph drawn on the graph paper has been enclosed herewith.

Input Output Characteristics 1
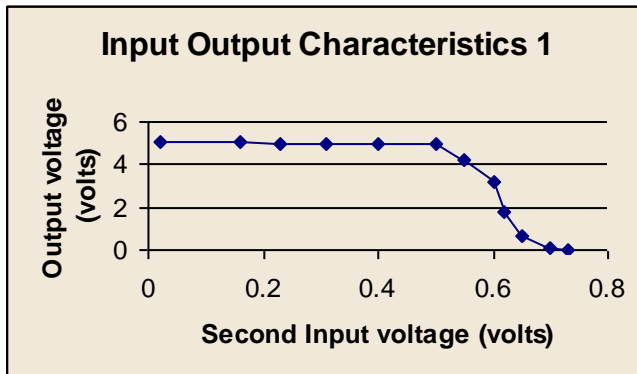
First graph is shown above.

Input Output Characteristics 2
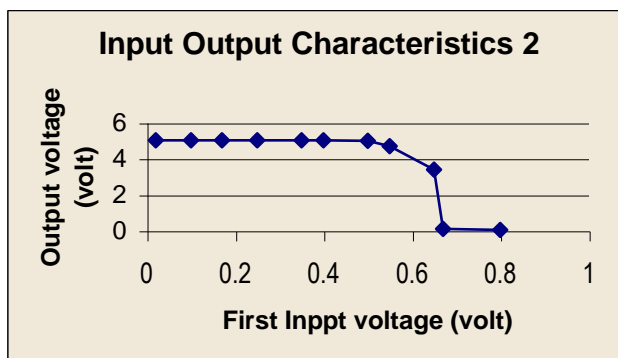
Second graph is enclosed in the above.

Discussion:

Doing this experiment following are the notable things:
- ❖ Noise margin of V(1) of RTL gate is very low.
- ❖ Both the transistors should be of same type.