Group No. 1

Course No. : CSE 210N
Course Name : Digital Electronics and Pulse Techniques Sessional

Experiment No. : 3

STUDY OF A TTL NAND GATE WITH TOTEM-POLE OUTPUT

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Level : 2
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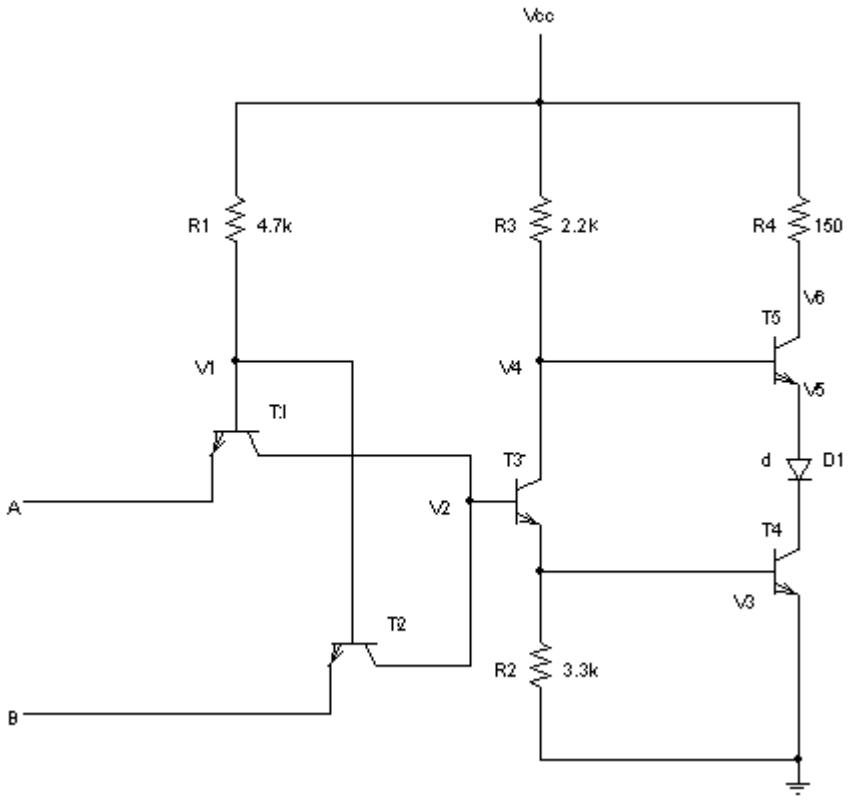
Objective:

The objective of the experiment is to implement the NAND gate with totem-pole output.

Circuit Diagram:



Questions:

1. **Analyze the operation of TTL NAND gate with the experimental data.**

Answer:

Condition -1 (any of the input voltage is low):

Let, V_A = 1.5 mV and V_B = 3.51V.

Now, T_1 saturates. This reduces the base voltage of T_3 to almost zero (V_2 = 26.4 mV). Therefore, T_3 cuts off, forcing T_4 to cut-off. Under these conditions T_5 acts like an emitter follower and couples a high voltage to the output; V_O = 4.08 V.

Condition -2 (both of the input voltages are high):

V_A = 4.36 V and V_B = 4.4 V.

Now, the emitters of T_1 and T_2 are reverse-biased whereas the collectors go into forward conduction. Hence T_1 and T_2 operate in the inverted mode forcing T_3 and T_4 into saturation, producing a low output (V_O = 9.4 mV). The voltage at the collector of T_3 is 0.8144V which is not sufficient to turn T_5 and D_1.

2. What are the difference of transistors T_1 & T_2 with that of a multi-emitter transistor and discuss with respect to operations?

Answer:

If T_1 and T_2 are replaced by a multi-emitter transistor, then it can easily be verified that the circuit performs the NAND operation. The output will be low in only one case: when both inputs are high. Extensions to more than two inputs can be achieved by diffusing additional emitter regions.

Although theoretically an unused input terminal in a multi-emitter transistor may be left open circuited, this is generally not a good practice. An open-circuit input terminal acts as an "antenna" that "picks up" interfering signals and thus could cause erroneous gate switching. An unused input terminal should therefore be connected to the positive power supply through a resistance. In this way, the corresponding base-emitter junction will be reverse-biased and thus will have no effect on the operation of the gate. The series resistance is included in order to limit the current in case of breakdown of the bas-emitter junction due to transients on the power supply.

But when a multi-emitter transistor is not used, the circuit can be modified according to the total no. of inputs just by adding or removing additional transistors.

3. What is totem-pole stage?

Answer:

If the collector-circuit resistor, R_C of the inverter is replaced by an active pull-up circuit containing a transistor, then the output configuration is called a totem-pole amplifier, because the transistor T_5 "sits" upon T_4. It is also referred to as a power-driver, or power-buffer, output-stage.

4. Why totem-pole stage is used in place of passive pull-up resistor?

Answer:

At the output terminal of the DTL or TTL gate there is a capacitive load $C_{L,}$ consisting of the capacitances of the reverse-biased diodes of the fan-out gates and any stray wiring capacitance. If the collector-circuit resistor of the inverter is R_C (called a passive pull-up), then, when the output stage changes from the low to the high state, the output transistor is cut-off and the capacitance charges exponentially from $V_{CE(sat)}$ to $V_{CC.}$ The time constant R_CC_L of this waveform many introduce a prohibitively long delay time into the operation of these gates.

The output delay may be reduced by decreasing R_C, but this will increase the power dissipation when the output is in its low state and the voltage across R_C is V_{CC} – $V_{CE(sat)}$. In order to minimize the power dissipation, a better solution is applied by using a totem-pole stage where an active pull-up circuit (transistor) replaces the passive pull-up element, R_C.

5. What is the function of T_3?

Answer:

The transistor T_3 acts as a phase splitter, since the emitter voltage is out-of phase with the collector phase (for an increase in base current, the emitter voltage increases and the collector voltage decreases). Thus it is used to generate two complementary voltage signals required to drive the totem-pole circuit.

6. Why resistor R_4 is used?

Answer:

If the resistance R_4 were omitted, there would result a faster change un output from V(0) to V(1). However R_4 is needed to limit the current spikes during the turn-on and turn-off transients.

7. Why diode D_1 is used in the circuit?

Answer:

Without diode D_1 in the circuit, T_5 would conduct slightly when the output is low. To prevent this, the diode is inserted; its voltage drop keeps the base-emitter junction of T_5 reverse-biased. In this way, only T_4 conducts when the output is low.

8. Why two totem-pole gates cannot be WIRED-AND?

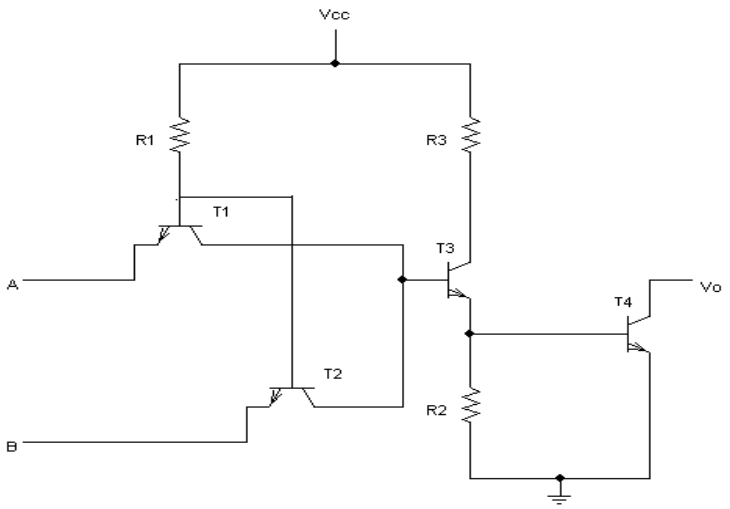
Answer:

If the output from one gate is high while that from a second gate is low, and if these two outputs are tied together, then this situation results in a transient current spikes. Hence if, the WIRED-AND were used, the power supply would deliver a steady current of 41mA under these circumstances.

This is why, two totem-pole gates should not WIRED-AND.

9. What do you mean by open collector gates?

Answer:



Circuit: Open-collector gate

Instead of a totem-pole output, some TTL devices have an *open-collector* output. This means they use only the lower transistor of a totem-pole pair. Because the collector of T_4 is open. A gate like this won't work properly until an external pull-up resistor is connected.

The output of open-collector gates can be wired together and connected to a common pull-up resistor. This is known as WIRE-AND. The big disadvantage of a open-collector gates is their slow switching speed.

10. What are the features and advantages of TTL gates?

Answer:

- TTL uses transistors almost exclusively; it has become the most popular family of SSI and MSI chips. It is the transistor which gives TTL the highest speed of any saturated logic.
- A standard TTL has a power dissipation of about 10 mW. It may vary from this value because of signal levels, tolerances, etc., but on the average, it's 10mW per gate.
- The propagation delay time of a TTL gate is in vicinity of 10 ns.
- The advantage of a totem-pole connection is its low output impedance.

Discussions :

1) The transistor Q2 acts as a phase splitter, since the emitter voltage is out of phase with the collector voltage.

2) The transistor Q4 is referred as a power-driver, or power power-buffer, output stage.

3) The configuration is called totem-pole amplifier because the transistor Q4 sits upon Q3.