OBJECTIVE:

The main objective of this experiment is to study and observe the operation of ECL OR / NOR gate.

CIRCUIT DIAGRAM:

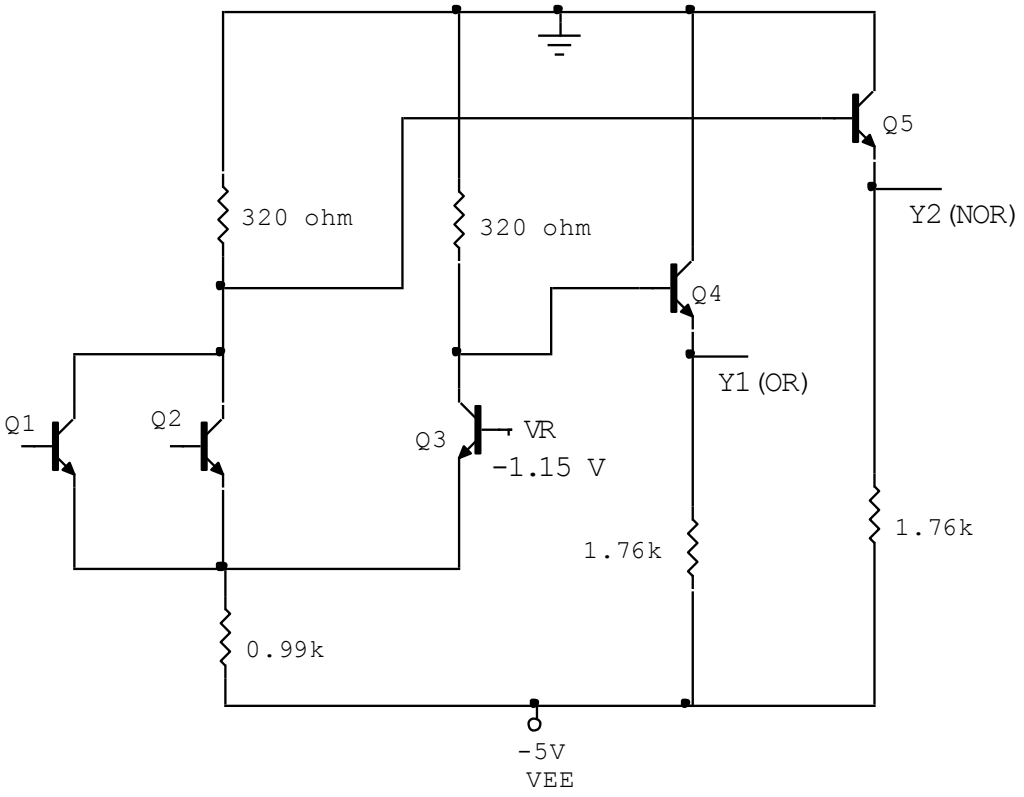

figure: ECL OR/NOR gate

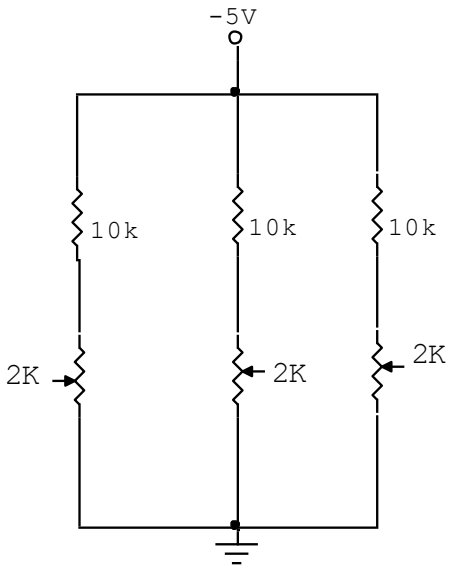

figure: Voltage divider circuit

1. Analyze the operation of ECL or/nor gate with the experimental data.
Answer:

In the experiment V(0) = -1.55 V, and V(1) = - 0.75 V. We find that in case of OR gate, the output was -1.653 V (= V(0)), when two inputs were at V(0) level. And in all other cases the output was at V(1) level.

In case of NOR gate the output was - 0.627 V (=V(1)), when two inputs were at V(0) level. In all other input combinations, the output was at V(0) level.

2. What are the purposes of emitter followers in the ECL circuit?
Answer:

Emitter followers are used at the outputs to provide a proper dc level shift. They also provide buffering and low impedance at the output terminals.

3. What are the advantages and disadvantages of ECL gates?
Answer:

Advantages:

- Outputs can be tied together to give implied OR function. So same gate can be used for either OR or NOR operation which very few gates can perform.
- It is highly speedy because its transistors don't operate in saturation region so storage time here is almost eliminated.
- Complemented output can be achieved at the same time.
- It is less temperature sensitive.
- Current swing spikes are not available in the power supply.

Disadvantages:

- As voltage difference is very low between logic levels so noise margin is low.
- Capacitive loading limits the fan-out.
- Power dissipation is quite high.
- Level shifters are required to interface with other families.

4. Why ECL is the fastest of all the logic gates?
Answer:

Since in ECL neither transistor is allowed to go into saturation, so here storage time for saturated charge is eliminated and hence ECL switches from one stage to another pretty quickly. For this reason ECL gate is the fastest of all the logic families. Since here transistors don't operate in saturation region, a propagation delay of 0.5 ns per gate is possible.

5. Calculate the noise margins.
Answer:

□ When all inputs are at V(0) = – 1.55 V then, input transistor's emitter-base voltage

$$V_{BE} = V_B - V_E$$
$$= -1.55 - (-1.836) = 0.286 \text{ V}$$

So a +ve spike of (0.5 – 0.286) = 0.214 V will cause the gates to malfunction.

□ If one input is at V(0), and the other is at V(1), then

$$V_{BE3} = V_{B3} - V_{E3}$$
$$= -1.15 - (-1.376) = 0.226 \text{ V}$$

So a –ve spike of (0.5 – 0.226) = 0.274 V will cause the gates to malfunction.

Hence,

NM(0) = 286 mV
NM(1) = 274 mV

DISCUSSION:

1. ECL is sometimes called difference amplifier because; the output is proportional to the difference between the two input voltages.
2. Since the input resistance is very high and the output resistance is very low, a large fan-out is possible at low frequency.
3. Noise margins are very low for this circuit.
4. We were not able to get –1.15 V, and – 0.75 V from the trainer board. So we made the voltage divider circuit, and get the desired voltage.