Md Abu Shayem

a.shayem44@gmail.com | www.linkedin.com/in/md-abu-shayem-a520b4198

+8801797496098 | Address: 450/1, Makki Masjid Road, Rampura, Dhaka-1219

Career Objective

I am a diligent and detail-oriented individual with a passion for continuous learning and growth. As an aspiring engineer, I am eager to expand my knowledge, gain valuable experience, and embrace new challenges within the dynamic semiconductor industry. My objective is to establish a successful career in semiconductor technology, leveraging my dedication, academic achievements, practical expertise, and integrity to excel in this innovative field.

Education

East West University, Dhaka, Bangladesh — CGPA: 3.86/4.00
Bachelor of Electrical and Electronic Engineering, Major in Electronics — *Jan. 2019 – Jan 2023*

Shah Neamatullah College, Chapai Nawabganj — GPA: 3.67/5.00
Higher Secondary School Certificate — *Aug. 2016 – May 2018*

Experience

Graduate Teaching Assistant — June 2023 – May 2024
Dept of Electrical & Electronic Engineering, East West University — *Dhaka, Bangladesh*

Assigned Courses: Embedded Systems, C Programming, and Electronic Circuits 1

Roles:

- Tutoring students to resolve course related issues
- Assisting the faculty member to conduct lab sessions
- Assist to check assignments, class works and lab reports

Technical Skills

EDA Tools:

- Cadence Design Suite, MPLAB, Xilinx ISE, Quartus II
- TCAD : Silvaco, Atlas, Athena, DevEdit, Tonyplot
- Others : MS Office, Proteus, Pspice, VLSI, etc.

Programming & Scripting Languages: Verilog, C, Embedded C, MATLAB

Operating Systems: Linux, Windows

Strong Suits

- Work under pressure
- Dedicated
- Strong work ethics
- Team worker
- Multitask ability

Relevant Academic Courses

Basic Electrical and Electronic Circuits, Computer Programming, Digital Logic Design, VLSI Circuits and Systems, Semiconductor Processing and Fabrication, Embedded Systems, Digital Signal Processing, etc.

Key Academic Projects

4 Bit Adder/Subtracter Using 1 Bit Full Adder. :

- Tools : Xilinx ISE
- Description : The Verilog code for a 1-bit full adder has been written, and using this module, a 4-bit adder/subtractor has been developed. If the user presses a key, the module will work as a subtractor; otherwise, it will work as an adder.

Design a 2 to 1 Mux using Verilog HDL and verify the design using Cadence CAD system.:

- Tools : Cadence: Incisive Enterprise Simulator
- Description : A 2 to 1 Mux has been designed using Verilog HDL and perform Compilation, Elaboration and Simulation. Also examine the design in graphical mode.

Design of a nMOS device in SILVACO platform and simulation of its characteristics :

- Tools : SILVACO: ATLAS
- Description :In this work, a nMOS device was designed and characterized using the ATLAS device simulation tool. Extracted different IV characteristics for different Gate voltage and compare the results with ideal plot of the nMOS.

Braille Display for Functionally Blind People:

- Tools : Fusion 360, Proteus, Arduino IDE
- Description : It is a cost effective, light weight and motor actuated 32 cells braille display. Instructor or parents can choose any text document from their smart phone to display as braille in the device, which will be done by android mobile app. Two IR sensor is placed in start and end position of the line, respectively..When student will start reading and reached to the end of the line, the display will be automatically refreshed for the second line by sensing the hand position.

Create A Web page using PIC18f87k22 and ESP8266.:

- Tools : Proteus, MPLAB
- Description : In this project, PIC18f87k22 MCU and ESP8266 Wi-Fi module are used. HTML and CSS code for the Web page is stored in the MCU and MCU communicate with ESP8266 using AT command. By accessing the IP address provided by ESP, user can access the web page and take necessary actions, e.g. turn ON/OFF LEDs or see live sensor data etc.

Password Based Locker System:

- Tools : Proteus, MPLAB
- Description : In this project, PIC16f690 MCU is used . User can set a 4 bit password and can change any time. In case of changing password, system will ask for old one and after verifying, it will take the new password and store in EEPROM by erasing old one. User should provide password within 15 seconds (for unlock or change) otherwise system will reset the options and ask again. The system will be unlocked for 20 seconds. To count the time, I have used Timer1 module with Pre-Scaler 4.

Achievements

- Finalist of "VLSI Design Competition 2022" organized by BUET and Neural Semiconductor Limited (NSL)
- Dean's List Scholarship-2020 - 2022 (East West University)

Extracurricular Activities

- Attended Several Workshops and Seminars on VLSI Technology
- Organizing panel member of "Prospective of VLSI Design in Bangladesh & Introduction to Analog Circuit Design with NSL" workshop
- Vice-Chairperson of IEEE Women in Engineering (WIE) Student Branch Chapter of EWU (2022-2023)
- Lead Volunteer of IEEE East West University Student Branch (2021-2022)
- Instructor of "Workshop on Proteus " organized by East West University Electronics Club

References

- **Dr. Muhammed Mazharul Islam**
  Assistant Professor, Dept of EEE, East West University
  E-mail: mmai@ewubd.edu

Dr. Mohammad Mojammel Al Hakim
Professor, Dept of EEE, East West University
E-mail: dmmah@ewubd.edu