

D

Title		
Size	Number	Revision
A4		
Date:	2019/10/10	Sheet of
File:	D:\work\..\Cortex-M Jtag.SchDoc	Drawn By:

1

2

3

4

A

A

B

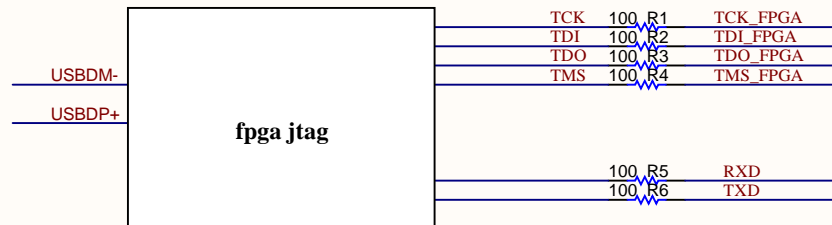
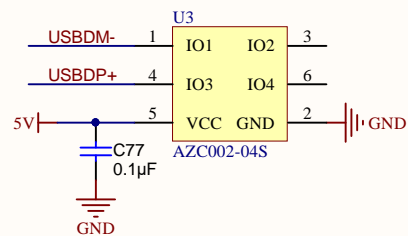
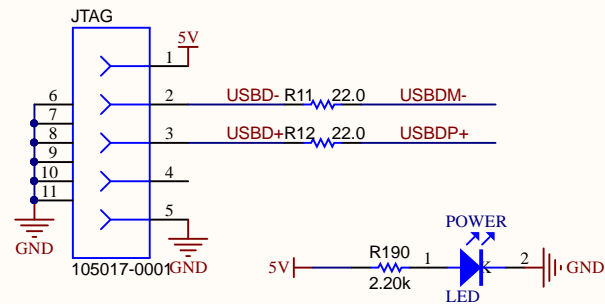
B

C

C

D

D



Title			
Size	Number		Revision
A4			
Date:	2019/10/10		Sheet of
File:	D:\work\...\FPGA Jtag & Uart.SchDoc		Drawn By:

1

2

3

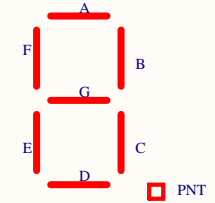
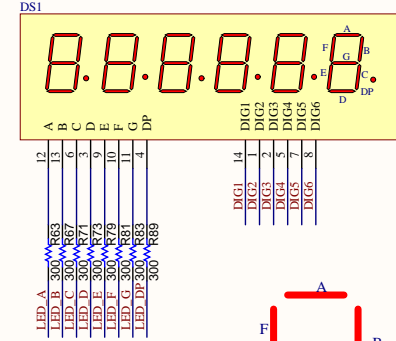
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SW

VGA

六位共阴数码管

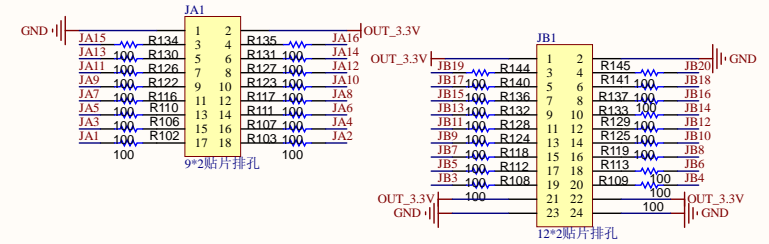
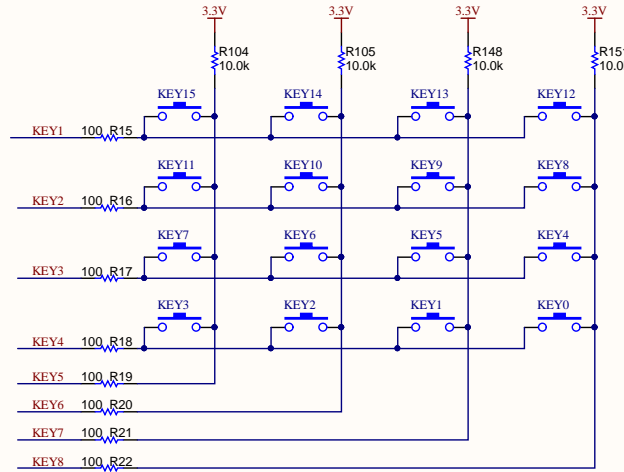
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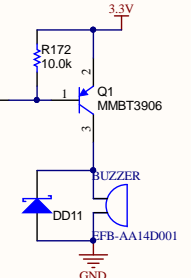
KEY

对外IO

LED

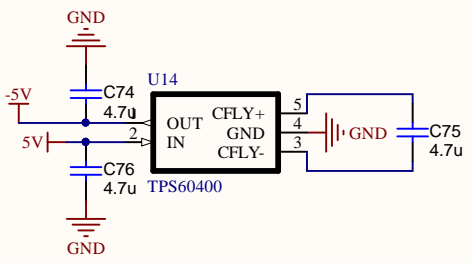
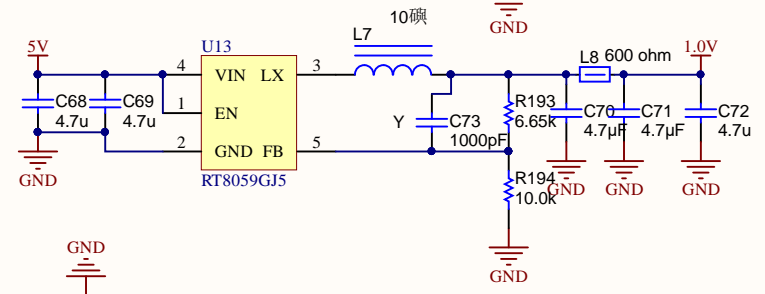
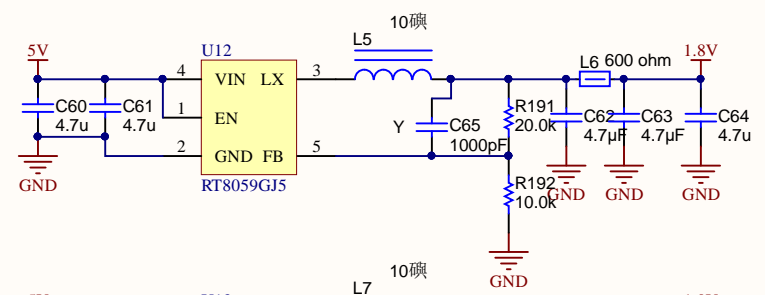
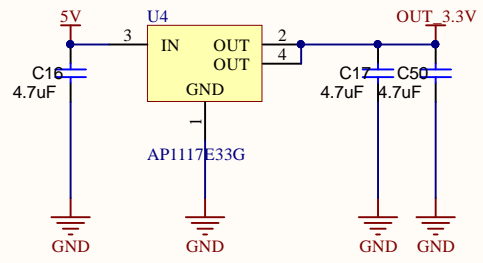
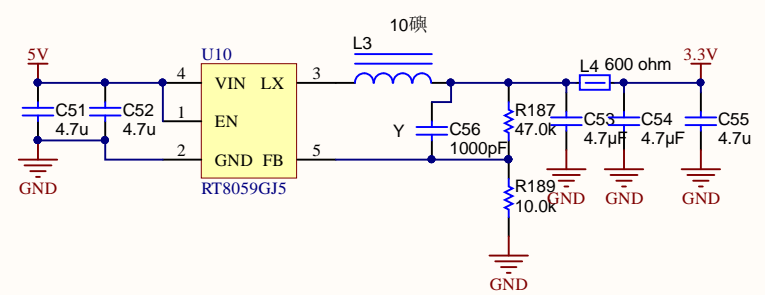


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Title		
Size	Number	Revision
A3		
Date:	2019/10/10	Sheet of
File:	D:\work\IO.SchDoc	Drawn By:

USB/Power



Title		
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A4		
Date:	2019/10/10	Sheet of
File:	D:\work\...\Power.SchDoc	Drawn By: