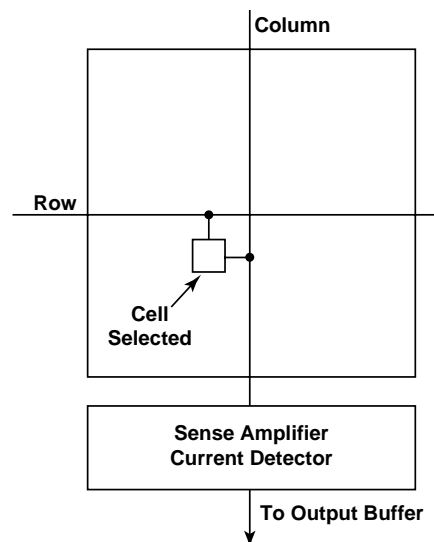# 9 ROM, EPROM, AND EEPROM TECHNOLOGY

## OVERVIEW

Read only memory devices are a special case of memory where, in normal system operation, the memory is read but not changed. Read only memories are non-volatile, that is, stored information is retained when the power is removed. The main read only memory devices are listed below:

ROM (Mask Programmable ROM—also called "MROMs")
EPROM (UV Erasable Programmable ROM)
OTP (One Time Programmable EPROM)
EEPROM (Electrically Erasable and Programmable ROM)
Flash Memory - This device is covered in Section 10.

## HOW THE DEVICE WORKS

The read only memory cell usually consists of a single transistor (ROM and EPROM cells consist of one transistor, EEPROM cells consist of one, one-and-a-half, or two transistors). The threshold voltage of the transistor determines whether it is a "1" or "0." During the read cycle, a voltage is placed on the gate of the cell. Depending on the programmed threshold voltage, the transistor will or will not drive a current. The sense amplifier will transform this current, or lack of current, into a "1" or "0." Figure 9-1 shows the basic principle of how a Read Only Memory works.



Source: ICE, "Memory 1997"    19956

**Figure 9-1. Read Only Memory Schematic**

**MASK PROGRAMMABLE ROMs**

Mask programmable read-only memories (ROMs) are the least expensive type of solid state memory.  They are primarily used for storing video game software and fixed data for electronic equipment, such as fonts for laser printers, dictionary data in word processors, and sound data in electronic musical instruments.

ROM programming is performed during IC fabrication.  Several process methods can be used to program a ROM.  These include

- Metal contact to connect a transistor to the bit line.
- Channel implant to create either an enhancement-mode transistor or a depletion-mode transistor.
- Thin or thick gate oxide, which creates either a standard transistor or a high threshold transistor, respectively.

The choice of these is a trade-off between process complexity, chip size, and manufacturing cycle time.  A ROM programmed at the metal contact level will have the shortest manufacturing cycle time, as metallization is one of the last process steps.  However, the size of the cell will be larger.
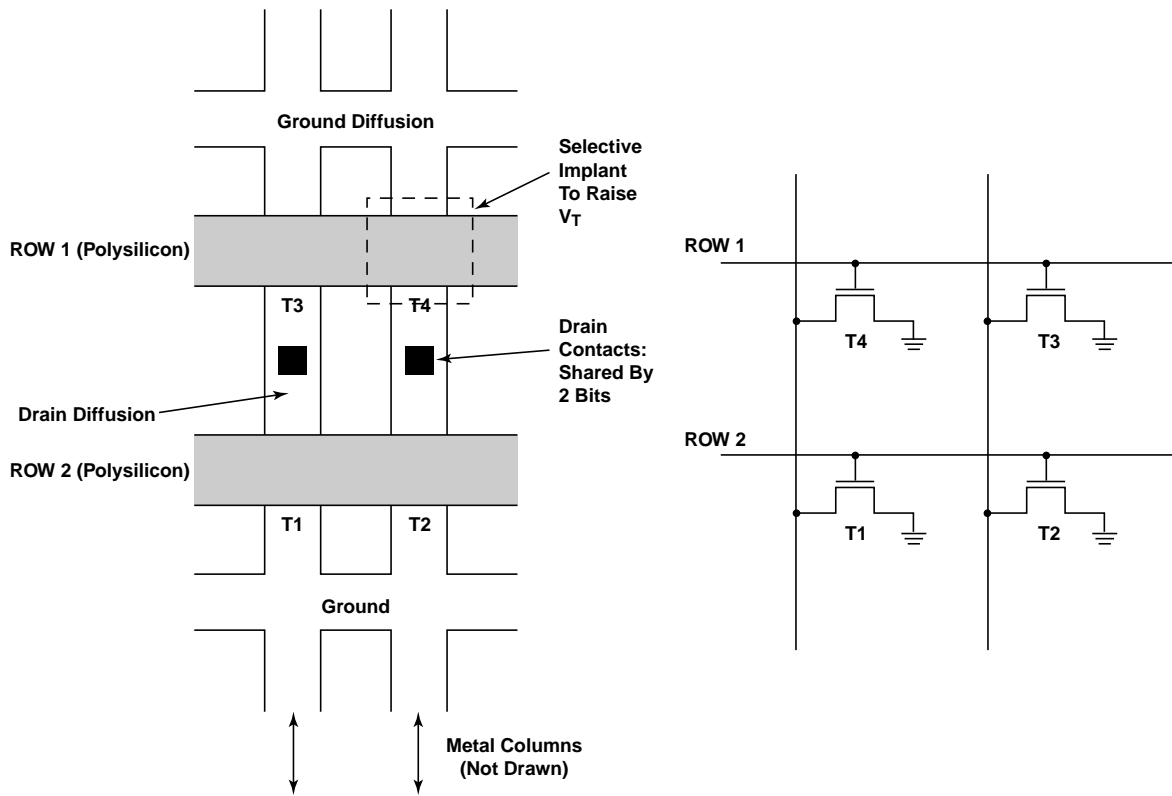
Figure 9-2 shows a ROM array programmed by channel implant. The transistor cell will have either a normal threshold  (enhancement-mode device) or a very high threshold (higher than $V_{CC}$ to assure the transistor will always be off).  The cell array architecture is NOR.  The different types of ROM architectures (NOR, NAND, etc.) are detailed in the flash memory section (Section 10) as they use the same principle.

Figure 9-3 shows an array of storage cells (NAND architecture).  This array consists of single transistors noted as devices 1 through 8 and 11 through 18 that is programmed with either a normal threshold (enhancement-mode device) or a negative threshold (depletion-mode device).

**ROM Cell Size and Die Size**

The cell size for the ROM is potentially the smallest of any type of memory device, as it is a single transistor.  A typical 8Mbit ROM would have a cell size of about $4.5\mu m^2$ for a $0.7\mu m$ feature size process, and a chip area of about $76mm^2$.  An announced 64Mbit ROM, manufactured with a $0.6\mu m$ feature size, has a $1.23\mu m^2$ cell on a $200mm^2$ die.
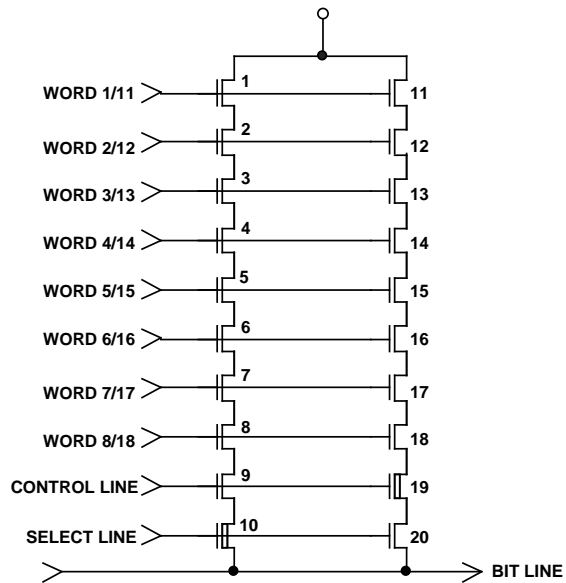
The ROM process is the simplest of all memory processes, usually requiring only one layer of polysilicon and one layer of metal.  There are no special film deposition or etch requirements, so yields are the highest among all the equivalent-density memory chips.

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**Ground Diffusion**

**Selective Implant To Raise V$_T$**

**ROW 1 (Polysilicon)**

**T3**    **T4**

**Drain Contacts: Shared By 2 Bits**

**Drain Diffusion**

**ROW 2 (Polysilicon)**

**T1**    **T2**

**Ground**

**Metal Columns (Not Drawn)**

**ROW 1**

**T4**    **T3**

**ROW 2**

**T1**    **T2**

*Source: ICE, "Memory 1997"*    20845

**Figure 9-2.  ROM Programmed by Channel Implant**

WORD 1/11    1    11
WORD 2/12    2    12
WORD 3/13    3    13
WORD 4/14    4    14
WORD 5/15    5    15
WORD 6/16    6    16
WORD 7/17    7    17
WORD 8/18    8    18
CONTROL LINE    9    19
SELECT LINE    10    20
BIT LINE

*Source: ICE, "Memory 1997"*    19050

**Figure 9-3.  Memory Cell Schematic**

### Multimedia Card

In 1996, Siemens announced the introduction of a new solid-state memory chip technology that enables the creation of a multimedia card that is sized 37mm x 45mm x 1.4mm, or roughly 40 percent the size of a credit card. It is offered with either 16Mbit or 64Mbit of ROM.

### EPROM

EPROM (UV Erasable Programmable Read Only Memory) is a special type of ROM that is programmed electrically and yet is erasable under UV light.

The EPROM device is programmed by forcing an electrical charge on a small piece of polysilicon material (called the floating gate) located in the memory cell. When this charge is present on this gate, the cell is "programmed," usually a logic "0," and when this charge is not present, it is a logic "1." Figure 9-4 shows the cell used in a typical EPROM. The floating gate is where the electrical charge is stored.



Source: Intel/ICE, "Memory 1997"                                                                 18474
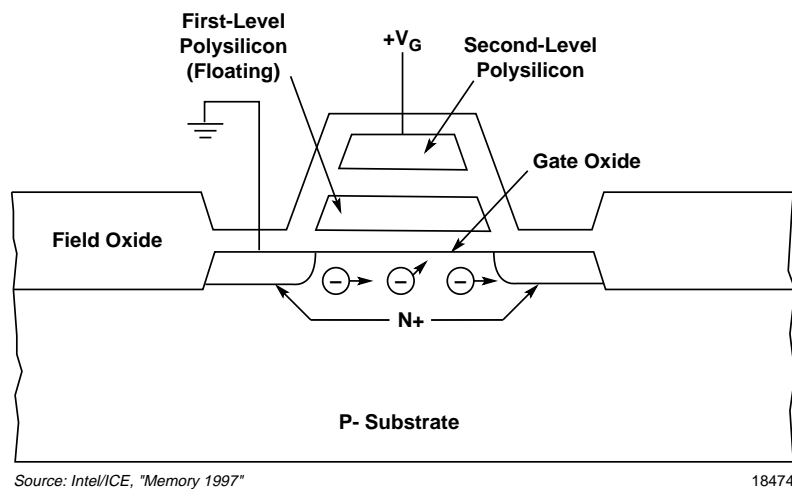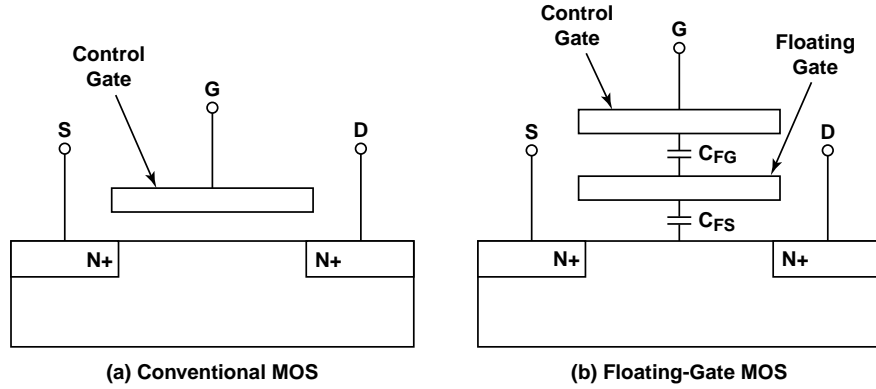
**Figure 9-4. Double-Poly Structure (EPROM/Flash Memory Cell)**

Prior to being programmed, an EPROM has to be erased. To erase the EPROM, it is exposed to an ultraviolet light for approximately 20 minutes through a quartz window in its ceramic package. After erasure, new information can be programmed to the EPROM. After writing the data to the EPROM, an opaque label has to be placed over the quartz window to prevent accidental erasure.

Programming is accomplished through a phenomenon called hot electron injection. High voltages are applied to the select gate and drain connections of the cell transistor. The select gate of the transistor is pulsed "on" causing a large drain current to flow. The large bias voltage on the gate connection attracts electrons that penetrate the thin gate oxide and are stored on the floating gate.

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**EPROM Floating Gate Transistor Characteristic Theory**

The following explanation of EPROM floating gate transistor characteristic theory also applies to EEPROM and flash devices. Figures 9-5 (a) and (b) show the cross section of a conventional MOS transistor and a floating gate transistor, respectively. The upper gate in Figure 9-5 (b) is the control gate and the lower gate, completely isolated within the gate oxide, is the floating gate.



(a) Conventional MOS    (b) Floating-Gate MOS

*Source: ICE, "Memory 1997"*                    20846

**Figure 9-5.  Cross Section of a Conventional MOS Transistor and a Floating-Gate MOS Transistor**

$C_{FG}$ and $C_{FS}$ are the capacitances between the floating gate and the control gate and substrate, respectively. $V_G$ and $V_F$ are the voltages of the control gate and the floating gate, respectively. $-Q_F$ is the charge in the floating gate. (As electrons have a negative charge, a negative sign was added). In an equilibrium state, the sum of the charges equals zero.

$$\left(V_G - V_F\right) C_{FG} + \left(0 - V_F\right) C_{FS} - Q_F = 0$$

$$V_F \left(\frac{C_{FG}}{C_{FG} + C_{FS}}\right) V_G - \frac{Q_F}{C_{FG} + C_{FS}}$$
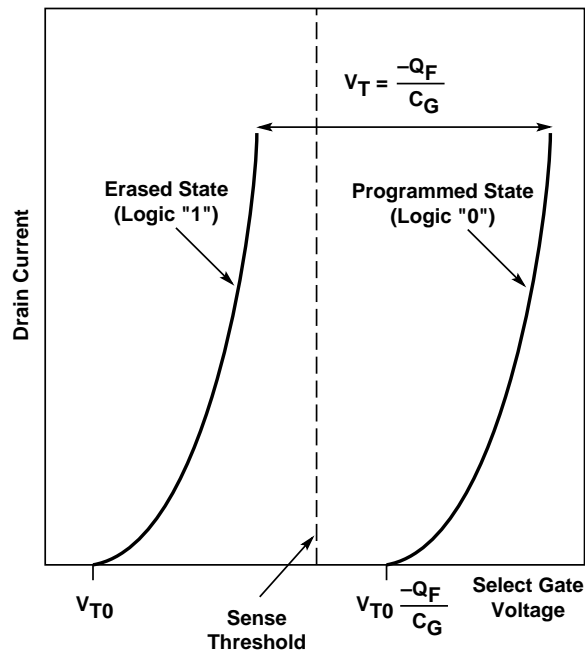
$V_{TC}$ is the threshold voltage of the conventional transistor, and $V_{TCG}$ is the threshold voltage of the floating gate transistor.

$$V_{TCG} = \left( \frac{C_{FG}}{C_{FG} + C_{FS}} \right) V_{TC} - \frac{Q_F}{C_{FG} + C_{FS}}$$

$$V_{TCG} = V_{TO} - \frac{Q_F}{C_G}$$

$$\text{Where} \quad V_{TO} = \left( \frac{C_{FG}}{C_{FG} + C_{FS}} \right) V_{TC} \quad \text{and} \quad C_G = C_{FG} + C_{FS}$$

The threshold voltage of the floating gate transistor ($V_{TCG}$) will be $V_{TO}$ (around 1V) plus a term depending on the charge trapped in the floating gate. If no electrons are in the floating gate, then $V_{TCG} = V_{TO}$ (around 1V). If electrons have been trapped in the floating gate, then $V_{TCG} = V_{TO}$ -$Q_F/C_G$ (around 8V for a 5V part). This voltage is process and design dependent. Figure 9-6 shows the threshold voltage shift of an EPROM cell before and after programming.
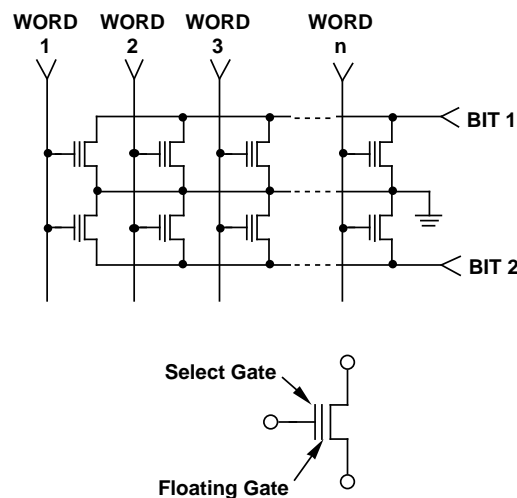


Source: ICE, "Memory 1997"  17548A

**Figure 9-6. Electrical Characteristics of an EPROM**

The programming (write cycle) of an EPROM takes several hundred milliseconds. Usually a byte—eight bits—is addressed with each write cycle. The read time is comparable to that of fast ROMs and DRAMs (i.e., several tens of nanoseconds). In those applications where programs are stored in EPROMs, the CPU can run at normal speeds.

Field programmability is the EPROM's main advantage over the ROM. It allows the user to buy mass-produced devices and program each device for a specific need. This characteristic also makes the EPROM ideal for small-volume applications, as the devices are usually programmed in very small quantities. Also, the systems supplier can program any last minute upgrades to the program just before shipment. EPROM cells may be configured in the NAND structure shown previously, or, more commonly, in the NOR configuration shown in Figure 9-7.
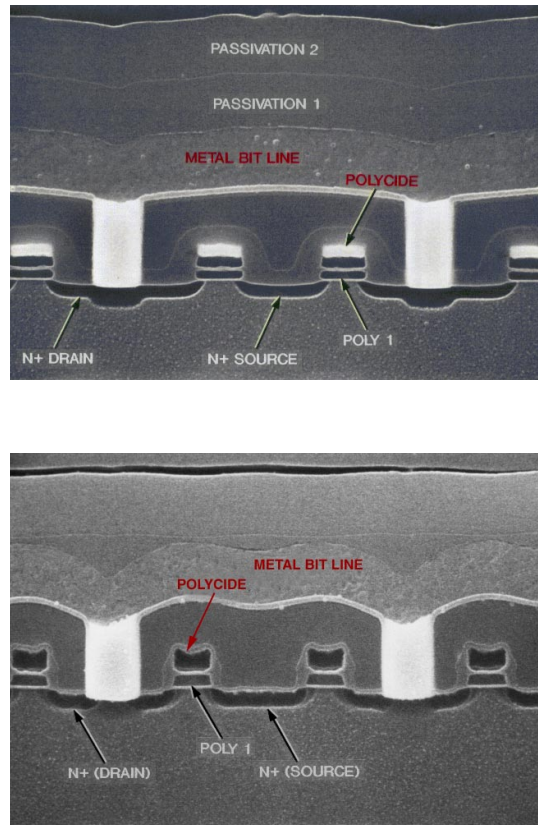


Source: ICE, "Memory 1997"                                        19051

**Figure 9-7. NOR EPROM Configuration**

EPROMs were created in the 1970s and have long been the cornerstone of the non-volatile memory market. But the development of flash memory devices (see Section 10) will lead to a loss of EPROM marketshare. EPROM uses a mature technology and design and is on the decline part of its lifecycle. For this reason there is not a lot of R&D expenditure made for EPROM devices. Figure 9-8 shows a cross section of a 1Mbit EPROM cell from two different manufacturers. The main difference between the processes is the polysilicon gate. One manufacturer uses a polycide to improve the speed.

**EPROM Cell Size and Die Size**

The cell size of the EPROM is also relatively small. The EPROM requires one additional polysilicon layer, and will usually have slightly lower yields due to the requirement for nearly perfect (and thin) gate oxides.

22462

**Figure 9-8.  Typical 1Mbit EPROM Cells**

These factors, plus the fact that an EPROM is encased in a ceramic package with a quartz window, make the EPROM average selling price three to five times the price of the mask ROM.  Figure 9-9 shows the main feature sizes of 1Mbit EPROM analyzed by ICE's laboratory.

| Manufacturer | Density | Date Code | Cell Size $(\mu m^2)$ | Die Size $(mm^2)$ | Min. Gate Length $(\mu m)$ |
|---|---|---|---|---|---|
| Atmel | 1Mbit | 9428 | 4.40 | 14.6 | 0.6 |
| AMD | 1Mbit | 9634 | 5.52 | 15.9 | 0.7 |
| ST | 1Mbit | 9514 | 3.60 | 11.5 | 0.5 |
| ISSI | 1Mbit | 94/95 | 6.80 | 18.0 | 0.7 |

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**Figure 9-9.  EPROM Feature Sizes**

**OTP (One Time Programmable) EPROM**

In most applications, EPROMs are programmed one time and will never have to be erased. To reduce the cost for these applications, EPROMs may be manufactured in opaque plastic packages since the standard ceramic package of an EPROM is expensive. EPROMs that are programmed one time for a specific use and cannot be erased are referred to as One Time Programmable (OTP) devices.

**EEPROM**

EEPROM (Electrically Erasable Programmable ROM) offer users excellent capabilities and performance. Only one external power supply is required since the high voltage for program/erase is internally generated. Write and erase operations are performed on a byte per byte basis.

The EEPROM uses the same principle as the UV-EPROM. Electrons trapped in a floating gate will modify the characteristics of the cell, and so a logic "0" or a logic "1" will be stored.

The EEPROM is the memory device that implements the fewest standards in cell design. The more common cell is composed of two transistors. The storage transistor has a floating gate (similar to the EPROM storage transistor) that will trap electrons. In addition, there is an access transistor, which is required for operations. Figure 9-10 shows the voltages applied on the memory cell to program/erase a cell. Note that an EPROM cell is erased when electrons are removed from the floating gate and that the EEPROM cell is erased when the electrons are trapped in the floating cell. To have products electrically compatible, the logic path of both types of product will give a "1" for erase state and a "0" for a programmed state. Figure 9-11 shows the electrical differences between EPROM and EEPROM cells.

**Parallel EEPROM**

There are two distinct EEPROM families: serial and parallel access. The serial access represents 90 percent of the overall EEPROM market, and parallel EEPROMs about 10 percent. Parallel devices are available in higher densities ($\geq$256Kbit), are generally faster, offer high endurance and reliability, and are found mostly in the military market. They are pin compatible with EPROMs and flash memory devices. Figure 9-12 shows feature sizes of three 1Mbit parallel EEPROM from different manufacturers, analyzed by ICE's laboratory. Figures 9-13 to 9-15 show photographs and schematics of the respective cells. It is interesting to see the wide differences in these cells.

**Serial EEPROM**

Serial EEPROMs are less dense (typically from 256 bit to 256Kbit) and are slower than parallel devices. They are much cheaper and used in more "commodity" applications.
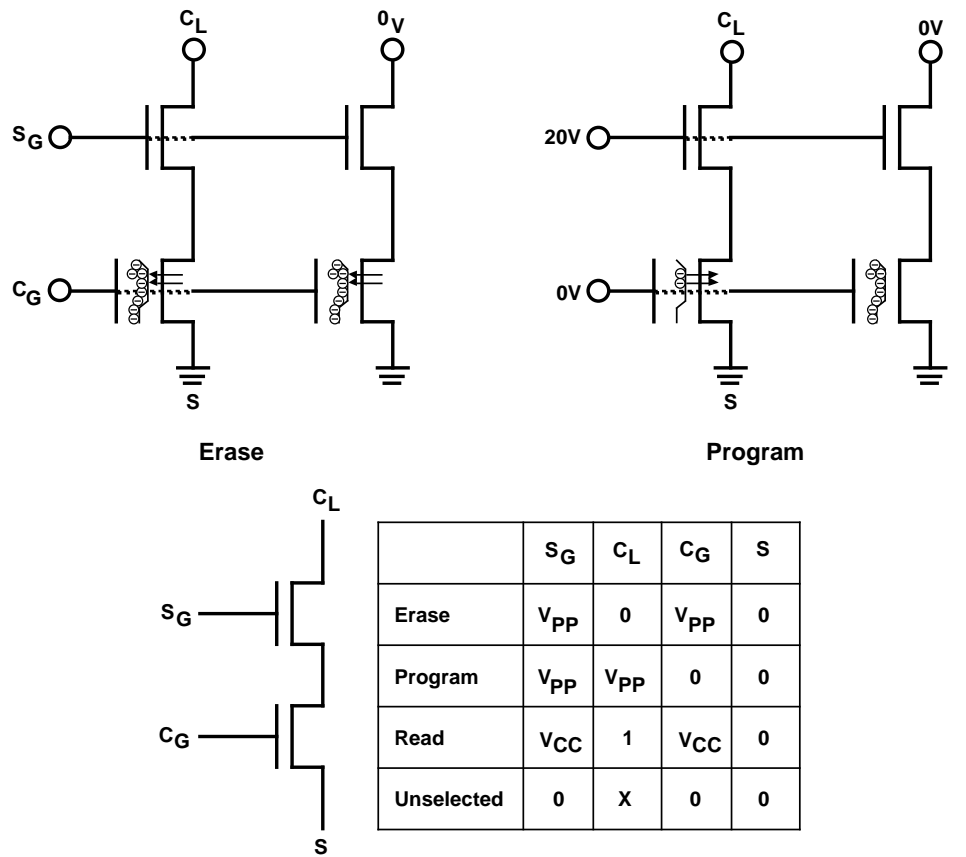
**Erase**                              **Program**

|           | $S_G$    | $C_L$    | $C_G$    | S |
|-----------|----------|----------|----------|---|
| **Erase** | $V_{PP}$ | 0        | $V_{PP}$ | 0 |
| **Program** | $V_{PP}$ | $V_{PP}$ | 0      | 0 |
| **Read**  | $V_{CC}$ | 1        | $V_{CC}$ | 0 |
| **Unselected** | 0   | X        | 0        | 0 |

*Source: ICE, "Memory 1997"*                                      17554A

**Figure 9-10.  EEPROM Cell Program/Erase**

**EPROM programming:  Hot electron**
- **High $V_{PP}$ Current**
- **High ISUB**
- **$V_{PP}$ must be an external supply**
- **No $V_{BB}$ generator**

**EEPROM programming:  Tunneling**
- **$V_{PP}$ is generated by an internal pump.**

*Source: ICE, "Memory 1997"*                      17556

**Figure 9-11.  $V_{PP}$ EPROM Versus $V_{PP}$ EEPROM**

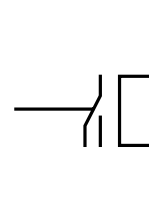| Manufacturer | Density | Date Code | Cell Size ($\mu m^2$) | Die Size ($mm^2$) | Min Gate Length ($\mu m$) |
|---|---|---|---|---|---|
| Winbond | 1Mbit | 9432 | 7.8 | 22.6 | 0.9 |
| Xicor | 1Mbit | 9443 | 21.0 | 51.0 | 1.3 |
| Hitachi | 1Mbit | 94/95 | 22.5 | 51.0 | 0.6 |

*Source: ICE, "Memory 1997"*                          22463

**Figure 9-12.  1Mbit Parallel EEPROM Feature Sizes**



*Source: ICE, "Memory 1997"*                          22468

**Figure 9-13.  Winbond 1Mbit EEPROM Cell**

Serial access EEPROMs feature low pin count.  Typically they are packaged in an 8-pin package.  As illustrated in Figure 9-16, Xicor's 128Kbit serial EEPROM uses the 8 pins in the following manner:

- $V_{CC}$ and $V_{SS}$ for supply voltage
- SCL (Serial Clock) to clock the data
- SDA (Serial Data) is a bi-directional pin used to transfer data into and out of the device
- S0, S1, S2 are select inputs used to set the first three bits of the 8-bit slave address
- WP (Write Protection) controls Write Protection features.

Serial EEPROMs use data transfer interface protocols for embedded control applications.  These protocols include the Microwave bus, the $I^2C$ bus, the $XI^2C$ (Extended $I^2C$) or the SPI (Serial Peripheral Interface) bus interfaces.

There continues to be an ongoing effort to reduce the size of serial EEPROMs. Microchip Technology, for example, introduced a 128bit serial EEPROM in a five-lead SOT-23 package.
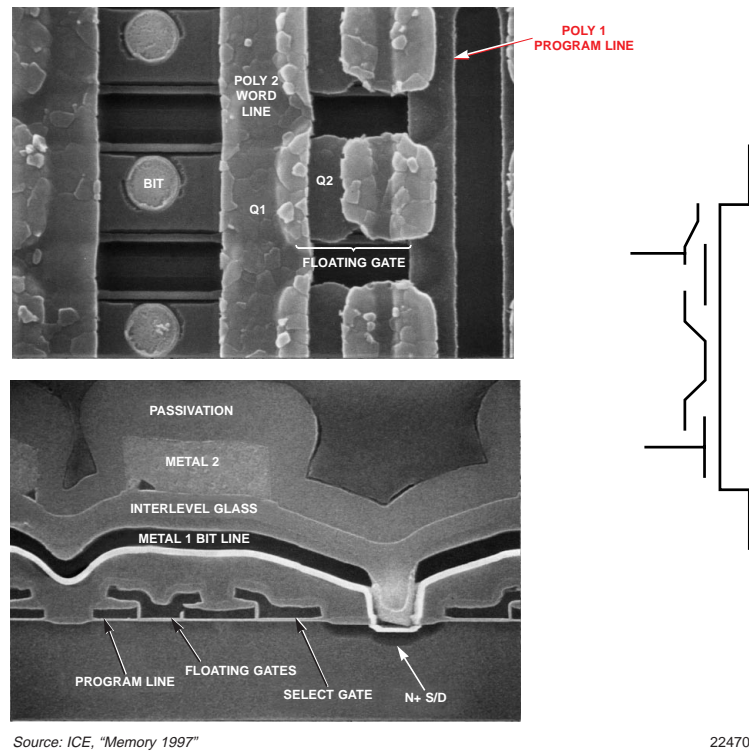
Source: ICE, "Memory 1997"                          22470

**Figure 9-14.  Xicor 1Mbit EEPROM Cell**



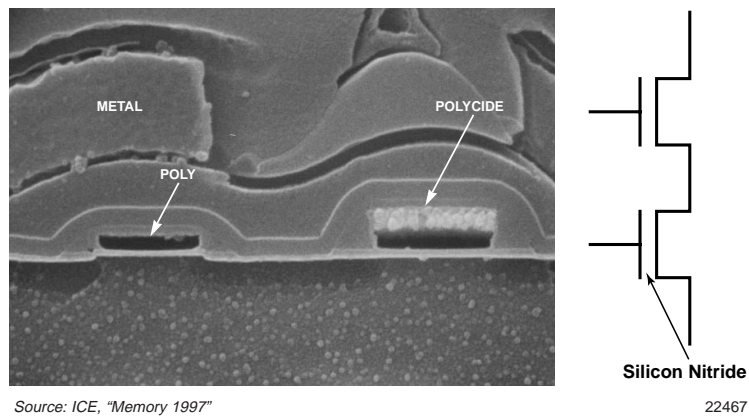Source: ICE, "Memory 1997"                          22467

**Figure 9-15.  Hitachi 1Mbit EEPROM Cell**

Figure 9-17 shows feature sizes of three serial EEPROMs from different manufacturers that were analyzed by ICE's laboratory.  Note that larger cell sizes accompany low-density EEPROM devices.  When building an EEPROM chip that contains sense amplifiers, controllers, and other peripheral circuitry, cell size is not as great a factor at low (1Kbit, 2Kbit) densities.  At larger densities, the size of the cell array is more critical.  It becomes a larger portion of the chip.  Therefore, greater consideration must be given to the size of the cell.
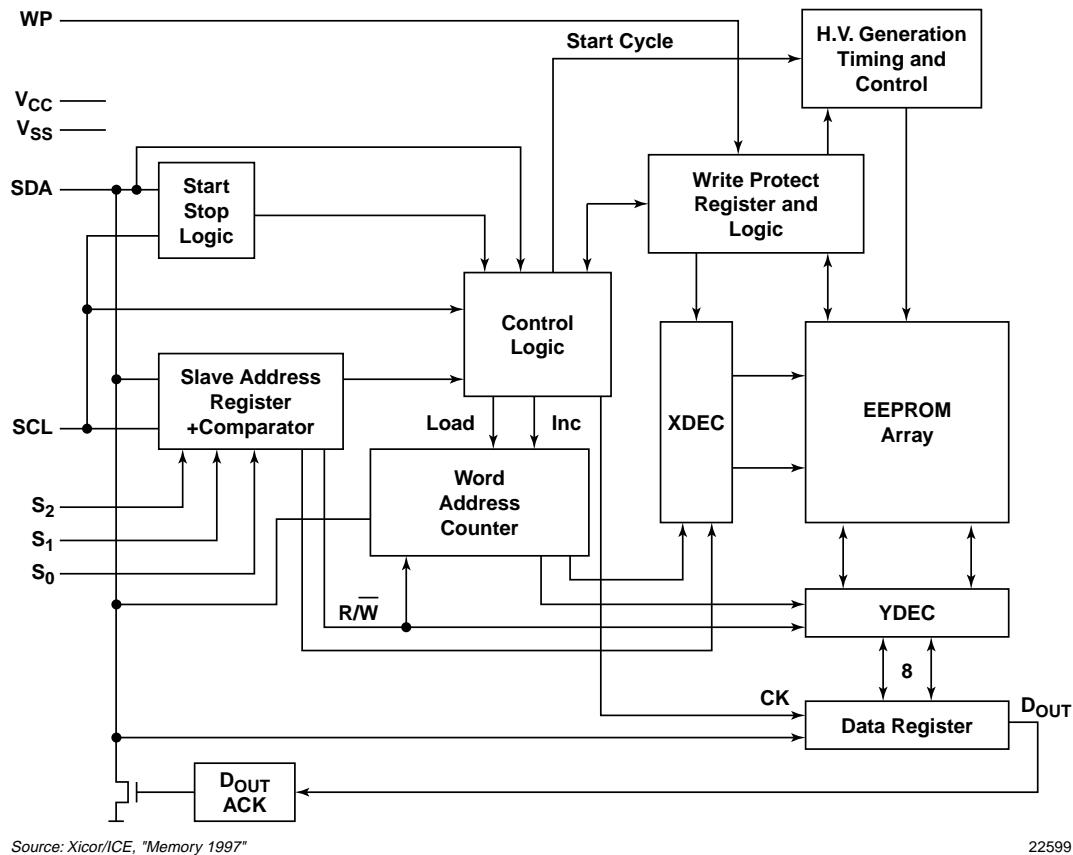
22599

**Figure 9-16.  Xicor 128Kbit Serial EEPROM Functional Diagram**

| Manufacturer | Density | Date Code | Cell Size ($\mu$m$^2$) | Die Size (mm$^2$) | Min Gate Length ($\mu$m) |
|:---:|:---:|:---:|:---:|:---:|:---:|
| Microchip | 16K | 9540 | 60.5 | 6.0 | 2.0 |
| Xicor | 2K | 9432 | 100.0 | 4.0 | 2.0 |
| ST | 1K | 9618 | 286.0 | 2.6 | 1.2 |

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**Figure 9-17.  EEPROM Serial Configuration Feature Sizes**

This size impact is illustrated in Figure 9-18 using a 1Kbit serial EEPROM example from SGS-Thomson.  The cell array represents only 11 percent of the total surface of the chip.

Figures 9-19 and 9-20 show additional EEPROM cells.  As noted, there is no design standard for this type of cell.  In laying out the EEPROM cell, the designer must take into consideration the elements of size, performance, and process complexity.
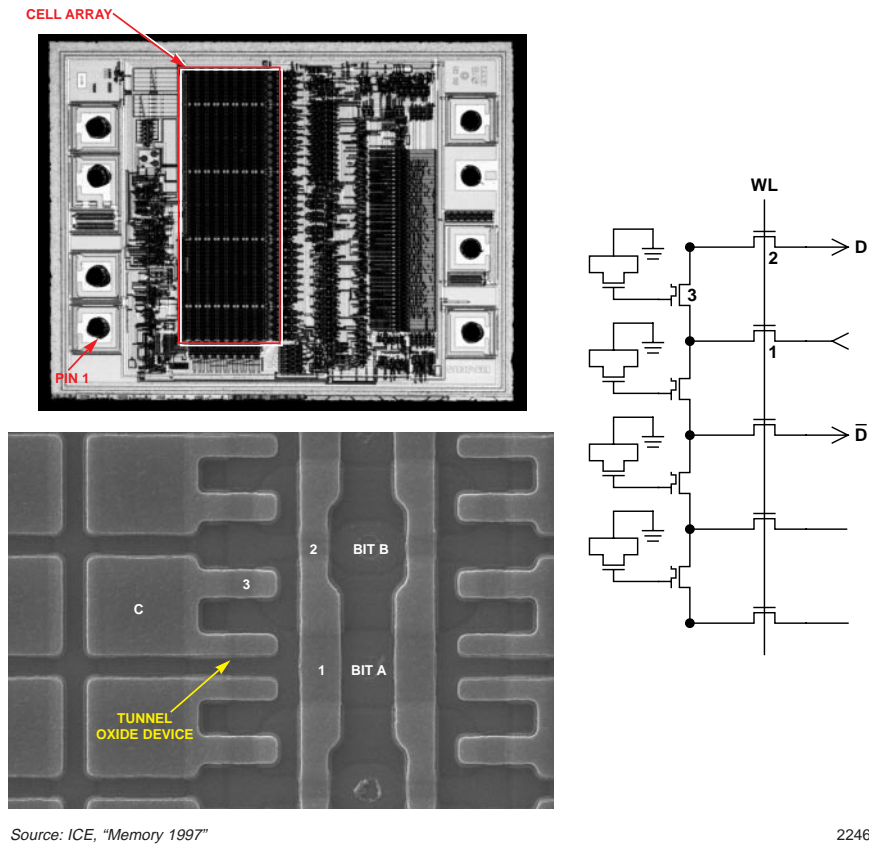
22465

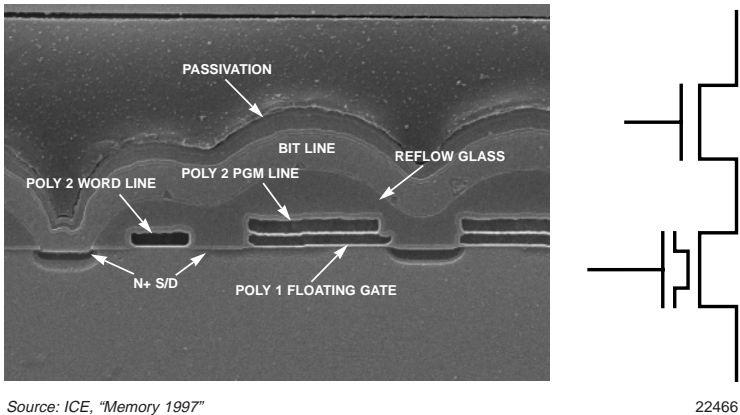**Figure 9-18.  SGS-Thomson 1Kbit Serial EEPROM**



22466

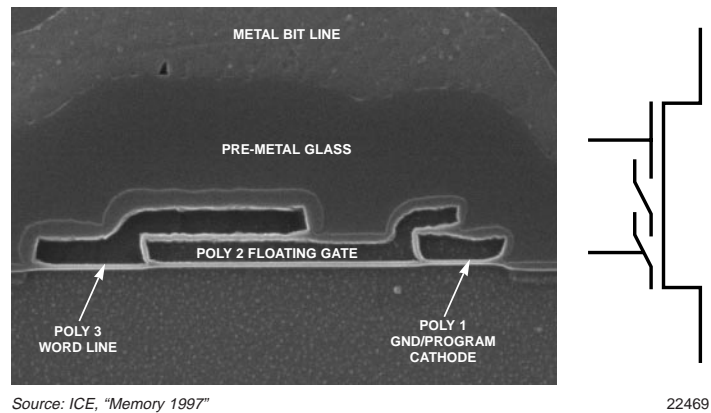**Figure 9-19.  Microchip 16Kbit Serial EEPROM Cell**

22469

Figure 9-20.  Xicor 2Kbit Serial EEPROM Cell

Multi-Level Analog Storage EEPROM

The goal of multi-level cell (MLC) is to store more than one bit of information in a single cell. Much work has already been done regarding MLC as applied to flash memory devices.  The typical development for digital flash memories is to store four different levels in the same cell, and thus divide the number of cells by two (four data are given by two bits : 00, 01, 10, and 11).

However, for several years now, Information Storage Devices (ISD), a San Jose based company, has proposed multi-level analog storage EEPROMs for analog storage.  ISD presented a 480Kbit EEPROM at the 1996 ISSCC conference.  The multi-level storage cell is able to store 256 different levels of charge between 0V and 2V. This means the cell needs to have a 7.5mV resolution.  The 256 different levels in one cell corresponds to eight bits of information.  A comparable digital implementation requires 3.84Mbit memory elements to store the same amount of information. The information stored will not be 100 percent accurate but is good enough for audio applications, which allows some errors.