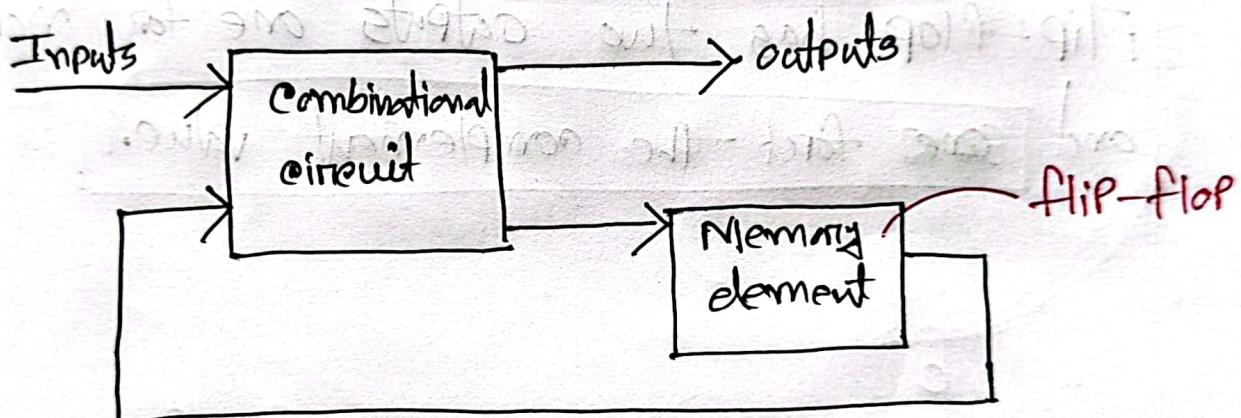


Chap-6

A sequential circuit is a logical circuit, where the output depends on the present value of the input as well as the sequence of past inputs/outputs.

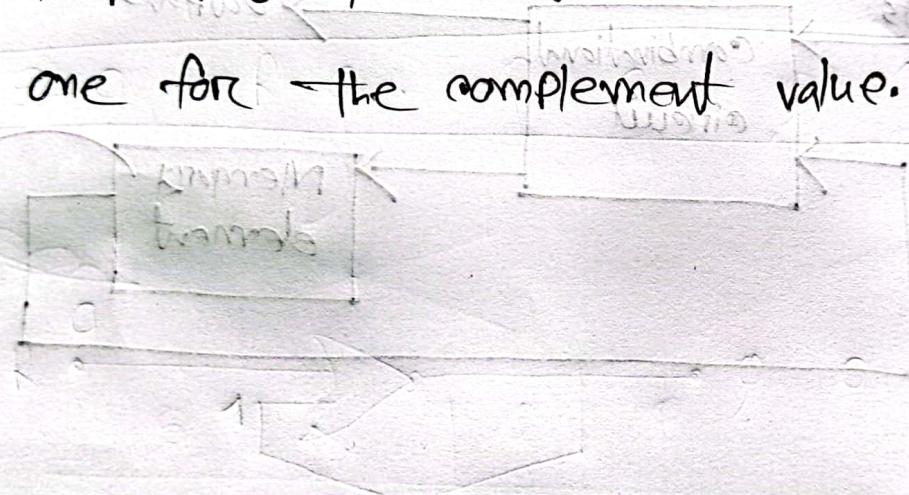


Asynchronous	Synchronous
O/P changes at any time. There is no clock	O/P changes only for clock pulse
Latches - use	Flip-flop - use

Flip-flop are memory elements used in the sequential circuit. They can store one bit of information.

Flip-flop maintain ~~the~~ a state until directed by input to change the state.

Flip-flop has two outputs one for normal values and one for the complement value.



Set	Reset
1	0
0	1
0	0



④ Sequential circuit
 यह output previous
 state को लेता है

SR Latch

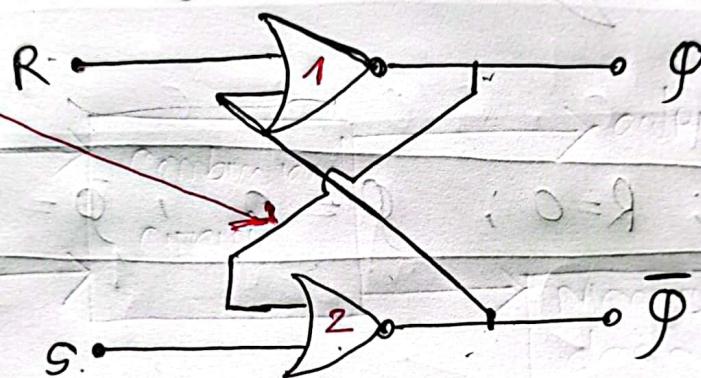
Dinied coupled RS flip-flop

depend The basic storage element is called Latch.

परंतु

As the name suggests it latches "0" or "1".

$$R = \text{Reset} ; S = \text{Set} \Rightarrow Q = 1 \\ \Rightarrow P = 0$$

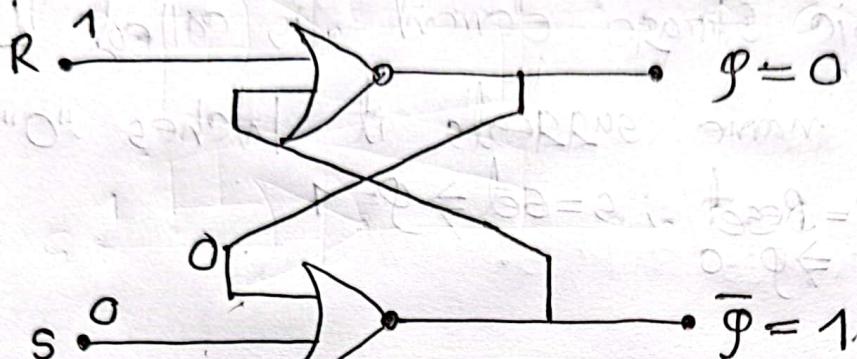
T.T for NOR-gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Input 1 - इसके output 0

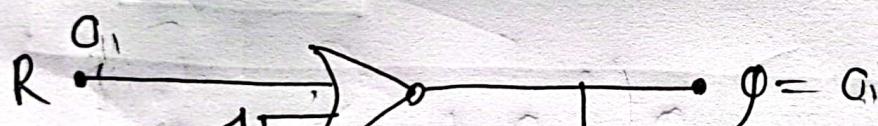


Case 1: $S=0, R=1, \varphi=0, \bar{\varphi}=1$

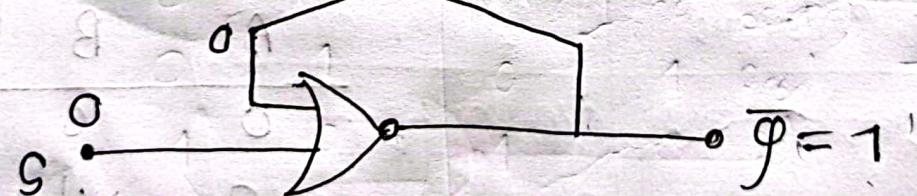


At is reset state. Cz $\varphi = 0$

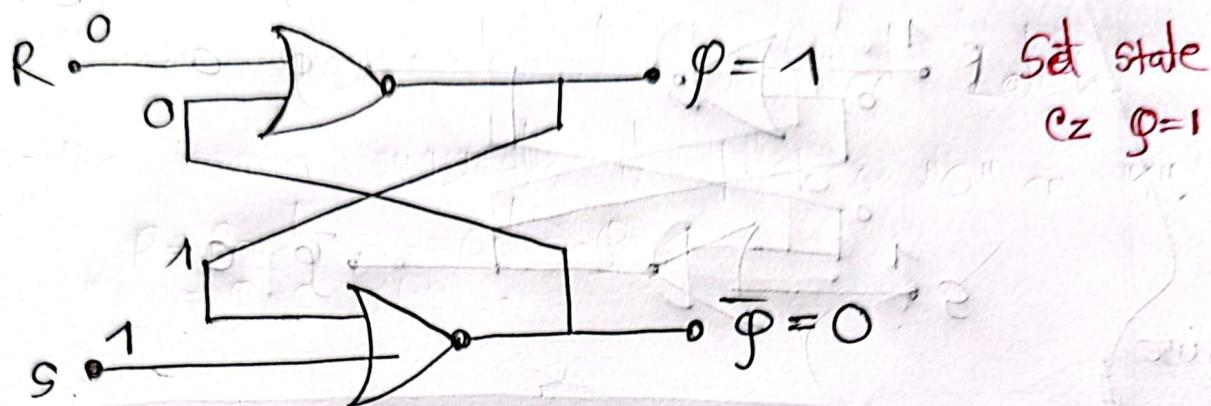
$S=0 ; R=0 ; \varphi=0 ; \bar{\varphi}=1$ memory



Previous state

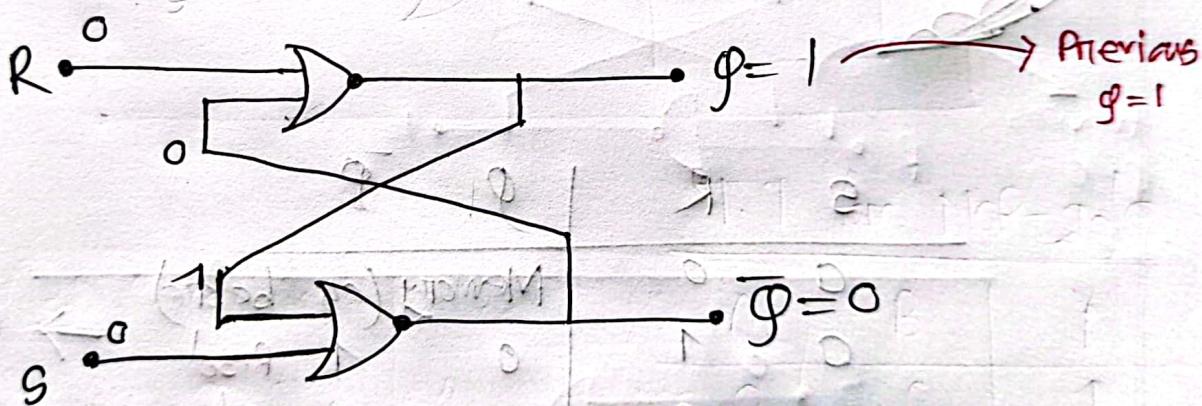


Case 2: $S=1, R=0, Q=1; \bar{Q}=0$



*$S=1$ প্রয়োজন এবং
কাউন্ট করা
করা হলে উদ্বিধ
input 1 হলে output
0 হবে, সুতরাং $\bar{Q}=0$.*

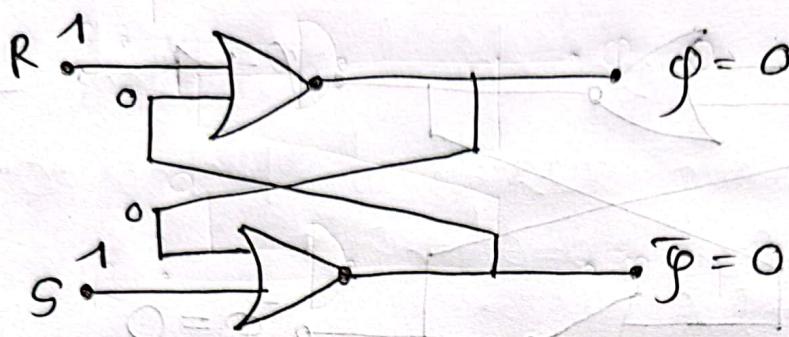
$S=0, R=0, Q=1; \bar{Q}=0$ } memory



Case 3 :

$$R=1, S=1, \bar{Q}=0; Q=0$$

But $Q \neq \bar{Q}$



$$\text{Again, } R=0, S=0, Q=0, \bar{Q}=1$$

$$\text{and, } Q=1, \bar{Q}=0$$

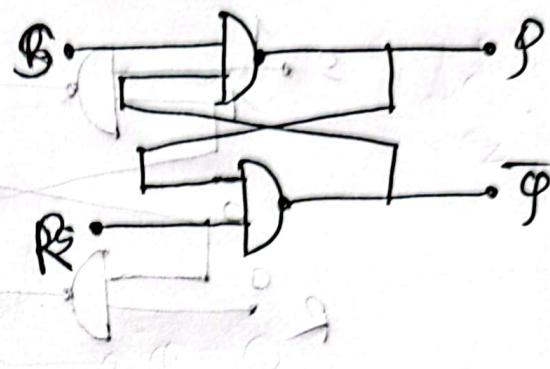
S	R	Q	\bar{Q}
0	0	Memory (as before)	
0	1	0	1
1	0	1	0
1	1	Not used (invalid).	

S	R	Q	\bar{Q}
0	0	invalid	
0	1	1	0
1	0	0	1
1	1	Memory state	

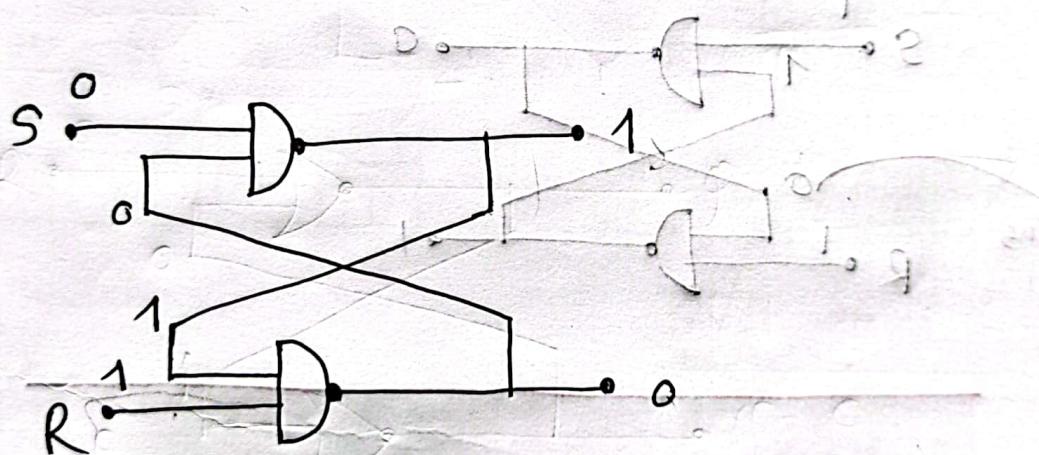
Using NAND

T.T for Nand

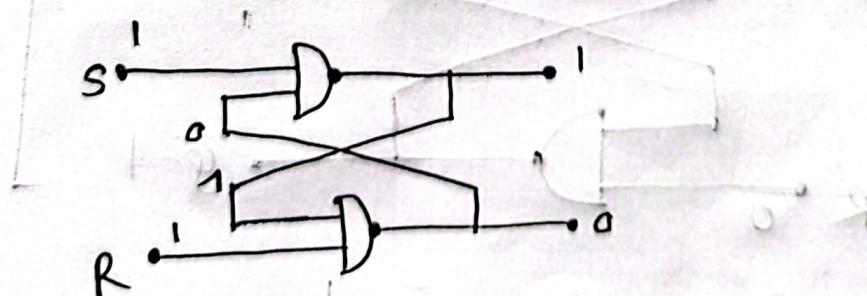
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



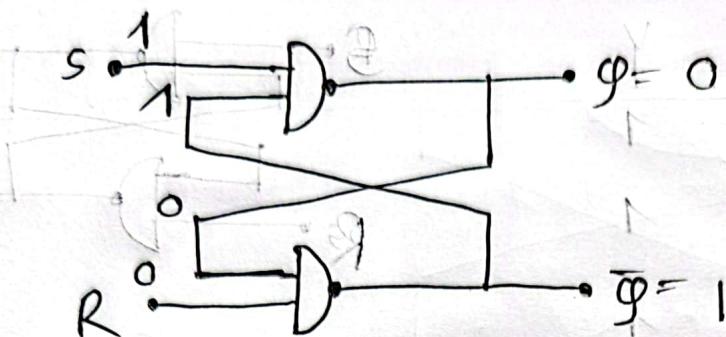
Case 1: $S=0, R=1, Q=1; \bar{Q}=0$



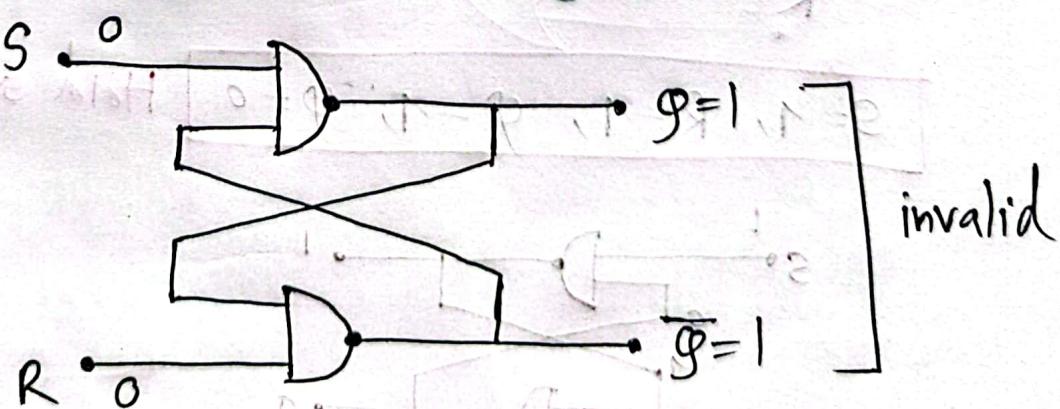
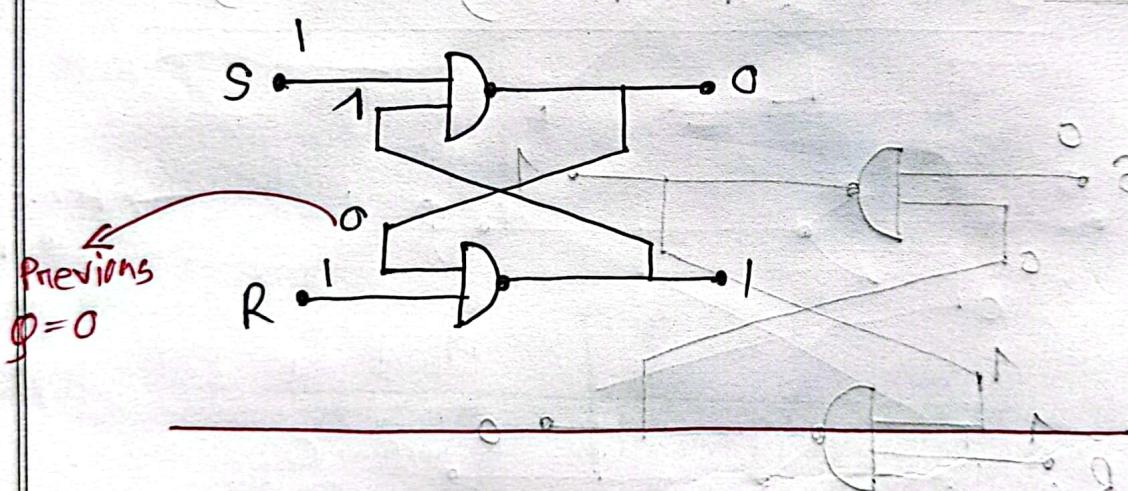
$S=1, R=1, Q=1; \bar{Q}=0$ Hold state



Case 2: $S=1, R=0, \varphi=0, \bar{\varphi}=1$



$S=1, R=1, \varphi=0, \bar{\varphi}=1$ Hold state



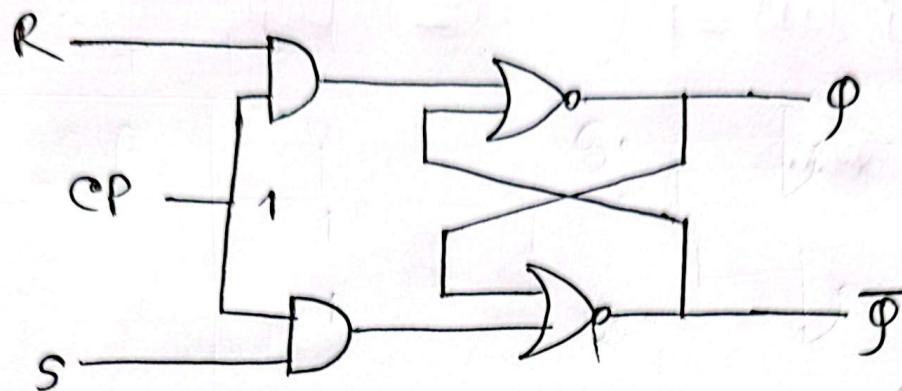
$S=0$	$R=0$	$\varphi=1$	$\bar{\varphi}=1$
$S=1$	$R=1$	$\varphi=0$	$\bar{\varphi}=1$
$S=1$	$R=1$	$\varphi=1$	$\bar{\varphi}=0$

\rightarrow Up থেকে নিয়ে
 \rightarrow Down থেকে নিয়ে

Sub.: _____

SAT SUN MON TUE WED THU FRI
○ ○ ○ ○ ○ ○ ○

Clocked RS Flip-Flop STATE: / /



RS latch NOR
Gate GEN
স্যুরি.
ডেটা কে
use its
truth table

পদবী.

যখন $CP = 0$, তখন

তাণে কাজ হবে না।

RSR		00	01	1*	10
0			X	1	
1	1		X	1	

$$Q(t+1) = S + R'Q$$

(CP)	Q(t)	S	R	Q(t+1)
↑	0	0	0	0
↑	0	0	1	0
↑	0	1	0	1
↑	1	0	0	1
↑	1	0	1	0
↑	1	1	0	1
↑	1	1	1	invalid

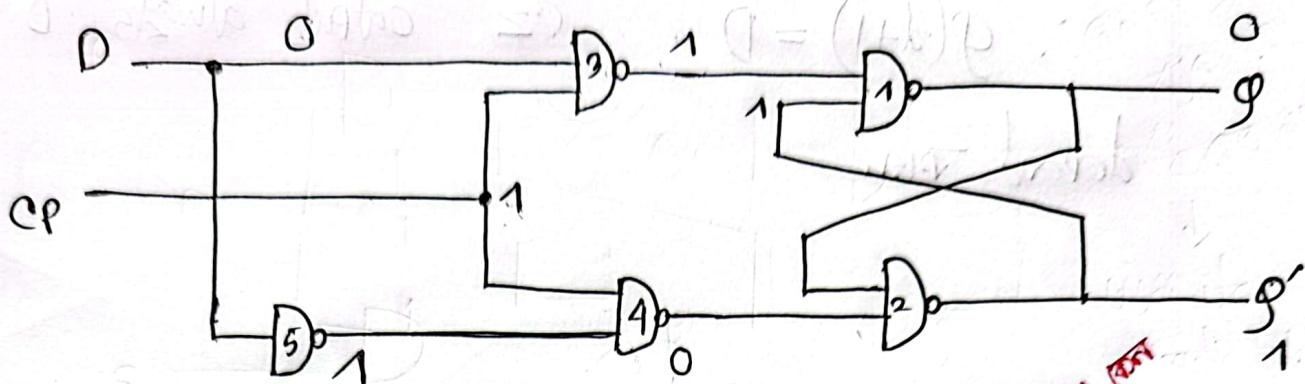
don't care

NoR T.T		
0	0	1
0	1	0
1	0	0
1	1	0

SR latch truth table Non gate		
S	R	Q
0	0	Previous
0	1	Reset $\rightarrow Q=0$
1	0	Set $\rightarrow Q=1$
1	1	invalid

D - Flip - Flop

DATE: / /



NAND

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

CP	Q(t)	D	Q(t+1)	Previous state
↓ 0	X	X	0	0.
↑ 1	X	0	1	1
↑ 1	X	1	1	1

* CP যখন 0 থাকে তখন Flip-Flop এর পোলা charge হবে না, আগের অবস্থায় রয়েব।

* CP যখন 1 থাকে তখন Flip-Flop সরিখভাবে রয়েব।

* যখন D = 0 হয়, Previous(Q(t)) যাই রয়েব না কেন Q(t+1) ও 0 হব।

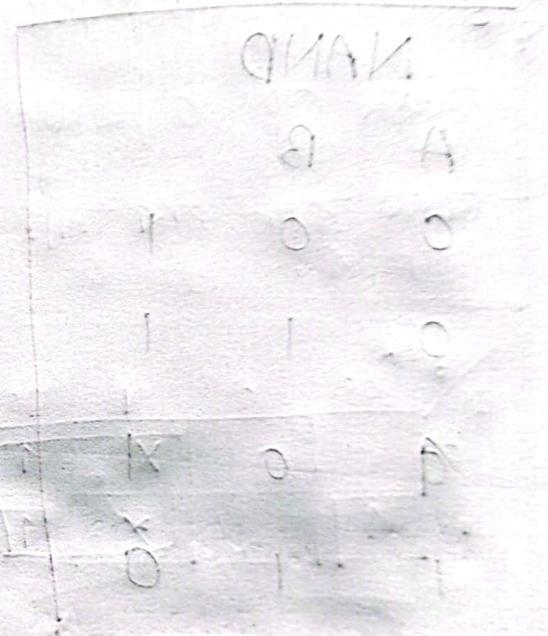
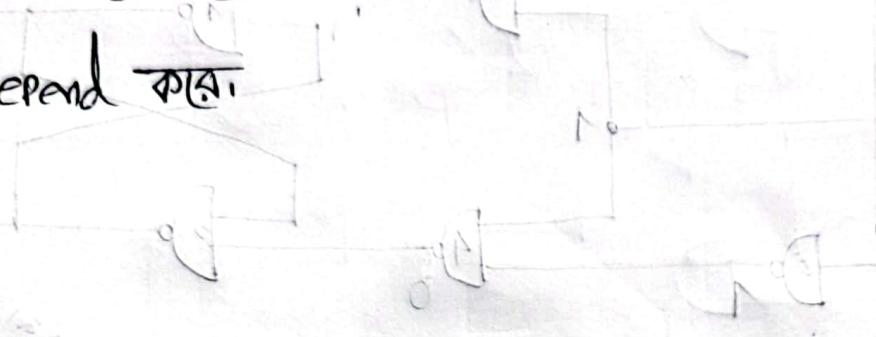


Sub.: _____

SAT SUN MON TUE WED THU FRI
O O O O O O O

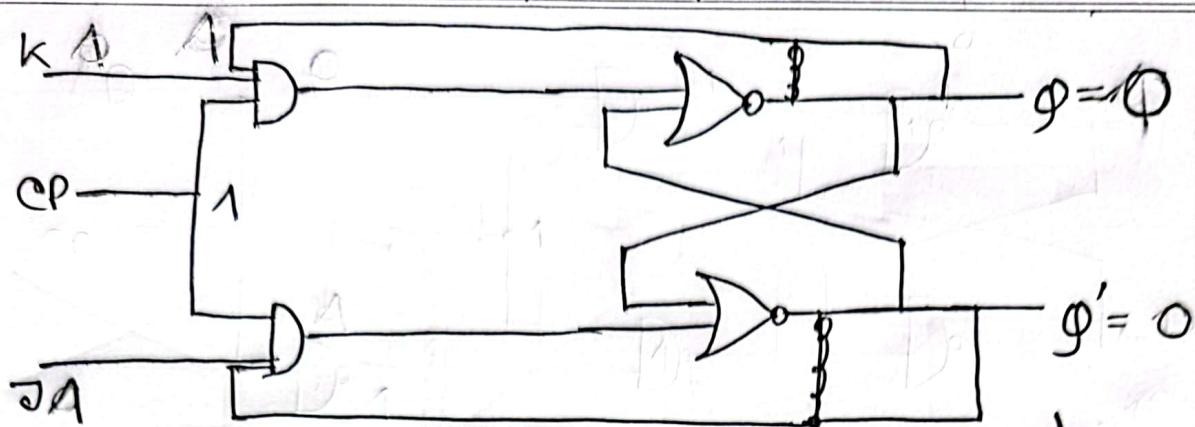
DATE: / /

$\therefore g(t+1) = D$ cz output always D হয়ে থাকা
 depend করা।



JK Flip-Flop

dated 10/10/2023



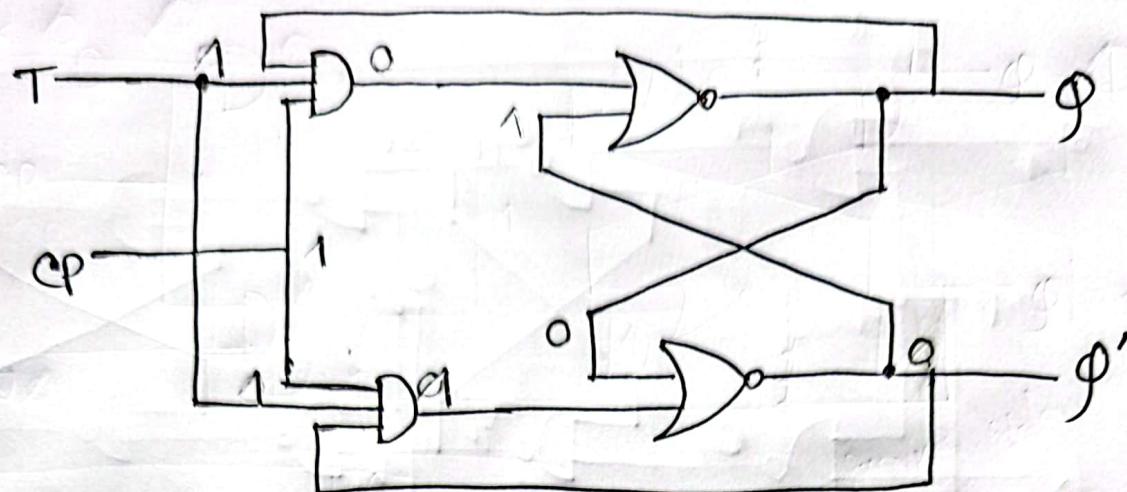
		RS		CP	$Q(t)$	J	K	$Q(t+1)$
A	B	S	R					
0	0	1	0	0	X	X	X	No Change
0	0	0	1	1	0	0	0	0
0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	0	1	0
1	1	0	1	1	1	0	1	0
		P.S		1	0	1	0	0
		Reset						
		Set		1	1	0	1	1
		Invalid						
				1	0	1	0	1
				1	1	1	0	1
				1	0	1	1	0
				1	1	0	1	1
				1	1	1	1	0

JK

00	01	11	10
0	1	1	1
1	1	1	1

$$Q(t+1) = Q'J + Q'K'$$

T Flip-Flop \rightarrow এক এক single input
version



NOR		O/P
A	B	O/P
0	0	1
0	1	0
1	0	0
1	1	0

CP	$Q(t)$	T	$Q(t+1)$
↑	0	0	0
↑	1	0	1
↑	0	1	1
↑	1	1	0

$$Q(t+1) = \bar{Q}T + Q\bar{T}$$

$T=0$ এক same output

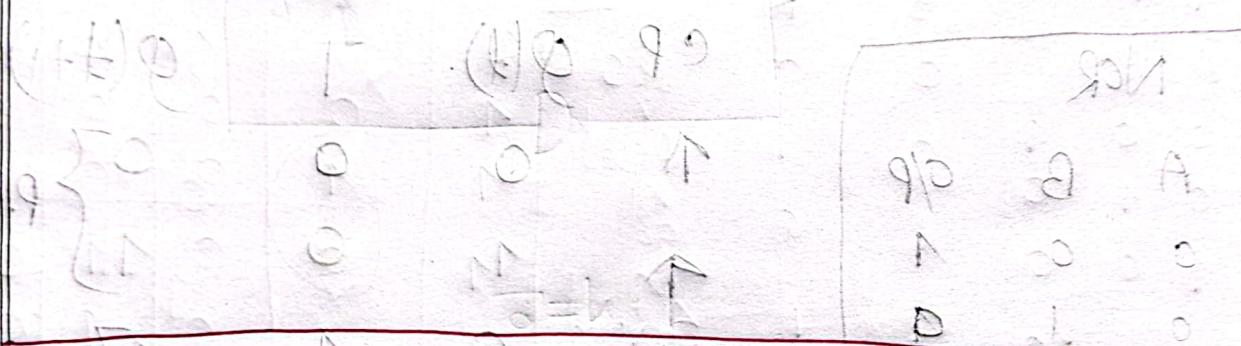
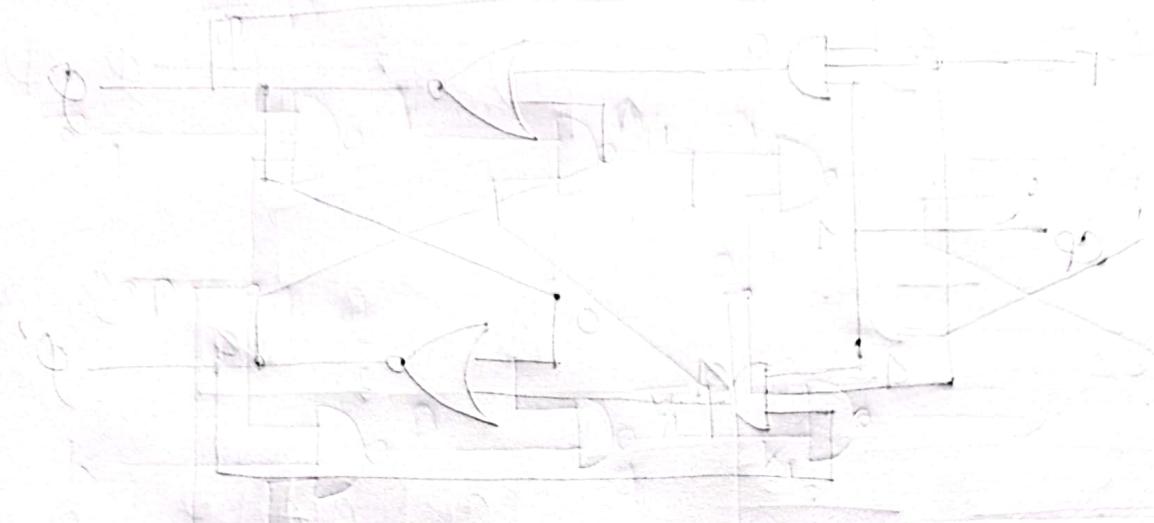
$T=1$ এক toggle output



Sub.: _____

SAT SUN MON TUE WED THU FRI
○ ○ ○ ○ ○ ○ ○

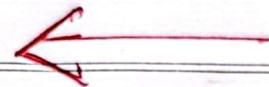
DATE: / /



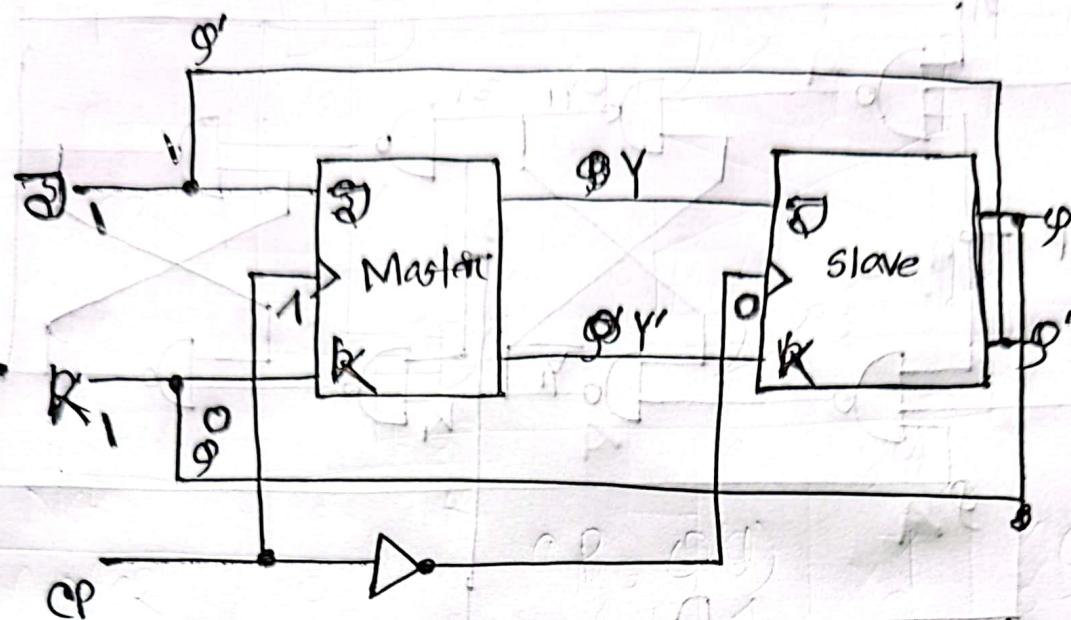
Master slave ~~condition~~ এক flip-flop ক্ষেত্রের main কাণ্ড হচ্ছে Race condition দ্বারা ক্ষণে।

Race condition: যখন ক্ষেত্রের এক flip-flop কে ১ \rightarrow ০ থাকে এবং clock pulse দ্বাৰা তা অখণ্ড output toggle হতে থাকে ($0 \rightarrow 1$ বা $1 \rightarrow 0$) , But clock pulse কে অম্বুক্তি কৰে তারে ক্ষেত্রে এক থাকে এবং stable এবং আছে না। এটিই এক race condition

বিন্দু।



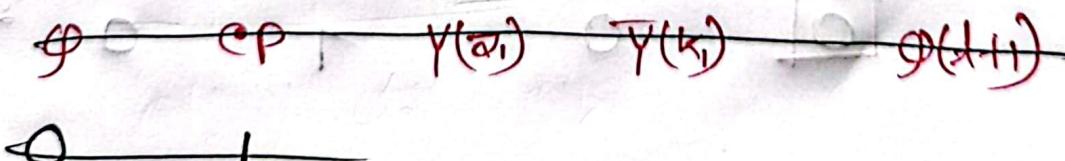
Master slave flip-flop:

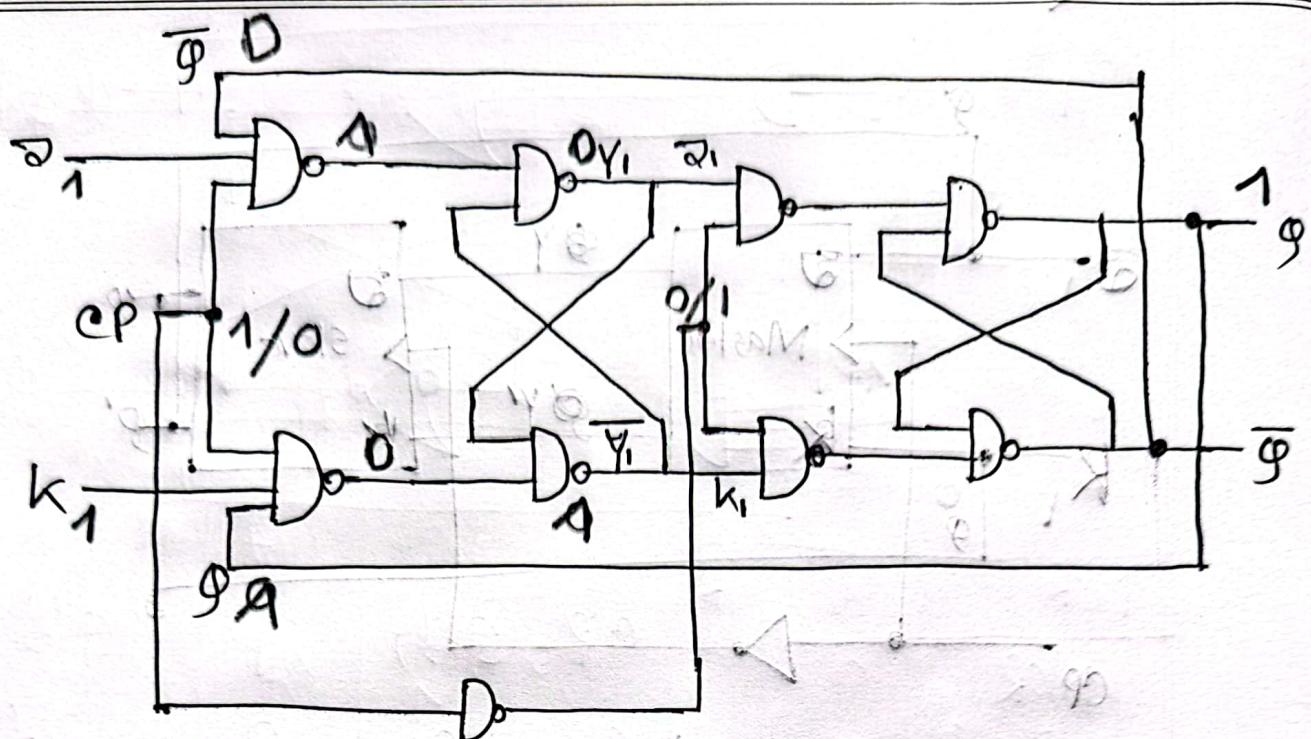


Logic diagram of master slave flip-flop

When $CP = 1$ — then Master will work and slave will be disabled, so there was no output. But when $C=1$ — then Master will disable and Slave will enable and there was output.

$$Z = k - 1 \quad \text{परन्तु}$$





$$\bar{D} = k = 1$$

\emptyset CP $Y_0(\bar{Q}_1)$ $\bar{Y}(K_1)$ $\emptyset(t+1)$

0	1	1	0	-
---	---	---	---	---

0	0	1	0	-
---	---	---	---	---

1	1	0	1	-
---	---	---	---	---

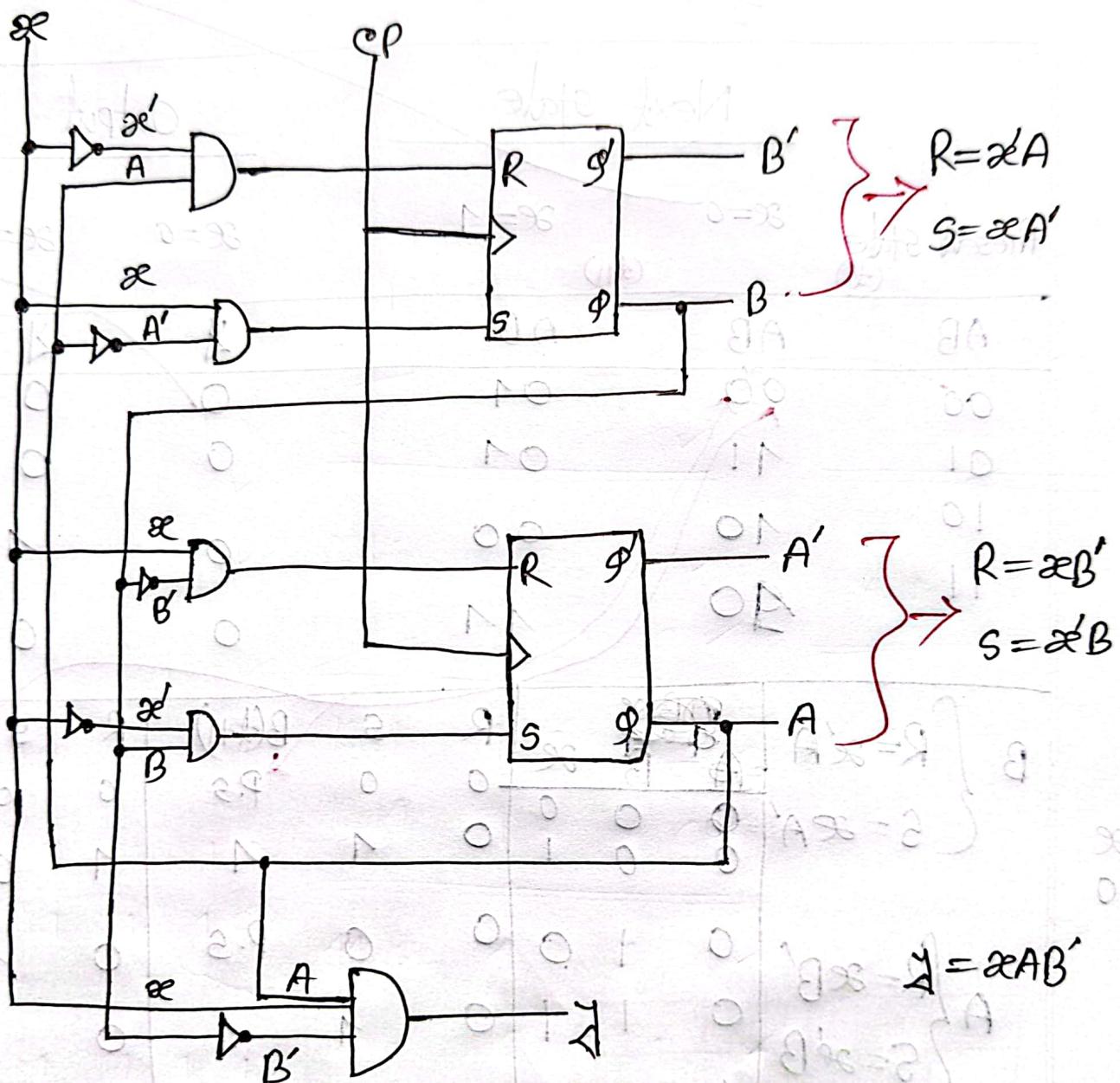
1	0	0	1	0
---	---	---	---	---

1 → output আজ্ঞা
যন্ত্রে $CP=0$

- থার প্রঃ
slave enable
হুয়ে।



Analysis of Clocked Sequential Circuits



Output $Y = \alpha AB' = 110$ হলো এই

State Table

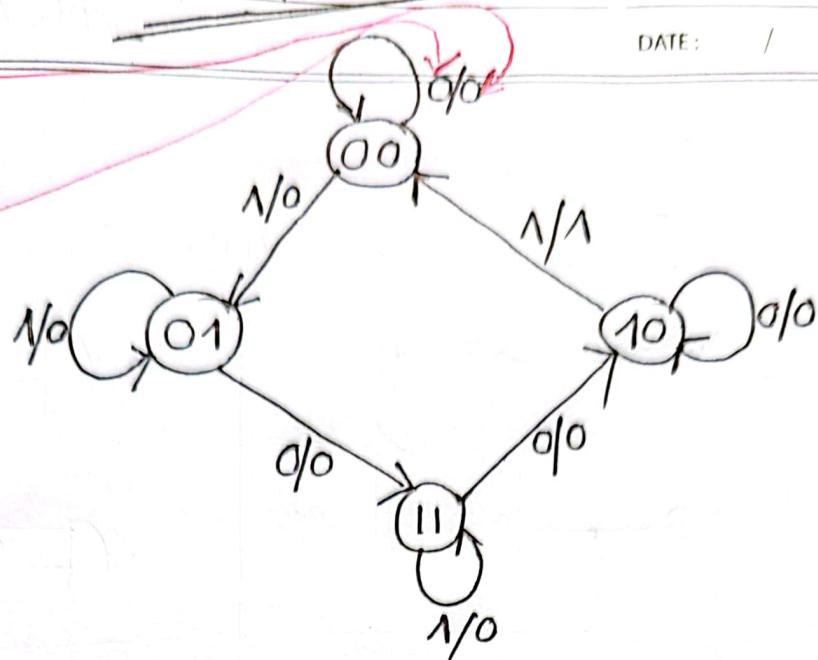
Present State	Next state		Output	
	$x=0$	$x=1$	$x=0$	$x=1$
AB	AB	AB	1	1
00	00	01	0	0
01	11	01	0	0
10	10	00	0	1
11	00	11	0	0

ABx	B			R	S	B(x+1)	R	S	A(x+1)
	$R = x'A'$	$S = xA'$	x	0	0	P.S	0	10	P.S
010	0	0	0	0	1	1	1	0	0
	0	0	1	0	1	1	0	0	P.S
	0	1	0	1	0	0	0	0	P.S
	1	0	0	1	0	0	0	0	P.S
	1	0	1	0	0	P.S	1	0	0
	1	1	0	1	0	0	0	1	P.S
	1	1	1	0	0	P.S	0	0	P.S

Sub.: _____

State DiagramSAT SUN MON TUE WED THU FRI
○ ○ ○ ○ ○ ○ ○

DATE: / /

State Equation

$$A(t+1) = \alpha' A'B + \alpha' AB' + \alpha' AB + \alpha A B$$

$$B(t+1) = \alpha' A'B + \alpha A'B' + \alpha A'B + \alpha A B$$

		AB	00	01	11	10
		α'	0	1	1	1
α'	0	1	0	1	1	1
1	1	1	1	1	0	1

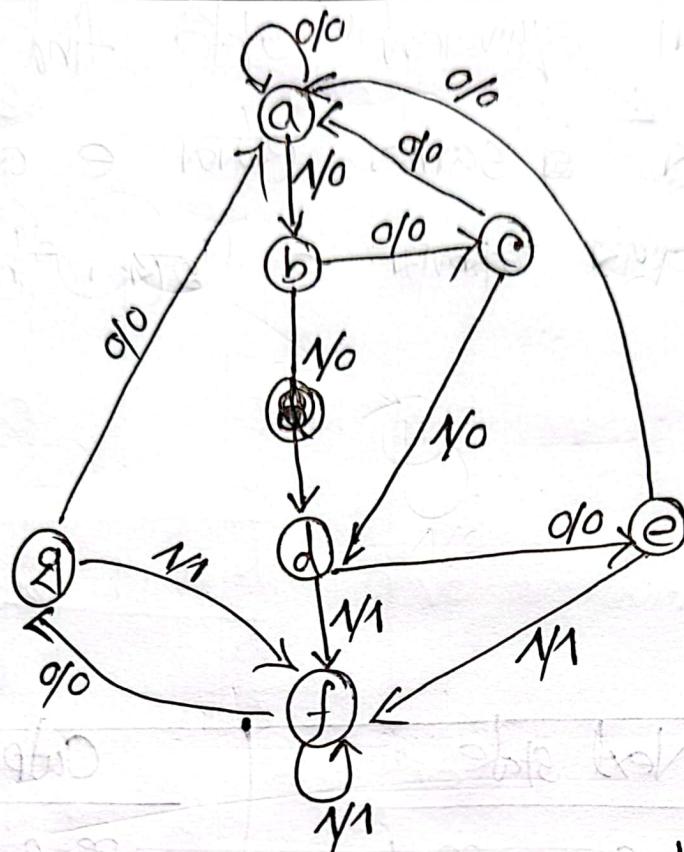
		AB	00	01	11	10
		α'	0	1	1	1
α'	0	1	1	1	1	1
1	1	1	1	1	1	1

$$S = \alpha' B \\ R = \alpha B'$$

$$\begin{aligned}
 A(t+1) &= \alpha' B + \alpha' A + A B \\
 &= S + A(\alpha' + B) \\
 &= S + A(\alpha B')' \\
 &= S + A(R)'
 \end{aligned}$$

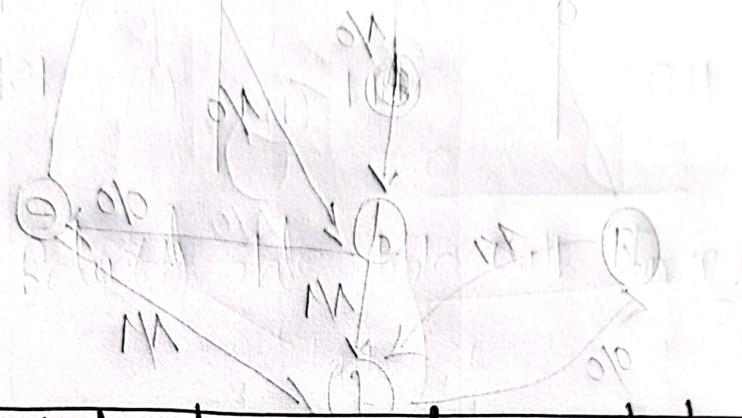
$$\begin{aligned}
 B(t+1) &= \alpha A' + \alpha B + A' B \\
 &= A' B + \alpha B + \alpha A' \\
 &= B(A' + \alpha) + \alpha A' \\
 &= B(\alpha \alpha')' + \alpha A' \\
 &= S + B R'
 \end{aligned}$$

State Reduction and Assignment /



PS	Next state		output	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

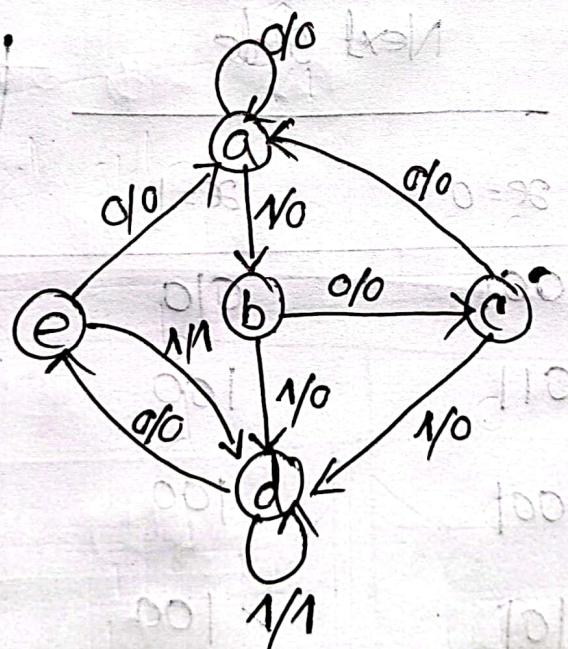
এখন আমরা equivalent state find out করবো,
 যাদের প্রথম এবং দ্বিতীয় e same. যেমন e and f.
 তাহলে e এর স্বত্ত্বালয় e হবে, then d = f



PS	Next State		Output	
	$\alpha=0$	$\alpha=1$	$\alpha=0$	$\alpha=1$
a	a c	b d	0 0	0 0
b	c d	d	0 0	0 0
c	a d	d	0 0	0 0
d	e d	f d	0 0	1 1
e	a d	f d	0 0	1 1
f	g e	f	0 0	+
g	a f	f	0 0	+

New State Table

PS	Next state		O/P	
	$\alpha=0$	$\alpha=1$	$\beta=0$	$\beta=1$
a	a	b	0	0
b	c	d	0	1
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1



Sub.: _____

SAT SUN MON TUE WED THU FRI
O O O O O O O

Binary

State Assignment

DATE: / /

State	Assignment 1	Assignment 2	Assignment 3
a	001	000	000
b	010	010	100
c	011	011	010
d	100	101	101
e	101	111	011
	0	0	0

Reduced state table with binary assignment.

খালি রেজিস্টার
২,৬ মুক্ত অস্টেট মান
অস্টেট

Present State	Next State		Output	
	$\alpha=0$	$\alpha=1$	$\alpha=0$	$\alpha=1$
001	001	010	0	0
010	011	100	0	0
011	001	100	0	0
100	101	100	0	1
101	001	100	0	1

Excitation Table of RS flip-flop

Characteristic Table				Excitation Table			
R	S	$\varphi(t)$	$\varphi(t+1)$	$\varphi(t)$	$\varphi(t+1)$	R	S
0	0	0	0	0	0	X	0
0	0	1	1	0	1	0	1
0	1	X(0/1)	1	1	0	1	0
1	0	X(0/1)	0	1	1	0	X
1	1	0	1				

④ Excitation table shows the minimum inputs that are necessary to generate a specific particular state.

J-K Flip-Flop

Characteristic Table				Excitation Table			
J	K	$\varphi(t)$	$\varphi(t+1)$	$\varphi(t)$	$\varphi(t+1)$	J	K
0	0	0	0	0	0	0	X
0	0	1	1	0	1	1	X
0	1	X(0/1)	0	1	0	X	1
1	0	X(0/1)	1	1	1	X	0
1	1	0	1				
1	1	1	0				



T- Flip Flop

Characteristic Table

T	$\phi(t+1)$
0	0
1	$\phi'(t)$

Excitation Table

$\phi(t)$	$\phi(t+1)$	T
0	(No) X	0
0	(No) X	1
1	0	1
1	1	0

Toggle অর্থে তাৰ মান $T=1$ D Flip-Flop

D	$\phi(t+1)$
0	0
1	1
X	0

$\phi(t)$	$\phi(t+1)$	D
0	0	0
0	1	0
0	(No) X	1
1	0	0
1	1	1

D প্ৰয়োজন যা হ'ব

 $\phi(t+1)$ প্ৰয়োজন কোনো

হ'বে।

