

1. Description

1.1. Project

Project Name	SLEEP EXT WAKEUP
	custom
	STM32CubeMX 6.12.0
	08/19/2024

1.2. MCU

MCU Series	STM32H5
MCU Line	STM32H563/H573
MCU name	STM32H563ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	ARM Cortex-M33

2. Pinout Configuration

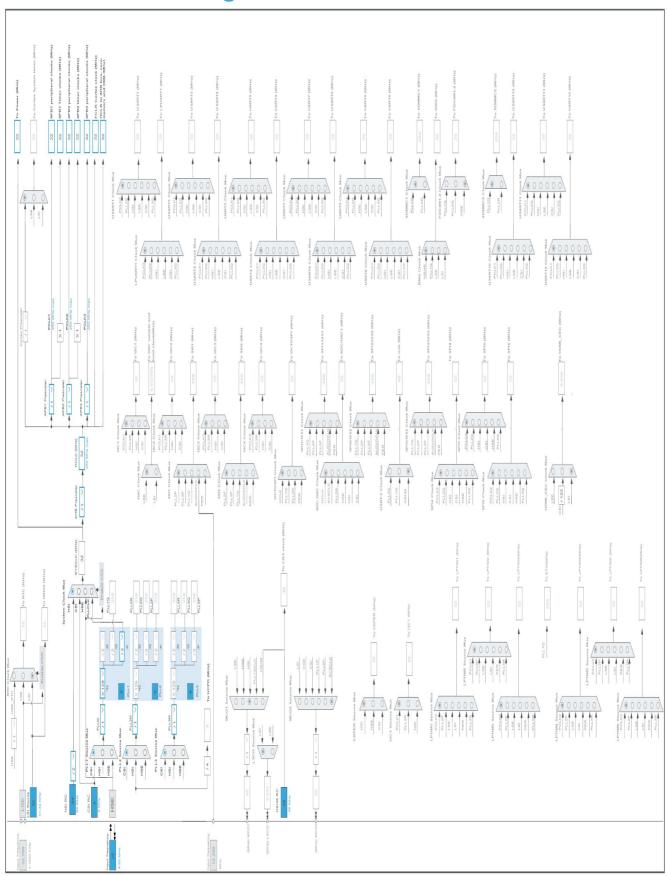


3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after		Function(s)	
	reset)			
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN(PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT(PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
46	PB0 *	I/O	GPIO_Output	
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
70	VCAP	Power		
71	VSS	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDD	Power		
106	VDDUSB	Power		
107	VSS	Power		
108	VDD	Power		
120	VSS	Power		
121	VDDIO2	Power		
130	VSS	Power		
131	VDD	Power		
138	BOOT0	Boot		
142	VCAP	Power		
143	VSS	Power		
144	VDD	Power		

* The pin is affected with an I/O function		

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H5
Line	STM32H563/H573
мси	STM32H563ZITx
Datasheet	DS00000_Rev0

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

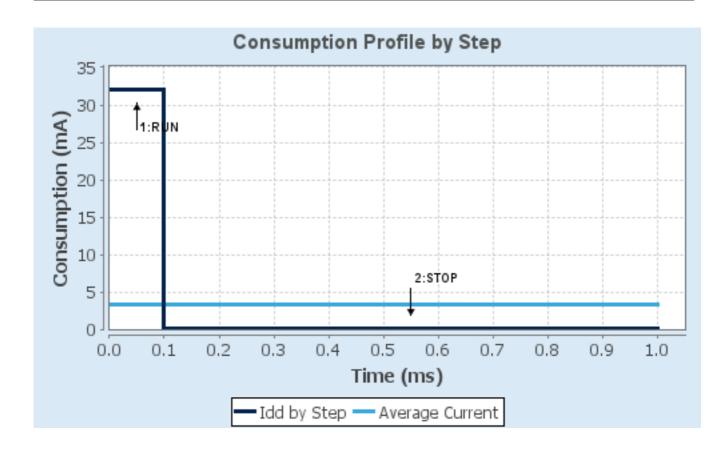
1.4. Sequence

	1	
Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0 SVOS5: System- Scale5/SMPS	
Fetch Type	FLASH_ON/Cache2Ways_A LL_RAM_RETENTION	
CPU Frequency	250 MHz	0 Hz
Clock Configuration		
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	32 mA	51.5 μA
Duration	0.1 ms	0.9 ms
DMIPS	535.0	0.0
Ta Max	120.78	124.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	3.25 mA
Battery Life	1 month, 13 days,	Average DMIPS	535.0 DMIPS
	4 hours		

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value	
Project Name	SLEEP_EXT_WAKEUP	
Project Folder	D:\Kiran's Embedded course\My worskspace\target\SLEEP_EXT_WAKEUP	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_H5 V1.3.0	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name	
1	SystemClock_Config	RCC	
2	MX_GPIO_Init	GPIO	
3	MX_TIM3_Init	TIM3	

3. Peripherals and Middlewares Configuration

3.1. BOOTPATH mode: Activated

3.2. MEMORYMAP

mode: Activated

3.3. PWR

mode: Dead Battery Signals disabled

mode: Power saving mode mode: Privilege attributes

3.3.1. PWR Privilege:

Privilege PWR:

PWR Privilege Disable

3.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

3.4.1. RCC Privilege:

Privilege RCC:

Privilege of RCC Non-Secure Items Disable

3.4.2. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 1 WS (2 CPU cycle)

Flash Programming Delay 0

RCC Parameters:

HSI Calibration Value 64
CSI Calibration Value 32
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000
TIM Prescaler Selection Disabled

Power Parameters:

Power Regulator Voltage Scale

Power Regulator Voltage Scale 3

3.5. SYS

Timebase Source: SysTick

3.6. TIM3

Clock Source : Internal Clock

3.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Dithering Disable
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0- OSC_IN(PH 0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT(P H1)	RCC_OSC_OUT	n/a	n/a	n/a	
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

- 4.2. GPDMA1
- 4.3. GPDMA2
- 4.4. LINKEDLIST

4.5. NVIC configuration

4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
EXTI Line13 interrupt	true	0	0	
TIM3 global interrupt	true	0	0	
Flash non-secure global interrupt	unused			
RCC non-secure global interrupt	unused			
FPU global interrupt	unused			

4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI Line13 interrupt	false	true	true
TIM3 global interrupt	false	true	true

^{*} User modified value

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32h5-bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32h5-ibis.zip

System View https://www.st.com/resource/en/svd/stm32h5-svd.zip

Description

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