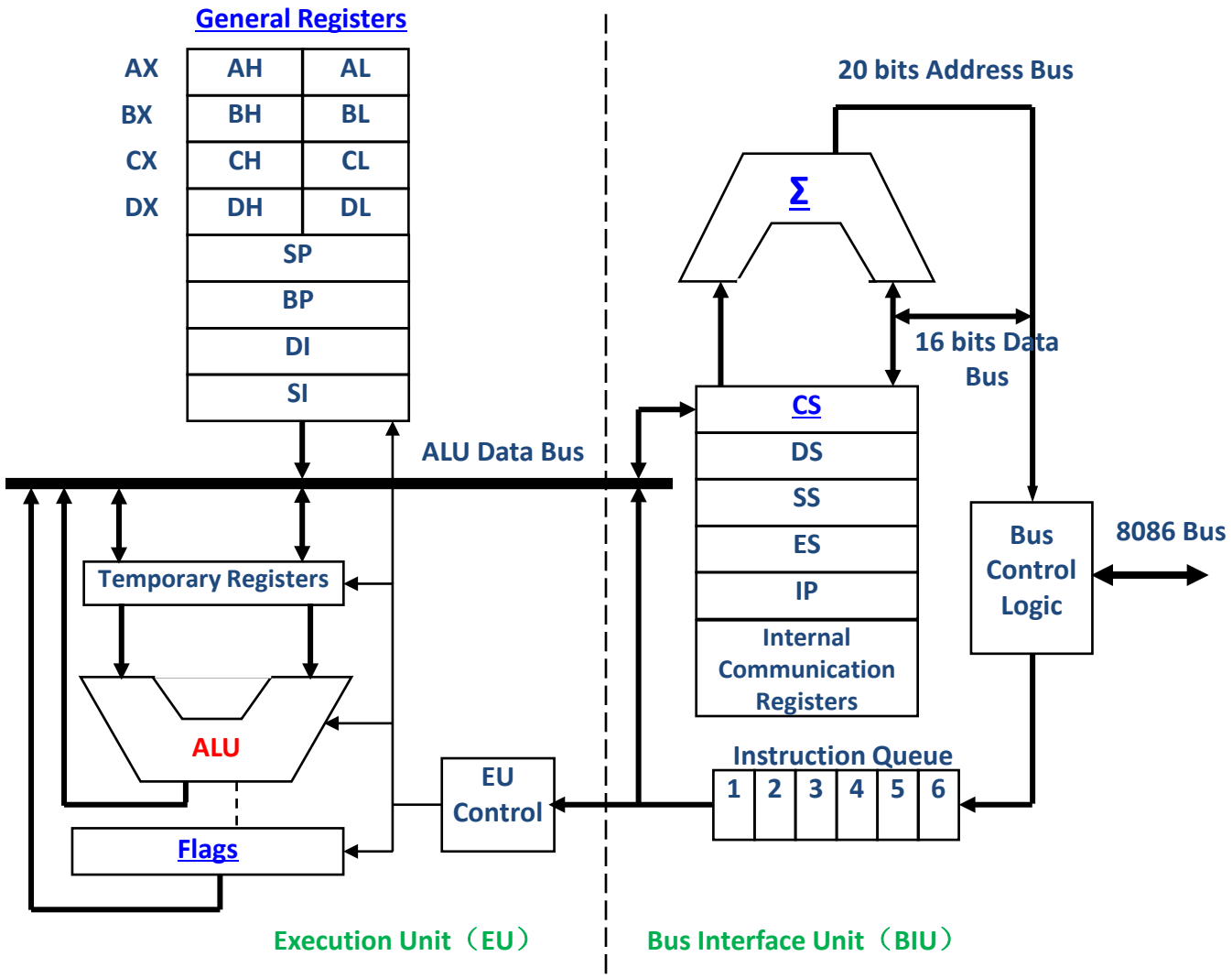
Chapter 2

Architecture of 8086 Microprocessor

Contents

2.1 8086 Architecture



Registers Organisation

General purpose Registers

R	Register
AX	Accumulator
BX	
CX	Counter
DX	

Pointer and index Registers

R	Register
SI	Source Index Register
DI	Destination Index Register
BP	Base Pointer Register
SP	Stack Pointer Register
IP	Instruction Pointer Register

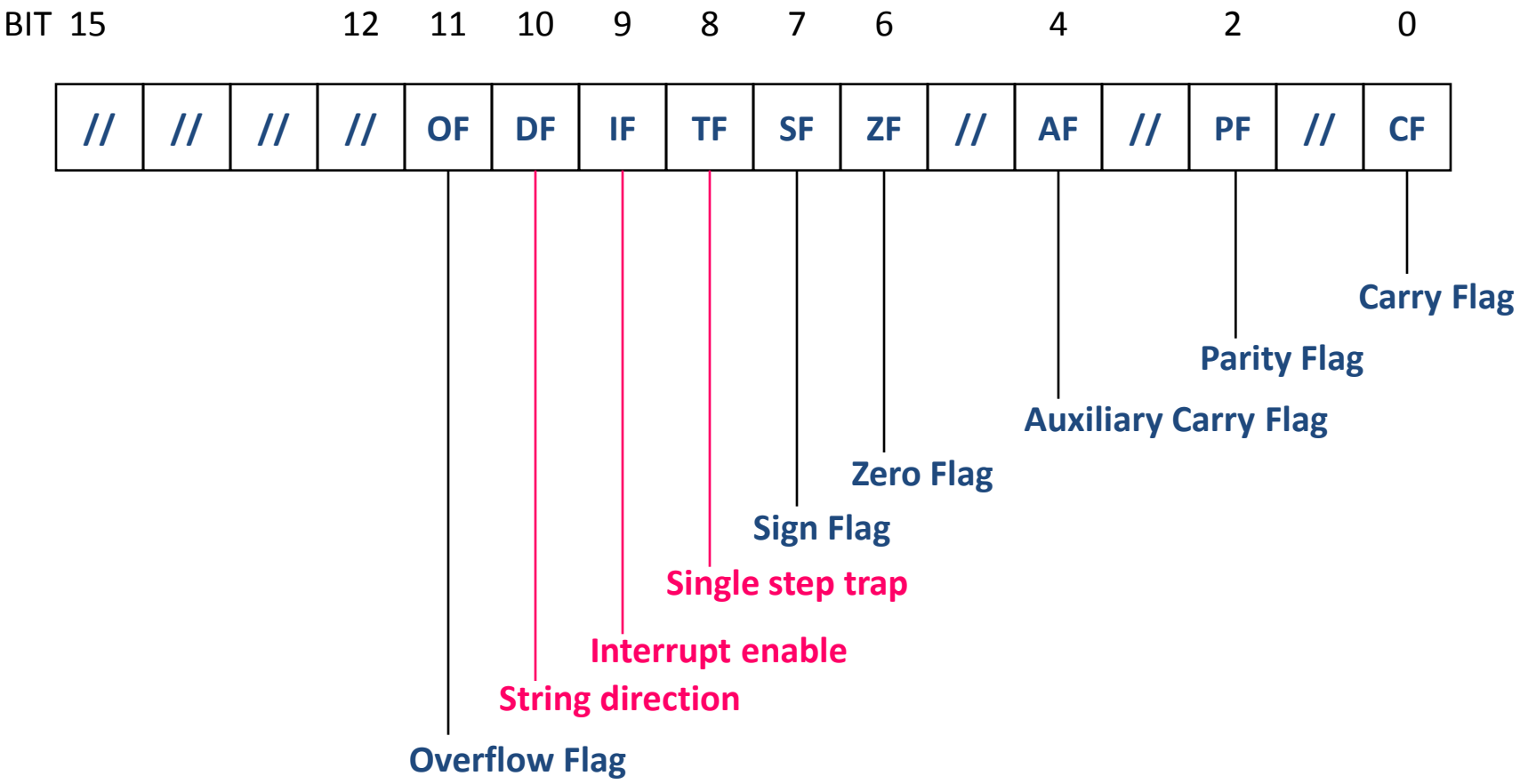
Segment Registers

R	Register
CS	Code Segment Register
DS	Data Segment Register
ES	Extra Segment Register
SS	Stack Segment Register

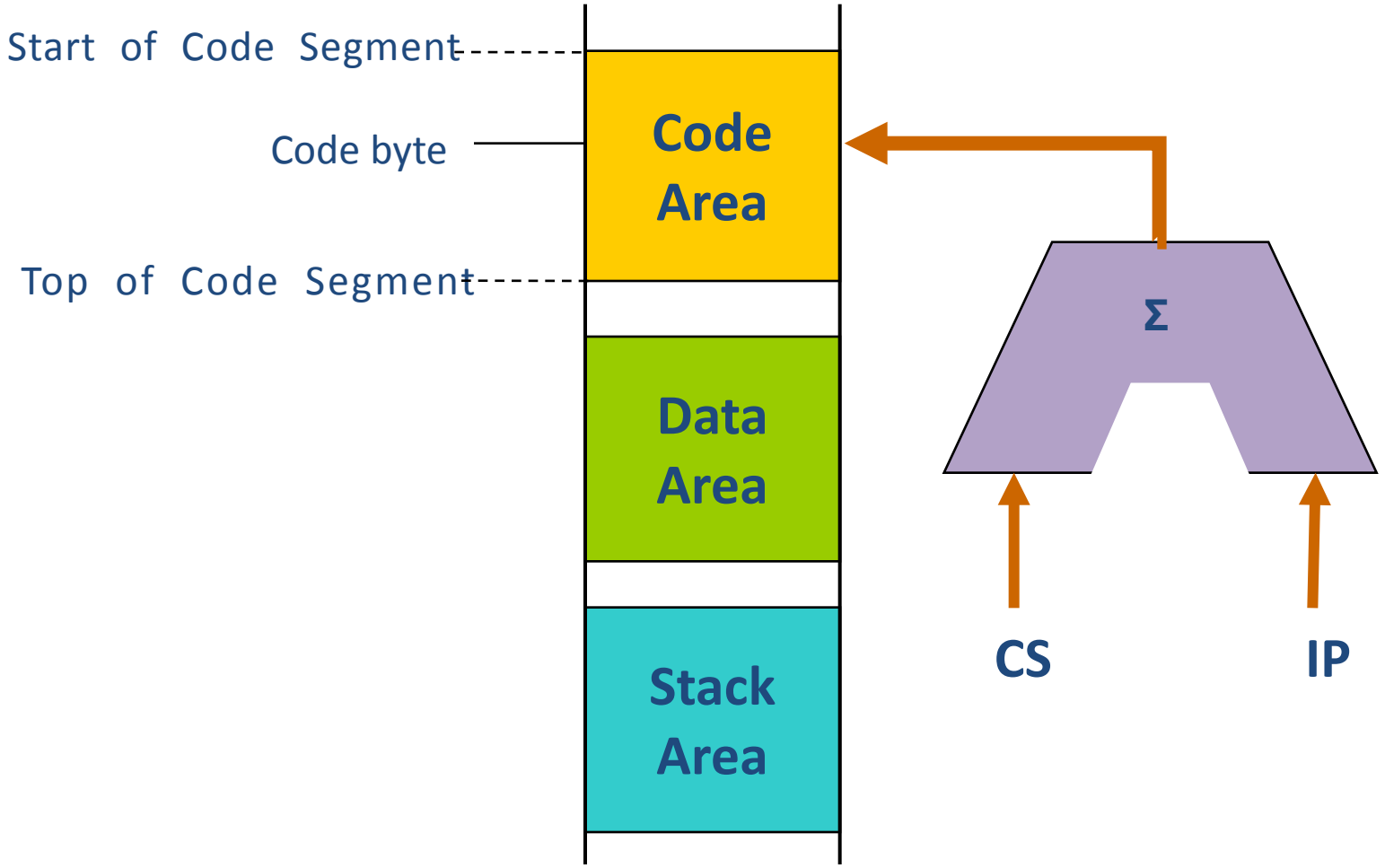
Flag Register

R	Register
FR	CPU Status Flags Register

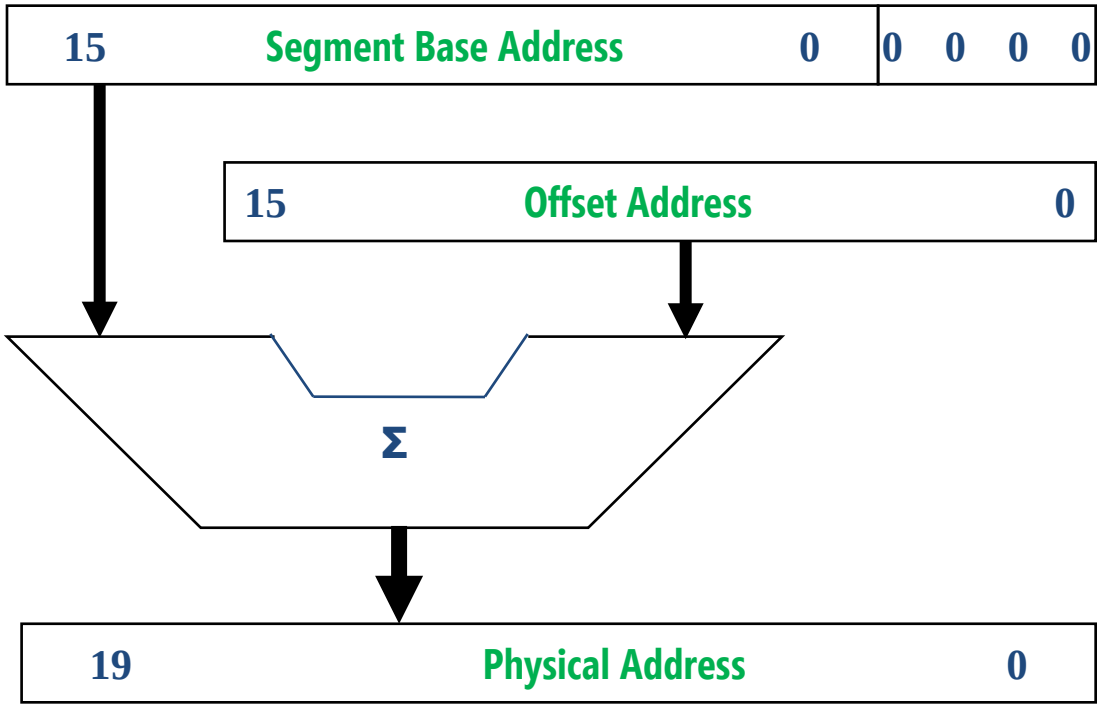
Flag Register



Memory Segmentation



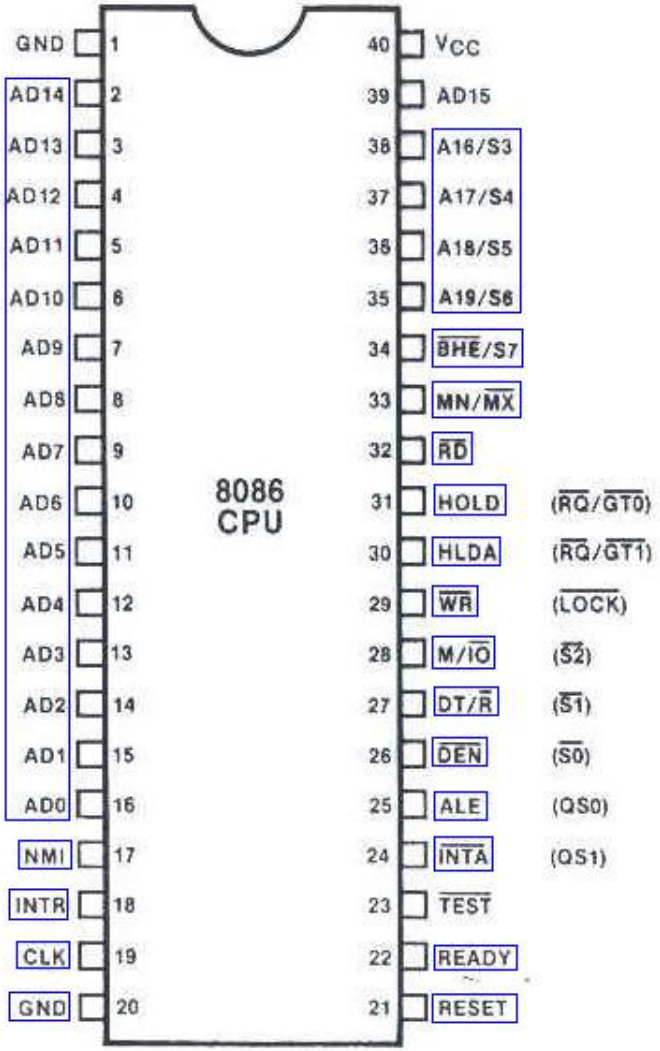
Generation of Physical Address



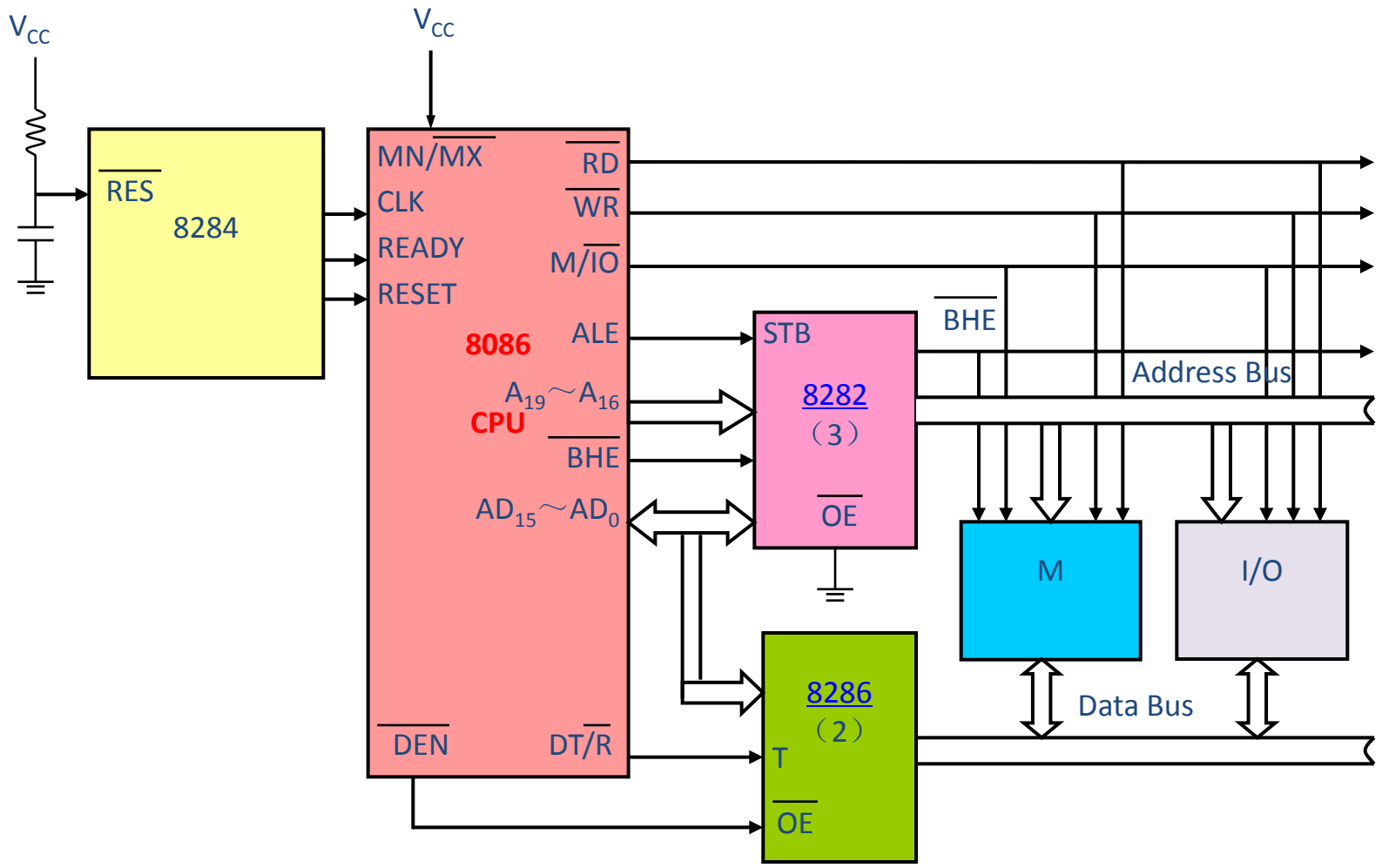
Physical Address=Segment Base Address×10H+Offset Address

2.2 Signal Description of 8086

- MN/ $\overline{MX}$
- AD_{15}～AD_0
- ALE
- DT/$\overline{R}$（Data transmit/Receive）
- $\overline{DEN}$（Data Enable）
- A_{16}/S_3～A_{19}/S_6
- $\overline{BHE}/S_7$
- M/$\overline{IO}$
- $\overline{RD}$（Read）
- $\overline{WR}$（Write）
- READY
- INTR（Maskable Interrupt Request）
- $\overline{INTA}$（Interrupt Acknowledge）
- NMI
- HOLD
- HLDA
- RESET
- CLK

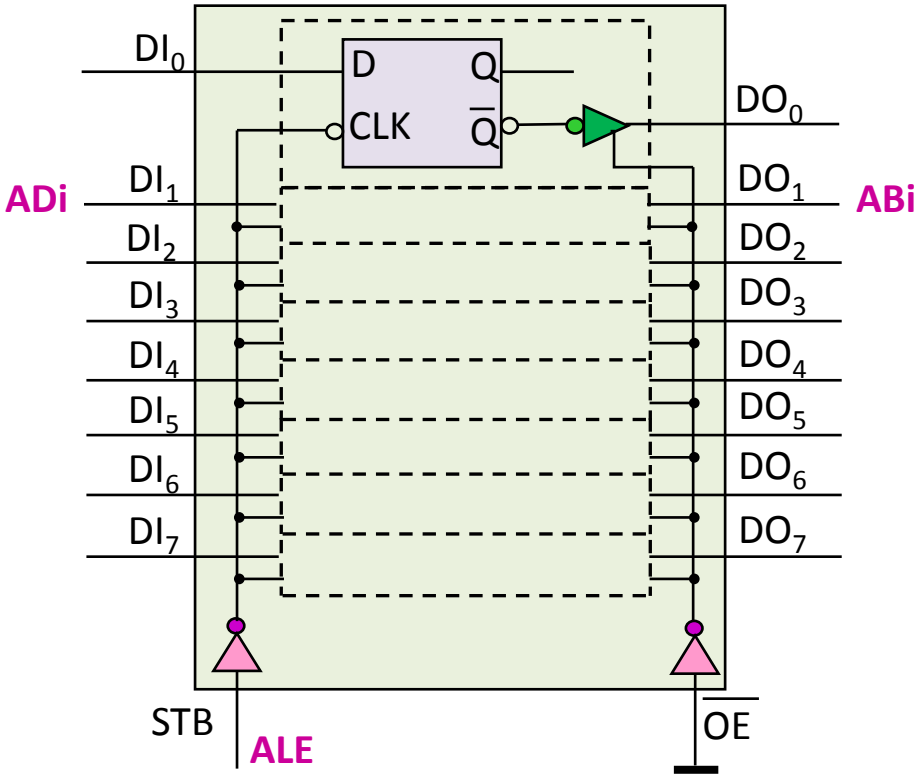


Typical Minimum Mode configuration

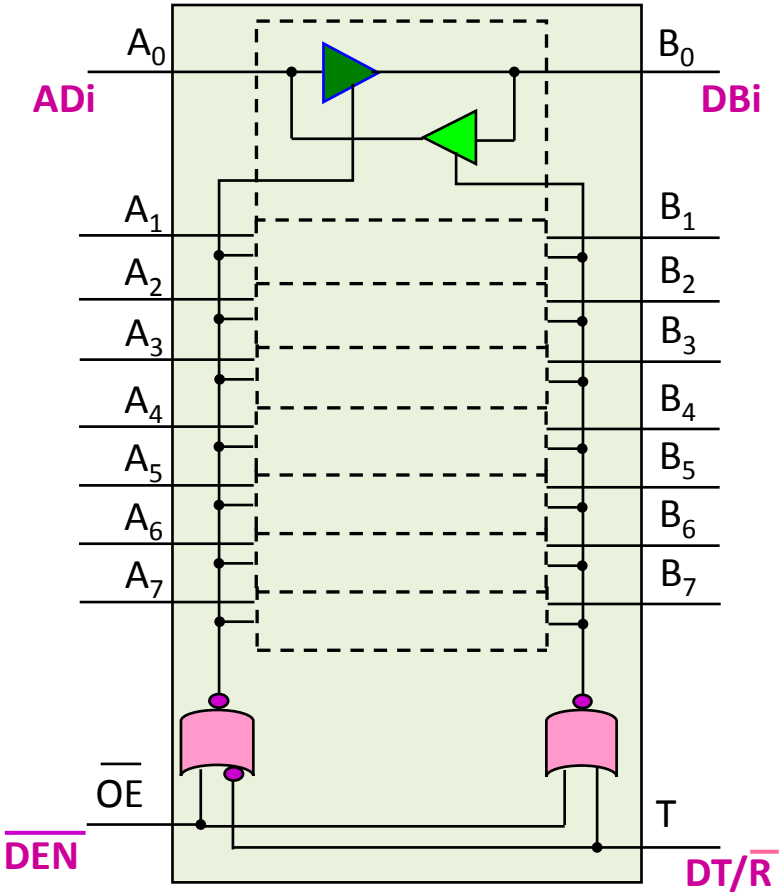


Timings

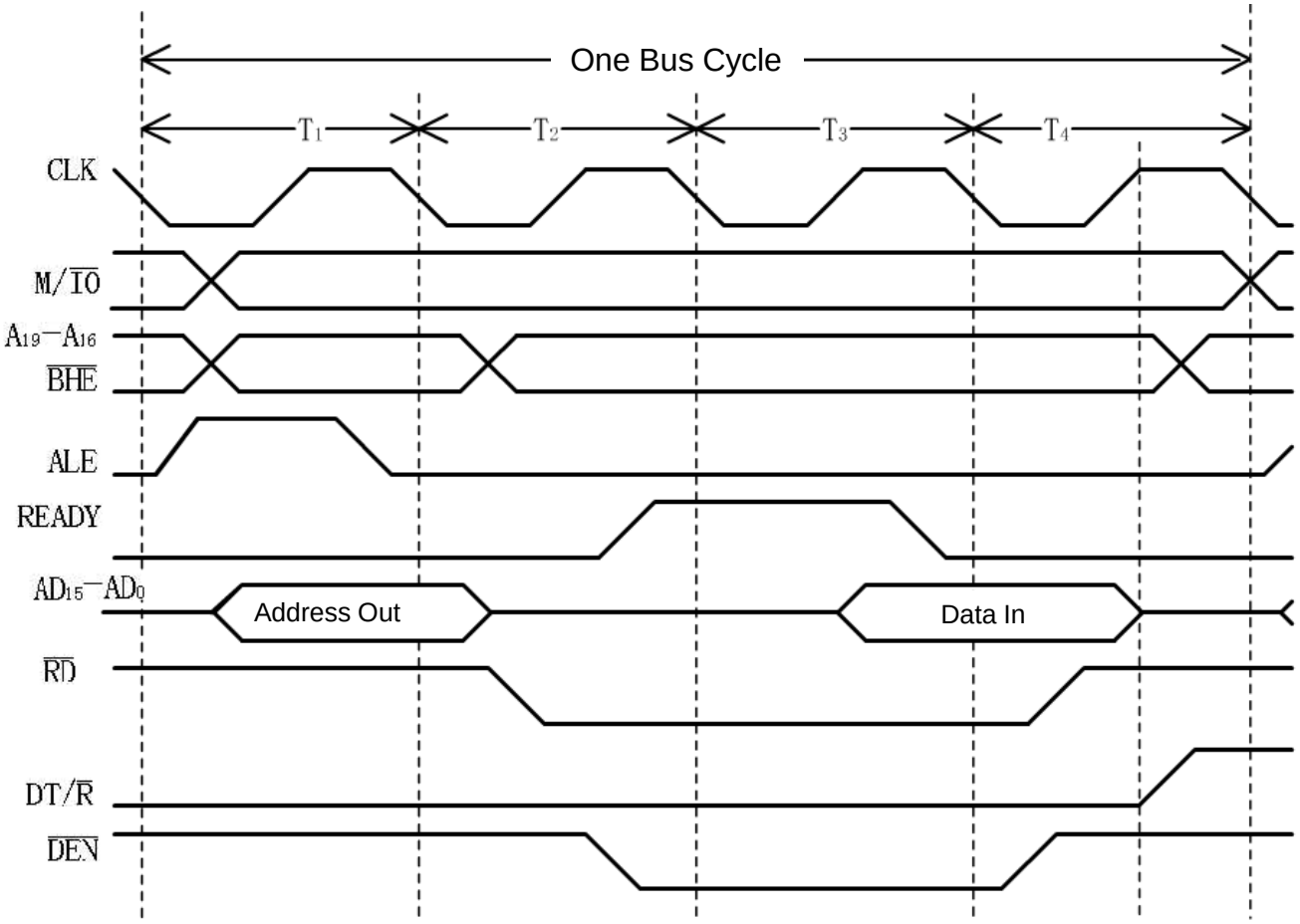
Address Latch ——8282



Transceriver——8286

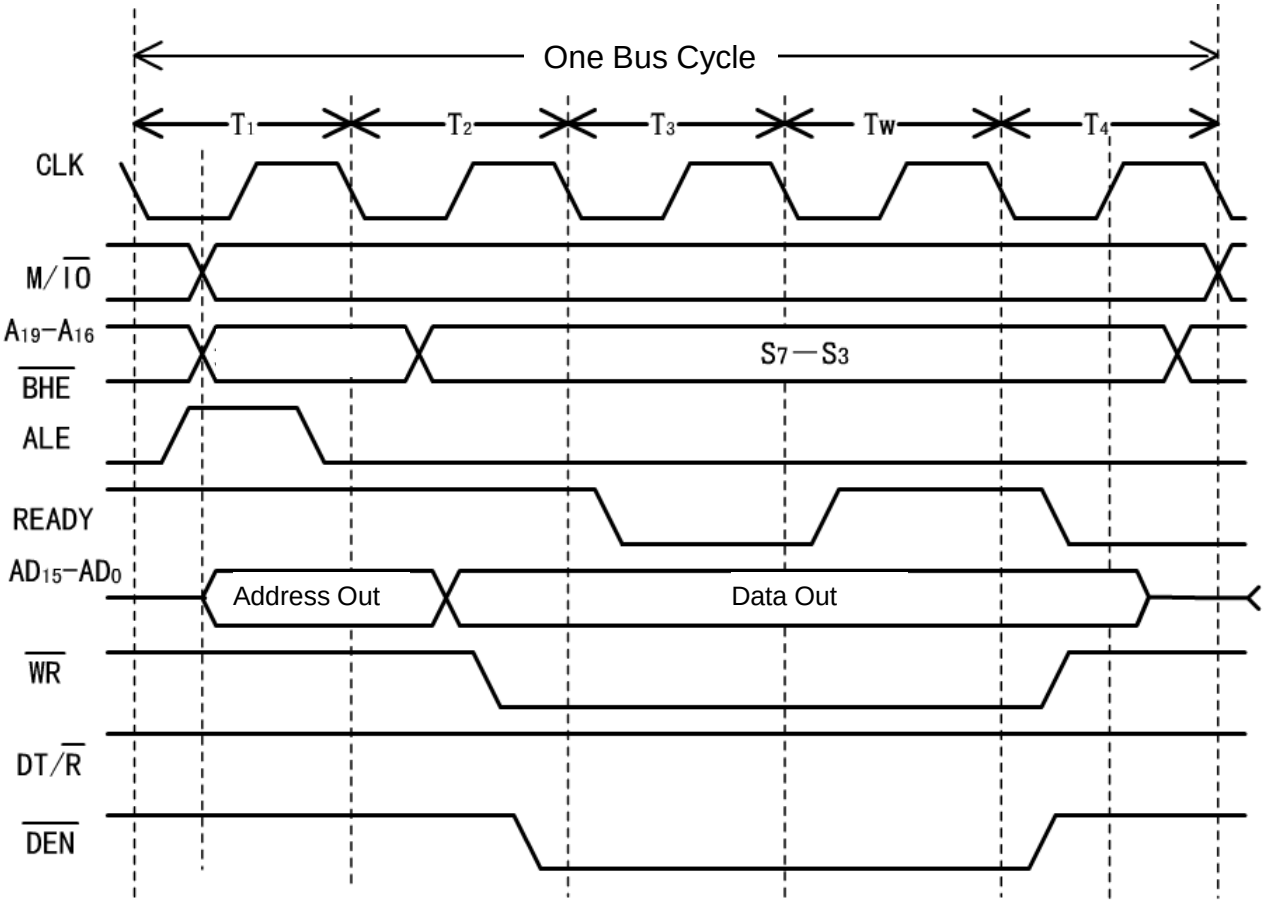


2.3 Bus Timing for Minimum Mode—Input

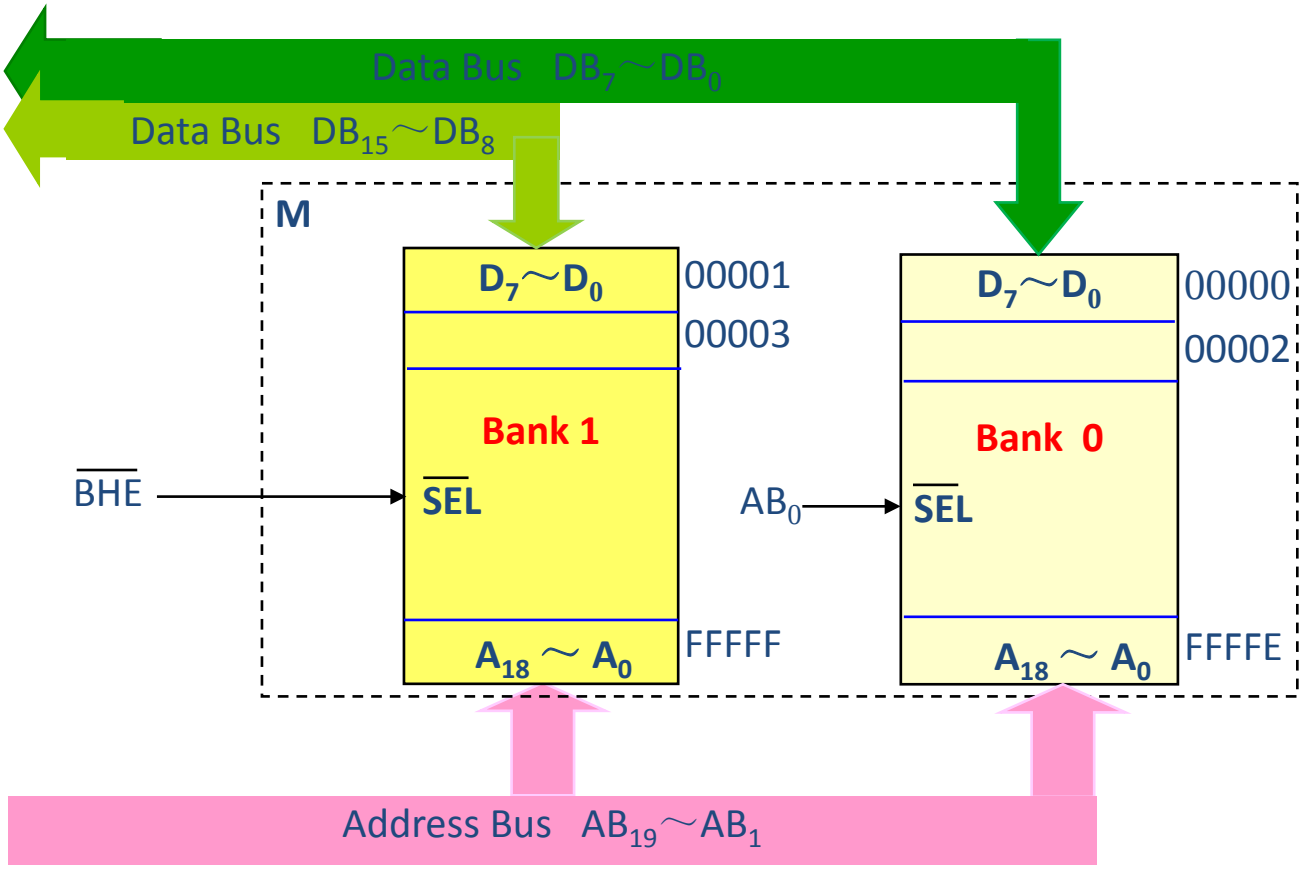


configuration

Bus Timing for Minimum Mode—Output



2.4 8086 Physics memory Organisation



Data Type in Memory

- **Byte**

  Even Address

  Odd Address

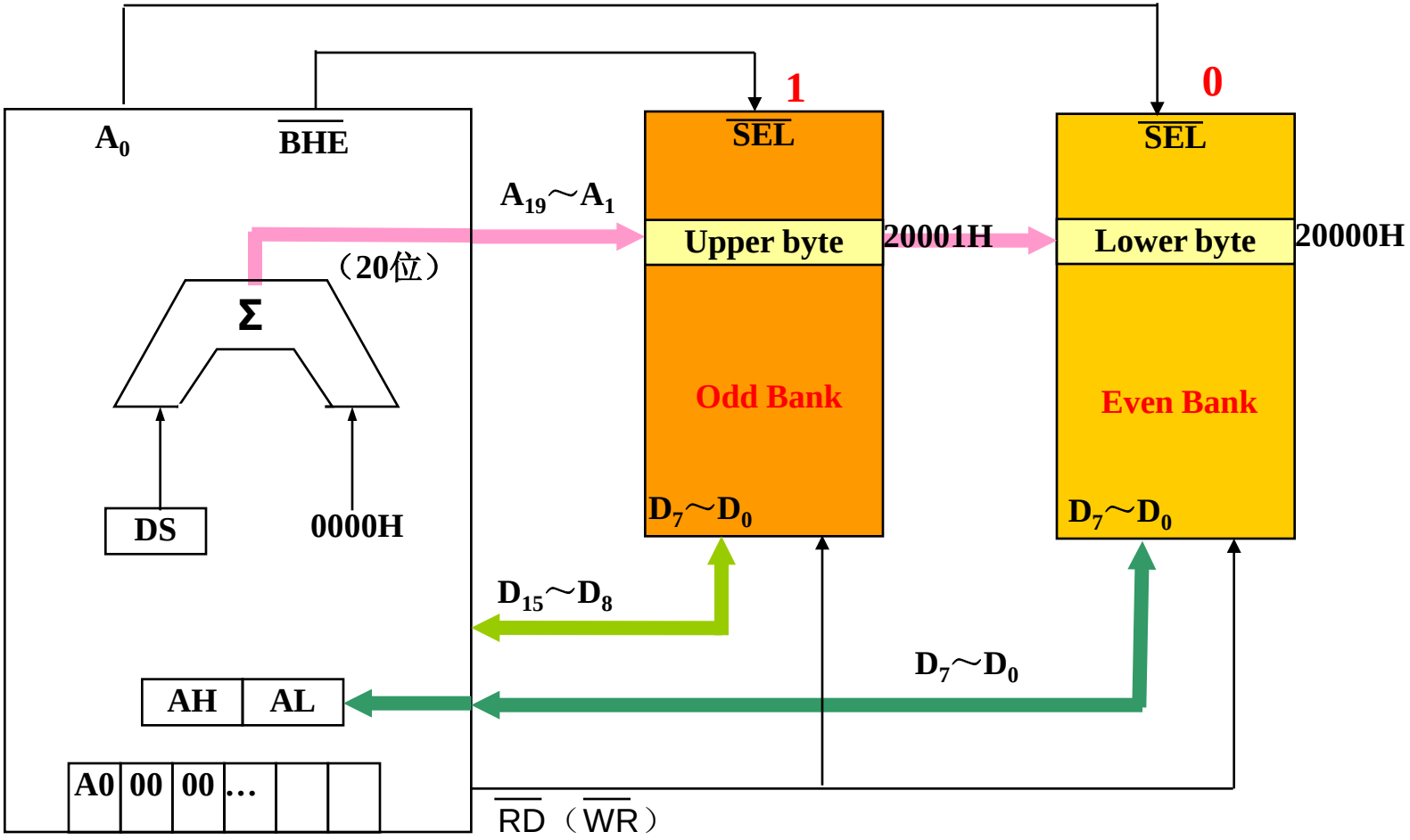
- **Word**

  Even Address

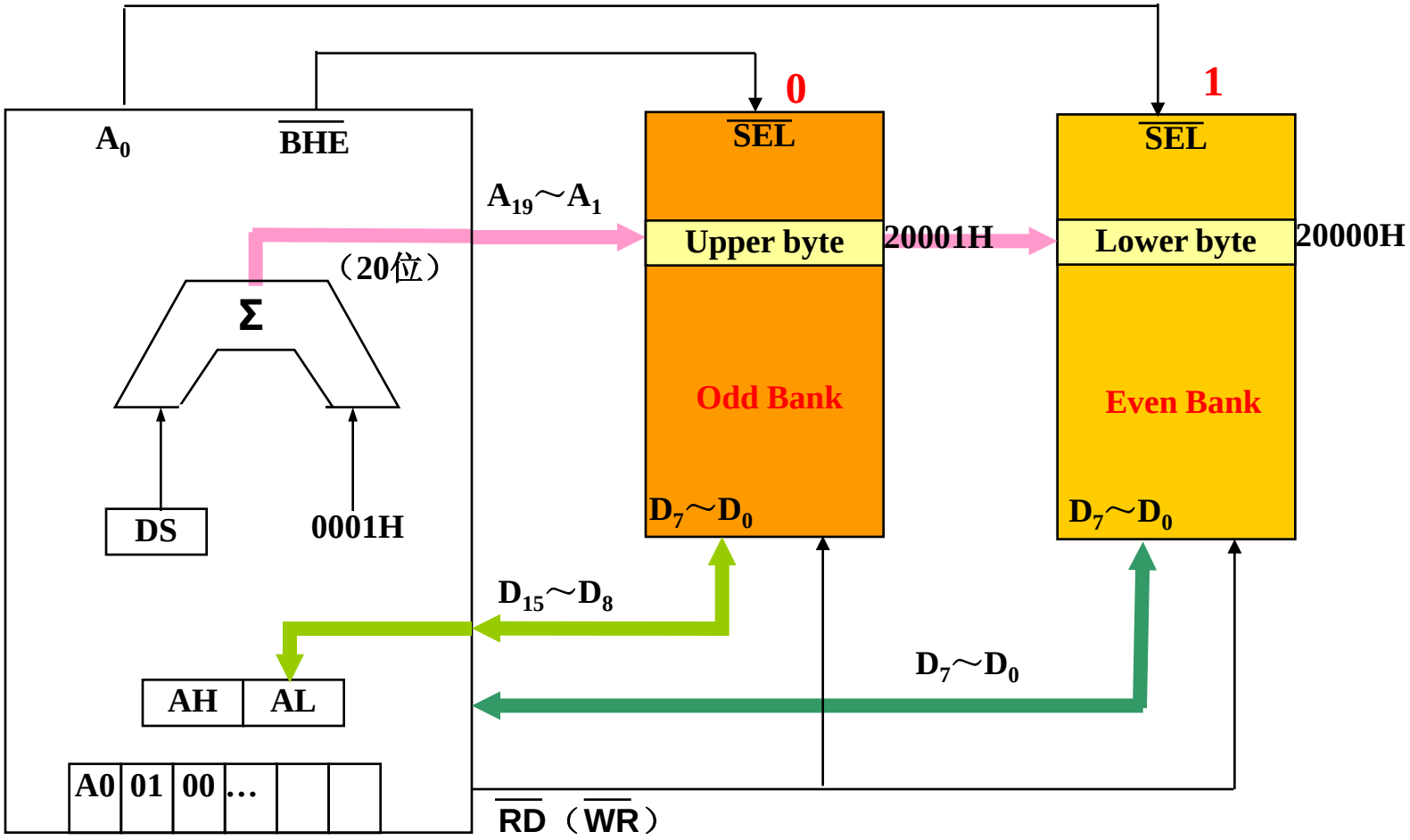
  Odd Address

- **DoubleWord**

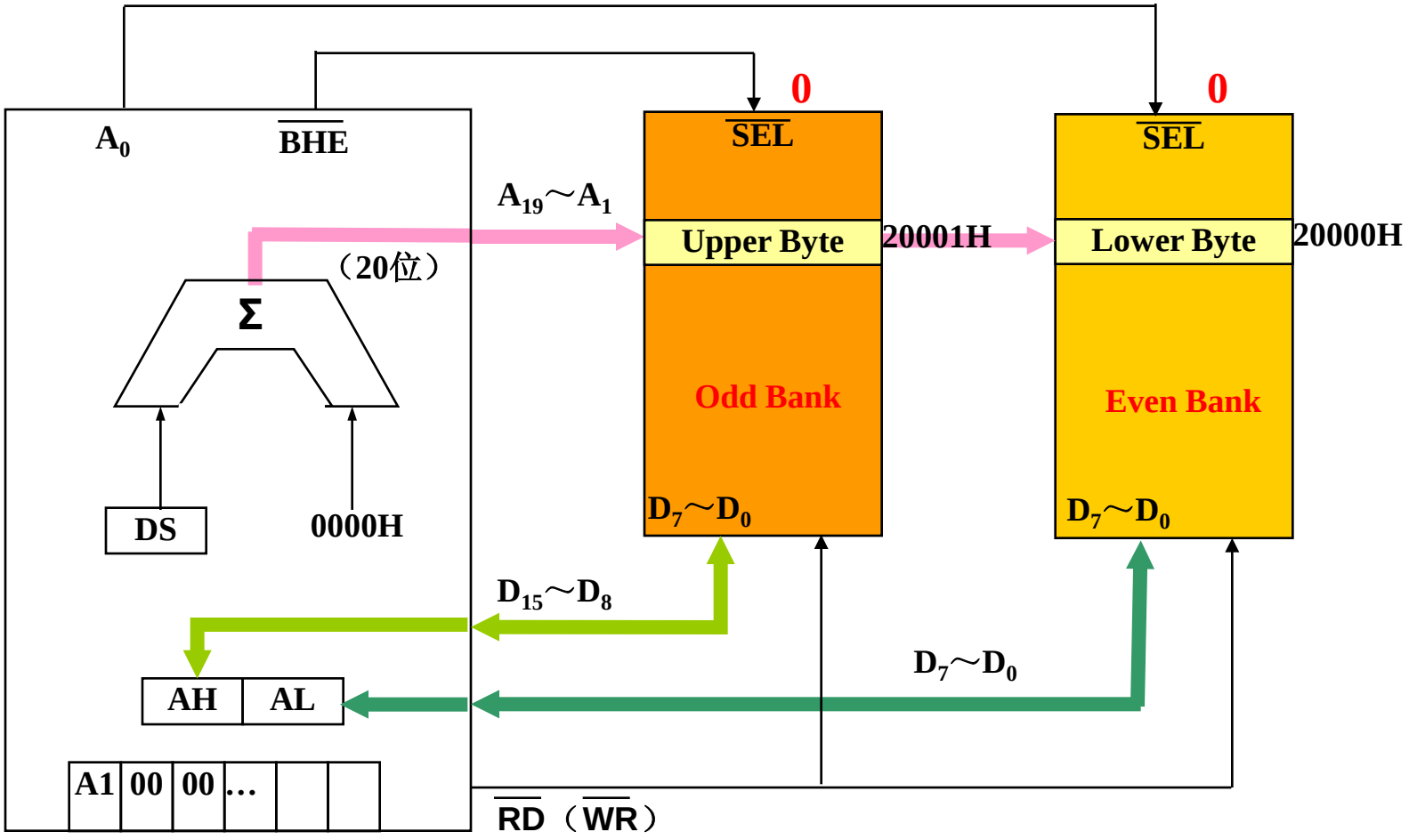
Data Transfer ——Even Address Byte



Data Transfer——Odd Address Byte



Data Transfer ——Even Address Word



Data Transfer ——Odd Address Word