Automatic Control

Practical issues in digital control implementation

Digital controller realization

Block diagram representation of digital controllers

- We have been concerned with designing digital controllers of the form

$$C(z) = \frac{U(z)}{E(z)} = \frac{b_0 z^n + b_{n-1} z^{n-1} + \cdots + b_n}{z^n + a_1 z^{n-1} + \cdots + a_n} = \frac{b_0 + b_1 z^{-1} + \cdots + b_n z^{-n}}{1 + a_1 z^{-1} + \cdots + a_n z^{-n}}$$

$$U(z) = C(z)E(z)$$

$$\rightarrow (1 + a_1 z^{-1} + \cdots + a_n z^{-n})U(z) = (b_0 + b_1 z^{-1} + \cdots + b_n z^{-n})E(z)$$

introducing the time domain delay notation $q^{-h} f(k) = f(k-h)$

$$\rightarrow (1 + a_1 q^{-1} + \cdots + a_n q^{-n})u(k) = (b_0 + b_1 q^{-1} + \cdots + b_n q^{-n})e(k)$$

$$\rightarrow u(k) =$$
$$= -a_1 u(k-1) - \cdots - a_n u(k-n) + b_0 e(k) + b_1 e(k-1) + \cdots + b_n e(k-n)$$

Block diagram representation of digital controllers

- Now, we consider the problem of controller block diagram realization by means of basic operator blocks such as
  - time delay,
  - adder,
  - multiplier.
- Block diagram realization of digital controllers allows us to deal with implementation issues like
  - algorithm design,
  - analysis of quantization effects,
  - sensitivity analysis in the presence of parameter variation.

Direct canonical structure of digital controllers

- **Direct canonical structure (D1)**

$$C(z)=\frac{U(z)}{E(z)}=\frac{b_0+b_1z^{-1}+\cdots+b_nz^{-n}}{1+a_1z^{-1}+\cdots+a_nz^{-n}}$$

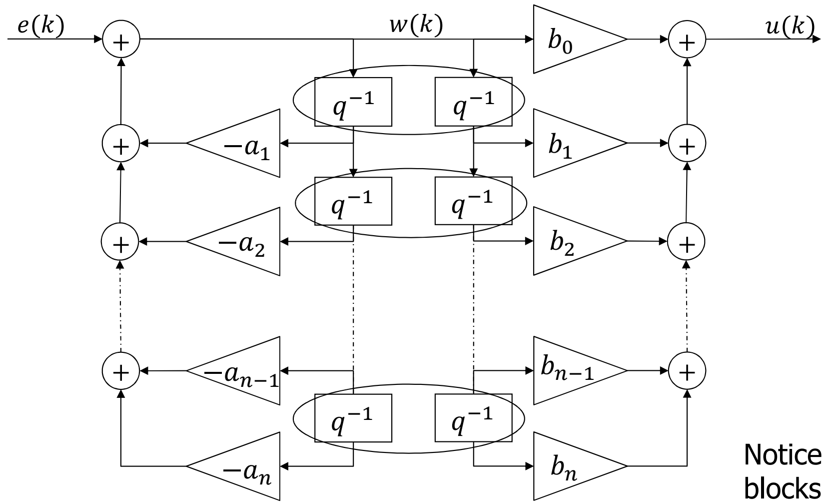
$$C(z)=\underbrace{(b_0+b_1z^{-1}+\cdots+b_nz^{-n})}_{H_1(z)}\overbrace{\frac{1}{1+a_1z^{-1}+\cdots+a_nz^{-n}}}^{H_2(z)}$$

$$W(z)\triangleq H_2(z)E(z)\rightarrow U(z)=H_1(z)W(z)$$

$$w(k)=-a_1w(k-1)-\cdots-a_nw(k-n)+e(k),$$
$$u(k)=b_0w(k)+b_1w(k-1)+\cdots+b_nw(k-n),$$

Direct canonical structure of digital controllers

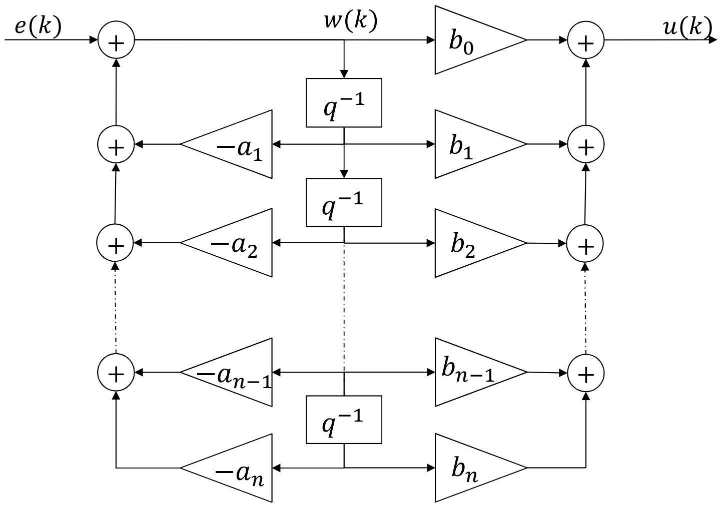
- **Direct canonical structure (D1)**



Notice that delay blocks can be grouped

Direct canonical structure of digital controllers

- **Direct canonical structure (D1)**

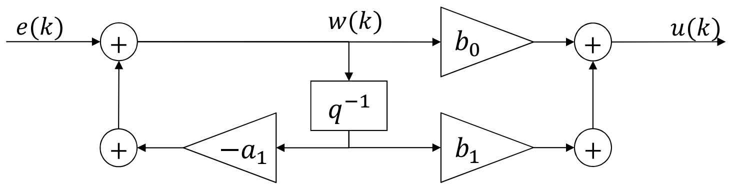


Notice that coefficients a_i and b_i appear as multipliers.

1st order filter direct canonical structure

- **Direct canonical D1 structure** for a digital 1st order filter

$$C(z)=\frac{b_0z+b_1}{z+a_1}=\frac{b_0+b_1z^{-1}}{1+a_1z^{-1}}$$

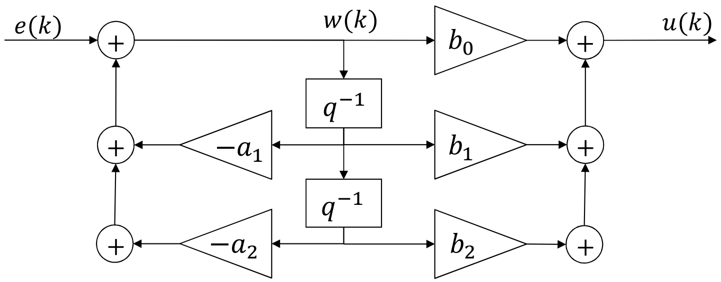


$$\rightarrow u(k)=-a_1u(k-1)+b_0e(k)+b_1e(k-1)$$

2^{nd} order filter direct canonical D1 structure

- The **direct canonical D1 structure** for digital 2^{nd} order filter of the form

$$C(z) = \frac{b_0 z^2 + b_1 z + b_2}{z^2 + a_1 z + a_2} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

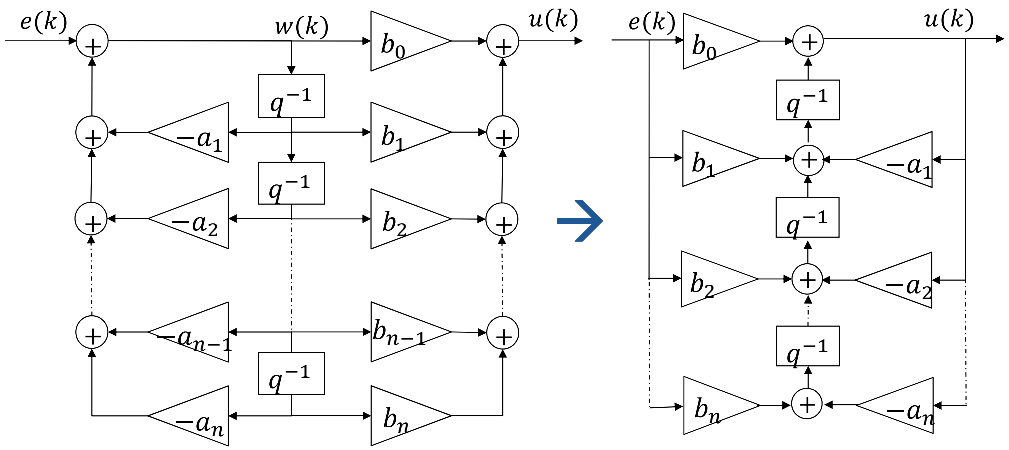


Transposed canonical structure

- Given a controller realization block diagram, an equivalent structures can be derived through the "transpose" procedure defined as
  - reverse the signal flow in all the branches of the block diagram
  - signal distribution points are transformed in summing junctions and vice versa
  - in signal derivation points and summing junctions, the inputs become outputs and vice versa.
- The transpose of a filter structure has the same transfer function as the original structure, i.e. it is equivalent.
- Transpose procedure can be exploited to derive a second direct structure.

Direct canonical structure of digital controllers

- **Direct canonical structure D2**

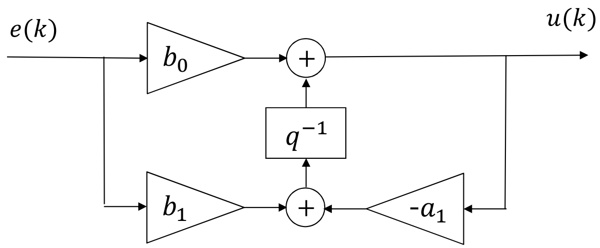


Direct D1 **Direct D2**

1^{st} order filter direct canonical D2 structure

- The **direct canonical D2 structure** for digital 1^{st} order filter of the form

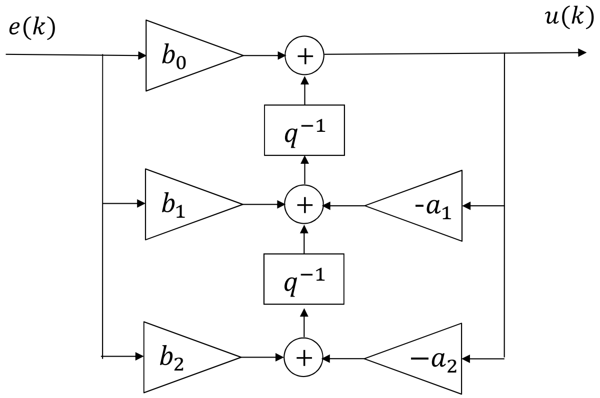
$$C(z) = \frac{b_0 z + b_1}{z + a_1} = \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}}$$



2^{nd} order filter direct canonical D2 structure

- The **direct canonical D2 structure** for digital 2^{nd} order filter of the form

$$C(z)=\frac{b_0z^2+b_1z+b_1}{z^2+a_1z+a_2}=\frac{b_0+b_1z^{-1}+b_2z^{-2}}{1+a_1z^{-1}+a_2z^{-2}}$$



Direct structure of digital controllers

- **Direct structure (D2 non canonical)**

$$C(z)=\frac{U(z)}{E(z)}=\frac{b_0+b_1z^{-1}+\cdots+b_nz^{-n}}{1+a_1z^{-1}+\cdots+a_nz^{-n}}$$

$$C(z)=\underbrace{(b_0+b_1z^{-1}+\cdots+b_nz^{-n})}_{H_1(z)}\overbrace{\frac{1}{1+a_1z^{-1}+\cdots+a_nz^{-n}}}^{H_2(z)}$$

$$V(z)\triangleq H_1(z)E(z)\rightarrow U(z)=H_2(z)V(z)$$

$$v(k)=b_0e(k)+b_1e(k-1)+\cdots+b_ne(k-n),$$
$$u(k)=-a_1u(k-1)-\cdots-a_nu(k-n)+v(k)$$

Parallel structure of digital controllers

- **Parallel structure**

$$C(z)=\frac{U(z)}{E(z)}=\frac{b_0z^n+b_{n-1}z^{n-1}+\cdots+b_n}{z^n+a_1z^{n-1}+\cdots+a_n}=\frac{b_0+b_1z^{-1}+\cdots+b_nz^{-n}}{1+a_1z^{-1}+\cdots+a_nz^{-n}}$$

- In this case the PFE of $C(z)$ is considered:

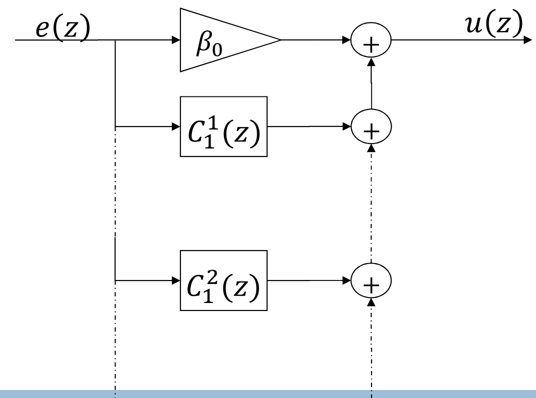
$$\tilde{C}(z)=\frac{C(z)}{z}=\frac{\beta_0}{z}+\sum_{i=1}^{n_r}\frac{\beta_i}{z-\alpha_i}+\sum_{i=1}^{n_c}\frac{\beta_{0i}z+\beta_{1i}}{z^2+\alpha_{1i}z+\alpha_{2i}},n_r+2n_c=n$$

$$C(z)=\beta_0+\sum_{i=1}^{n_r}\frac{\beta_iz}{z-\alpha_i}+\sum_{i=1}^{n_c}\frac{z(\beta_{0i}z+\beta_{1i})}{z^2+\alpha_{1i}z+\alpha_{2i}},$$
$$=\beta_0+\sum_{i=1}^{n_r}\frac{\beta_i}{1-\alpha_iz^{-1}}+\sum_{i=1}^{n_c}\frac{\beta_{0i}+\beta_{1i}z^{-1}}{1+\alpha_{1i}z^{-1}+\alpha_{2i}z^{-2}},$$

Parallel structure of digital controllers

- **Parallel structure.** The controller transfer function is realized as the parallel connection of the elementary terms

$$\beta_0,\frac{\beta_i}{1-\alpha_iz^{-1}}\rightarrow C_i^1(z),\frac{\beta_{0i}+\beta_{1i}z^{-1}}{1+\alpha_{1i}z^{-1}+\alpha_{2i}z^{-2}}\rightarrow C_i^2(z)$$

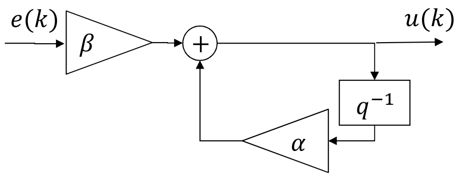


Parallel structure of digital controllers

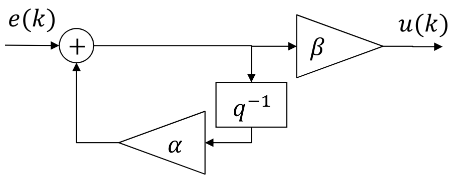
- **Parallel structure.** The basic 1st order block

$$C^1(z) = \frac{\beta}{1-\alpha z^{-1}}$$

can be realized through the following structures



pre-multiplication



post-multiplication

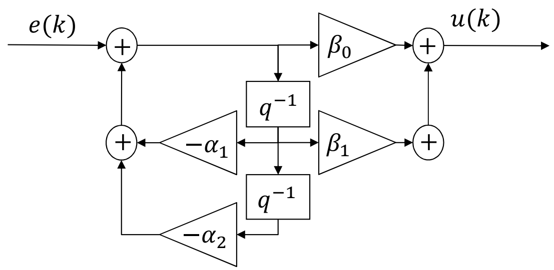
- Notice that pole α and gain β appear as multipliers.

Parallel structure of digital controllers

- **Parallel structure.** The basic 2nd order block

$$C^1(z) = \frac{\beta_0 + \beta_1 z^{-1}}{1+\alpha_1 z^{-1} + \alpha_2 z^{-2}}$$

can be realized through the structure



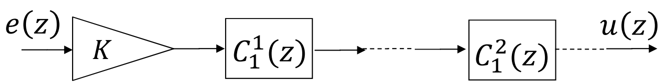
Cascade structure of digital controllers

- **Cascade structure**

$$C(z) = \frac{U(z)}{E(z)} = \frac{b_0 z^n + b_{n-1} z^{n-1} + \cdots + b_n}{z^n + a_1 z^{n-1} + \cdots + a_n} = \frac{b_0 + b_1 z^{-1} + \cdots + b_n z^{-n}}{1 + a_1 z^{-1} + \cdots + a_n z^{-n}}$$

- In this case a zero-pole factorization of $C(z)$ is considered:

$$C(z) = K \prod_{i=1}^{n_1} \underbrace{\frac{z-\beta_i}{z-\alpha_i}}_{C_i^1(z)} \prod_{i=1}^{n_2} \underbrace{\frac{z^2 + b_{1i} z + b_{2i}}{z^2 + a_{1i} z + a_{2i}}}_{C_i^2(z)}$$

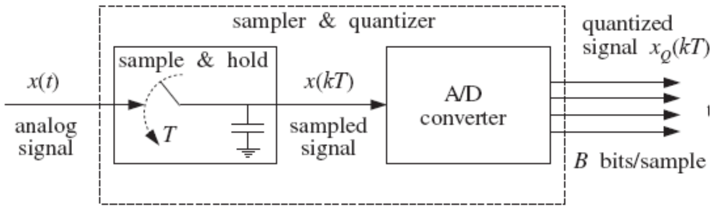


- The single blocks can be realized through similar structures as in the parallel form.

Quantization and arithmetic errors analysis

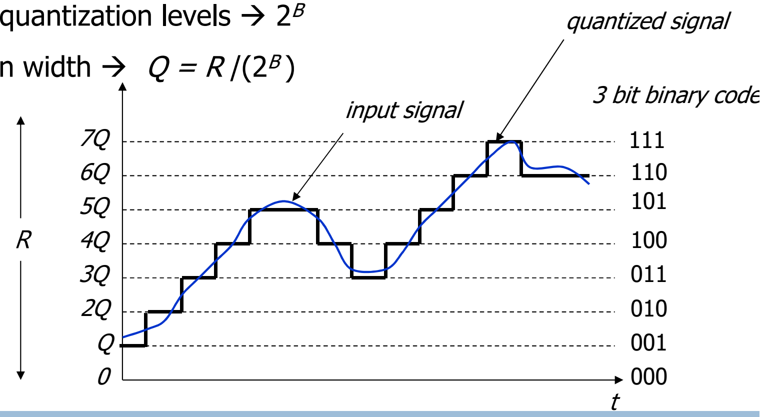
Quantization error

- Sampling and quantization are the necessary prerequisites for any analog to digital conversion.
- Quantization
  - converts actual sample values (usually voltage measurements) into an integer approximation;
  - rounds off a continuous value so that it can be represented by a fixed number of binary digits.



Quantization error

- Key parameters for an A/D converter
  - full-scale voltage range (FSR) → R
  - number of bits → B
  - number of quantization levels → 2^B
  - quantization width → $Q = R/(2^B)$



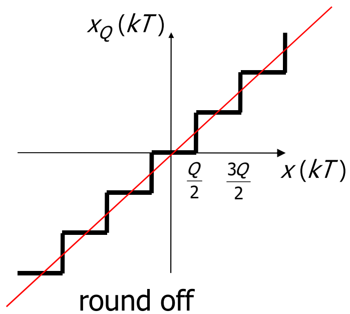
Quantization error

- Quantization can be obtained through
  - **round off**, each $x(kT)$ is replaced by the value of the nearest quantization level;
  - **truncation**, each $x(kT)$ is replaced by the quantization level below its value.
- Round off is preferred in practice because it produces a less biased quantized representation of the analog signal.
- The quantization error is defined as

$$e_Q(kT) = x_Q(kT) - x(kT)$$

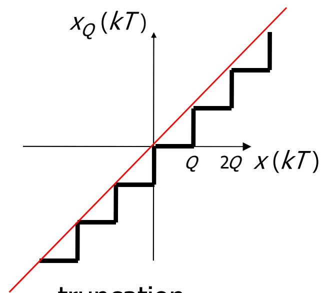
Quantization error

- Plots of the quantized value vs. variable



round off

$$-\frac{Q}{2} \le e_Q(kT) \le \frac{Q}{2}$$

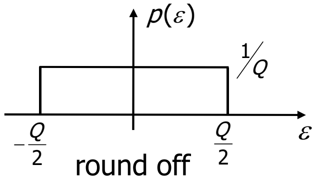


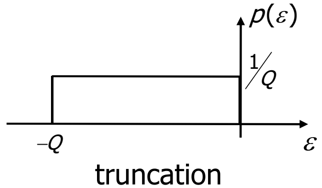
truncation

$$0 \le e_Q(kT) \le Q$$

Quantization error

- The quantization error e_Q can be described as a random variable ε which is uniformly distributed over the range.
- The probability density functions for the round off and truncation case are





$\mu_R(\varepsilon) = 0 \rightarrow$ mean value

$\sigma_R^2(\varepsilon) = \dfrac{Q^2}{12} \rightarrow$ variance

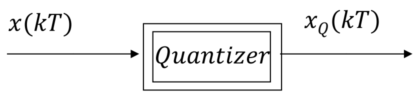
$\mu_T(\varepsilon) = -\dfrac{Q}{2} \rightarrow$ mean value

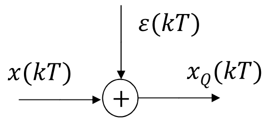
$\sigma_T^2(\varepsilon) = \dfrac{Q^2}{12} \rightarrow$ variance

Quantization error

- The probabilistic interpretation of the quantization error is useful for determining the effects of quantization as they propagate through the rest of the digital control system.
- We may think of the quantized signal x_Q as a noisy version of the original unquantized signal x to which a noise component ε has been added

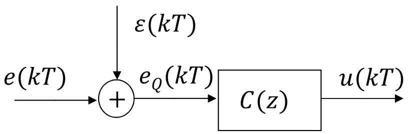
$$x_Q(kT) = x(kT) + \varepsilon(kT)$$





Quantization error propagation

- Exploiting the statistical description of the quantization error ε we can study its propagation of the over the digital controller.



- It can be shown that

$$\mu_u = \mu_\varepsilon \lim_{z\to 1} C(z)$$

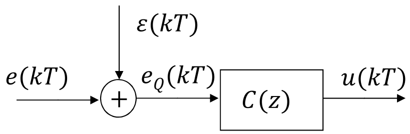
$$\sigma_u^2 = \sigma_\varepsilon^2 \sum_{i=1}^{n} \lim_{z\to z_i} \left[(z - z_i)C(z)C(z^{-1})z^{-1}\right], z_i \rightarrow i^{th} \text{ pole of } C(z)$$

- This means that the quantization propagation error depends only on the transfer function $C(z)$ and not on its realization architecture.

Quantization error propagation

- Example

$$C(z) = \frac{1}{1-\alpha z^{-1}} = \frac{z}{z-\alpha}, \alpha = e^{pT}$$



- It can be shown that

$$\mu_u = \frac{\mu_\varepsilon}{1-\alpha} = \frac{\mu_\varepsilon}{1-e^{pT}} \qquad \sigma_u^2 = \frac{\sigma_\varepsilon^2}{1-\alpha^2} = \frac{\sigma_\varepsilon^2}{1-(e^{pT})^2}$$

- Notice that

$$\sigma_u^2 \rightarrow \infty \text{ as } T \rightarrow 0$$

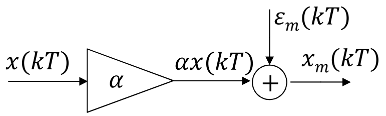
- This means that “small” sampling times emphasize quantization propagation error effects.

Multiplication error propagation

- A similar procedure can be exploited to analyze the effect of the multiplication error e_m due to the finite precision arithmetic in computing the product between a controller parameter α and a variable x

$$x_m(kT) = \alpha x(kT) + e_m(kT)$$

- The quantization error e_m can be described as a random variable ε_m with mean value μ_m and variance σ^2_m.



Multiplication error propagation: example

- Consider the controller transfer function:

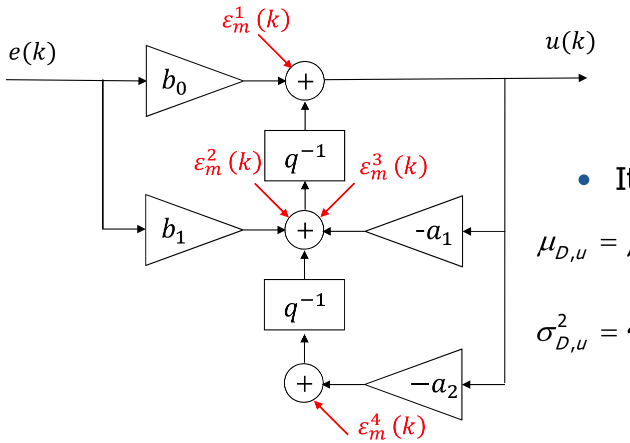
$$C(z) = \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1} + a_2 z^{-2}} = \frac{\beta_1}{1 - \alpha_1 z^{-1}} + \frac{\beta_2}{1 - \alpha_2 z^{-1}}$$

$$b_0 = \beta_1 + \beta_2, b_1 = -(\beta_1\alpha_2 + \beta_2\alpha_1), a_1 = -(\alpha_1 + \alpha_2), a_2 = \alpha_1\alpha_2$$

- We want to derive the effects of the multiplication errors propagation on the controller output.
- It is supposed that the all multiplication errors are characterized by the same mean value μ_m and variance σ^2_m.

Multiplication error propagation: example

- **Direct canonical D2 structure**



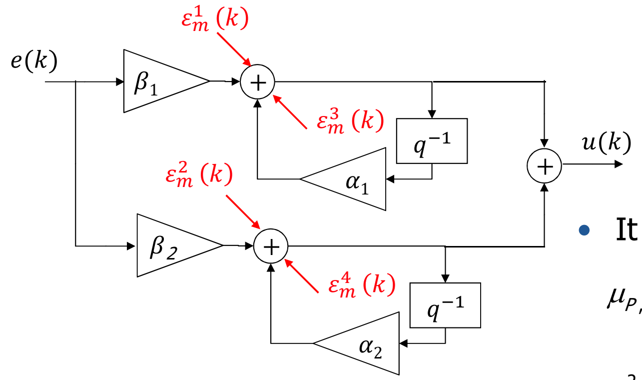
- It can be shown that

$$\mu_{D,u} = \mu_m \frac{4}{(1-\alpha_1)(1-\alpha_2)}$$

$$\sigma^2_{D,u} = 4\sigma^2_m \frac{1 + \alpha_1\alpha_2}{(1-\alpha_1\alpha_2)(1-\alpha_1^2)(1-\alpha_2^2)}$$

Multiplication error propagation: example

- **Parallel structure with pre-multiplication**



- It can be shown that

$$\mu_{P,u} = 2\mu_m\left(\frac{1}{1-\alpha_1} + \frac{1}{1-\alpha_2}\right)$$

$$\sigma^2_{P,u} = 2\sigma^2_m\left(\frac{1}{1-\alpha_1^2} + \frac{1}{1-\alpha_2^2}\right)$$

- The multiplication propagation error depends on the transfer function realization architecture.

Multiplication error propagation: example

- **Comparison**

$$\mu_{D,u} = \mu_m \frac{4}{(1-\alpha_1)(1-\alpha_2)} \qquad \mu_{P,u} = 2\mu_m\left(\frac{1}{1-\alpha_1}+\frac{1}{1-\alpha_2}\right)$$

$$\sigma^2_{D,u} = 4\sigma^2_m \frac{1+\alpha_1\alpha_2}{(1-\alpha_1\alpha_2)(1-\alpha_1^2)(1-\alpha_2^2)} \qquad \sigma^2_{P,u} = 2\sigma^2_m\left(\frac{1}{1-\alpha_1^2}+\frac{1}{1-\alpha_2^2}\right)$$

$$\frac{\mu_{P,u}}{\mu_{D,u}} = \frac{2-\alpha_1-\alpha_2}{2}, \frac{\sigma^2_{P,u}}{\sigma^2_{D,u}} = \frac{(2-\alpha_1^2-\alpha_2^2)(1-\alpha_1\alpha_2)}{2(1+\alpha_1\alpha_2)}$$

- The multiplication propagation error is improved when a parallel architecture is adopted for implementation.

Multiplication error propagation: example

- **Comparison**

$$\alpha_1 = e^{p_1T}, \alpha_2 = e^{p_2T}$$

$$\frac{\mu_{P,u}}{\mu_{D,u}} = \frac{2-\alpha_1-\alpha_2}{2} = \frac{2-e^{p_1T}-e^{p_2T}}{2},$$

$$\frac{\sigma^2_{P,u}}{\sigma^2_{D,u}} = \frac{(2-\alpha_1^2-\alpha_2^2)(1-\alpha_1\alpha_2)}{2(1+\alpha_1\alpha_2)} = \frac{(2-(e^{p_1T})^2-(e^{p_2T})^2)(1-e^{(p_1+p_2)T})}{2(1+e^{(p_1+p_2)T})}$$

- Notice also that the parallel architecture improves the multiplication propagation error as $T \to 0$.

Parameter perturbation effects

Parameter quantization error

- All the introduced controller realization architectures are equivalent when coefficients are stored with infinite precision.

$$C(z) = \frac{U(z)}{E(z)} = \frac{b_0z^n + b_{n-1}z^{n-1}+\cdots+b_n}{z^n + a_1z^{n-1}+\cdots+a_n} = \frac{b_0+b_1z^{-1}+\cdots+b_nz^{-n}}{1+a_1z^{-1}+\cdots+a_nz^{-n}}$$

- Implementation procedures require to round off the polynomial coefficients according to the machine accuracy (in the case of fixed point computation devices).
- Now, we analyze the effects induced by a parameter perturbation to a pole of the controller transfer function.

Parameter quantization error

- We consider the denominator polynomial

$$P(z) = z^n + a_1 z^{n-1} + \cdots + a_n$$

of

$$C(z) = \frac{b_0 z^n + b_1 z^{n-1} + \cdots + b_n}{z^n + a_1 z^{n-1} + \cdots + a_n}$$

- Suppose that in the presence of a perturbation of the nominal parameter

$$a_i = \bar{a}_i$$
$$\rightarrow a_i = \bar{a}_i + \delta a_i$$

the j^{th} root of polynomial P is moved in $z_j + \delta z_j$

$$\rightarrow P(z_j + \delta z_j, \bar{a} + \delta a) = 0$$

Parameter quantization error

- We can study the properties of the perturbed polynomial

$$P(z_j + \delta z_j, \bar{a}_i + \delta a_i)$$

through its 1st order Taylor expansion

$$P(z_j + \delta z_j, \bar{a}_i + \delta a_i) = P(z_j, \bar{a}_i) + \left.\frac{\partial P}{\partial z}\right|_{z=z_j} \delta z_j + \frac{\partial P}{\partial a_i}\delta a_i + \ldots = 0$$

- We obtain

$$\delta z_j = -\frac{\partial P/\partial a_i}{\left.\partial P/\partial z\right|_{z=z_j}}\delta a_i$$

Structure of digital controllers: example

- Example. Given

$$C(z) = \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1} + a_2 z^{-2}} = \frac{\beta_1}{1 - \alpha_1 z^{-1}} + \frac{\beta_2}{1 - \alpha_2 z^{-1}}$$

- Suppose that it is implemented through the D2 canonical form
- The denominator polynomial is

$P(z) = z^2 + a_1 z + a_2$,

parameters are $a_1 = -(\alpha_1 + \alpha_2), a_2 = \alpha_1\alpha_2$

poles are $z_1 = \alpha_1, z_2 = \alpha_2$

$$\frac{\partial P}{\partial a_1} = z, \frac{\partial P}{\partial a_2} = 1, \frac{\partial P}{\partial z} = 2z + a_1$$

Structure of digital controllers: example

$$\frac{\partial P}{\partial a_1} = z, \frac{\partial P}{\partial a_2} = 1, \frac{\partial P}{\partial z} = 2z + a_1 \qquad \delta z_j = -\frac{\partial P/\partial a_i}{\left.\partial P/\partial z\right|_{z=z_j}}\delta a_i$$

$$\delta z_1 = -\frac{\partial P/\partial a_1}{\left.\partial P/\partial z\right|_{z=z_1}}\delta a_1 = -\frac{\alpha_1}{\alpha_1 - \alpha_2}\delta a_1$$

$$\delta z_1 = -\frac{\partial P/\partial a_2}{\left.\partial P/\partial z\right|_{z=z_1}}\delta a_2 = \frac{1}{\alpha_1 - \alpha_2}\delta a_2$$

- If $z_1 = \alpha_1 = e^{p_1 T_s}, z_2 = \alpha_2 = e^{p_2 T_s} \quad T_s \rightarrow 0 \Rightarrow \alpha_1 \approx \alpha_2$

controller poles are quite sensitive to parameter variation if a direct structure is used for implementation.

Structure of digital controllers: example

- On the other hand, if a parallel structure is chosen for implementation

$$C(z)=\frac{\beta_1 z}{z-\alpha_1}+\frac{\beta_2 z}{z-\alpha_2}$$

- Perturbation on either α_1 or α_2 , directly affects the pole value, thus the sensitivity is constant to 1 and does not depend on the sampling time.

Concluding remarks

- Small sampling times emphasize quantization errors and controller parameters perturbation.
- Parallel architectures improve both parametric and arithmetic computation errors.
- Direct architectures are weak in the presence of both parametric and arithmetic computation errors.