

EMMAN ACE G. MENION
BSCpE 3A

LABORATORY 6

LOGIC GATE SYMBOL:

The screenshot displays the Intel FPGA IDE interface with the following components:

- Project Navigator:** Shows the project hierarchy with 'Cyclone IV E: AUTO' and 'xor_gate'.
- Entity Instance:** Lists the components in the design, including 'xor_gate'.
- Tasks:** A list of tasks such as 'Compile Design', 'Analysis & Synthesis', 'Fitter (Place & Route)', 'Assembler (Generate programming files)', 'Timing Analysis', 'EDA Netlist Writer', and 'Edit Settings'.
- RTL Viewer:** Displays the Verilog code for the 'xor_gate' entity. The code defines the entity with two inputs (X, Y) and one output (Z), and implements the XOR logic using a behavioral model.
- Netlist Navigator:** Shows the netlist for the 'xor_gate' entity.
- RTL Diagram:** A graphical representation of the XOR gate logic, showing two inputs (X and Y) connected to an XOR gate symbol, which produces the output Z.

The bottom status bar shows the system clock at 10:48 AM on 2/16/2023, and the CPU usage is 100%.

VHDL CODE:

```

1      Library IEEE;
2          use IEEE.std_logic_1164.all;
3
4      entity xor_gate is
5      Port (
6          X: in STD_LOGIC;
7          Y: in STD_LOGIC;
8          Z: out STD_LOGIC
9      );
10     end xor_gate;
11     --Dataflow model
12
13     architecture behav1 of xor_gate is
14     begin
15
16         Z<= x xor y; --Signal Assignment Statement
17
18     end behav1;
19
20
21     architecture behav2 of xor_gate is
22     begin
23
24     process (x, y)
25     begin
26
27     If (x/=y) then          -- Compare with truth table
28         Z <= '1';
29     else
30         Z<= '0';
31     end if;
32
33     end process;
34     end behav2;

```

OUTPUT WAVEFORM:

