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BSCPE 3A

VHDL CODE FOR 2-bit comparator:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity comparator is
   Port (
      a : in  STD_LOGIC_VECTOR(1 downto 0);
      b : in  STD_LOGIC_VECTOR(1 downto 0);
      y : out STD_LOGIC_VECTOR(2 downto 0)
   );
end comparator;

architecture Behavioral of comparator is
   signal a_u, b_u : unsigned(1 downto 0);
begin
   a_u <= unsigned(a);
   b_u <= unsigned(b);

   process(a_u, b_u)
   begin
      if a_u > b_u then
         y <= "100";
      elsif a_u < b_u then
         y <= "001";
      else
         y <= "010";
      end if;
   end process;
end Behavioral;
```