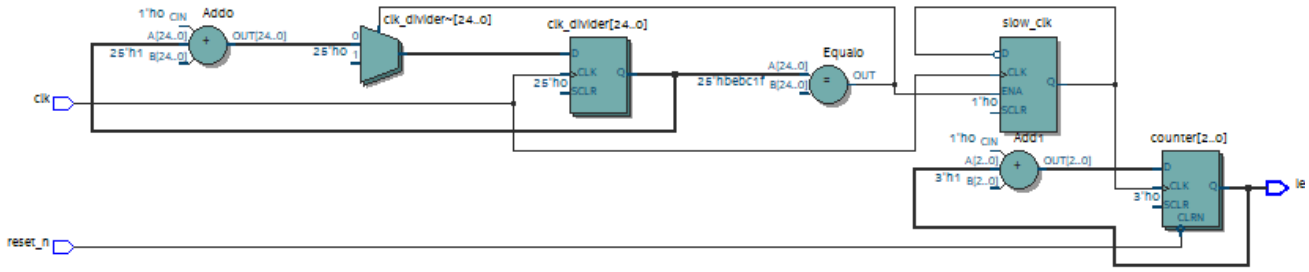
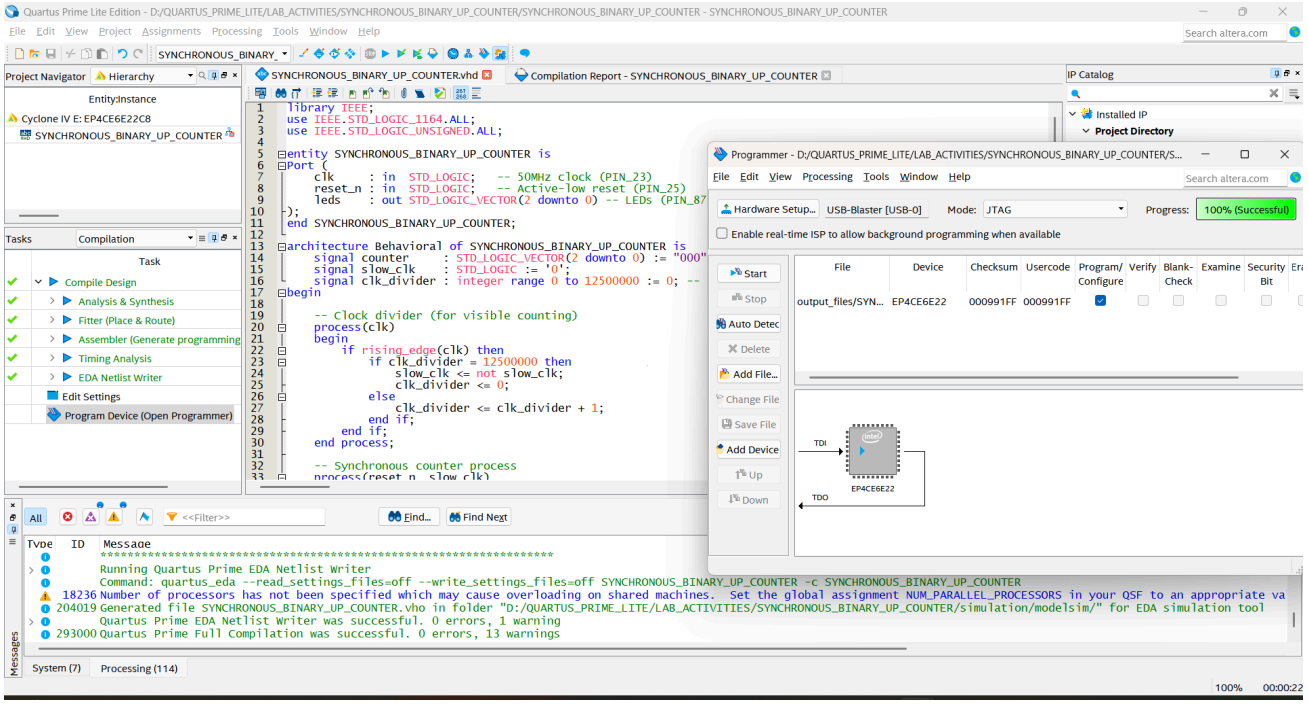
EMMAN ACE G. MENION
BSCPE 3A

SYNCHRONOUS BINARY UP COUNTER

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity practice is
Port (
   clk     : in  STD_LOGIC;                -- 50MHz clock (PIN_23)
   reset_n : in  STD_LOGIC;                -- Active-low reset (PIN_25)
   leds    : out STD_LOGIC_VECTOR(2 downto 0) -- LEDs (PIN_87,86,85)
);
end practice;

architecture Behavioral of practice is
   signal counter     : unsigned(2 downto 0) := (others => '0');
   signal slow_clk    : STD_LOGIC := '0';
   signal clk_divider : unsigned(24 downto 0) := (others => '0'); -- 25 bits for 2Hz toggle @50MHz
begin
   -- Clock divider process (50MHz → 2Hz slow clock)
   process(clk)
   begin
      if rising_edge(clk) then
         if clk_divider = 12499999 then  -- Counts to half period (for 2Hz toggle)
            clk_divider <= (others => '0');
            slow_clk <= not slow_clk;
         else
            clk_divider <= clk_divider + 1;
         end if;
      end if;
   end process;

   -- Synchronous counter
   process(reset_n, slow_clk)
   begin
      if reset_n = '0' then
         counter <= (others => '0');
      elsif rising_edge(slow_clk) then
         counter <= counter + 1;
      end if;
   end process;

   leds <= std_logic_vector(counter);

end Behavioral;
```


Add0
clk_divider~[24..0]
clk_divider[24..0]
Equal0
slow_clk
Add1
counter[2..0]
clk
reset_n


Quartus Prime Lite Edition - D:/QUARTUS_PRIME_LITE/LAB_ACTIVITIES/SYNCHRONOUS_BINARY_UP_COUNTER/SYNCHRONOUS_BINARY_UP_COUNTER - SYNCHRONOUS_BINARY_UP_COUNTER
Project Navigator
Hierarchy
Cyclone IV E: EP4CE6E22C8
SYNCHRONOUS_BINARY_UP_COUNTER
Tasks
Compilation
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
SYNCHRONOUS_BINARY_UP_COUNTER.vhd
Compilation Report - SYNCHRONOUS_BINARY_UP_COUNTER
IP Catalog
Installed IP
Project Directory
Programmer - D:/QUARTUS_PRIME_LITE/LAB_ACTIVITIES/SYNCHRONOUS_BINARY_UP_COUNTER/S...
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress:
100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detec
Delete
Add File...
Change File
Save File
Add Device
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
output_files/SYN...
EP4CE6E22
000991FF
000991FF
TDI
TDO
EP4CE6E22
Find...
Find Next
Type
ID
Message
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off SYNCHRONOUS_BINARY_UP_COUNTER -c SYNCHRONOUS_BINARY_UP_COUNTER
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate va
204019 Generated file SYNCHRONOUS_BINARY_UP_COUNTER.vho in folder "D:/QUARTUS_PRIME_LITE/LAB_ACTIVITIES/SYNCHRONOUS_BINARY_UP_COUNTER/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 13 warnings
System (7)
Processing (114)
100%
00:00:22