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BSCPE 3A

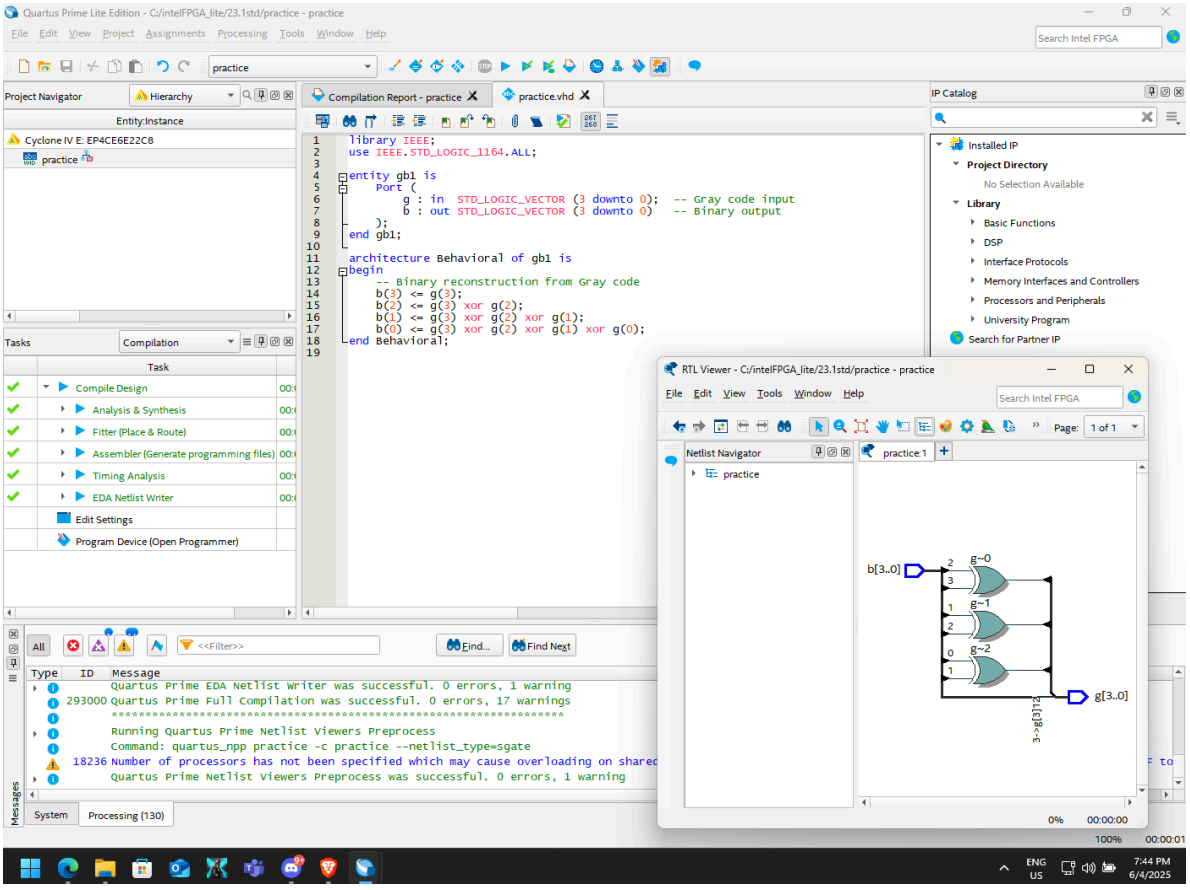
VHDL CODE FOR GRAY TO BINARY:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Binary_Gray is
   port (
      b : in  std_logic_vector(3 downto 0);  -- Binary input
      g : out std_logic_vector(3 downto 0)   -- Gray code output
   );
end Binary_Gray;

architecture Behavioral of Binary_Gray is
begin
   -- Gray code calculation:
   -- MSB is same, others are XOR of adjacent bits in binary input
   g(3) <= b(3);
   g(2) <= b(3) xor b(2);
   g(1) <= b(2) xor b(1);
   g(0) <= b(1) xor b(0);
end Behavioral;
```

INPUT				OUTPUT			
G(3)	G(2)	G(1)	G(0)	B (3)	B (2)	B (1)	B (0)
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1



Clock	QD	QC	QB	QA
0	1	0	0	1
1	1	0	0	0
2	0	1	1	1
3	0	1	1	0
4	0	1	0	1
5	0	1	0	0
6	0	0	1	1
7	0	0	1	0
8	0	0	0	1
9	0	0	0	0