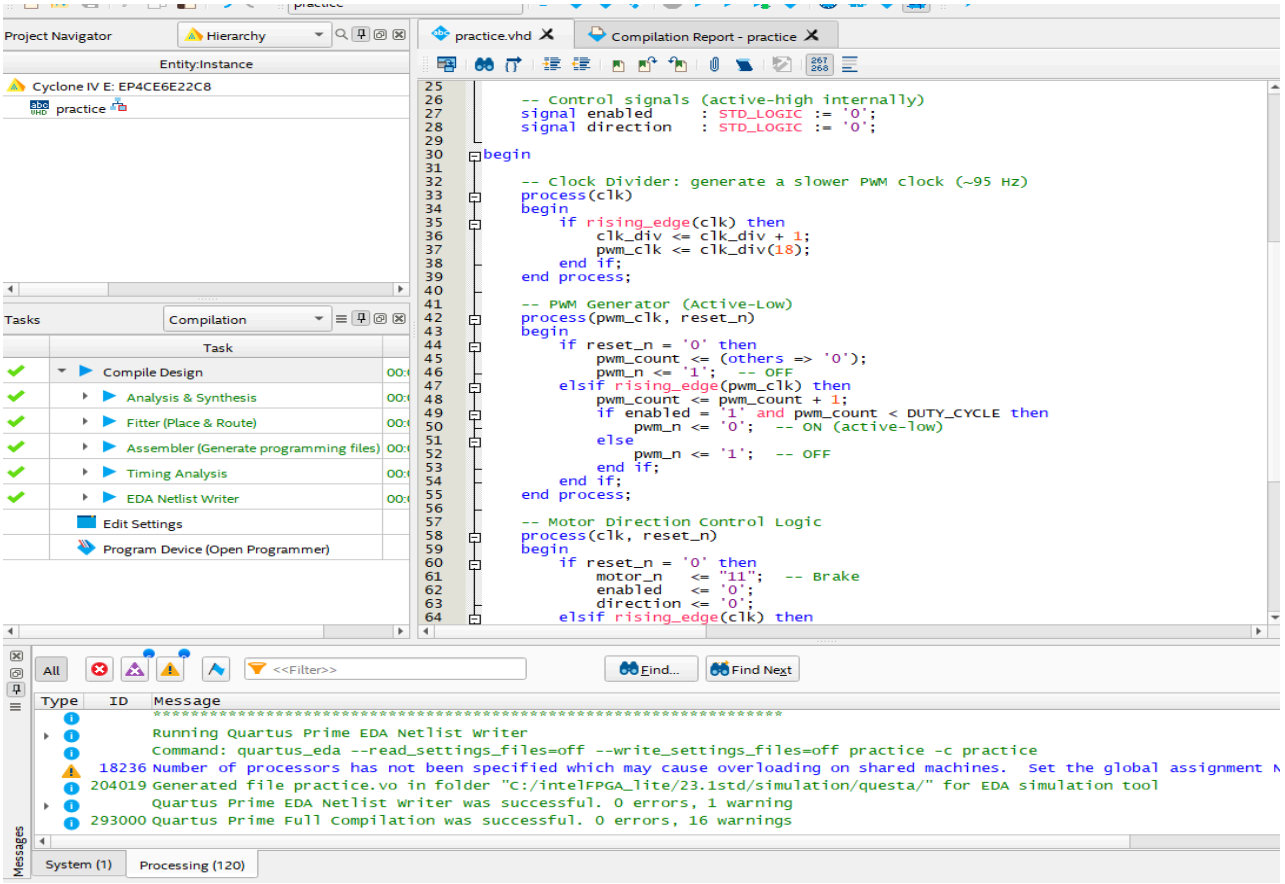
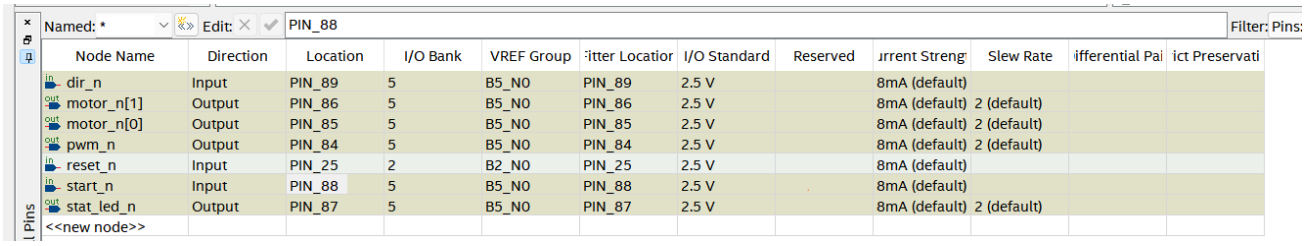
EMMAN ACE G MENION
BSCPE 3A

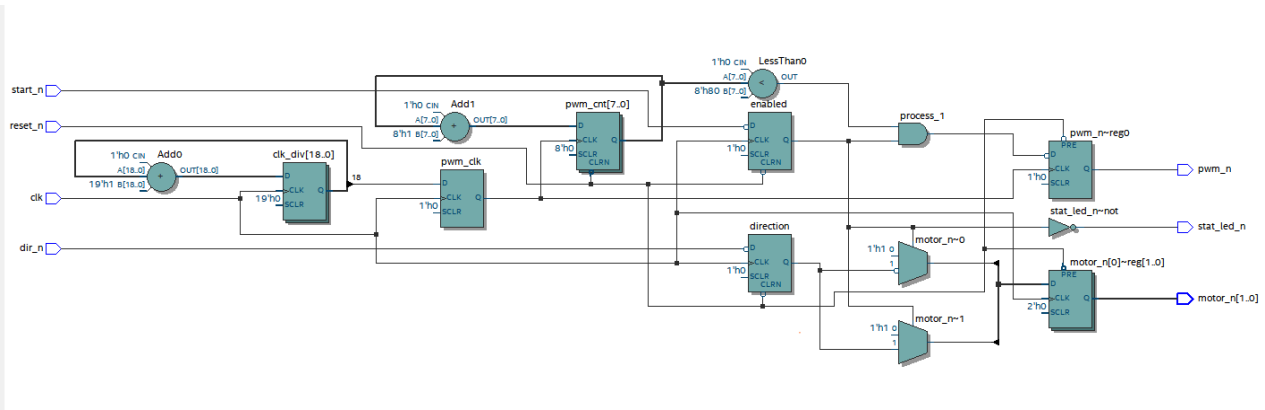
18. DC MOTOR INTERFACE

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity DC_MOTOR_INTERFACE is
    Port (
        clk        : in  STD_LOGIC;             -- 50 MHz system clock
        reset_n    : in  STD_LOGIC;             -- Active-low reset
        start_n    : in  STD_LOGIC;             -- Active-low start
        dir_n      : in  STD_LOGIC;             -- Active-low direction
        pwm_n      : out STD_LOGIC;             -- Active-low PWM output
        motor_n    : out STD_LOGIC_VECTOR(1 downto 0); -- Active-low motor direction control
        stat_led_n : out STD_LOGIC              -- Active-low status LED
    );
end DC_MOTOR_INTERFACE;

architecture Behavioral of DC_MOTOR_INTERFACE is
    -- Clock divider
    signal clk_div    : unsigned(18 downto 0) := (others => '0');
    signal pwm_clk    : STD_LOGIC := '0';

    -- PWM control
    signal pwm_count  : unsigned(7 downto 0) := (others => '0');
    constant DUTY_CYCLE : unsigned(7 downto 0) := x"80"; -- 50% duty

    -- Control signals (active-high internally)
    signal enabled    : STD_LOGIC := '0';
    signal direction  : STD_LOGIC := '0';

begin

    -- Clock Divider: generate a slower PWM clock (~95 Hz)
    process(clk)
    begin
        if rising_edge(clk) then
            clk_div <= clk_div + 1;
            pwm_clk <= clk_div(18);
        end if;
    end process;

    -- PWM Generator (Active-Low)
    process(pwm_clk, reset_n)
    begin
        if reset_n = '0' then
            pwm_count <= (others => '0');
```

```
            pwm_n <= '1';  -- OFF
        elsif rising_edge(pwm_clk) then
            pwm_count <= pwm_count + 1;
            if enabled = '1' and pwm_count < DUTY_CYCLE then
                pwm_n <= '0';  -- ON (active-low)
            else
                pwm_n <= '1';  -- OFF
            end if;
        end if;
    end process;

    -- Motor Direction Control Logic
    process(clk, reset_n)
    begin
        if reset_n = '0' then
            motor_n   <= "11";  -- Brake
            enabled   <= '0';
            direction <= '0';
        elsif rising_edge(clk) then
            enabled   <= not start_n;
            direction <= not dir_n;

            if enabled = '1' then
                if direction = '1' then
                    motor_n <= "01";  -- CW (active-low)
                else
                    motor_n <= "10";  -- CCW (active-low)
                end if;
            else
                motor_n <= "11";  -- Brake
            end if;
        end if;
    end process;

    -- Status LED ON when enabled (active-low)
    stat_led_n <= not enabled;

end Behavioral;
```


Project Navigator
Hierarchy
Entity:Instance
Cyclone IV E: EP4CE6E22C8
practice
practice.vhd
Compilation Report - practice
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
-- Control signals (active-high internally)
signal enabled : STD_LOGIC := '0';
signal direction : STD_LOGIC := '0';
begin
-- Clock Divider: generate a slower PWM clock (~95 Hz)
process(clk)
begin
if rising_edge(clk) then
clk_div <= clk_div + 1;
pwm_clk <= clk_div(18);
end if;
end process;
-- PWM Generator (Active-Low)
process(pwm_clk, reset_n)
begin
if reset_n = '0' then
pwm_count <= (others => '0');
pwm_n <= '1'; -- OFF
elsif rising_edge(pwm_clk) then
pwm_count <= pwm_count + 1;
if enabled = '1' and pwm_count < DUTY_CYCLE then
pwm_n <= '0'; -- ON (active-low)
else
pwm_n <= '1'; -- OFF
end if;
end if;
end process;
-- Motor Direction Control Logic
process(clk, reset_n)
begin
if reset_n = '0' then
motor_n <= "11"; -- Brake
enabled <= '0';
direction <= '0';
elsif rising_edge(clk) then
All
<<Filter>>
Find...
Find Next
Type ID Message
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off practice -c practice
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment N
204019 Generated file practice.vo in folder "C:/intelFPGA_lite/23.1std/simulation/questa/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 16 warnings
Messages
System (1)
Processing (120)


Named: *
Edit:
PIN_88
Filter: Pins:
Node Name | Direction | Location | I/O Bank | VREF Group | itter Location | I/O Standard | Reserved | urrent Streng | Slew Rate | ifferential Pai | ict Preservati
dir_n | Input | PIN_89 | 5 | B5_N0 | PIN_89 | 2.5 V | | 8mA (default) | | |
motor_n[1] | Output | PIN_86 | 5 | B5_N0 | PIN_86 | 2.5 V | | 8mA (default) | 2 (default) | |
motor_n[0] | Output | PIN_85 | 5 | B5_N0 | PIN_85 | 2.5 V | | 8mA (default) | 2 (default) | |
pwm_n | Output | PIN_84 | 5 | B5_N0 | PIN_84 | 2.5 V | | 8mA (default) | 2 (default) | |
reset_n | Input | PIN_25 | 2 | B2_N0 | PIN_25 | 2.5 V | | 8mA (default) | | |
start_n | Input | PIN_88 | 5 | B5_N0 | PIN_88 | 2.5 V | | 8mA (default) | | |
stat_led_n | Output | PIN_87 | 5 | B5_N0 | PIN_87 | 2.5 V | | 8mA (default) | 2 (default) | |
<<new node>>
All Pins


start_n
reset_n
clk
dir_n
Add0
Add1
LessThan0
clk_div[18..0]
pwm_clk
pwm_cnt[7..0]
enabled
direction
process_1
pwm_n~reg0
pwm_n
stat_led_n~not
stat_led_n
motor_n~0
motor_n~1
motor_n[0]~reg[1..0]
motor_n[1..0]