

EMMAN ACE G. MENION

BSCPE 3A

BCD DOWN COUNTER:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity practice is
Port (
    clk : in STD_LOGIC;          -- Clock (PIN_23)
    reset_n : in STD_LOGIC;      -- Active-low reset (PIN_25)
    bcd_out : out STD_LOGIC_VECTOR(3 downto 0) -- QD,QC,QB,QA (MSB to LSB)
);
end practice;

architecture Behavioral of practice is
    signal counter : unsigned(3 downto 0) := "1001"; -- Start at 9
    signal slow_clk : STD_LOGIC := '0';
    signal clk_divider : unsigned(24 downto 0) := (others => '0'); -- For 2Hz @ 50MHz
begin

    -- Clock divider for visible counting (2Hz)
    process(clk)
    begin
        if rising_edge(clk) then
            if clk_divider = 12499999 then
                clk_divider <= (others => '0');
                slow_clk <= not slow_clk;
            else
                clk_divider <= clk_divider + 1;
            end if;
        end if;
    end process;

    -- BCD Down Counter Logic
    process(reset_n, slow_clk)
    begin
        if reset_n = '0' then
            counter <= "1001"; -- Reset to 9
        elsif rising_edge(slow_clk) then
            if counter = "0000" then
                counter <= "1001"; -- Reset to 9
            else
                counter <= counter - 1;
            end if;
        end if;
    end process;
```

-- Active-low LED output (0=LED ON, 1=LED OFF)

bcd_out <= not std_logic_vector(counter);

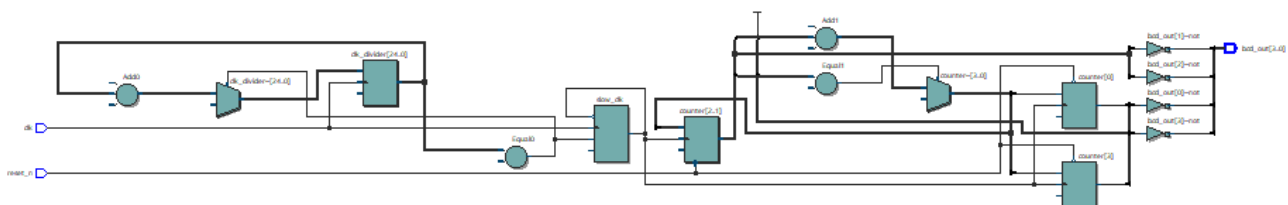
end Behavioral;

The screenshot displays the Quartus II IDE interface. The top pane shows the VHDL code for an entity named 'practice'. The code implements a BCD counter with a clock divider and a BCD down counter logic. The bottom pane shows the compilation messages, indicating that the compilation was successful with 0 errors and 16 warnings.

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.NUMERIC_STD.ALL;
4
5 entity practice is
6 port (
7     clk : in STD_LOGIC;           -- Clock (PIN_23)
8     reset_n : in STD_LOGIC;       -- Active-low reset (PIN_25)
9     bcd_out : out STD_LOGIC_VECTOR(3 downto 0) -- QD,QC,QB,QA (MSB to LSB)
10 );
11 end practice;
12
13 architecture Behavioral of practice is
14     signal counter : unsigned(3 downto 0) := "1001"; -- Start at 9
15     signal slow_clk : STD_LOGIC := '0';
16     signal clk_divider : unsigned(24 downto 0) := (others => '0'); -- For 2Hz @ 50M
17 begin
18     -- Clock divider for visible counting (2Hz)
19     process(clk)
20     begin
21         if rising_edge(clk) then
22             if clk_divider = 12499999 then
23                 clk_divider <= (others => '0');
24                 slow_clk <= not slow_clk;
25             else
26                 clk_divider <= clk_divider + 1;
27             end if;
28         end if;
29     end process;
30
31     -- BCD Down Counter Logic
32     process(reset_n, slow_clk)
33     begin
34         if reset_n = '0' then
35             counter <= "1001"; -- Reset to 9
36         elsif rising_edge(slow_clk) then
37             if counter = "0000" then
38                 counter <= "1001"; -- Reset to 9
39             else
40                 counter <= counter - 1;
41             end if;
42         end if;
43     end process;
44
45     bcd_out <= not std_logic_vector(counter);
46 end;
```

Compilation Messages:

- Running Quartus Prime EDA Netlist writer
- Command: quartus_eda --read_settings_files=off --write_settings_files=off practice -c practice
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PAR
- 204019 Generated file practice.vo in folder "C:/intelFPGA_lite/23.1std/simulation/questa/" for EDA simulation tool
- Quartus Prime EDA Netlist writer was successful. 0 errors, 1 warning
- 293000 Quartus Prime Full compilation was successful. 0 errors, 16 warnings



Clock	QD	QC	QB	QA
0	1	0	0	1
1	1	0	0	0
2	0	1	1	1
3	0	1	1	0
4	0	1	0	1
5	0	1	0	0
6	0	0	1	1
7	0	0	1	0
8	0	0	0	1
9	0	0	0	0