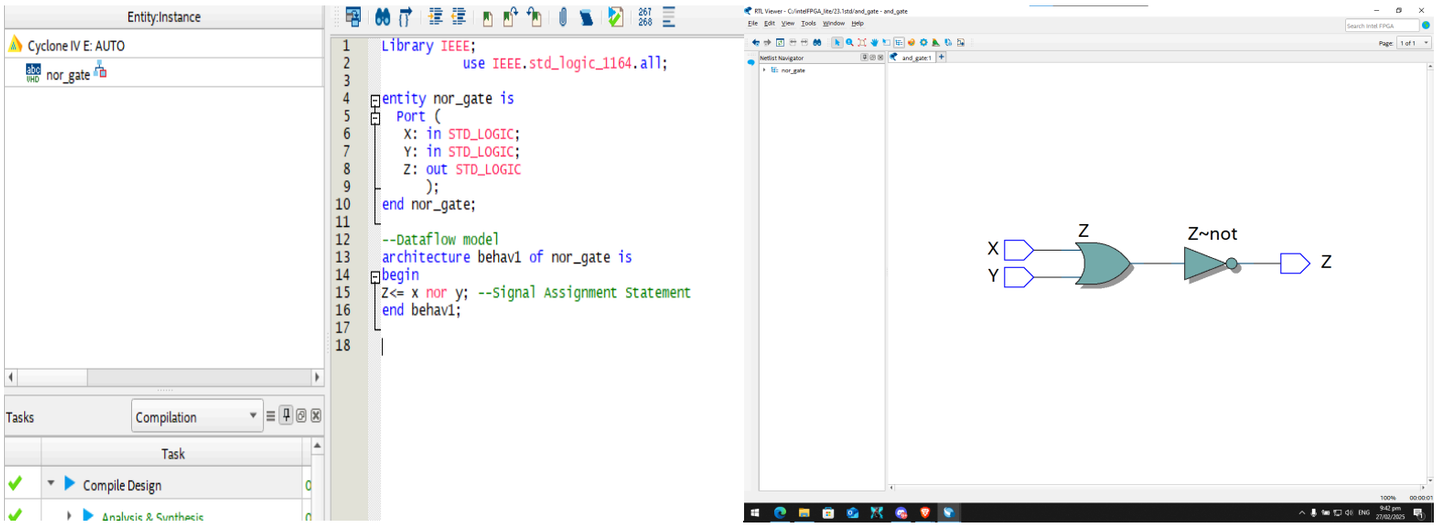
**EMMAN ACE G. MENION**
**BSCpE 3A**

## LABORATORY 5

## LOGIC GATE SYMBOL:




## VHDL CODE:

```
Ln#
 1
 2   Library IEEE;
 3               use IEEE.std_logic_1164.all;
 4
 5   entity nor_gate is
 6     Port (
 7       X: in STD_LOGIC;
 8       Y: in STD_LOGIC;
 9       Z: out STD_LOGIC
10         );
11   end nor_gate;
12
13   --Dataflow model
14   architecture behav1 of nor_gate is
15   begin
16   Z<= x nor y; --Signal Assignment Statement
17   end behav1; -- Behavioral model
18   architecture behav2 of nor_gate is
19   begin
20   process (x, y)
21   begin
22   If (x='0' and y='0') then    -- Compare with truth table
23   Z <= '1';
24   else
25   Z <= '0';
26   end if;
27   end process;
28   end behav2;
```

**OUTPUT WAVEFORM:**