EMMAN ACE G. MENION
BSCPE 3A

VHDL CODE FOR JK FLIP FLOP WITH ASYNCHRONOUS RESET: (Master Slave JK Flip-Flop)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity practice is
  Port (
    j    : in  STD_LOGIC;
    k    : in  STD_LOGIC;
    clk  : in  STD_LOGIC;
    reset : in  STD_LOGIC; -- Active-low reset
    Q    : out STD_LOGIC
  );
end practice;

architecture Behavioral of practice is
  signal counter  : unsigned(22 downto 0) := (others => '0');
  signal slow_clk : STD_LOGIC := '0';
  signal q_reg    : STD_LOGIC := '0';
  signal jk_input : STD_LOGIC_VECTOR(1 downto 0); -- For case statement
begin

  -- Clock Divider
  process(clk)
  begin
    if rising_edge(clk) then
      counter <= counter + 1;
    end if;
  end process;

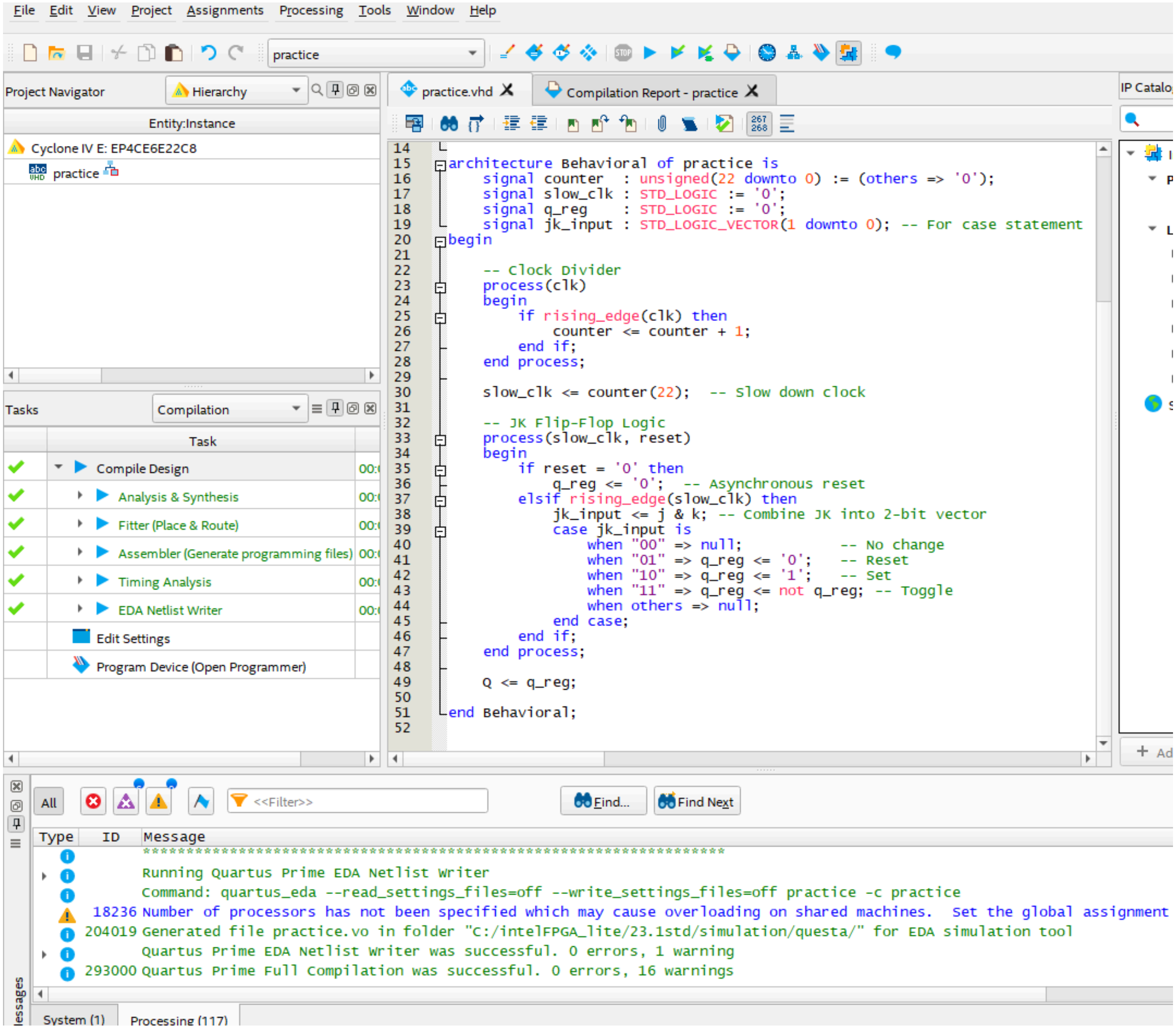
  slow_clk <= counter(22);  -- Slow down clock

  -- JK Flip-Flop Logic
  process(slow_clk, reset)
  begin
    if reset = '0' then
      q_reg <= '0';  -- Asynchronous reset
    elsif rising_edge(slow_clk) then
      jk_input <= j & k; -- Combine JK into 2-bit vector
      case jk_input is
        when "00" => null;          -- No change
        when "01" => q_reg <= '0';   -- Reset
        when "10" => q_reg <= '1';   -- Set
        when "11" => q_reg <= not q_reg; -- Toggle
        when others => null;
      end case;
```

```
        end if;
    end process;

    Q <= q_reg;

end Behavioral;
```



- ✓ Compile Design 00:
- ✓ Analysis & Synthesis 00:
- ✓ Fitter (Place & Route) 00:
- ✓ Assembler (Generate programming files) 00:
- ✓ Timing Analysis 00:
- ✓ EDA Netlist Writer 00:
- Edit Settings
- Program Device (Open Programmer)

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            end case;
        end if;
    end process;

    Q <= q_reg;

end Behavioral;
```

```
Type  ID     Message
             ******************************************************************
             Running Quartus Prime EDA Netlist Writer
             Command: quartus_eda --read_settings_files=off --write_settings_files=off practice -c practice
      18236  Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment
      204019 Generated file practice.vo in folder "C:/intelFPGA_lite/23.1std/simulation/questa/" for EDA simulation tool
             Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
      293000 Quartus Prime Full Compilation was successful. 0 errors, 16 warnings
```