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BSCPE 3A

VHDL CODE FOR JK FLIP FLOP WITH ASYNCHRONOUS RESET:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Binary_Gray is
   port (
      b : in  std_logic_vector(3 downto 0);  -- Binary input
      g : out std_logic_vector(3 downto 0)   -- Gray code output
   );
end Binary_Gray;

architecture Behavioral of Binary_Gray is
begin
   -- Gray code calculation:
   -- MSB is same, others are XOR of adjacent bits in binary input
   g(3) <= b(3);
   g(2) <= b(3) xor b(2);
   g(1) <= b(2) xor b(1);
   g(0) <= b(1) xor b(0);
end Behavioral;
```

Reset	J	K	Clock	Qn+1	$\overline{Qn+1}$	Status
1	X	X	X	0	1	Reset
0	0	0	⎍	Qn	$\overline{Qn}$	No Change
0	0	1	⎍	0	1	Reset
0	1	0	⎍	1	0	Set
0	1	1	⎍	$\overline{Qn}$	Qn	Toggle