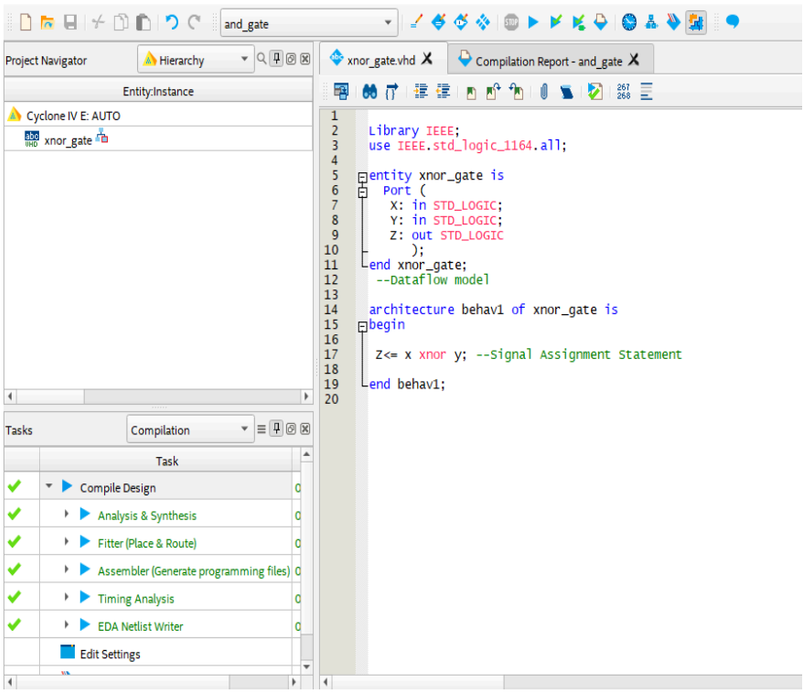
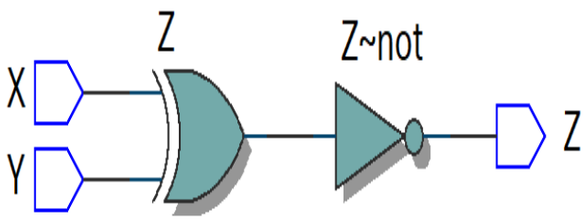
EMMAN ACE G. MENION
BSCpE 3A

LABORATORY 7

LOGIC GATE SYMBOL:





VHDL CODE:

```
Ln#
 1
 2   Library IEEE;
 3               use IEEE.std_logic_1164.all;
 4
 5   entity xnor_gate is
 6     Port (
 7       X: in STD_LOGIC;
 8       Y: in STD_LOGIC;
 9       Z: out STD_LOGIC
10       );
11   end xnor_gate;
12    --Dataflow model
13
14   architecture behav1 of xnor_gate is
15   begin
16
17    Z<= x xnor y; --Signal Assignment Statement
18
19   end behav1;
20
21    -- Behavioral model
22
23   architecture behav2 of xnor_gate is
24   begin
25
26        process (x, y)
27         begin
28
29   If (x=y) then
30   Z <= '1';
31   else
32   Z<= '0';
33   end if;
34   end process;
35   end behav2;
```

OUTPUT WAVEFORM: