

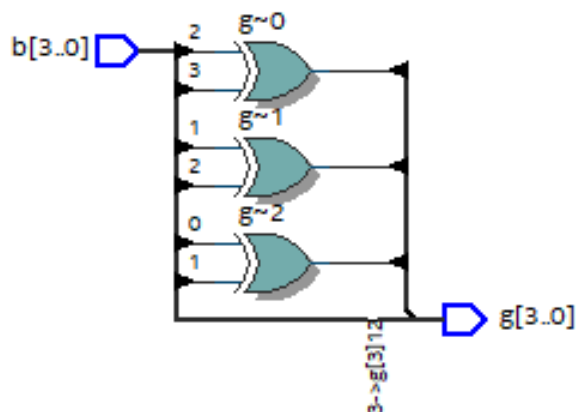
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**BSCPE 3A**

**VHDL CODE FOR Binary to gray (USING EXOR GATES):**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Binary_Gray is
    port (
        b : in  std_logic_vector(3 downto 0); -- Binary input
        g : out std_logic_vector(3 downto 0) -- Gray code output
    );
end Binary_Gray;

architecture Behavioral of Binary_Gray is
begin
    -- Gray code calculation:
    -- MSB is same, others are XOR of adjacent bits in binary input
    g(3) <= b(3);
    g(2) <= b(3) xor b(2);
    g(1) <= b(2) xor b(1);
    g(0) <= b(1) xor b(0);
end Behavioral;
```



Inputs				Outputs			
B (3)	B (2)	B (1)	B (0)	G (3)	G (2)	G (1)	G (0)
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

The screenshot displays the Quartus Prime IDE interface. The top pane shows the VHDL code for an entity named `Binary_Gray`. The code implements a behavioral model where the Gray code output `g` is calculated from the binary input `b` using XOR operations on adjacent bits.

```

1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity Binary_Gray is
5      port (
6          b : in  std_logic_vector(3 downto 0); -- Binary input
7          g : out std_logic_vector(3 downto 0) -- Gray code output
8      );
9  end Binary_Gray;
10
11 architecture Behavioral of Binary_Gray is
12 begin
13     -- Gray code calculation:
14     -- MSB is same, others are XOR of adjacent bits in binary input
15     g(3) <= b(3);
16     g(2) <= b(3) xor b(2);
17     g(1) <= b(2) xor b(1);
18     g(0) <= b(1) xor b(0);
19 end Behavioral;
20

```

The bottom pane shows the compilation tasks and messages. The tasks list includes Compile Design, Analysis & Synthesis, Fitter (Place & Route), Assembler (Generate programming files), Timing Analysis, and EDA Netlist Writer, all of which completed successfully. The messages pane shows the following output:

```

*****
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off practice -c practice
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NI
204019 Generated file practice.vo in folder "c:/intelFPGA_lite/23.1std/simulation/questa/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 17 warnings

```