EMMAN ACE G. MENION
BSCPE 3A

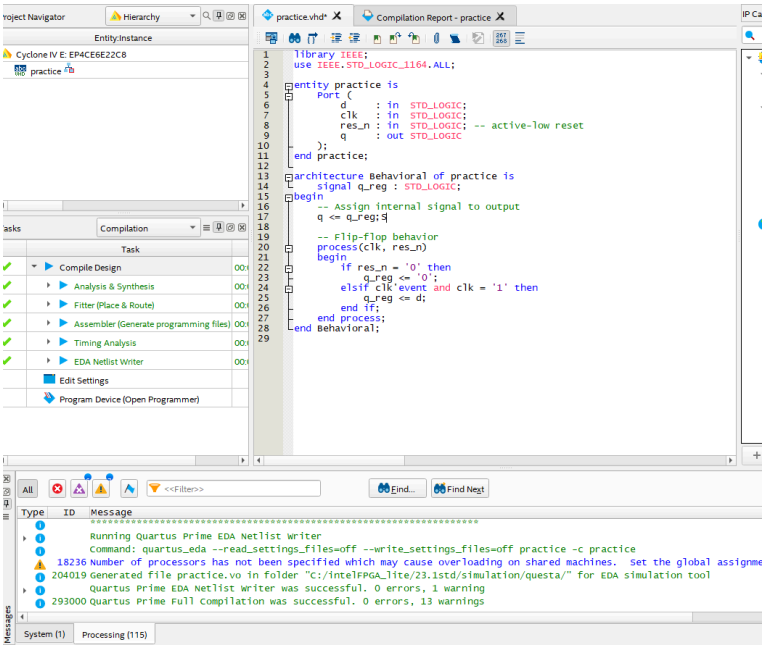
VHDL CODE FOR D FLIP FLOP:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity practice is
   Port (
      d    : in  STD_LOGIC;
      clk  : in  STD_LOGIC;
      res_n : in  STD_LOGIC; -- active-low reset
      q    : out STD_LOGIC
   );
end practice;

architecture Behavioral of practice is
   signal q_reg : STD_LOGIC;
begin
   -- Assign internal signal to output
   q <= q_reg;

   -- Flip-flop behavior
   process(clk, res_n)
   begin
      if res_n = '0' then
         q_reg <= '0';
      elsif clk'event and clk = '1' then
         q_reg <= d;
      end if;
   end process;
end Behavioral;
```



Clear	D	Clock	Qn+1	$\overline{Qn+1}$
1	0	0	0	1
0	1	⎍	1	0