Gray counter

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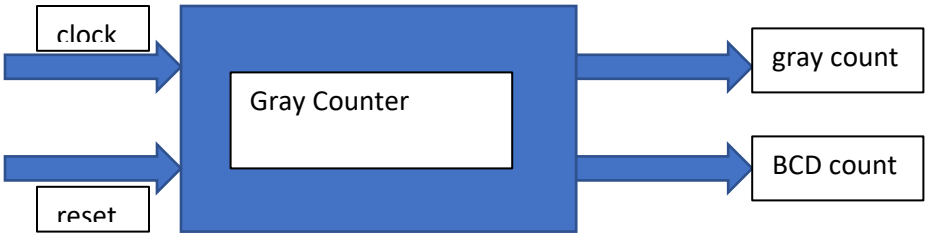
Abstract - This document is a model and analysis of a Gray counter. This model will contain a 4 bit number gray counter and its corresponding BCD count too. A reset can be triggered to start the gray counter from 0 again. It is simulated using verilog.

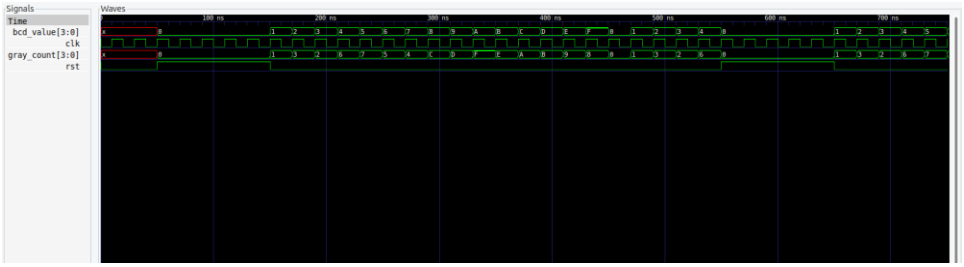
Index Terms—Reset, Clock

Intoduction- A gray counter changes 1-bit only during one state to another state transition. The counter is same like the normal incremental counter. The only difference is in binary representation. Today gray code is widely used in the digital world. It will be helpful for error correction and signal transmission. The Gray counter is also useful in design and verification in the VLSI domain.

Gray codes are widely used to prevent spurious output from electromechanical switches and to facilitate error correction in digital communications such as digital terrestrial television and some cable TV systems.

This design code has clock and reset signals and two 4 bit outputs that will generate BCD count and its respective gray count. Below are block diagram of implementation and outputs.





References:

https://www.rfwireless-world.com/source-code/VERILOG/4-bit-BCD-Synchronous-reset-counter-Verilog-code.html

https://en.wikipedia.org/wiki/Gray_code