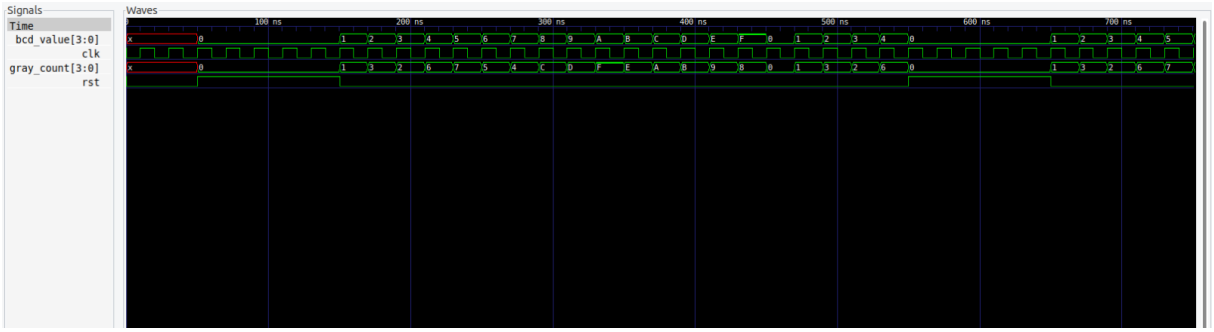
Gray Counter Report

PreSynthesis

To simulate the results, compile the source code and testbench in the verilog folder. Run GTKwave on the obtained dump file.

The resultant observed is-



Here's the expected output as taken from internet to verify the obtained results -

Decimal	Binary	Gray	Decimal of Gray
0	0000	0000	0
1	0001	0001	1
2	0010	0011	3
3	0011	0010	2
4	0100	0110	6
5	0101	0111	7
6	0110	0101	5
7	0111	0100	4
8	1000	1100	12
9	1001	1101	13
10	1010	1111	15
11	1011	1110	14
12	1100	1010	10
13	1101	1011	11
14	1110	1001	9
15	1111	1000	8

With this step we have effectively finished the Synthesis Part.

PostSynthesis

Open Yosys.

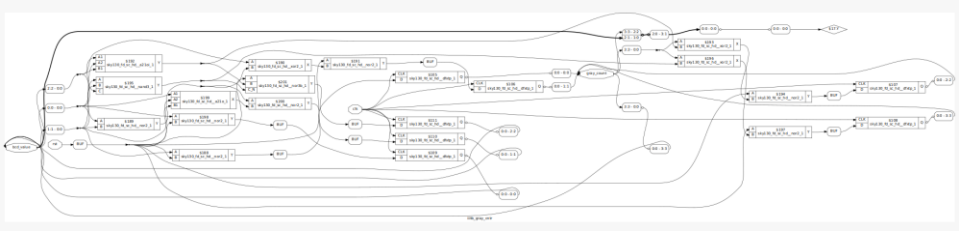
Read the library files include in the lib directory. The lib file contains the definitions of the logic cells that are to be used.

Now we synthesise the source code (iiitb_gray_cntr.v) and map the logic in gate form.

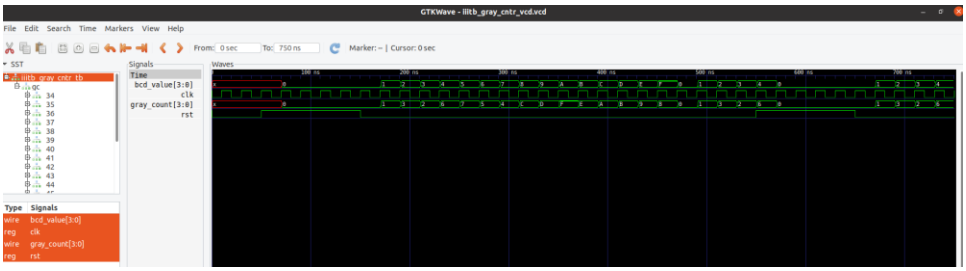
We can click ‘stat’ to see the gates count used on yosys.

```
yosys> stat

6. Printing statistics.

=== iiitb_gray_cntr ===

   Number of wires:                 38
   Number of wire bits:             50
   Number of public wires:           4
   Number of public wire bits:      10
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                 21
     sky130_fd_sc_hd__a21o_1         1
     sky130_fd_sc_hd__a21oi_1        1
     sky130_fd_sc_hd__dfxtp_1        7
     sky130_fd_sc_hd__nand3_1        1
     sky130_fd_sc_hd__nor2_1         7
     sky130_fd_sc_hd__nor3b_1        1
     sky130_fd_sc_hd__xor2_1         3
```

If we type ‘show’ we can see the output which looks as shown below.



Once we are done, we can save the netlist verilog file. To check if we are having the same outputs we can run it against testbench again. Here are the results-



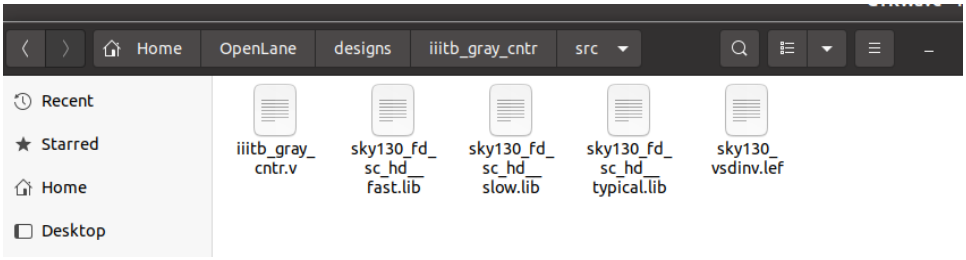
Creating Custom Inverter Cell

>Followed all the same steps for this stage from 'https://github.com/DantuNandiniDevi/iiitb_freqdiv'

An output lef file is created which will be later included in the layout stage.

Layout

Created a directory for the project design in OpenLane directory. The config file which includes all the libraries we will use has been added to our design directory. Also copied the libraries into the src directory which now looks like-



The design verilog file is the initial design and not the netlist.

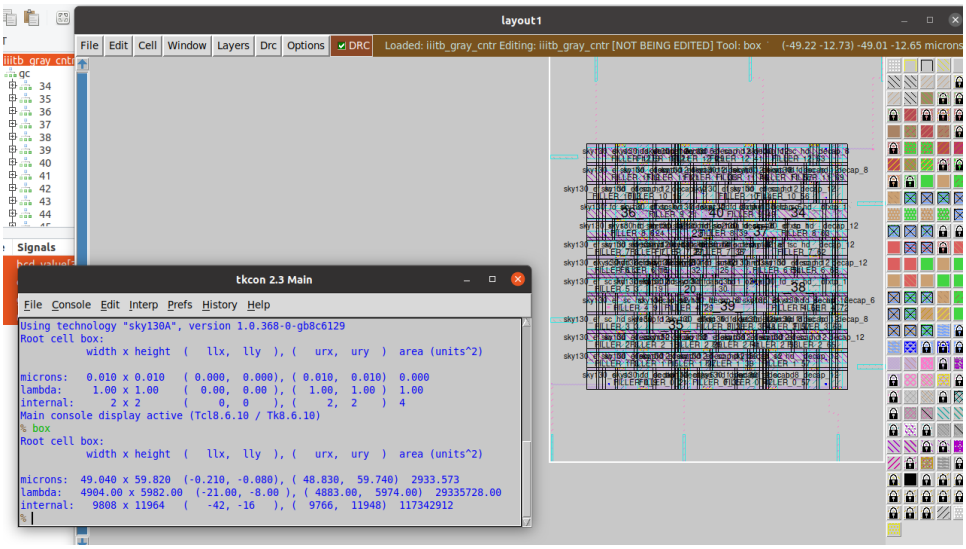
Now we type sudo make mount. This opens a container where we can do our runs.

Chip area is going to be-

```
24. Printing statistics.

=== iiitb_gray_cntr ===

   Number of wires:                 21
   Number of wire bits:             27
   Number of public wires:           4
   Number of public wire bits:      10
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                 25
     sky130_fd_sc_hd__a21boi_2       1
     sky130_fd_sc_hd__a21o_2         1
     sky130_fd_sc_hd__a21oi_2        2
     sky130_fd_sc_hd__and2_2         1
     sky130_fd_sc_hd__and3_2         1
     sky130_fd_sc_hd__and3b_2        1
     sky130_fd_sc_hd__buf_1          2
     sky130_fd_sc_hd__buf_2          1
     sky130_fd_sc_hd__dfxtp_2        7
     sky130_fd_sc_hd__nor2_2         3
     sky130_fd_sc_hd__o21a_2         2
     sky130_fd_sc_hd__o21ai_2        1
     sky130_fd_sc_hd__o21ba_2        1
     sky130_fd_sc_hd__or3_2          1

   Chip area for module '\iiitb_gray_cntr': 286.524800
```

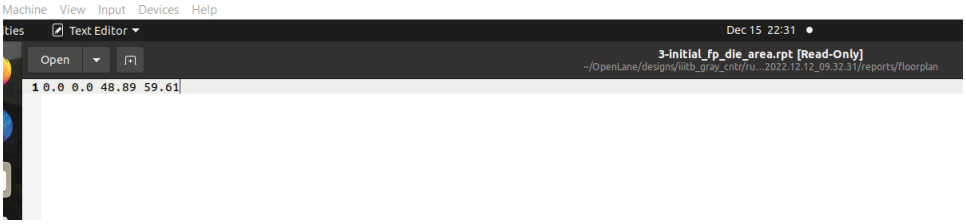
Area when checked manually tallies with what is shown in the synthesis report.

Also as seen from above report, Flop ratio = 7/25 = 0.28

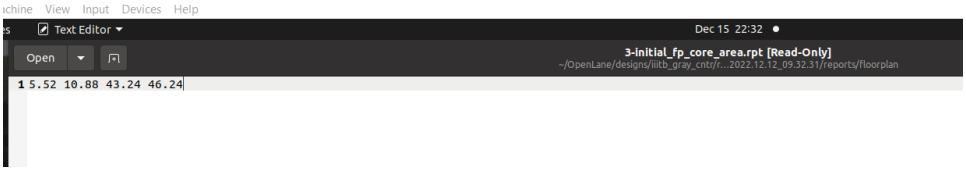


Floorplan Reports-

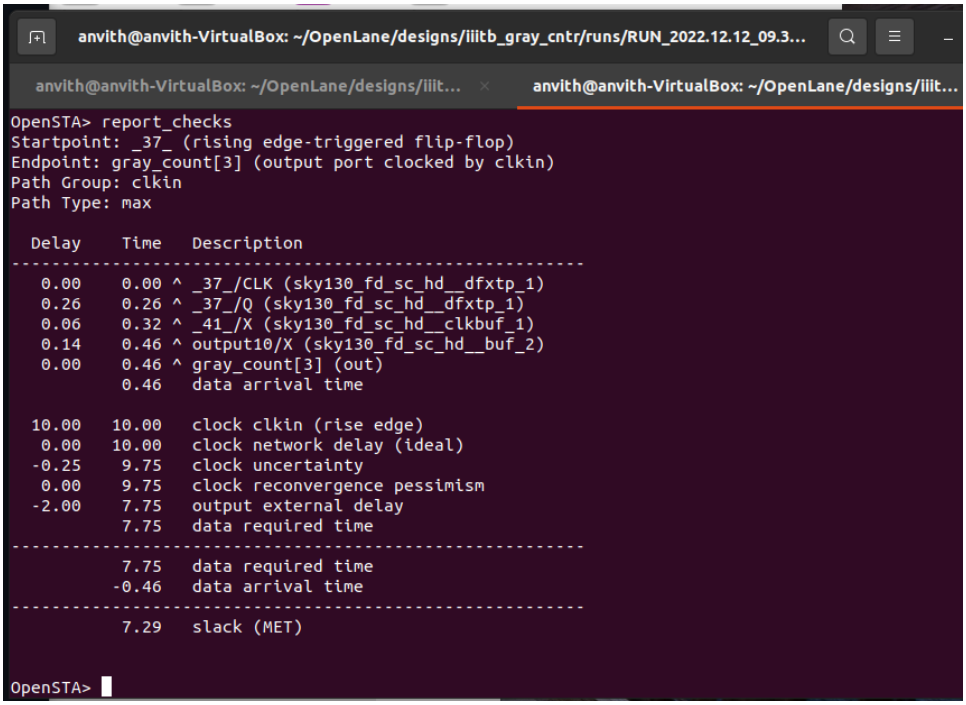
Die Area



Core Area

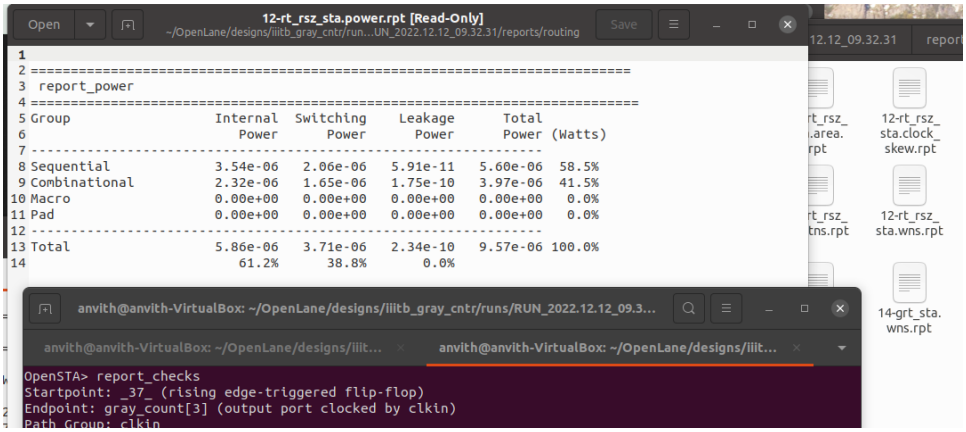


Performance and Slack Reports



Performance = 1/ (clock period - slack) = 1/(10-7.29)ns = 369MHz

Power Reports-



Internal Power = 5.86 uW (61.2%)

Switching Power = 3.71 uW (38.8%)

Leakage Power = 0.234 nW (0.00%)

Total Power = 9.57uW (100%)