

# Open SoC Debug – Software Trace Module

work-in-progress

## Introduction

This document specifies the implementation of the software trace module.

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Fill in your name here!

## Core Interface: Software Trace Port

Software Trace Port: OpenRISC

Software Trace Port: RISC-V Rocket

## Memory Map

The following map applies to the interface.

Address Range	Description	-----		-----	(TODO)		(TODO)
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