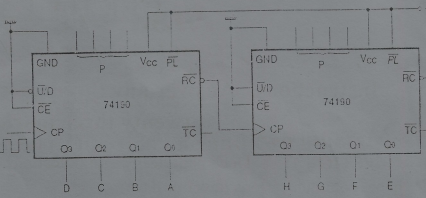
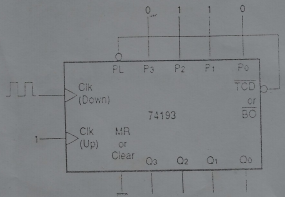
FACULTY OF FACULTY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF COMPUTER ENGINEERING
SECOND SEMESTER EXAMINATIONS 2012/2013
DIGITAL ELECTRONICS II (CEF 312) Time allowed: 3 hours

QUESTION 1 - UP/DOWN RIPPLE COUNTER (10 Marks)

a) The following figure shows a cascade arrangement of two UP/DOWN counters wired as UP counters. What will be the logic status of outputs designated as A, B, C, D, E, F, G and H after the 34th clock pulse?





b) Determine the modulus of the presettable counter shown in figure.
Does it count Upward or Downward?
If the counter were initially in the 0110 state, what would be the state of the counter immediately after the eighth clock pulse be?

QUESTION 2 - SERIAL COUNTER (20 Marks)

a) Design the serial counter that count sequence is given as follow:
   i) 1111-1110-1101-1100-1011-1010- ... -0101-1111
   ii) 0000-1010-1001-1000-0111-0110- ... -0001-0000
b) Give the modulus of the counter and draw the timing waveform diagram in each case.

QUESTION 3 - PARALLEL COUNTER (30 Marks)

a) Discuss the different possibilities of J and K logic states for the following:
   i) $Q_n = 0$, $Q_{n+1} = x$ ii) $Q_n = 1$, $Q_{n+1} = x$ iii) Conclude

b) Design a synchronous counter that counts 000-011-001-100-010-101-000-011... Ensure that the unused states of 110 and 111 go to 000 on the next clock pulse. Use J-K flip-flops.

c) What will the counter hardware look like if the unused states are to be considered as don't care's.

QUESTION 4 - SHIFT COUNTER (10 Marks)

a) Draw the time waveforms for a four-bit ring counter and a four-bit Johnson counter.
b) Determine the frequency of the output of the output flip-flop in the two cases if each counter is clocked by a 10 MHz clock signal.

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