UNIVERSITY OF BUEA

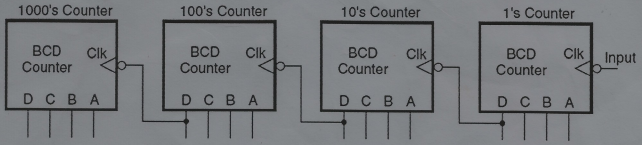
FACULTY OF ENGINEERING AND TECHNOLOGY / DEPARTMENT OF ELECTRICAL ENGINEERING

CONTINOUS ASSESMENT OF DIGITAL ELECTRONICS II (EEF 206) - June 2013

(02 Hours)

Question 1 (03 Marks)

The clock pulses are applied to the cascade arrangement of BCD counters that follows at time instant t_1 when at 0000 state. At another instant t_2 later the counter is observed to read 7364. How many negative-going clock transitions have occurred between t_1 and t_2?



Question 2 (07 Marks)

a) Design a mod-11 serial counter that counts in the reverse direction.

b) Give the count sequence and draw the timing waveform diagram.

Question 3 (08 Marks)

a) Design a binary ripple counter that counts 0000 and 1111 and skips the remaining fourteen states, that is, 0001 to 1110 (in the forward direction). Use presentable, clearable negative edge-triggered J-K flip-flops with active LOW PRESET and CLEAR inputs. Also, draw the timing waveforms

b) Draw the time waveform of the counter and determine the frequency of different flip-flop outputs for a given clock frequency, f_c.

Question 4 (12 Marks)

a) Design a synchronous counter that counts as 000, 010, 100, 110, 000, 010… Ensure that the unused states of 001, 011, 101 and 111 go to 000 on the next clock pulse. Use J-K flip-flops.

b) What will the counter hardware look like if the unused states are to be considered as don't care's.