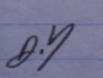


Course Title	Electronic Circuits 1
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Instructor	Dr. Fei Yuan
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Assignment/Lab Number:	N/A
Assignment/Lab Title:	Design Project

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*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a “0” on the work, an “F” in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: <http://www.ryerson.ca/senate/current/>

1. Introduction

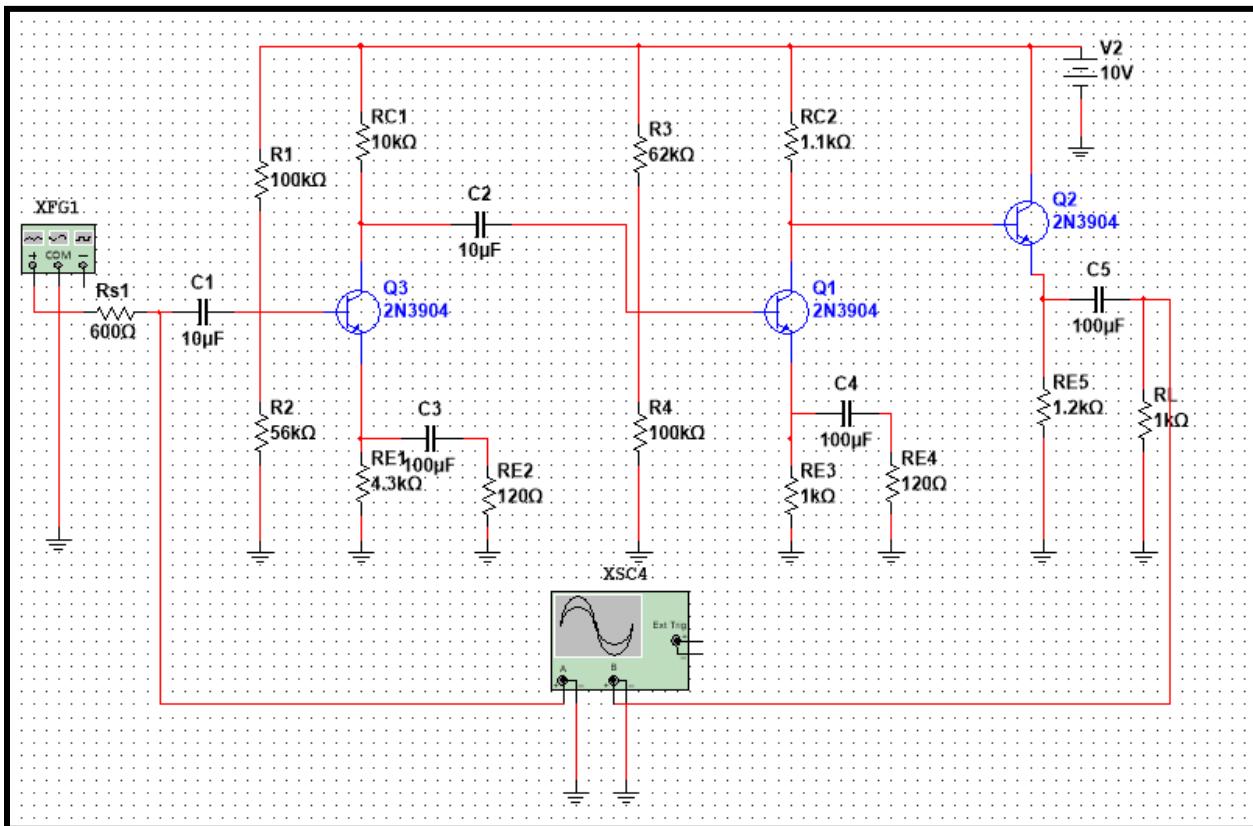
In this project I created a three stage amplifier that attempts to complete the requirements given in the design project document. Throughout this report it will show the circuit chosen, how the circuit was chosen and my entire thinking process. Not to mention the manual calculations created to find all these values and the simulations to test these values were also included. It overall shows my journey through this entire design project.

2. Objectives

- Power supply: **+10V** relative to the ground;
- Quiescent current drawn from the power supply: **no larger than 10 mA**;
- No-load voltage gain (at 1 kHz): $|A_{vo}| = 50(\pm 10\%)$;
- Maximum no-load output voltage swing (at 1 kHz): **no smaller than 8 V peak to peak**;
- Loaded voltage gain (at 1 kHz and with $R_L = 1 \text{ k}\Omega$): **no smaller than 90% of the no-load voltage gain**;
- Maximum loaded output voltage swing (at 1 kHz and $R_L = 1 \text{ k}\Omega$): **no smaller than 4 V peak to peak**;
- Input resistance (at 1 kHz): **no smaller than 20 kΩ**;
- Amplifier type: **inverting or non-inverting**;
- Frequency response: **20 Hz to 50 kHz (-3dB response)**;
- Type of transistors: **BJT**;
- Number of transistors (stages): **no more than 3**;
- Resistance permitted: **values smaller than 220 k from the E24 series**;
- Capacitors permitted: **0.1 uF, 1.0 uF, 2.2 uF, 4.7 uF, 10 uF, 47 uF, 100 uF, 220 uF**;
- Other components (BJTs, diodes, Zener diodes, etc.): **only from your ELE404 lab kit**.

3. Chosen Circuit

Diagram 1. Circuit in Multisim



4. Summary of Values

Table 1. Circuits's Capacitor Values

C1	C2	C3	C4	C5
10 μ F	10 μ F	100 μ F	100 μ F	100 μ F

Table 2. Circuits's Resistor Values

R1	R2	R3	R4	RC1	RC2	RE1	RE2	RE3	RE4	RE5	RL
100 k Ω	56 k Ω	62 k Ω	100 k Ω	10 k Ω	1.1 k Ω	4.3 k Ω	120 Ω	1 k Ω	120 Ω	1.2 k Ω	1 k Ω

5. Process of Choosing the Values

The route I decided to choose was a three stage amplifier and it consists of two CE amplifiers and one CC amplifier. It is connected in the figuration of CE-CE-CC. In order to attempt to solve this design I decided on how I wanted to break down the voltage gain of the two CE amplifiers since the third stage has a voltage gain of nearly 1. The way I decided to break it down was simply -5 and -10, so when multiplied together it would get a total voltage gain of 50. So first I worked backwards and got the values for my second stage, in order to do that I created a load line and noted down the collector current as well as a base current for the collector voltage was 5V. I did this two times because I wanted two different voltage gains, however since I planned to have a higher voltage gain in the second amplifier I chose a collector current and base current that was higher than the currents at the first amplifier. All these values were chosen from the graph created from a DC sweep. The circuit used to get these values was just a DC power source of 10 volts attached to the collector of BJT and a DC current source of 1A to the base with the emitter attached to the ground. I did not do this for the last amplifier because I didn't use any biasing resistors and all the current and node voltages can be calculated using the values given. So now let me state the steps used to determine all the node voltages, other currents, and resistors. First for the second amplifier I calculated the B value by dividing the collector current and base current. Next I calculated the gm value and also used that to determine the rbe value, after all these values were determined I was able to determine the biasing resistors and collector as well as emitter resistors. First I calculated the collector resistor because we had Vcc, the collector voltage and the collector current. After doing so I calculated only one of the resistors attached to the node at Ve because when we calculate these values in DC the capacitor becomes an open circuit. I first did the KVL loop to determine the base voltage and so first that equation I set the value for the resistor myself by checking a bunch of values. After doing so, I was able to pick the values for the biasing resistor attached to the node in a way that it works out properly for the node equation, I chose big resistors in order to increase the voltage gain of the first amplifier because it affect the small signal circuit of the first amplifier because it is the input resistance. In this design of two cascading CE's and a CC amplifier the resistance of the CC amplifier barely affects the second amplifier which is why when I drew the small signal of the second amplifier the input resistance of the third amplifier was not included. After doing all that I was able to calculate the voltage gain of the second amplifier, and find all the resistor values, node voltage, and current values for that section. Next we move onto the stage one amplifier. We again already have the collector current and base current using the DC sweep and the B, gm, and rbe value was calculated. Again we can calculate the collector resistor easily because we have all the values, and the emitter resistor was found by testing a bunch of possible values that can work. After using the nodal analysis R1 and R2 were found by using the biggest resistors possible to which also worked in the equation. Then when calculating the voltage gain, it has a similar small signal circuit to stage 2 however, the input resistance was included because it affects this amplifier and then the voltage gain was calculated. Furthermore in order to get values of -10 and -5 the missing values for any resistor were solved by simply isolating for that number. Lastly for the third amplifier the collector current was calculated as we assume the

emitter resistor in parallel with load resistor to be similar to that value. After determining this collector the base current can be found as we assume as B can be, after doing all this the rest of the numbers can easily be calculated. The voltage gain with and without the load resistor and then multiplying all these numbers to get the total values.

Stage 1. Essential Values

IC (A)	IB (A)	VB (V)	B	Gm (s)	Rbe Ω	VC (V)	$A_{vo}[V/V]$
$5 \cdot 10^{-4}$	$4 \cdot 10^{-6}$	2.8672	125	0.0192	6510.42	5.0	-5.039

Stage 2. Essential Values

IC (A)	IB (A)	VB (V)	B	Gm (s)	Rbe Ω	VC (V)	$A_{vo}[V/V]$
$4.3 \cdot 10^{-3}$	$2.7 \cdot 10^{-5}$	5.02	159	0.165	953.63	5.0	-9.67

Stage 3. Essential Values

IC (A)	VB (V)	B	Gm (s)	Rbe Ω	$A_{vo}[V/V]$	$A_{vo}[V/V]$ With load
$3.58 \cdot 10^{-3}$	5.0	150	0.13765	1090	0.99	0.987

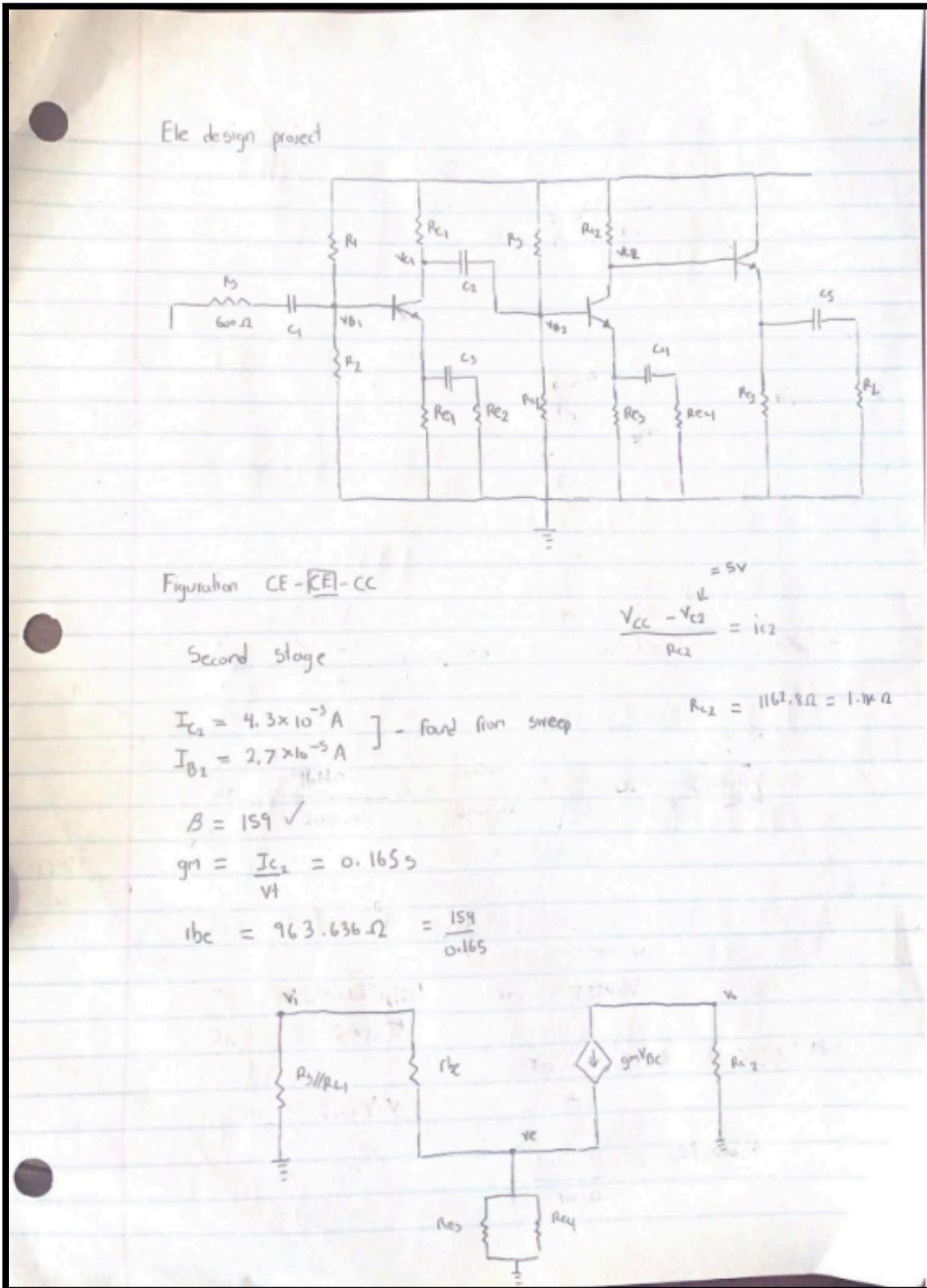
Circuit Essential Values

Rin Ω	$A_{vo}[V/V]$	Quiescent Current (mA)	$A_{vo}[V/V]$ With load
13290	48.241	8.5	48.09

Regarding the capacitor values it is important to choose values that don't affect the voltage gain. Since the biasing resistors are very large I used capacitors that were low while the emitter resistors were smaller so bigger capacitors were used. All of these values were checked using calculations and it was found that with all of these capacitors values for every scenario that resistance calculated were very low so it would relatively not affect the voltage gain. As you can see based on the multisim and the circuit draw for both the calculated values and the

experimental values the capacitors chosen did not affect the voltage gain as we get a voltage gain of 50 without the load and 47 with the load.

6. Workings



In A

KVL @ loop 2

Chosen to be
set this to 1000Ω

$$0.7 + (15911) I_{B_2} (R_{E_2}) - V_{B_2} = 0$$

$$V_{B_2} = 5.02V \quad \checkmark$$

KCL @ V_{B2} * chose big resistor

$$\frac{V_{B_2} - V_{CE}}{R_E} + \frac{V_{B_2}}{R_E} + I_{B_2} = 0$$

↓
0.02

$$\frac{5.02V - 10V}{62.000\Omega} + \frac{5.02V}{100.000\Omega} + 2.7 \times 10^{-5}A = \approx \text{close to } 0$$

Voltage gain

KCL @ V_E

$$\frac{V_E}{R_{E_2}/R_{E_1}} + \frac{V_E - V_I}{R_C} - g_m V_{BE} = 0$$

↓
V_{BE}

$$V_E \left(\frac{1}{R_{E_2}/R_{E_1}} + \frac{1}{R_C} \right) - \frac{V_I}{R_C} - g_m V_I + g_m V_C = 0$$

$$V_E = \frac{V_I \left(\frac{1}{R_C} + g_m \right)}{\left(\frac{1}{R_{E_2}/R_{E_1}} + \frac{1}{R_C} + g_m \right)}$$

KCL @ V_O

$$\frac{V_O}{R_L} + g_m (V_I - V_C)$$

Key choice
to be 120Ω

$$\frac{V_O}{V_I} = R_L \left(-g_m + \frac{g_m \left(\frac{1}{R_C} + g_m \right)}{\left(\frac{1}{R_{E_2}/R_{E_1}} + \frac{1}{R_C} + g_m \right)} \right)$$

$$\frac{V_O}{V_I} = 1100 \left(-0.165 + \frac{0.165 \left(\frac{1}{96.000} + 0.165 \right)}{\left(\frac{1}{120.000} + \frac{1}{96.000} + 0.165 \right)} \right)$$

$$A_{V_O} = -9.67$$

with no load *Hilary*to get a
voltage gain
with no

Calculating stage 1 values

$$I_{C1} = 5 \times 10^{-4} A \quad rbe = \frac{125}{g_m} = 6510.42$$

$$I_{B1} = 4 \times 10^{-6} A$$

$$\beta = 125$$

$$g_m = \frac{5 \times 10^{-4}}{0.02\mu}$$

$$\frac{10V - 5V}{R_L} = i_C$$

$$g_m = 0.0192$$

$$R_L = 10000 \Omega$$

In Qc

KVL @ loop 1

$$0.7 + (125 + 1) I_{B1} (R_{e1}) - V_{B1} = 0$$

$$V_{B1} = 2.8672 V$$

\downarrow
Change to V_C
 $4.342 V$

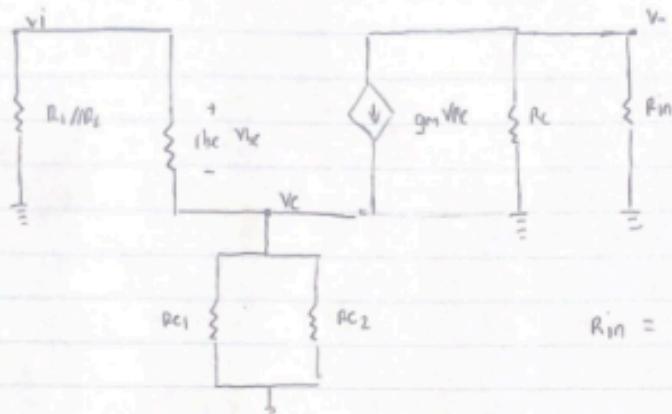
KVL @ V_{B1}

$$\frac{V_{B1} - V_{CC}}{R_1} + \frac{V_{B1}}{R_L} + I_{B1} = 0$$

$$\frac{2.8672V - 10V}{100000 \Omega} + \frac{2.8672V}{56000 \Omega} + 4 \times 10^{-6} A = 0$$

\hookrightarrow clear as it is
fill for the equation

Voltage gain



$$R_{IN} = 9.39, 97.12 \text{ for second amplification}$$

KCL @ VC

KCL @ VO

$$\frac{V_C}{V_I} = \frac{V_I \left(\frac{1}{R_E} + g_m \right)}{\left(\frac{1}{R_{C1} // R_{C2}} + \frac{1}{R_E} + g_m \right)}$$

$$\frac{V_O}{V_I} = \frac{V_O}{R_E // R_{IN}} + g_m (V_I - V_C)$$

$$\frac{V_O}{V_I} = \left(R_L // R_{IN} \right) \left(-g_m + \frac{g_m \left(\frac{1}{R_E} + g_m \right)}{\left(\frac{1}{R_{C1} // R_{C2}} + \frac{1}{R_E} + g_m \right)} \right)$$

$$\frac{V_O}{V_I} = 859.2 \left(-0.0142 + 0.0142 \left(\frac{1}{4800 // 120} + 0.0142 \right) \right)$$

$$\left(\frac{1}{4800 // 120} + \frac{1}{6310 // 12} + 0.0142 \right)$$

$$\frac{V_O}{V_I} = -5.03942$$

No Load Voltage gain

$$(-5.03942)(-4.67)$$

$$= 46.7V$$

kvl L₃

$$5 = I_{E_3} R_{E_3} + 0.7$$

$$\frac{5 - 0.7}{1200 \Omega} = 3.51 \times 10^{-3} A$$

↓
I_{E3}

$$V_{E_3} = V_{B_3} - 0.7$$

$$V_{F_3} = 4.3V$$

$$g_m = 0.137 b_f$$

Small signal without RL

$$f_{bc} = \frac{150 - f_{cut}}{1200 \Omega}$$

$$\frac{V_o}{R_{E_3}} + \frac{V_o - V_i}{r_L} - g_m (V_i - V_o)$$

$$A_v o_1 = 0, \alpha_m$$

$$\frac{V_o}{V_i} = \frac{\left(\frac{1}{r_L} + g_m \right)}{\left(\frac{1}{r_{E_3}} + \frac{1}{r_L} + g_m \right)}$$

close to unity = 1

Small signal with RL

$$\frac{V_o}{R_{E_3}} + \frac{V_o}{r_L} + \frac{V_o - V_i}{R_L} - g_m V_{bc} = 0$$

$$\frac{V_o}{V_i} = \frac{\left(\frac{1}{r_L} + g_m \right)}{\left(\frac{1}{r_{E_3}} + \frac{1}{r_L} + \frac{1}{R_L} + g_m \right)}$$

$$\frac{V_o}{V_i} = 0.987$$

without load

$$A_v o = (-4.67)(-5.0542)(0.99) = 48.241V \quad \checkmark$$

$$A_v o = (-4.67)(-5.0542)(0.987) \quad \checkmark$$

$$= 48.04V$$

DC power ✓

No load voltage gain ✓

Load voltage gain ✓

Input resistance

$$R_{in} = R_1 \parallel R_2 \parallel b_{c1} (1 + g_m R_E)$$

$$\frac{1}{\frac{1}{100,000} + \frac{1}{56,000} + \frac{1}{65,000,000(1+0.01)(\frac{1}{100,000} + \frac{1}{120})}}$$

$$\text{Input resistance} = 13290 \Omega \text{ less than } 20,000 \Omega \times$$

$$\text{Quoted current} = I_{C1} + \frac{10}{R_1 R_2} + I_{C2} + \frac{10}{R_3 R_4} + I_C$$

$$= (5 \cdot 10^{-4} A) + (3.51 \times 10^{-5} A) + (4.3 \times 10^{-5} A) + \frac{10}{100,000 + 56,000} + \frac{10}{62,000 + 100,000}$$

$$= 8.5 \text{ mA} < 10 \text{ mA}$$

Since the bias resistors are high the capacitors collected for the low

However since the emitter resistors are lower higher capacity
are needed

The white point is to keep the voltage gain low

20 Hz

$$z = \frac{1}{j2\pi(20)(100)} \quad z = \frac{1}{j2\pi(20)(10)} \quad L = 7.96 \times 10^{-4} L - 90 \Omega$$

50 kHz

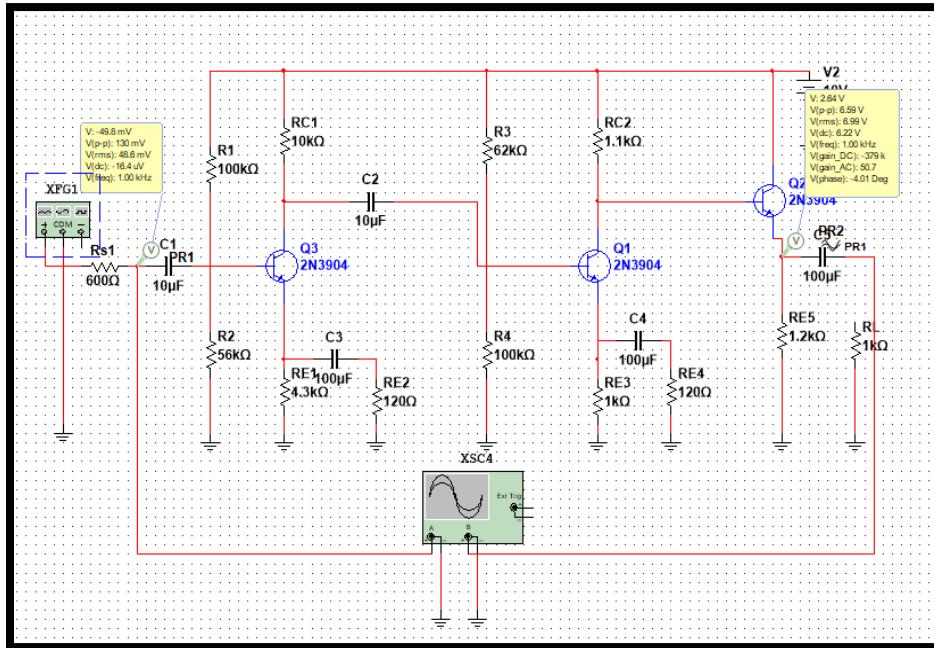
$$z = \frac{1}{j2\pi(50000)(100)} \quad z = \frac{1}{j2\pi(50000)(10)} \quad L = 3.2 \times 10^{-7} L - 90 \Omega$$

1 kHz

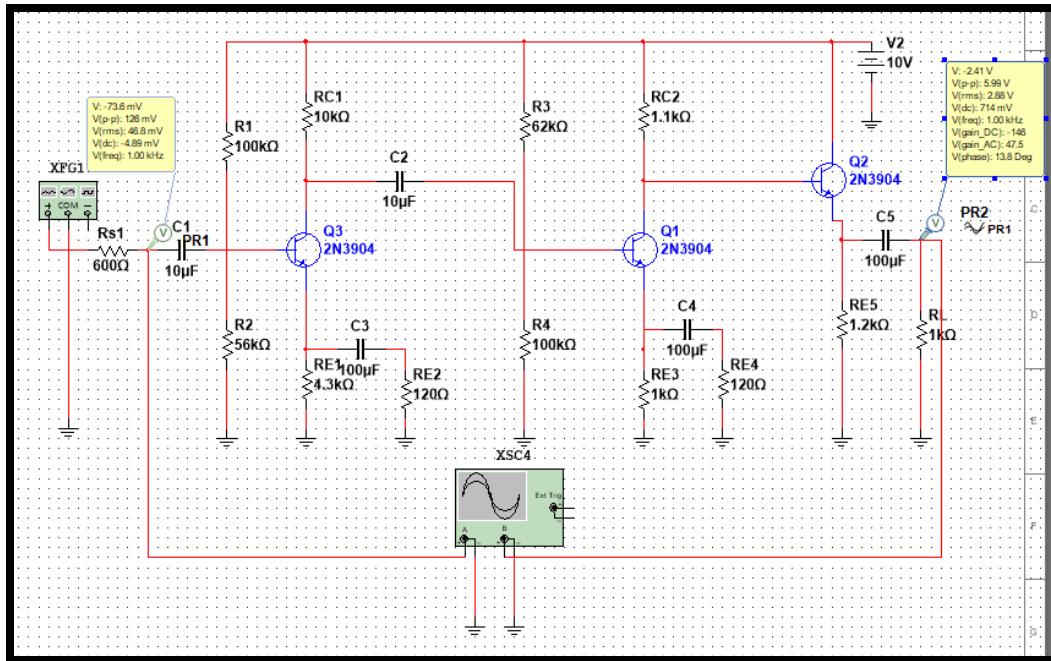
$$z = \frac{1}{j2\pi(1000)(100)} \quad z = \frac{1}{j2\pi(1000)(10)} \quad L = 1.57 \times 10^{-5} L - 90 \Omega$$

All of these values are very minimal so they won't affect
Voltage gain.

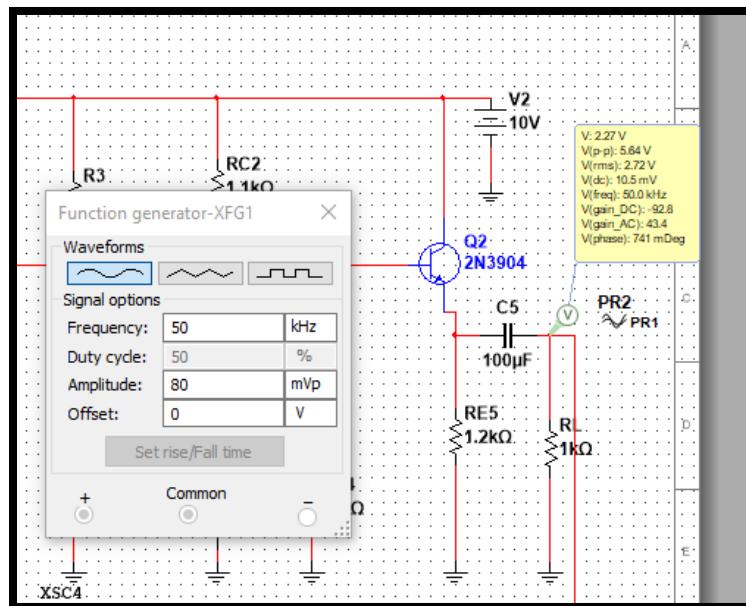
7. Experimental Results



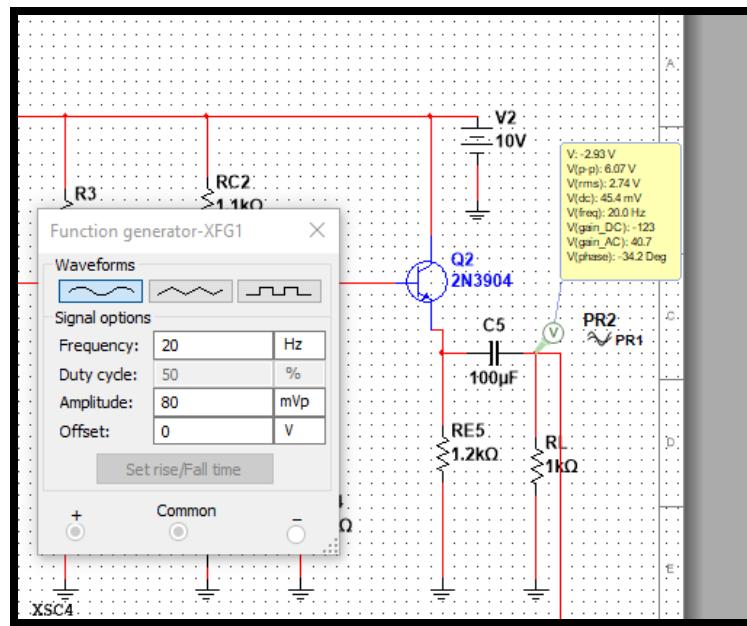
The voltage gain with no load when measured is approximately $A_{v_o}[V/V] = 50.7$ and the peak to peak is 6.59 V.



The voltage gain with load when measured is approximately $A_{vo}[V/V] = 47.5$ and the peak to peak is 5.99 V.



This verifies that the circuit is functional for 50 kHz.



This verifies that the circuit is functional for 20 Hz.

8. Errors and Conclusion

First, let us verify if we were able to meet all the requirements for this design project.

1. Power supply: **+10V** relative to the ground (Verified)
2. Quiescent current drawn from the power supply: **no larger than 10 mA**; (Verified
*Demonstrated in Workings)
3. Maximum no-load output voltage swing (at 1 kHz): **no smaller than 8 V peak to peak**; (Error)
4. No-load voltage gain (at 1 kHz): $|A_{vo}| = 50 (\pm 10\%)$; (Verified)
5. Loaded voltage gain (at 1 kHz and with $R_L = 1 \text{ k}\Omega$): **no smaller than 90% of the no-load voltage gain**; (Verified)

6. Maximum loaded output voltage swing (at 1 kHz and $R_L = 1 \text{ k}\Omega$): **no smaller than 4 V peak to peak;** (Verified)
7. Input resistance (at 1 kHz): **no smaller than 20 $\text{k}\Omega$;** (Error)
8. Amplifier type: **inverting or non-inverting;** (Verified)
9. Frequency response: **20 Hz to 50 kHz(-3dB response);** (Verified)
10. Type of transistors: **BJT;** (Verified)
11. Number of transistors (stages): **no more than 3;** (Verified)
12. A Resistance permitted: **values smaller than 220 $\text{k}\Omega$ from the E24 series;** (Verified)
13. Capacitors permitted: **0.1 μF , 1.0 μF , 2.2 μF , 4.7 μF , 10 μF , 47 μF , 100 μF , 220 $\mu\text{F};$** (Verified)

To summarize this entire project, most of the requirements were met and were proven using calculations as well as simulations. However there were some requirements that couldn't be reached for example I could not get the input resistance to over **20 $\text{k}\Omega$** , the no load voltage swing. These errors could be caused for a variety of reasons for example when creating my load line choosing a different current could have ultimately changed all the values and allowed for a higher voltage swing. Not to mention it could have also allowed my output voltage graph to be more accurate and sinusoidal rather than it looking the way it was. Furthermore, it also would have been able to make my input resistance higher, by using different current I could have been able to use higher resistances which would have not only increased the input resistance but would have allowed for higher voltage swing. Furthermore regarding the frequency response it was verified that the circuit is valid for all the frequencies and was checked using the capacitors. Overall, I believe the choice of the design was valid, however the currents chosen using the load line and DC operating point should have been different so I can reach the input resistance requirement and have a peak to peak of 8V when there is no load. Not to mention, the reason why the waveforms weren't provided was because they were not properly sinusoidal and were not adequate. Despite the fact that not all of the requirements were met, most of them were and I believe I was able to complete this design project to the best of my ability.