Advances in Wearable Brain-Computer Interfaces from an Algorithm-Hardware Co-Design Perspective

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Advances in Wearable Brain-Computer Interfaces from an Algorithm-Hardware Co-Design Perspective

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***Abstract*—Brain-computer interface (BCI), a communication technology between brain and computer developed for a long time since the 1970s, can be incorporated in wearable devices by developing powerful signal processing algorithms and semiconductor technologies. For the satisfactory user experience based on BCI, high information transfer rate and low power consumption should be considered together without losing accuracy. Although many existing BCI algorithms have been mainly focused solely on accuracy, their deployment on wearable devices is not straightforward due to the limited hardware resources and computational capabilities. This tutorial summarizes recent advances in wearable BCI algorithms and hardware implementations from an algorithm-hardware co-design perspective and discusses future directions.**

***Index Terms*—Brain-computer interface (BCI), algorithm-hardware co-design, domain-specific architecture, deep learning accelerator, linear algebra accelerator**

I. Introduction

BRAIN-computer interface (BCI) can translate electrical signals of brain activity into interpretable information that reflects the user's intent without neuromuscular control [1]–[3]. Because BCI technology requires only electrical signals, it can provide communication channels for people who have difficulty communicating with others due to devastating neuromuscular disorders such as amyotrophic lateral sclerosis, spinal cord injury, brainstem stroke, and cerebral palsy [1], [3].

BCI can be classified as invasive or non-invasive depending on the surgical need. Speller, the most representative application in non-invasive BCI, has been widely used for people with paralysis due to high temporal resolution, the safety of external electrodes, and a wide range of applications [4]–[6].

The conventional non-invasive BCI spelling systems have mainly used an electrode-array cap with an electroencephalogram (EEG) recording instrument and external signal processing machine, as indicated in Fig. 1(a). Although these systems have sufficient information transfer rates (ITR) to communicate, their high cost and massive form factors, as well as inconvenience and long installation times, limit their practicality [7]. Accordingly, research on algorithms and computing platforms for wearable BCI systems is being actively conducted [46]–[56].

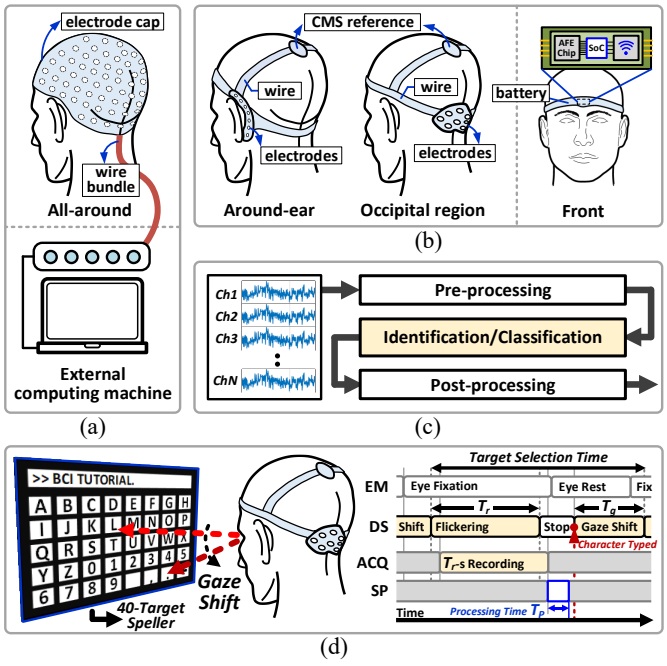

Fig. 1. (a) Conventional wired BCI system using electrode cap and external computing machine, (b) example of wearable BCI systems with small form factor computing device, (c) processing flow in typical BCI, (d) system operation of SSVEP-based wearable BCI (N_t=40), where EM is eye movement, DS is display status, ACQ is acquisition, and SP is signal processing.

As shown in Fig. 1(b), the wearable BCI system acquires EEG with the analog frontend (AFE) through electrodes located in different parts depending on the application, performs signal processing through SoC (System-on-Chip), and wirelessly transmits the results. In Fig. 1(c), pre-processing can typically be filtering and noise reduction, and post-processing can be compression or encryption. Algorithms that analyze the user's intention to be reviewed in this paper corresponds to the identification or classification step.

This brief describes wearable visual stimuli-based BCI that utilizes brain responses such as P300 and steady-state visual

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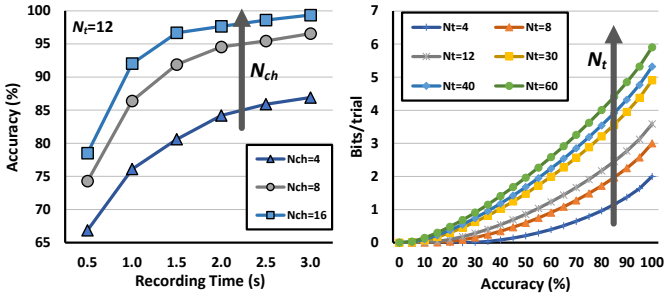

Fig. 2. Performance of target identification algorithms. (a) Example of accuracy P according to recording time T_r and number of channels N_{ch}, (b) bits/trial, B, calculated by P and number of visual targets N_t. For each N_t, bit rate is shown only for $P \geq 100/N_t$ (i.e. $\geq$ chance) [10]

evoked potential (SSVEP), reflecting the user's intentions to the brain signal by looking at the visual stimulus. For widespread deployment of BCI technology, enough information transfer capability with high accuracy is necessary. Among P300 and SSVEP, which are the main paradigms of visual stimuli-based BCI, SSVEP is more widely used due to its high communication speed capability and less user training requirements [8], [9]. Therefore, this brief focuses on SSVEP-based wearable BCI systems.

As shown in Fig. 1(d), a user can type the desired characters by gazing at the targets blinking at different frequencies and phases. The single cycle of repetitive operation is called target selection time T [seconds/selection], which is composed of brain-signal recording time T_r, processing time T_p, and predefined gaze shift time T_g. ITR [bits/min], derived by Shannon and Weaver in 1964 [11], [12], is a standard method for measuring performance of the BCI algorithm that expresses speed and accuracy as a single value described in (1)(2).

$$B = log_2 N_t + P \times log_2 P + (1-P) \times log_2 \left(\frac{1-P}{N_t - 1} \right) \quad (1)$$

$$ITR = B \times \frac{60}{T} = B \times \frac{60}{T_{r.p} + T_g} \geq B \times \frac{60}{T_r + T_p + T_g} \quad (2)$$

where B is bits per trial, N_t is the number of targets, P is target identification accuracy, and T_{rp} is the time when recording and processing are partially overlapped.

Recent studies evaluate ITR and accuracy as independent performance indicators. As illustrated in Fig. 2(a), increasing EEG recording time T_r and/or increasing the number of channels N_{ch} leads to better accuracy P. Also, as shown in Fig. 2(b), the amount of data transferred improves as the value of N_t increases and/or the accuracy increases. Although ITR is calculated by multiplying B by trials/time as indicated in (2), however, increasing accuracy does not always lead to improved ITR. According to (2), long EEG recording time T_r, which contributes to high accuracy, decreases ITR. In addition, the increase in T_r or N_{ch} for better accuracy increases the total amount of EEG data, thereby increasing the time T_p required for signal processing. Since the target identification algorithm occupies most of the total signal processing time T_p and has a significant impact on accuracy, an optimized implementation with less latency plays a key role in a successful wearable BCI system. Therefore, it is important to consider the algorithm and hardware together to achieve low power consumption, high speed processing, and the highest ITR for a given T_r / N_{ch} / T_g depending on the target applications.

TABLE I
TARGET IDENTIFICATION ALGORITHMS AND THEIR PRIMARY OPERATIONS

Paradigm	System	Algorithm	Primary Operations	Ref.
SSVEP (EP)	Machine Control	LDA	BLAS Level 1-3, EVD (by QRD or SVD)	[15][16]
	Speller	CNN	Convolution 1D/2D, BLAS Level 1-3, Activation, Pooling	[34]-[38]
		RNN	GRU, LSTM, BLAS Level 1-3, Activations, Pooling functions	[13][14]
		CCA	BLAS Level 1-3, Solve (by back substitution), QRD, SVD, Pearson's correlation, Sort	[17]-[22]
	Machine Control	CCA		[23]-[24]
		KNN	Euclidean norm, Sort	[23]

EP: evoked potential, BLAS: basic linear algebra subprograms
QRD: QR decomposition, SVD: singular value decomposition
EVD: eigenvalue decomposition, LDA: linear discriminant analysis
CCA: canonical correlation analysis, KNN: k-nearest neighbors
CNN: convolutional neural network, RNN: recurrent neural network
GRU: gated recurrent units, LSTM: long short-term memory

This brief is organized as follows. Section II introduces the state-of-the-art signal processing algorithm for the target identification. A review of the system architecture from an algorithm-hardware co-design perspective is presented in Section III. Future directions are discussed in Section IV, and Section V concludes this brief.

II. Target Identification: State-of-the-Art

The purpose of target identification is to identify the intended target as quickly and accurately as possible among N_t targets when the user gazes at a specific target. To achieve this, traditional linear algebra (LA)-based approaches have been actively studied, and recently, neural network-based deep learning (DL) approaches are attracting attention, as denoted in Table I. This section summarizes recent advances in LA-based and DL-based approaches to target identification algorithms.

A. Traditional Linear Algebra-based Approaches

The main distinguishable characteristics of visual stimuli reflected in SSVEP are frequency and phase. As the number of target N_t highly contributes to the information bits per trial as indicated in Fig. 2(b), current BCI speller systems have increased the number of visual stimuli by reducing the interval between adjacent target frequencies and phases [25]. Therefore, the target identification algorithm should identify the target by discriminating the small difference in the frequency or phase reflected in the SSVEP.

The earliest attempted approach is an FFT-based spectrum analysis such as PSDA [26], [27], but the inter-subject variability and low SNR of SSVEP limit its practical use [8], [28]. Wavelet transform (WT) [29], [30], Hilbert-Huang transform (HHT) [31], common spatial pattern (CSP) [32], LDA [15], [16], and KNN-based [23] algorithms have also been studied. The most practically used algorithm so far is

the canonical correlation analysis (CCA) which exploits the correlation relationship between two multivariate datasets [27]. CCA utilizes the harmonic component of the SSVEP more than other algorithms, has less variation between users, high SNR, and high accuracy [33].

Most of the existing target identification algorithms such as LDA, KNN, WT, HHT, and CSP, including many advanced variants of CCA, are composed of complex linear algebra operations. Particularly, as denoted in Table I, matrix decompositions such as QRD, SVD, and BLAS level 1-3 should be repeatedly performed in CCA. Multi-channel SSVEP constitutes a large two-dimensional matrix depending on the N_{ch}, a sampling rate of AFE, and filtering in pre-processing. In order to quickly and repeatedly process these complex operations on high-dimensional matrix data in wearable devices with low power consumption, it is essential to consider LA-friendly hardware architecture rather than performing scalar or vector operations. At the same time, it is necessary to optimize the algorithm to reduce the amount of computation.

B. Deep Learning-based Approaches

As neural network (NN)-based deep learning (DL) hardware and software frameworks evolve, DL-based BCI has become more mature following the advancement of DL in computer vision (CV) and natural language processing (NLP).

Recent DL-based approaches to EEG including SSVEP are DeepConvNet [34], ShallowConvNet [34], EEGNet [35], Compact-CNN [36], S-EEGNet [37], and DNN for SSVEP [38], and a detailed analysis has been reported in [39]–[42]. As indicated in Table I, most of them use a convolutional neural network (CNN) or recurrent neural network (RNN), and both network architectures consist of multidimensional matrix multiplication and various kinds of activation and pooling functions. In particular, in the case of RNN, the functionality of GRU [43] and LSTM [44] should be additionally implemented. The operations constituting the DL-based algorithm are relatively less complicated than the LA-based approach, but the number of matrix multiplication increases exponentially according to the depth of layers and the number of filters. Therefore, data reuse and memory bandwidth issues should be carefully considered.

Across many technical fields, NN-based DL often outperforms traditional algorithms when the amount of data is sufficient for training. However, the DL-based approach to the SSVEP-based BCI has a challenge in that it is difficult to obtain a large dataset due to the technical difficulties in SSVEP recording and eye fatigue from the blinking visual stimuli [45]. Therefore, LA-based approaches that achieve relatively stable performance even for the small dataset are still widely used in target identification algorithms. In the future, it is expected that the advanced DL-based approaches and the understanding of SSVEP identification built up in the LA-based approaches will be harmonized to achieve higher performance.

III. System Architecture for Wearable BCI

LA-based or DL-based target identification algorithm can be processed in the signal processing SoC or accelerator in the wearable BCI device, as shown in Fig. 3(a). In overall system architecture, various issues mentioned in Section II should be considered for system-level optimization. Fig. 3(b) summarizes the state-of-the-art for wearable BCI system architecture. Signal processing algorithm for BCI can be implemented entirely in software (SW) [22] [46] [47] or with only dedicated hardware (HW) [48] [50]. Also, there have been many approaches to optimize the architecture with well-suited HW/SW partitioning [52]–[56].

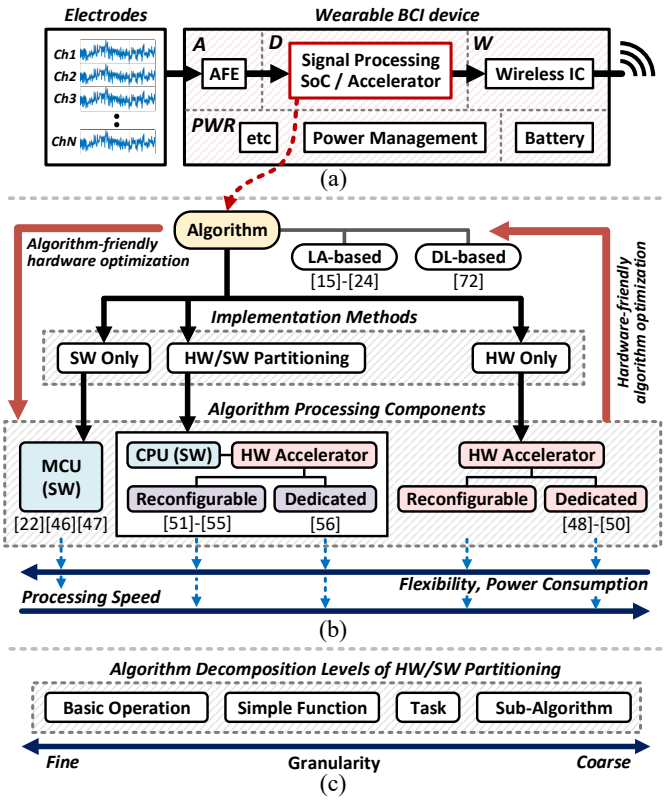

Fig. 3. (a) Main components in wearable BCI devices such as analog frontend *A*, digital signal processing *D*, wireless communication *W*, and power *PWR*. (b) Overview of algorithm-hardware co-design for wearable BCI, (c) granularity of algorithm decomposition during HW/SW partitioning

It is essential to consider both hardware-friendly algorithm optimization and algorithm-friendly hardware optimization, as indicated by the red line in Fig. 3(b). Among recent wearable or implantable BCI hardware studies, few of them consider algorithm-hardware co-design in both directions [53]–[55]. Most of the work presents the sub-optimal method of adopting the optimal hardware architecture for the algorithm [52], [56].

A. Implementations for Wearable BCI

In general, with programmable computing units, the overall system can provide greater flexibility at the expense of higher power consumption and slower processing speed. In order to determine the proper hardware architecture, it is necessary to decompose the algorithm in consideration of the granularity of the computational parts. A programmable computing unit with relatively simple operations is preferred if the algorithm can be finely decomposed, as illustrated in Fig. 3(c). In the SW-based approach, parallelism from the number of cores, DSP

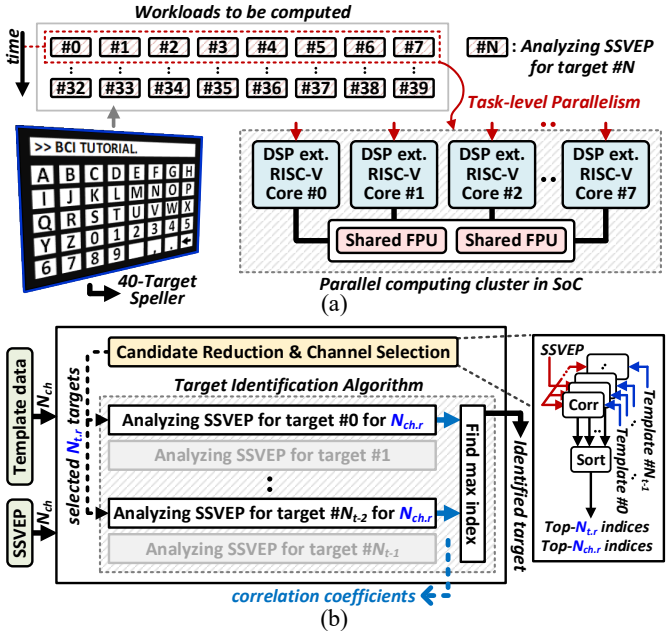

Fig. 4. (a) Example of task-level parallelism of target identification in multi-core MCU-based wearable BCI device [47], (b) algorithm optimization for computational complexity by reducing effective N_t and N_{ch} [52], [55].

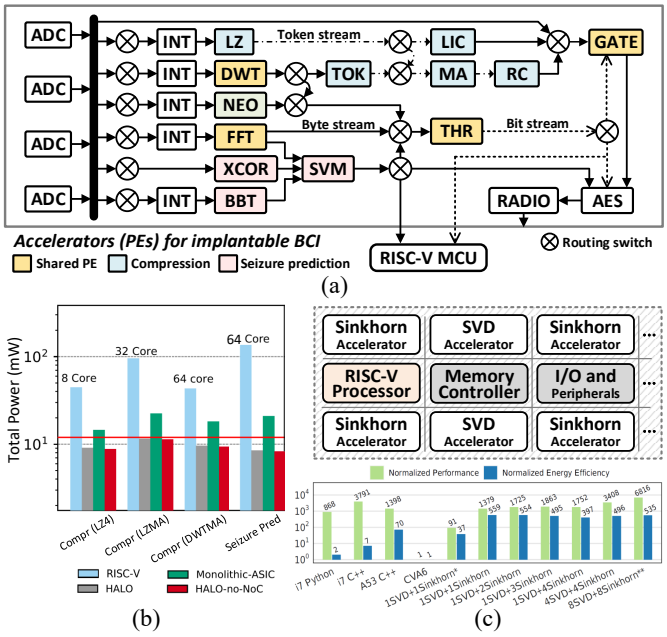

Fig. 5. Examples of algorithm-hardware co-design by the coarsely decomposing algorithm. (a) An array of heterogeneous accelerators (PEs) configured by RISC-V MCU [53] (The meaning of the abbreviation is not important in this context.) (b) consumes lower power than SW-only processing [53]. (c) Tile-based scalable SoC platform with high energy efficiency [56].

extension within the instruction set, and the presence of co-processors including floating-point unit (FPU) are significant factors of algorithm-hardware co-design [46], [47].

[47] is a representative MCU-based wearable BCI platform with nine RISC-V cores, including DSP extension and two shared FPUs. The CCA is implemented into SW by exploiting task-level parallelism, which allocates the operation for each target to each core, as indicated in Fig. 4(a). Because SVD has many iterative tasks with data dependencies, the loop-level parallelism cannot be applied to CCA processing. Also, there is a limit to speed improvement of floating-point operations because there are just two shared FPUs.

Since the LA-based algorithm is diverse and complicated, multi-core implementations can be suitable to pursue flexibility. However, even if the MCU has many cores, it has a limitation on parallelism, and as the size of data increases, the execution time increases exponentially. Therefore, the entire SW-based implementation is usually applicable only to a simple LA-based algorithm with a small N_{ch} [46], [47].

In order to overcome the performance limit in SW-based implementations, there have been many approaches with dedicated HW accelerators for LA-based algorithms, such as CCA [48], [49], QRD [57], [58], SVD [59]–[61], and DL-based algorithm [50], which can provide high throughput and low power consumption for specific workloads at the cost of less flexibility. With proper HW/SW partitioning that allocates repetitive and frequently used complex workloads to HW and the rest to SW, it is possible to balance processing speed, power consumption, and flexibility, as shown in Fig. 3(b)(c).

For the DL-based algorithm, the essential fixed-point functions constituting NN are provided in the form of a library such as CMSIS-NN [62], and there are studies on custom library and software stack for NN inference in MCU [63], [64]. In the DL-based algorithm, the processing performance is limited because the size of the matrix data is excessive for the MCU and the limited memory interface is not suitable for the high bandwidth requirements. Recently, there have been many works on NN acceleration with the specialized hardware, so-called NPU (Neural Processing Unit) [65]–[67]. Well-designed NPUs can provide better energy efficiency and high performance compared to MCU-based approaches.

B. Algorithm-Hardware Co-Design

For an optimal wearable BCI system, a signal processing algorithm should be analyzed in terms of computational complexity, parallelism, and well-fitting hardware architecture. Accordingly, there have been many approaches where algorithm-hardware co-design has been investigated.

1) Algorithm optimization for computational complexity: From the computational complexity point of view, N_t and/or N_{ch} are key factors in signal processing for BCI system. By applying the algorithm only to specific target candidates highly likely to gaze, effective N_t can be reduced. Also, the data dimension can be reduced by performing the target identification algorithm on only the effective channels rather than considering all N_{ch} channels. As shown in Fig. 4(b), [52] proposed a candidate reduction (CR) technique that reduces target candidates by a predetermined number. [55] reduces the size of data and the number of algorithm iterations as well by predetermining the optimal N_t and N_{ch} according to users.

2) Accelerators for coarsely-decomposed algorithms: As shown in Fig. 5(a), an implantable RISC-V-based SoC architecture [53] including multiple accelerators was designed by coarsely decomposing various implantable BCI algorithms

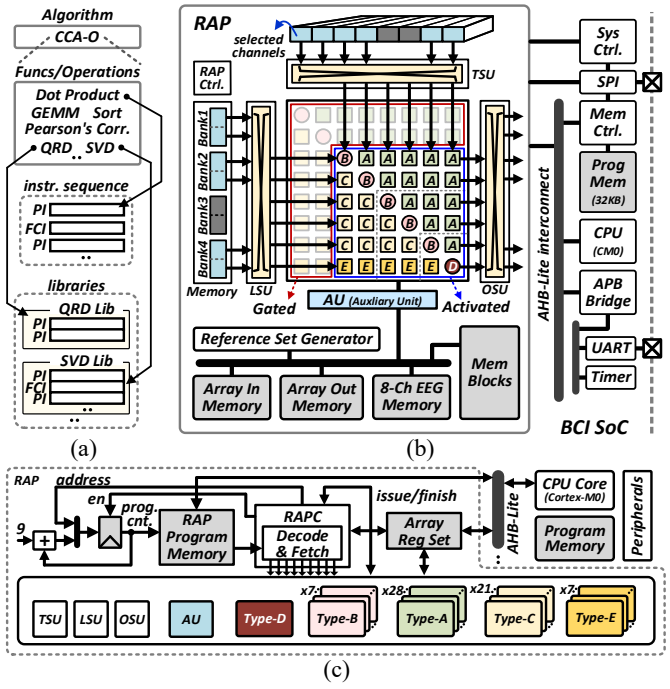

Fig. 6. Reconfigurable array processor (RAP) [55] for (a) finely-decomposed LA-based target identification algorithms. (b) Arm CPU core-based SoC includes RAP, consisting of a 5-heterogeneous PE-based scalable array, (b) reconfigured and controlled by finely defined instructions.

such as seizure prediction, movement intent, compression, spike detection, and encryption. Their commonly required workloads, such as FFT and discrete WT (DWT), are carefully implemented into accelerators from the algorithm-hardware co-design, and RISC-V MCU is responsible for configuring accelerators and support computations not currently within accelerators. This architecture shows significantly reduced power consumption than SW processing of the same algorithm on multiple RISC-V cores, as indicated in Fig. 5(b). This architecture can also be leveraged for wearable BCI SoCs.

A study of a wearable BCI SoC [56] decomposes the algorithm coarser than [53] to design accelerators and integrate them into a tile-based scalable SoC platform [68], as indicated in Fig. 5(c). In this architecture, one RISC-V core tile running Linux, one memory channel tile, and one I/O tile are integrated into SoC, and the required algorithms can be implemented as multiple accelerators through the software stack. This platform makes it easy to integrate accelerators to SoCs systematically at the expense of less hardware flexibility than [53].

There are studies in which DL-based BCI algorithms are implemented as accelerators by coarsely decomposing the NN model inference workload [50]. As in the previous two cases [53], [56], these DL-based acceleration designs have high processing speed and low power consumption for specific algorithms/workloads, but acceleration is unavailable for workloads exceeding the accelerator's configuration range. Therefore, the HW/SW partitioning in which the algorithm is coarsely decomposed is suitable when the required algorithms are limited to a specific range.

3) Accelerators for finely-decomposed algorithms: In order to accelerate all LA-based primary operations required in target identification algorithms as indicated in Table I, [55] finely decomposed algorithms and proposed a reconfigurable array processor (RAP) for accelerating these decomposed algorithms through custom instructions as shown in Fig. 6. The Arm Cortex-M0 in the SoC is responsible for simple tasks and system management, and LA operations such as BLAS level 1-3, QRD, and SVD are all accelerated by RAP.

As shown in Fig. 6(a), RAP instruction is composed of LA-based micro-operations, and relatively complex matrix decompositions such as QRD and SVD are prepared in the form of a library through instruction combination. In Fig. 6(b)(c), RAP consists of a two-dimensional processing element (PE) array composed of 5-types of heterogeneous PEs and 3-types of shaping units (SUs) serving as array interfaces. In addition, there is an auxiliary unit (AU) to support PE array.

Accelerators for finely decomposed algorithms are flexible for a specific domain. As shown in Fig. 3(b), SoC with reconfigurable hardware has flexibility close to SW implementation on MCU, but it may have disadvantages in power consumption and processing speed. Also, a software development kit including a compiler is required to generate an instruction-based microcode that includes the information of hardware reconfiguration and operation.

IV. Future Directions

Although BCI research has made many achievements, including advanced algorithms and innovative hardware architecture, there are still many challenges and unsolved problems. As a result of comprehensively discussing wearable BCI technology from the algorithm-hardware co-design perspective, the future directions are expected as follows.

From a system-level point of view, wearable BCI will be equipped with new form factors such as ear-EEG [69], [70] and smart glasses [71], and multimodality that utilizes bio-signals and spontaneous EEG with event-related potentials.

In addition, artificial intelligence-based user personalization algorithms are expected to analyze multimodal signals and improve the quality of BCI applications in new device form factors. Also, solving the limitations of the DL algorithm in the SSVEP-based system, where it is difficult to obtain a large amount of data for training, enables practical high-performance target identification by fusion of LA-based and DL-based approaches.

Also, algorithm-hardware co-design based on domain-specific reconfigurable hardware architecture will provide high accuracy and ITR of wearable BCI devices in a balanced way with high flexibility, low power consumption, and high processing speed.

V. Conclusion

This brief provided a comprehensive tutorial of recent advances in wearable BCI from an algorithm-hardware co-design perspective. Two categories of target identification algorithms and underlying system architectures with hardware accelerators were discussed, along with performance metrics analysis. We present the future direction for the comprehensive development of wearable BCI technology and call for active contributions in this emerging area.

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