TURBOT B

Rev : R200

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REVISION HISTORY:

Rev	Date	Notes
X001	2016/03/29	Initial Design Review
X002	2016/03/31	BOM Release for Pre-ordering Components
X003	2016/04/01	Pre-Release Design Review
X100	2016/04/08	Prototype Release
R100	2016/09/08	Production Release
R200	2016/10/27	Post DFx Release Production Release

For all design files, including bill of materials and gerber files, please visit www.minnowboard.org

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Minnowboard Turbot design derived from Minnowboard MAX as designed by CircuitCo LLC.

All derivative works are to be attributed to ADI Engineering and CircuitCo LLC .

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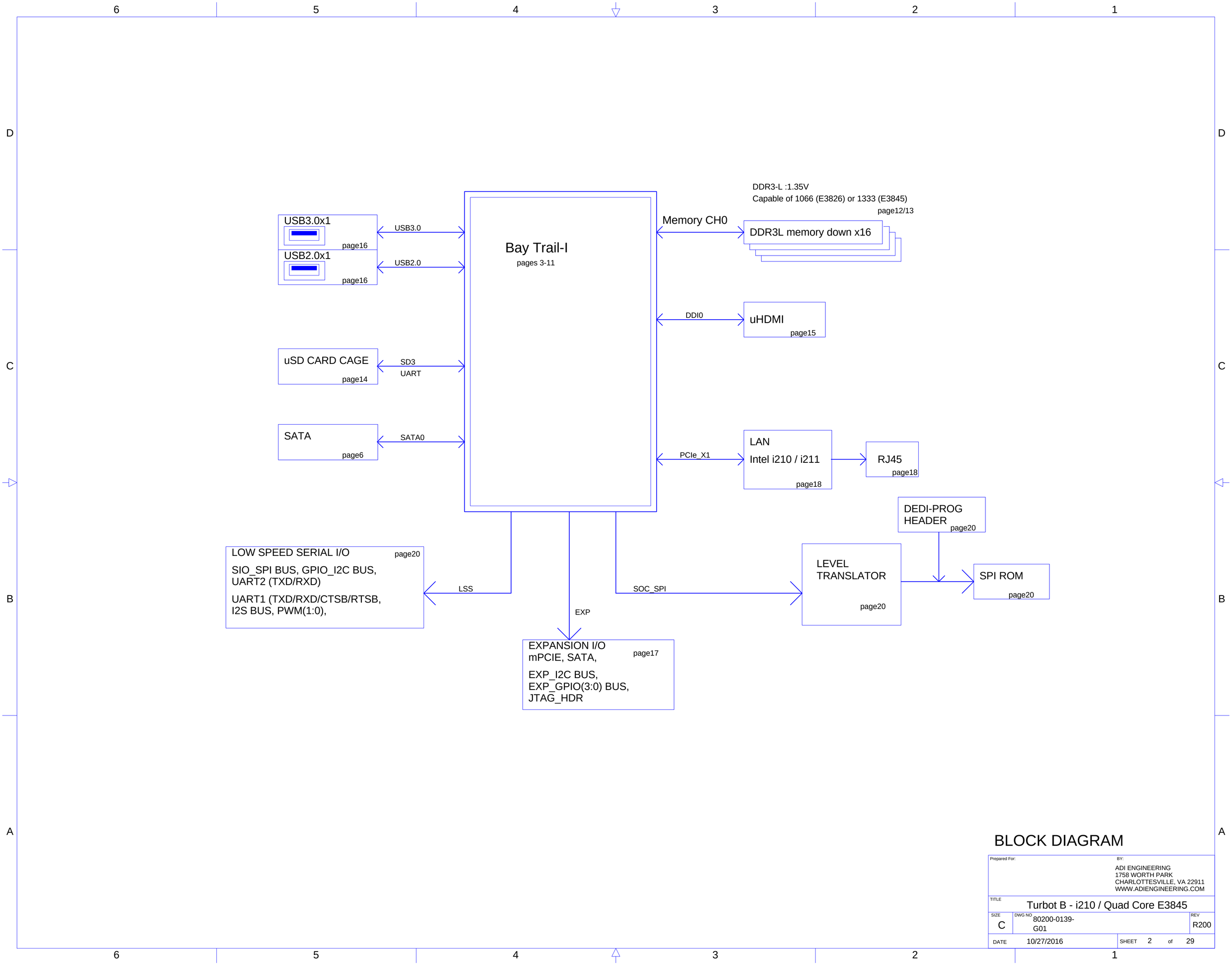
Prepared For:

BY:
ADI ENGINEERING
1758 WORTH PARK
CHARLOTTESVILLE, VA 22911
WWW.ADIENGINEERING.COM

TITLE: Turbot B - i210 / Quad Core E3845

SIZE: C | DWG NO: 80200-0139-G01 | REV: R200

DATE: 10/27/2016 | SHEET 1 of 29



BLOCK DIAGRAM

Prepared For:	BY: ADI ENGINEERING 1758 WORTH PARK CHARLOTTESVILLE, VA 22911 WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE: C	DWG NO: 80200-0139-G01 — REV: R200
DATE: 10/27/2016	SHEET 2 of 29

FOR HDMI VIDEO/AUDIO,

REVERSE BIT CONNECTIONS
FROM (0:2) TO (2:0), BIT3

IS THE CLOCK SIGNAL.
STRAIGHT BIT ORDER is

for EDP ONLY
HDMI

CPU1

HDMI_TX2_DP AV3 DDI0_TXP_0
HDMI_TX2_DN AV2 DDI0_TXN_0
HDMI_TX1_DP AT2 DDI0_TXP_1
HDMI_TX1_DN AT3 DDI0_TXN_1
HDMI_TX0_DP AR3 DDI0_TXP_2
HDMI_TX0_DN AR1 DDI0_TXN_2
HDMI_CLK_DP AP3 DDI0_TXP_3
HDMI_CLK_DN AP2 DDI0_TXN_3

(+V1P0S) AL3 DDI0_AUXP
(+V1P0S) AL1 DDI0_AUXN

HDMI_HPD_B (+V1P8S) D27 DDI0_HPD

HDMI_DDCDAT (+V1P8S) C26 DDI0_DDCDATA
HDMI_DDCCLK (+V1P8S) C28 DDI0_DDCCLK

(+V1P8S) B28 DDI0_VDDEN
(+V1P8S) C27 DDI0_BKLTEN
(+V1P8S) B26 DDI0_BKLTCTL

+V1P8S
GND C375 0.1uF
HDMI_HPD U39 SN74LVC1G14DCKR SC70-5 GND

1 R217 2 402 DDI_RCOMP_P (+V1P0S) AK13 DDI0_RCOMP
DDI_RCOMP_N (+V1P0S) AK12 DDI0_RCOMP_P
AM14 RESERVED_AM14
AM13 RESERVED_AM13
GND R42 1 2 0 AM3 RESERVED_VSS0
GND R41 1 2 0 AM2 RESERVED_VSS1
Bay Trail-I Different

T2 RESERVED_T2
T3 RESERVED_T3
AB3 RESERVED_AB3
AB2 RESERVED_AB2
Y3 RESERVED_Y3
Y2 RESERVED_Y2
W3 RESERVED_W3
W1 RESERVED_W1
V2 RESERVED_V2
V3 RESERVED_V3
R3 RESERVED_R3
R1 RESERVED_R1
AD6 RESERVED_AD6
AD4 RESERVED_AD4
AB9 RESERVED_AB9
AB7 RESERVED_AB7
Y4 RESERVED_Y4
Y6 RESERVED_Y6
V4 RESERVED_V4
V6 RESERVED_V6
A29 RESERVED_A29
C29 RESERVED_C29
AB14 RESERVED_AB14
B30 GPIO_S0_NC12
C30 RESERVED_C30

GND R102 10.0K GPIO_NC13
TP15

ATOM E3845 SOC
DISPLAY SECTION

Bay Trail-M Remove eDP Port

DDI1_TXP_0 AG3 (+V1P0S)
DDI1_TXN_0 AG1 (+V1P0S)
DDI1_TXP_1 AF3 (+V1P0S)
DDI1_TXN_1 AF2 (+V1P0S)
DDI1_TXP_2 AD3 (+V1P0S)
DDI1_TXN_2 AD2 (+V1P0S)
DDI1_TXP_3 AC3 (+V1P0S)
DDI1_TXN_3 AC1 (+V1P0S)

DDI1_AUXP AK3 (+V1P0S)
DDI1_AUXN AK2 (+V1P0S)

DDI1_HPD K30 (+V1P8S) GND

DDI1_DDCDATA P30 (+V1P8S) DDI1_DDCDAT 1 R257 2 2.2K GND
DDI1_DDCCLK G30 (+V1P8S) GND

DDI1_VDDEN N30 (+V1P8S)
DDI1_BKLTEN J30 (+V1P8S)
DDI1_BKLTCTL M30 (+V1P8S)

RESERVED_AH14 AH14
RESERVED_AH13 AH13
RESERVED_AF14 AF14
RESERVED_AF13 AF13
RESERVED_VSS2 AH3 R46 1 2 0 GND
RESERVED_VSS3 AH2 R43 1 2 0 GND

VGA_RED BA3 (VVGA_GPIO)
VGA_BLUE AY2 (VVGA_GPIO)
VGA_GREEN BA1 (VVGA_GPIO)
VGA_IREF AW1 R40 357 GND
VGA_IRTN AY3 GND

VGA_HSYNC BD2 (VVGA_GPIO)
VGA_VSYNC BF2 (VVGA_GPIO) CRT_CLK 1 R39 2 150 GND

VGA_DDCCLK BC1 (VVGA_GPIO)
VGA_DDCDATA BC2 (VVGA_GPIO) CRT_DAT 1 R38 2 150

RESERVED_T7 T7 (V1P24S)
RESERVED_T9 T9 (V1P24S)
RESERVED_AB13 AB13 (V1P24S)
RESERVED_AB12 AB12 (V1P24S)
RESERVED_Y12 Y12 (V1P24S)
RESERVED_Y13 Y13 (V1P24S)
RESERVED_V10 V10 (V1P24S)
RESERVED_V9 V9 (V1P24S)
RESERVED_T12 T12 (V1P24S)
RESERVED_T10 T10 (V1P24S)
RESERVED_V14 V14 (V1P24S)
RESERVED_V13 V13 (V1P24S)
RESERVED_T14 T14 (V1P24S)
RESERVED_T13 T13 (V1P24S)
RESERVED_T6 T6 (V1P24S)
RESERVED_T4 T4 (V1P24S)
RESERVED_P14 P14 (V1P24S) MCSI_RCOMP 1 R213 2 150 GND

RESERVED_K34 K34 (V1P24S)
RESERVED_D32 D32 (V1P24S)
RESERVED_N32 N32 (V1P24S)
RESERVED_J34 J34 (V1P24S)
RESERVED_K28 K28 (V1P24S)
RESERVED_F28 F28 (V1P24S)
RESERVED_F32 F32 (V1P24S)
RESERVED_D34 D34 (V1P24S)
RESERVED_J28 J28 (V1P24S)
RESERVED_D28 D28 (V1P24S)
RESERVED_M32 M32 (V1P24S)
RESERVED_F34 F34 (V1P24S)

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Bay Trail-I MCSI Port

CPU-DDI/VGA

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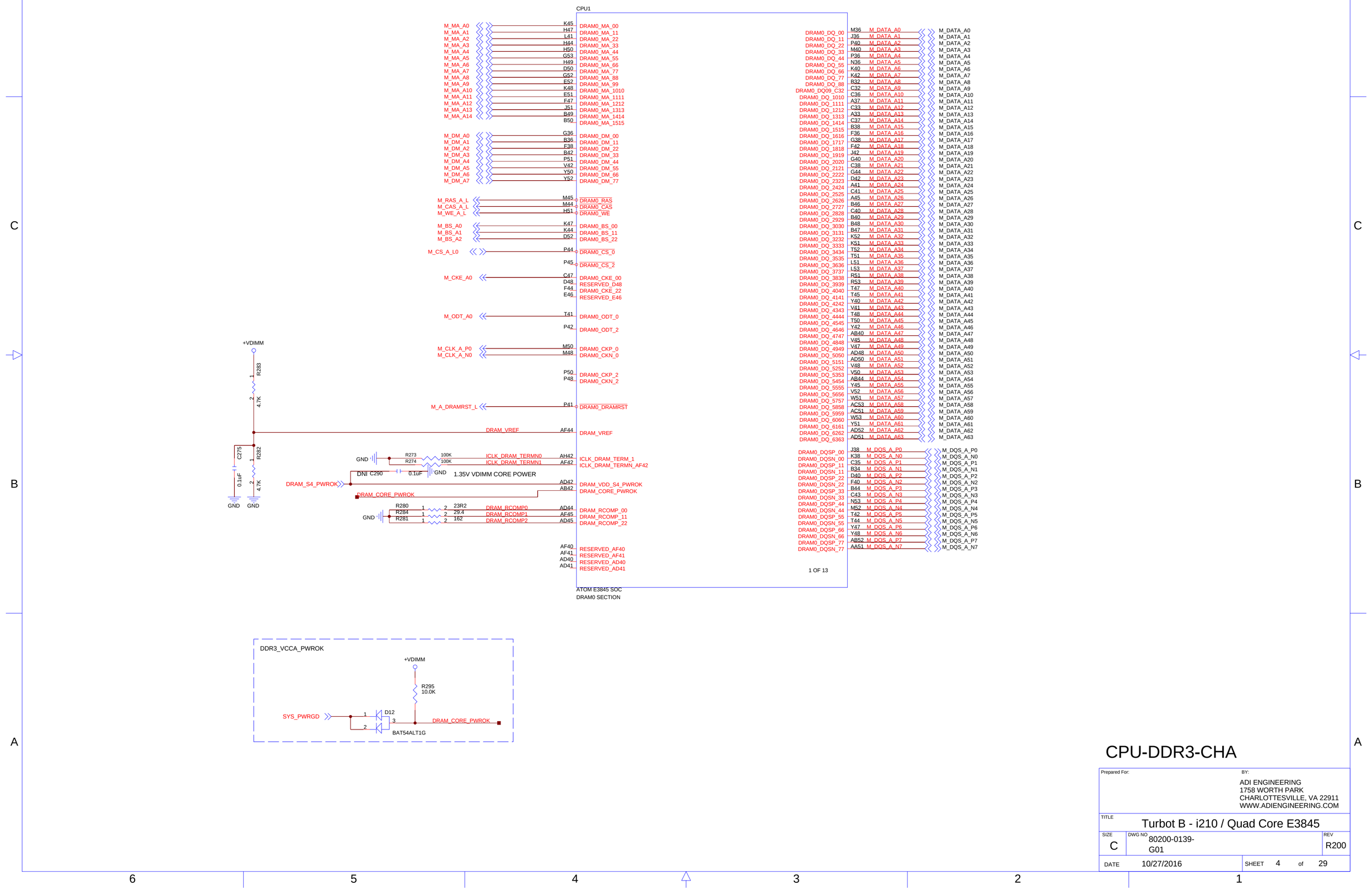
CHARLOTTESVILLE, VA 22911
WWW.ADIENGINEERING.COM

TITLE: Turbot B - i210 / Quad Core E3845

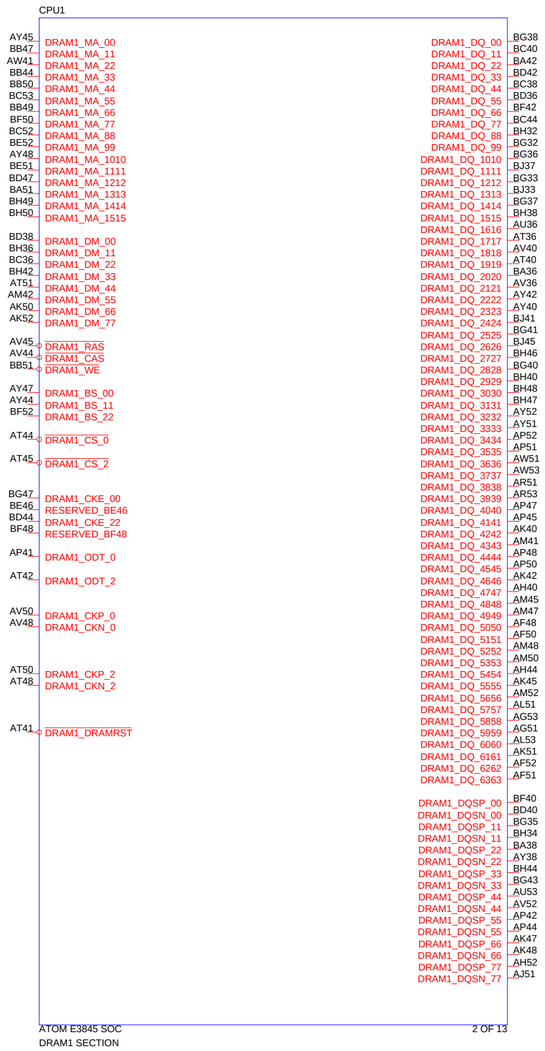
SIZE	DWG NO	REV
C	80200-0139-G01	R200

DATE	SHEET
10/27/2016	3 of 29



CPU-DDR3-CHA

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE: C	DWG NO: 80200-0139-G01
REV: R200	
DATE: 10/27/2016	SHEET 4 of 29



CPU-DDR3-CHB

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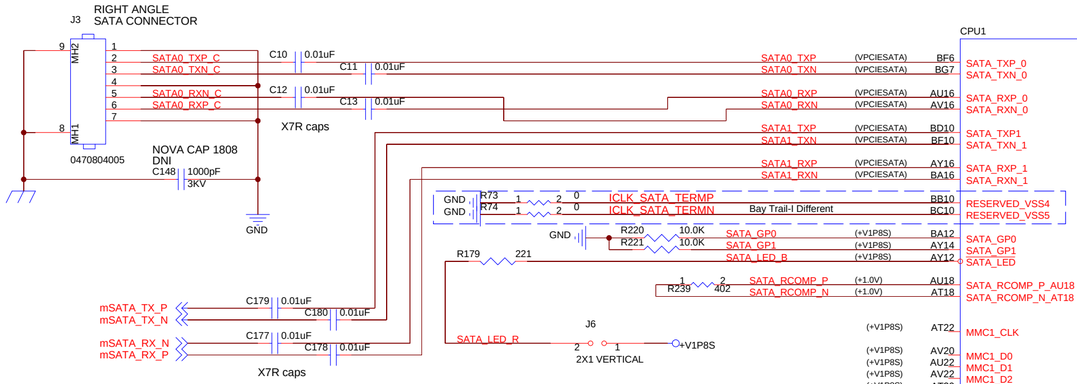
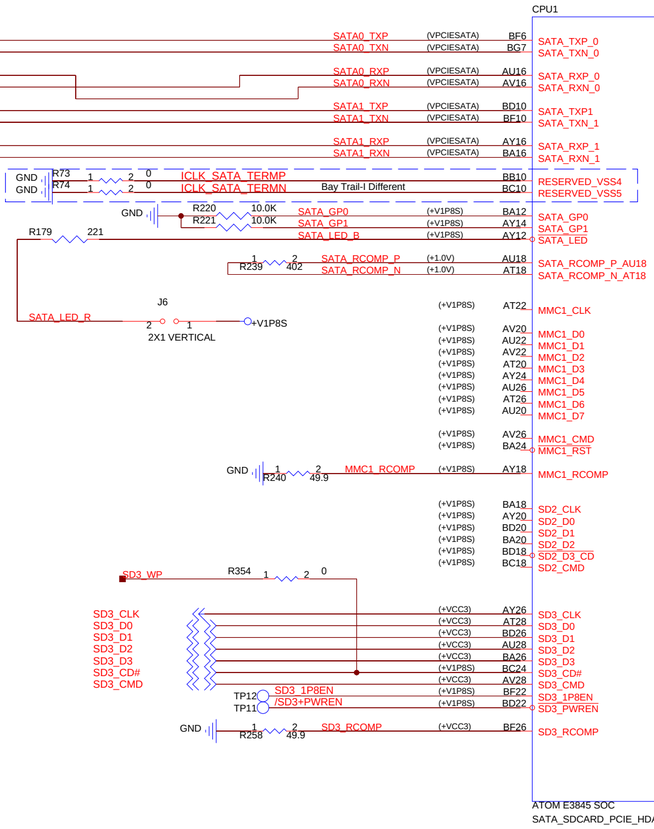
TITLE	Turbot B - i210 / Quad Core E3845
SIZE: C	DWG NO: 80200-0139-G01
REV: R200	
DATE: 10/27/2016	SHEET 5 of 29





BOM Option

Hardware Identification (HW ID)
"1001"

HW STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC

Top Swap(A16 Override)

H	Top address bit is unchanged
L	Top address bit is inverted

Strap Pin	Function
GPIO_S0_SC63 (LPE_I2S_FRM)	BIOS Boot Selection 0=LPC *1=SPI
GPIO_S0_SC65 (LPE_I2S_DATOUT)	Security Flash Descriptors 0=Override *1=Normal Operation

CPU-PE/HDA/SD/eMMC/Strap

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CHARLOTTESVILLE, VA 22911
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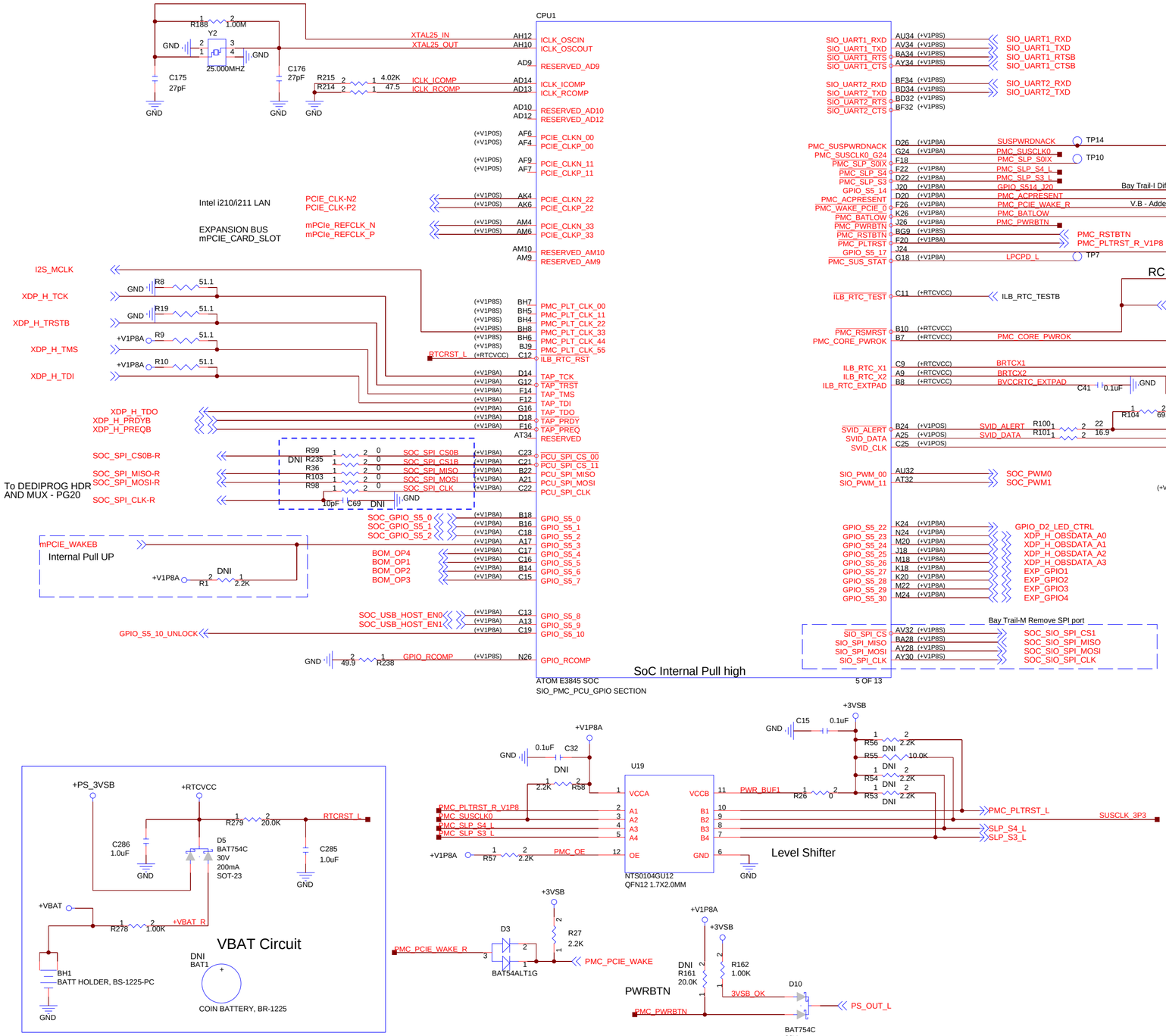

CPU-SPI/CLOCK/RTC/PMC/UART

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TITLE	Turbot B - i210 / Quad Core E3845
SIZE C	DWG NO 80200-0139-G01
REV	R200
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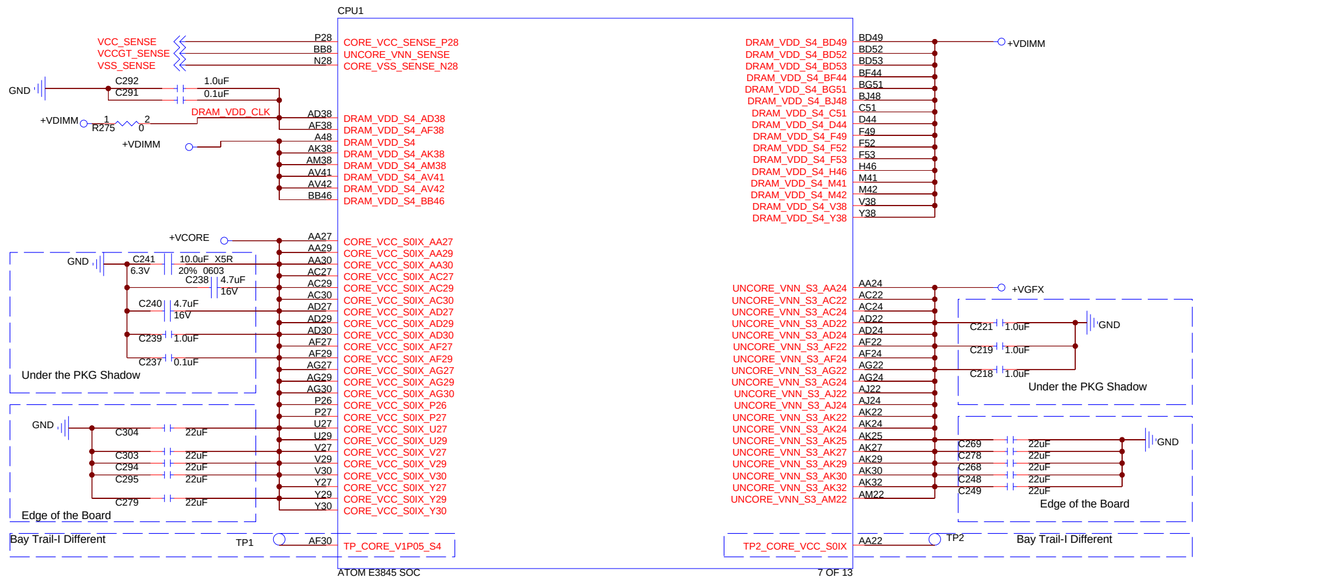
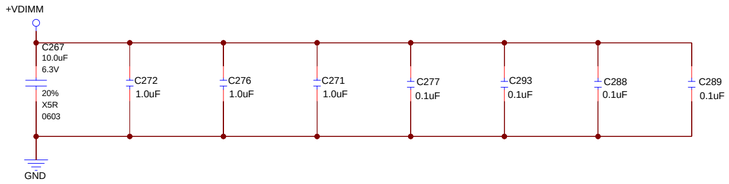
CPU-USB/LPC/SMB/I2C

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE: C	DWG NO: 80200-0139-G01
REV: R200	
DATE: 10/27/2016	SHEET 8 of 29





CPU-PWR1/TPM/LPC

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TITLE	Turbot B - i210 / Quad Core E3845
SIZE: C	DWG NO: 80200-0139-G01
REV: R200	
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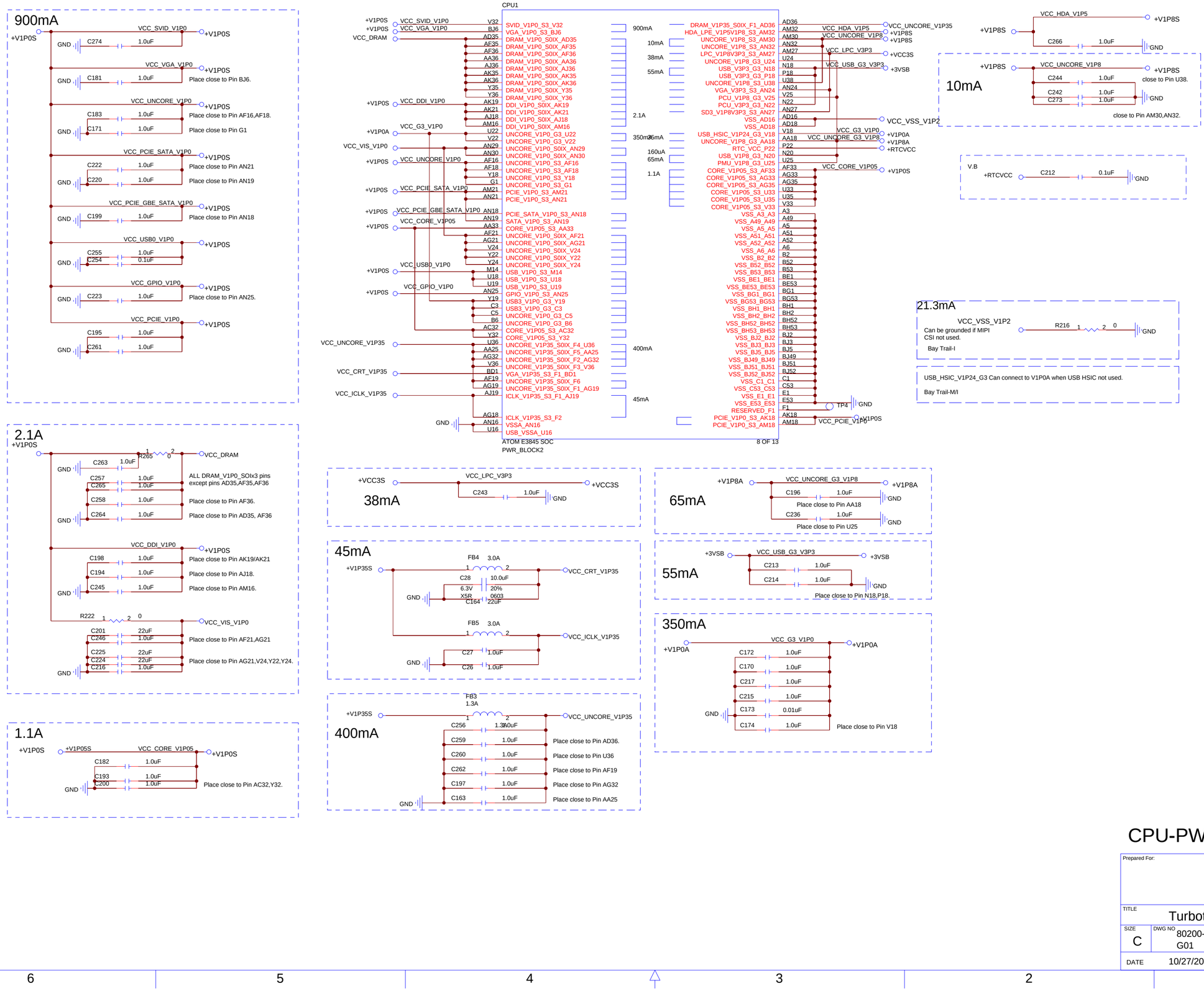
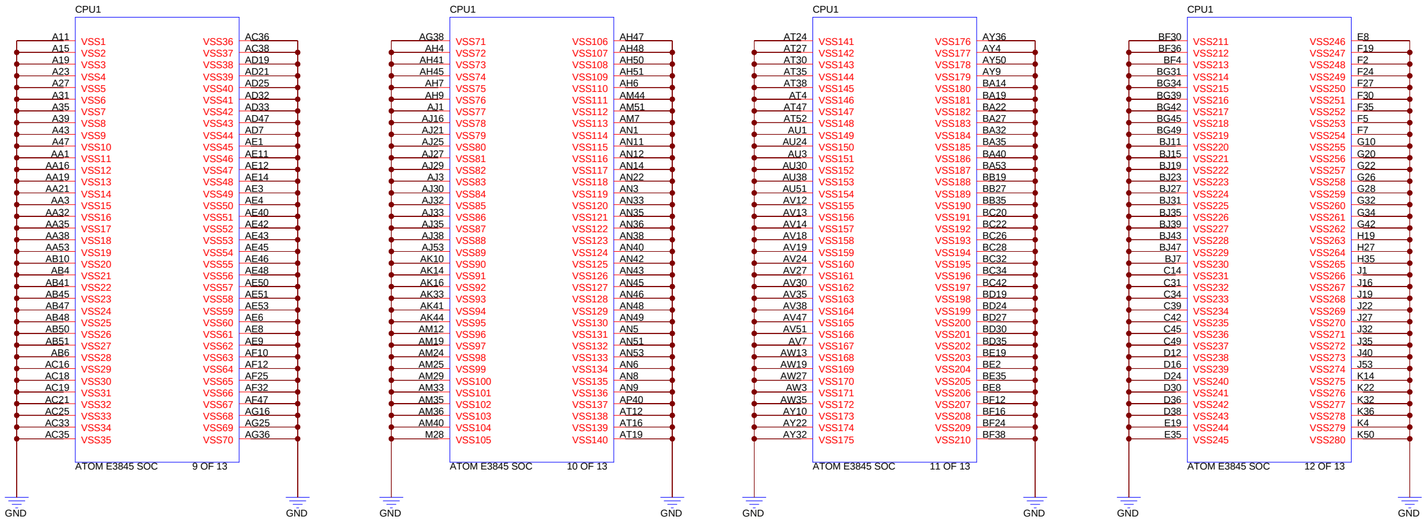
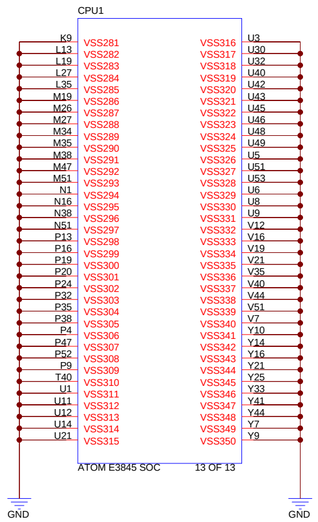


CPU-PWR2

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE: C	DWG NO: 80200-0139-G01
REV: R200	
DATE: 10/27/2016	SHEET 10 of 29





CPU-GND

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE C	DWG NO 80200-0139-G01
REV	R200
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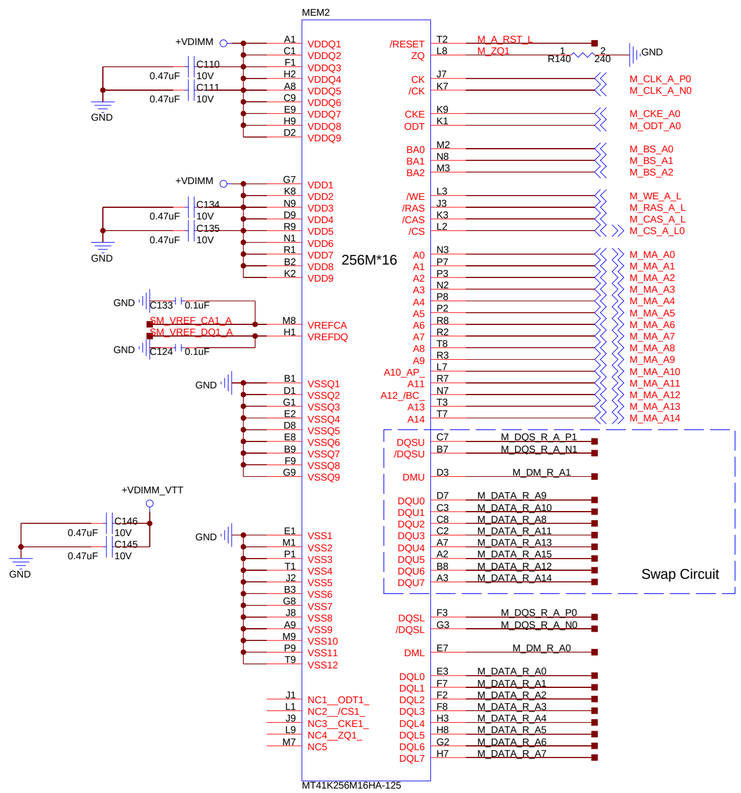

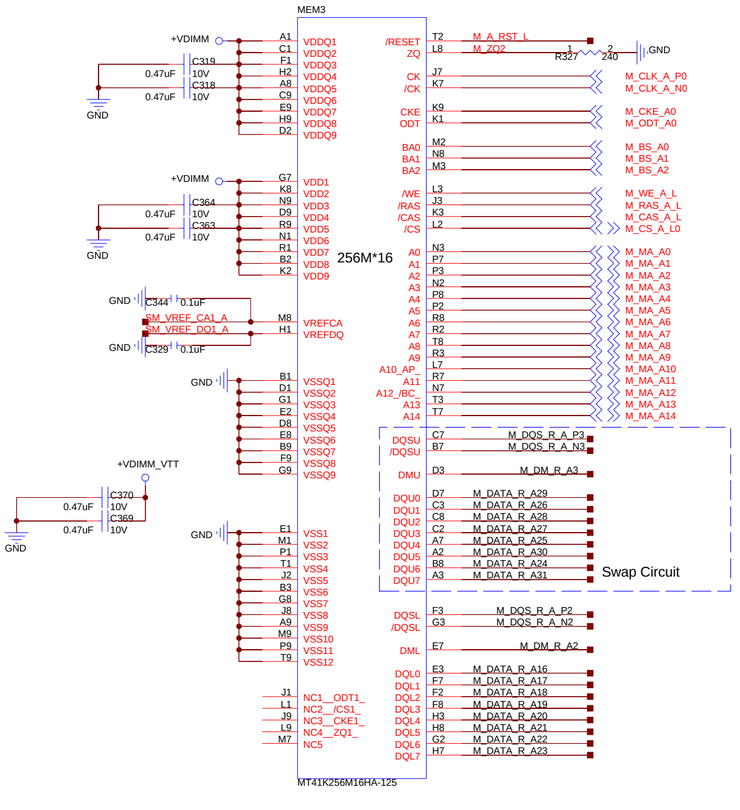

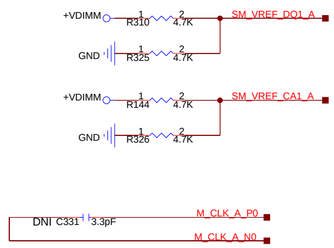

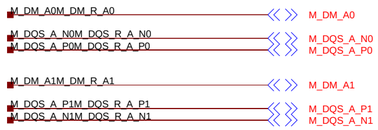

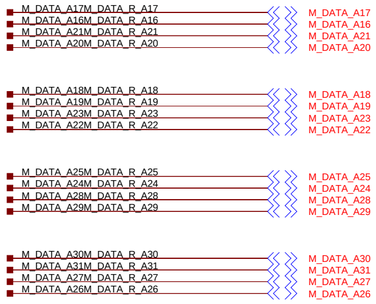

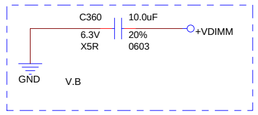

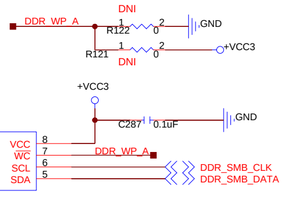

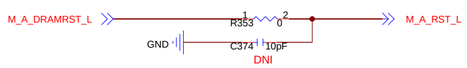

NOTE: COMPATIBLE DDR3L MEMORIES
FOR THE MINNOWMAX
ARE THE FOLLOWING:
MICRON MT41K128M16HA-125:D,
MICRON MT41K256M16HA-125:E,
MICRON MT41K512M16TNA-125:X

Memory_CHA-1

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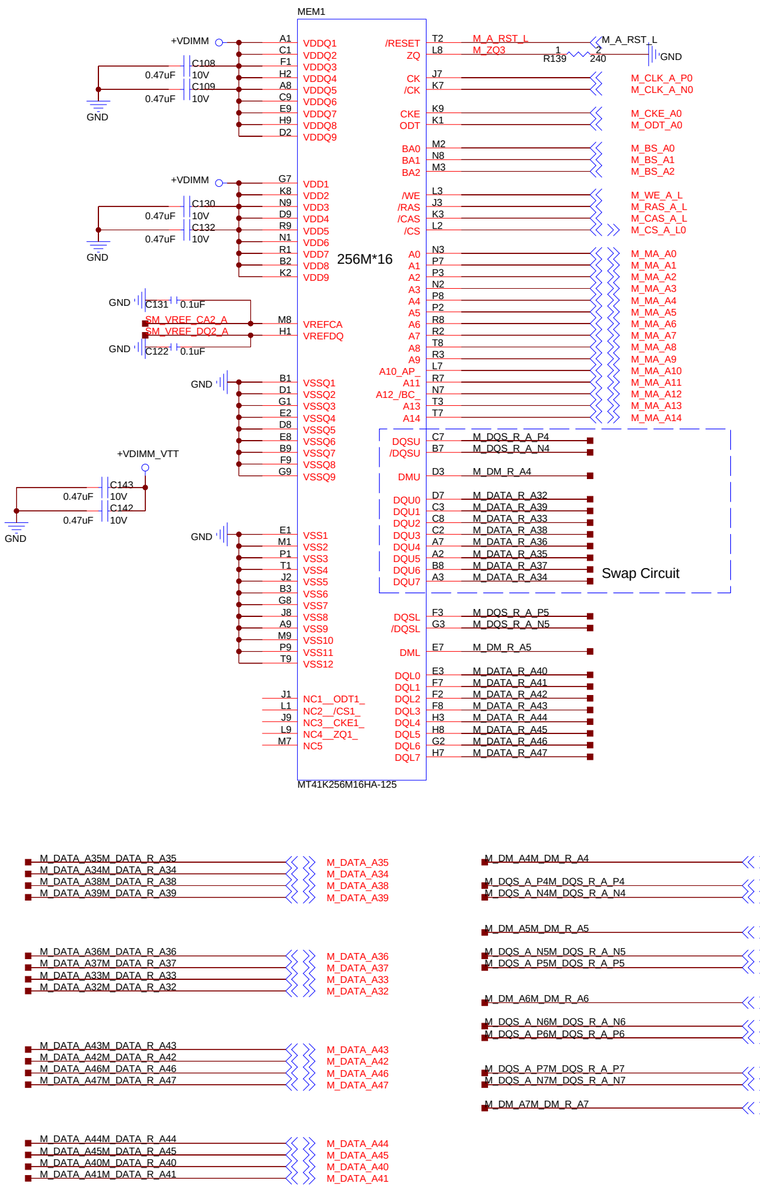

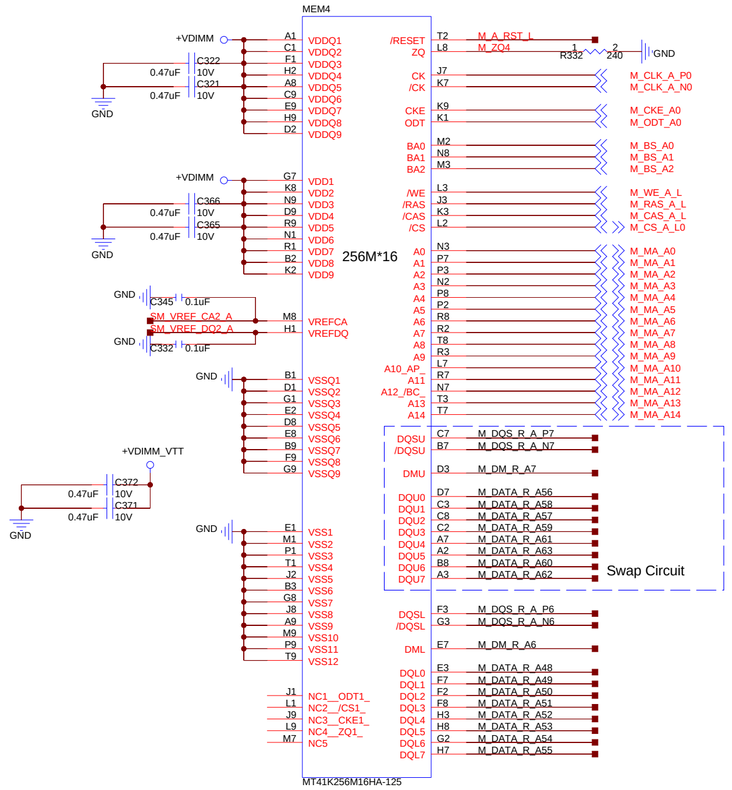

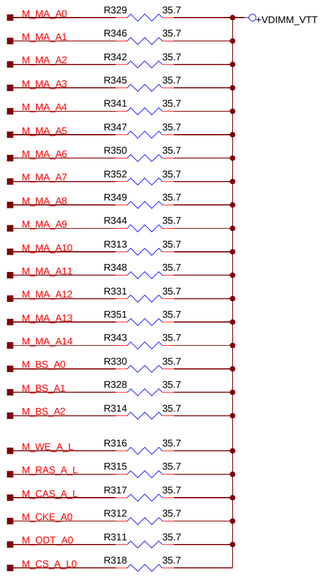

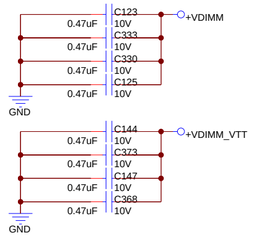

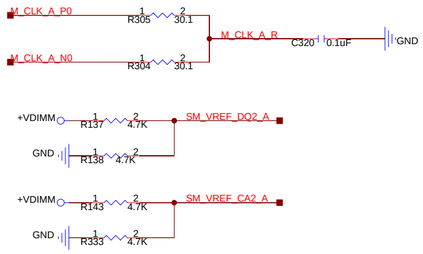

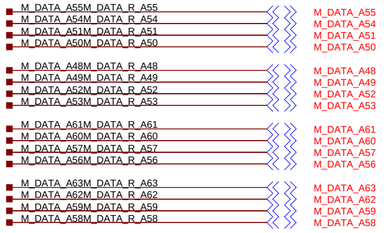

NOTE: COMPATIBLE DDR3L MEMORIES
FOR THE MINNOWMAX
ARE THE FOLLOWING:
MICRON MT41K128M16HA-125:D,
MICRON MT41K256M16HA-125:E,
MICRON MT41K512M16TNA-125:X

Memory_CHA-2

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SIZE C	DWG NO 80200-0139-G01
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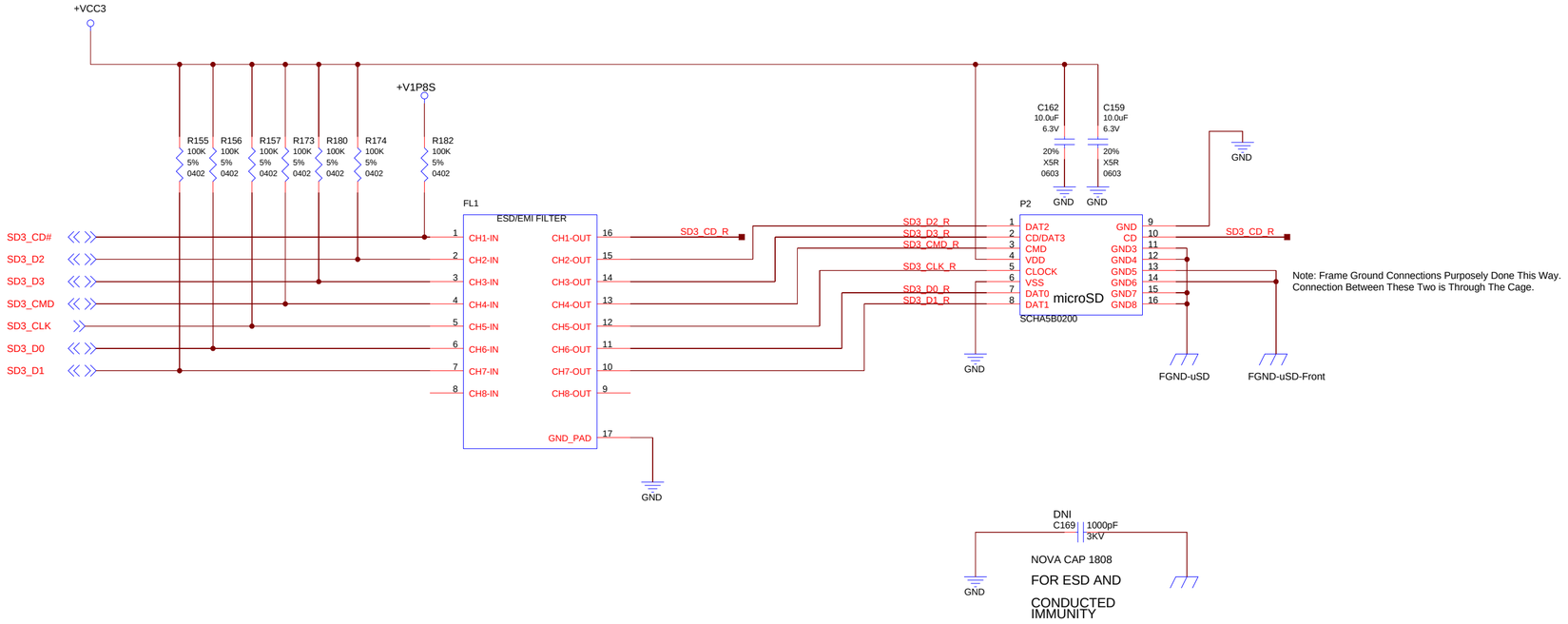

uSD CARD CAGE

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
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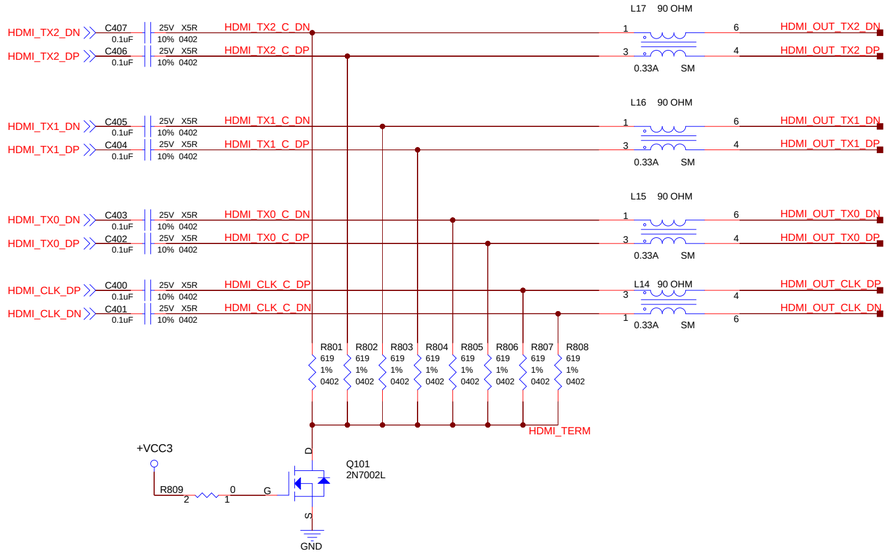
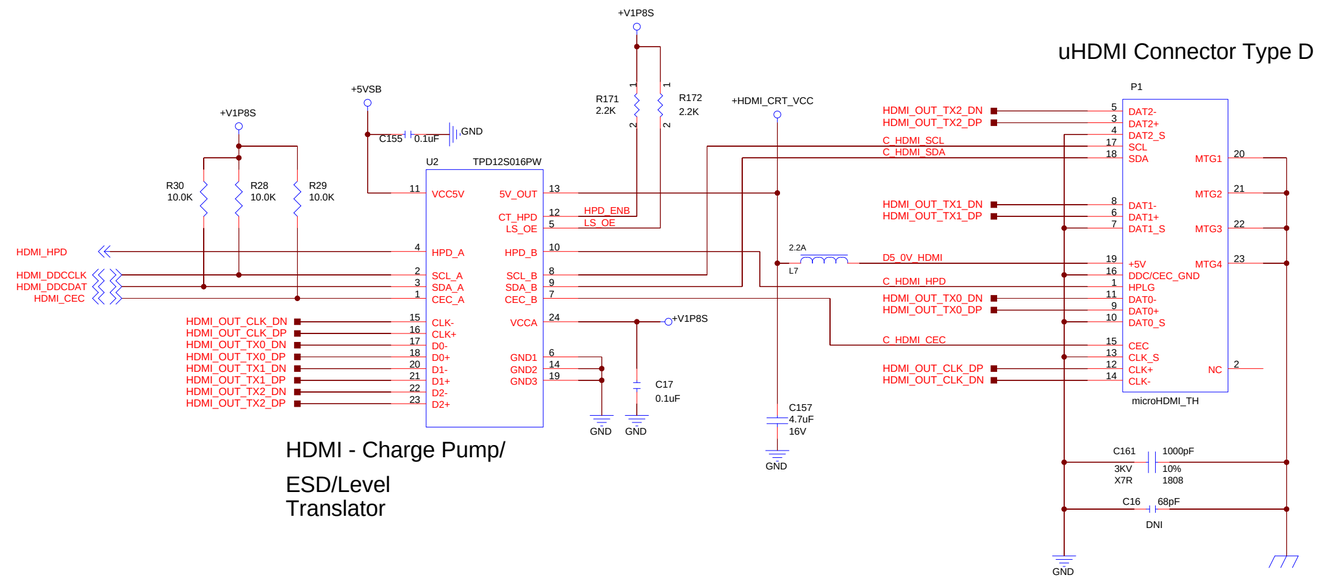
DATE: 10/27/2016	SHEET 14 of 29

HDMI_TXn_DP/N should be longer than HDMI_CLK_DN/P





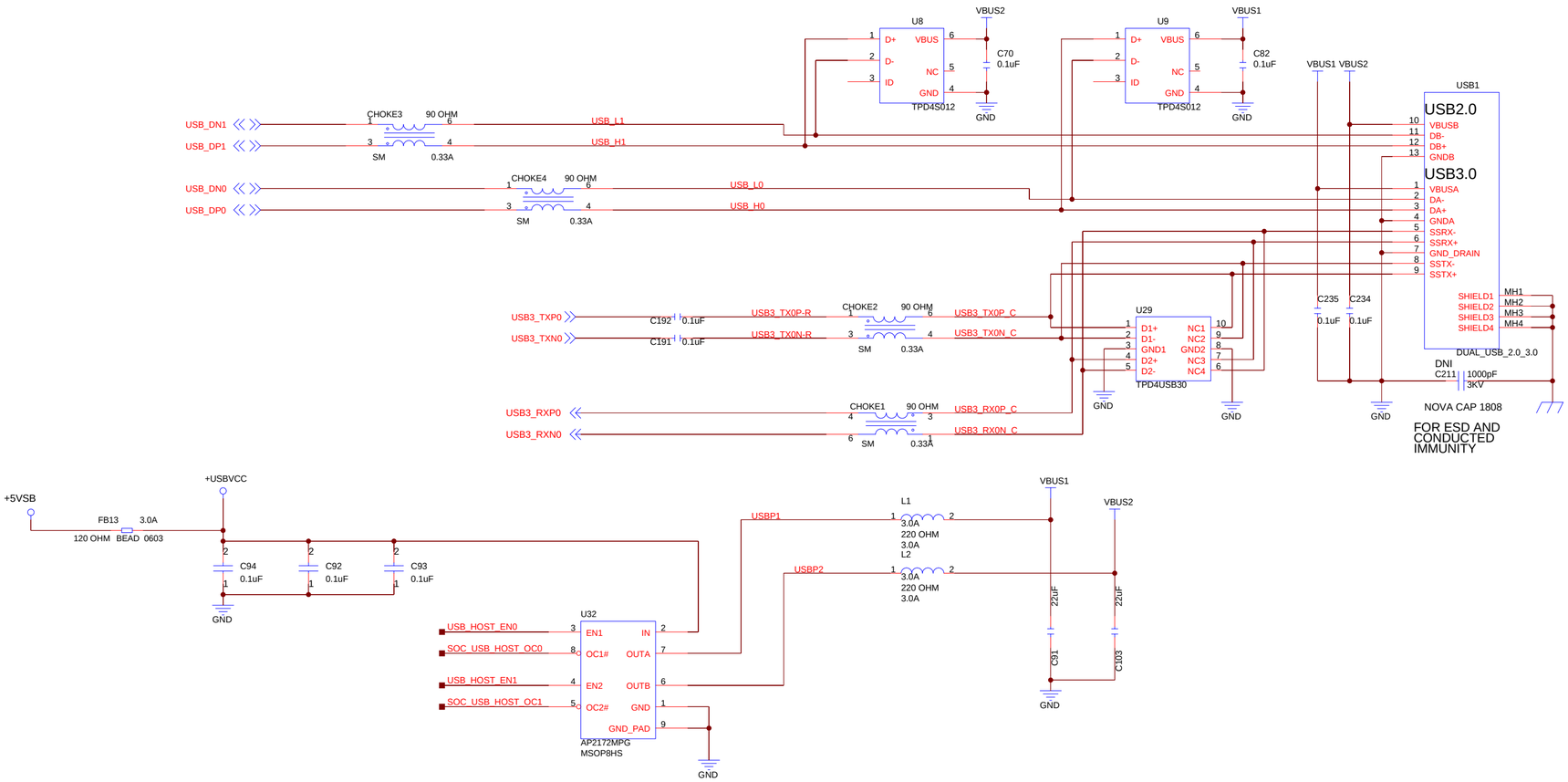
HDMI - Charge Pump/

ESD/Level
Translator

uHDMI Connector Type D

uHDMI

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE C	DWG NO 80200-0139-G01
REV	R200
DATE 10/27/2016	SHEET 15 of 29



USB3+USB2

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE C	DWG NO 80200-0139-G01
REV	R200
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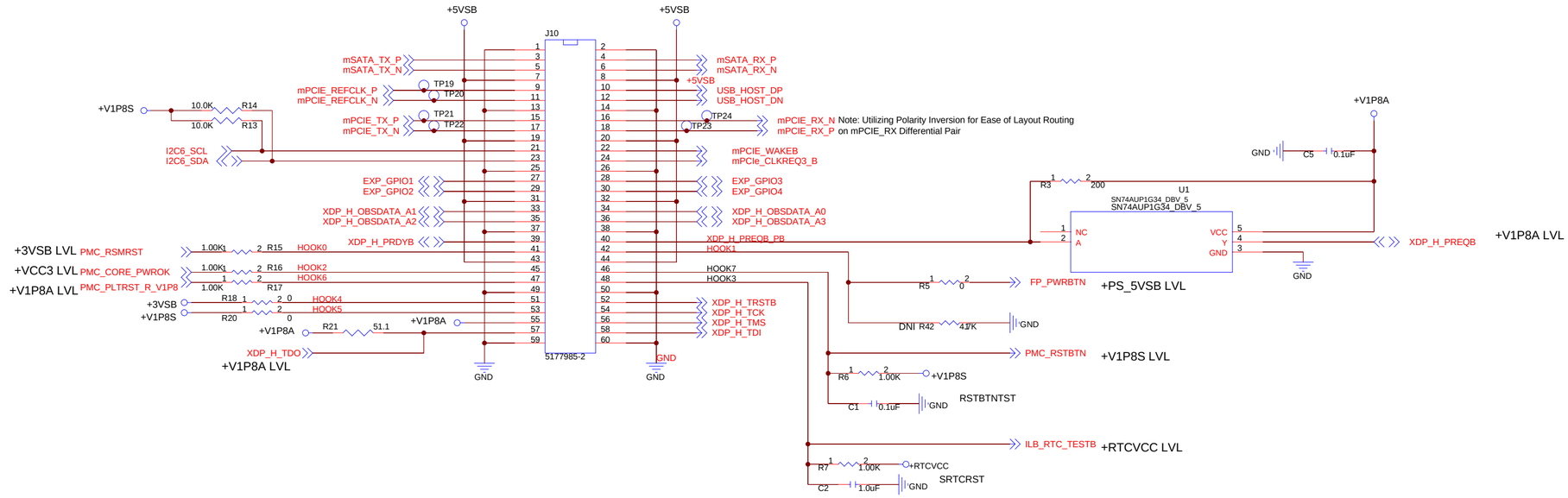
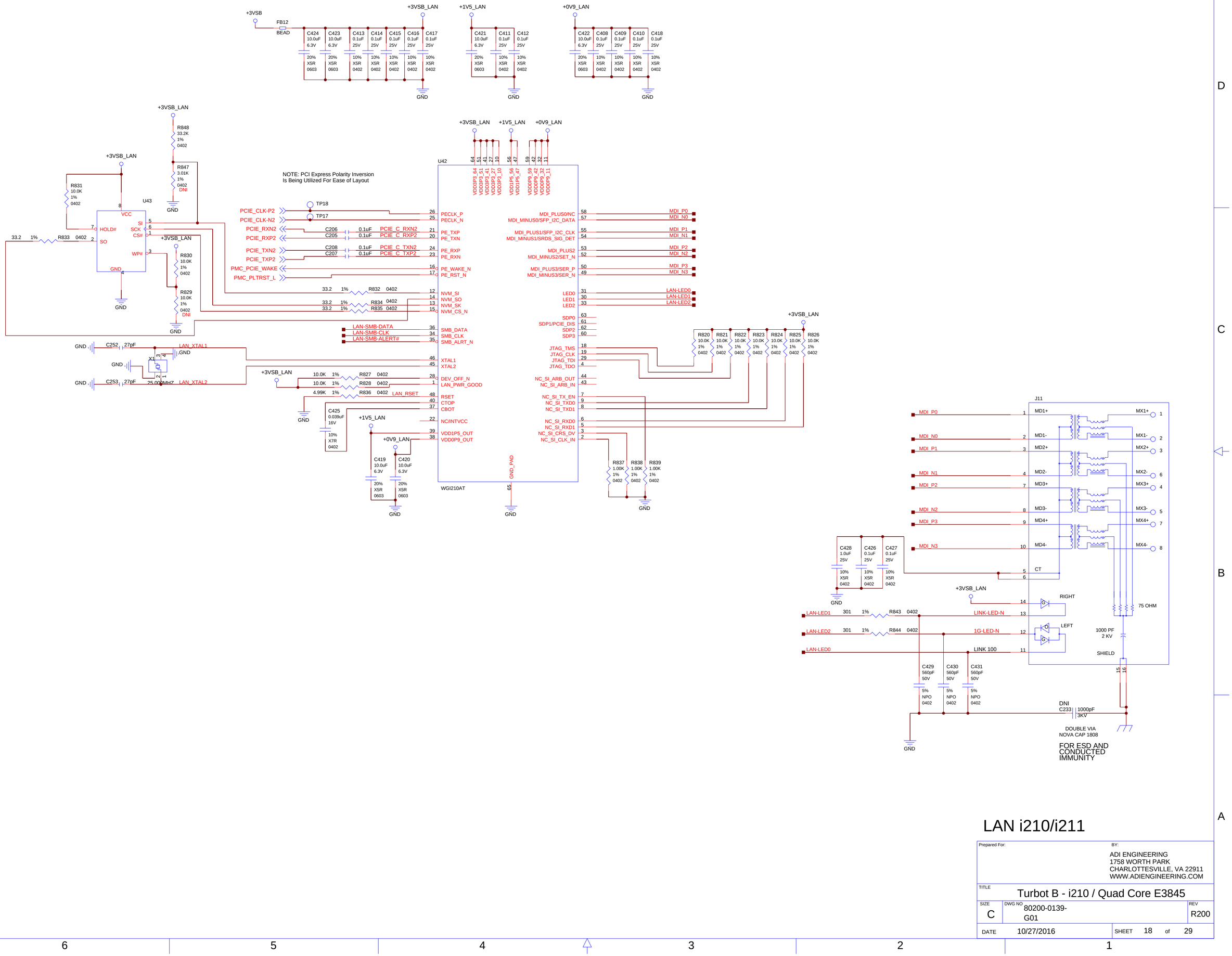
EXPANSION HS CONNECTOR WITH
mPCIE, mSATA, I2S AUDIO, GPIO, and XDP I/O



EXPANSION CONNECTOR I/O

Prepared For:	BY: ADI ENGINEERING 1758 WORTH PARK CHARLOTTESVILLE, VA 22911 WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE: C	DWG NO: 80200-0139-G01 — REV: R200
DATE: 10/27/2016	SHEET 17 of 29



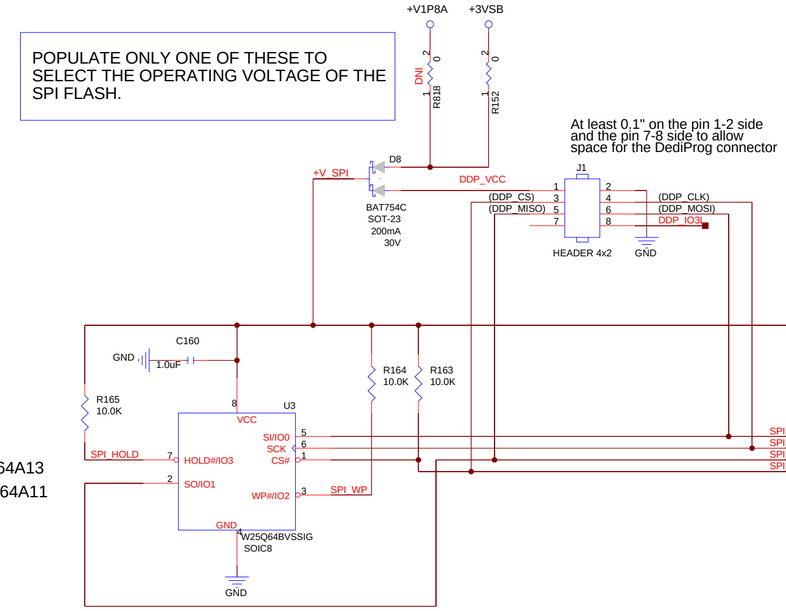
LAN i210/i211

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE: C	DWG NO: 80200-0139-G01
REV: R200	
DATE: 10/27/2016	SHEET 18 of 29

(BLANK)

Prepared For:	BY: ADI ENGINEERING 1758 WORTH PARK CHARLOTTESVILLE, VA 22911 WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE: C	DWG NO: 80200-0139-G01
REV: R200	
DATE: 10/27/2016	SHEET 19 of 29

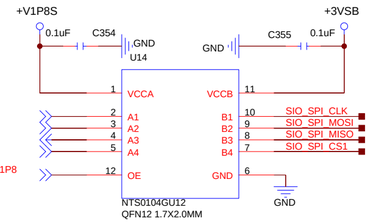
POPULATE ONLY ONE OF THESE TO SELECT THE OPERATING VOLTAGE OF THE SPI FLASH.

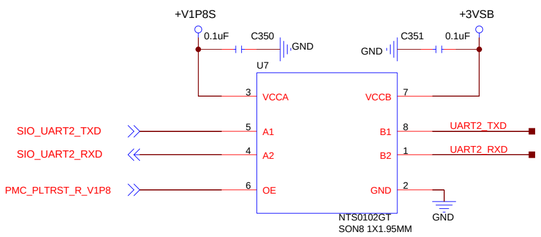


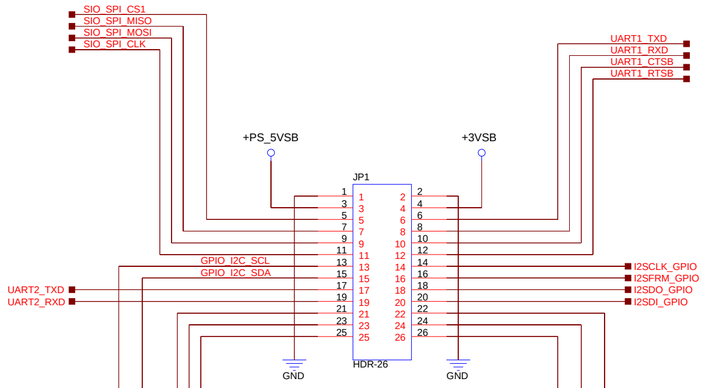
NOTE: COMPATIBLE U3 SPI ROM PARTS ARE THE FOLLOWING:

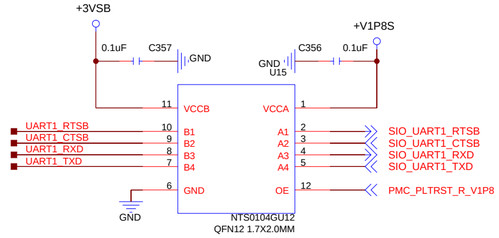
3.3V: WINBOND W25Q64BVSSIG, MICRON N25Q064A13

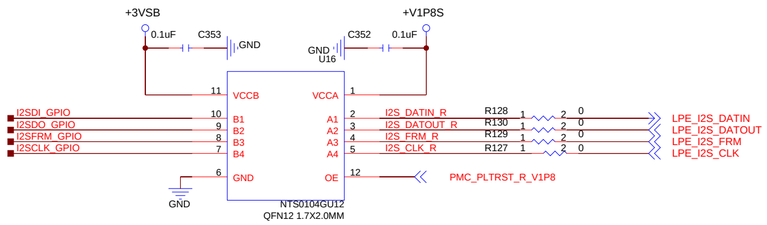
1.8V: WINBOND W25Q64FWSSIG, MICRON N25Q064A11



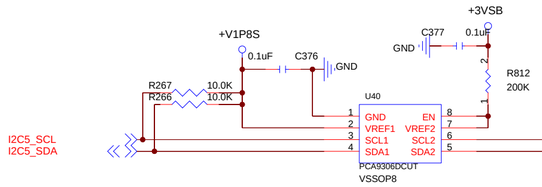


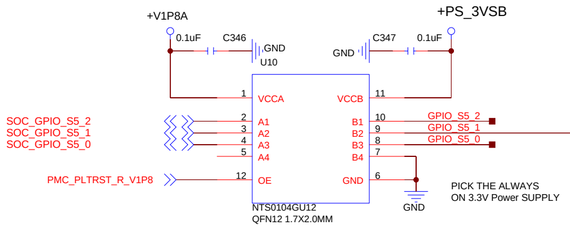




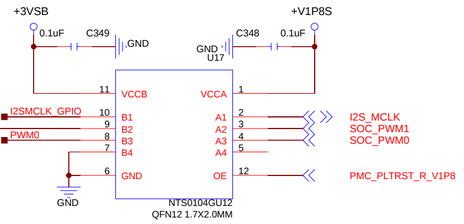


PICK THE ALWAYS ON 3.3V Power SUPPLY





PICK THE ALWAYS ON 3.3V Power SUPPLY

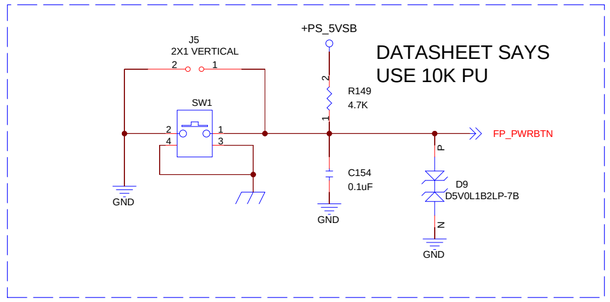


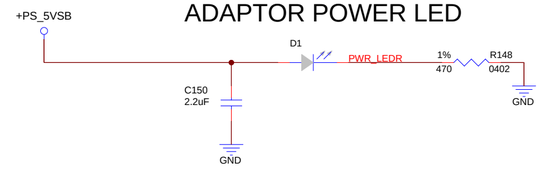
SPI PROM/LSS HEADER

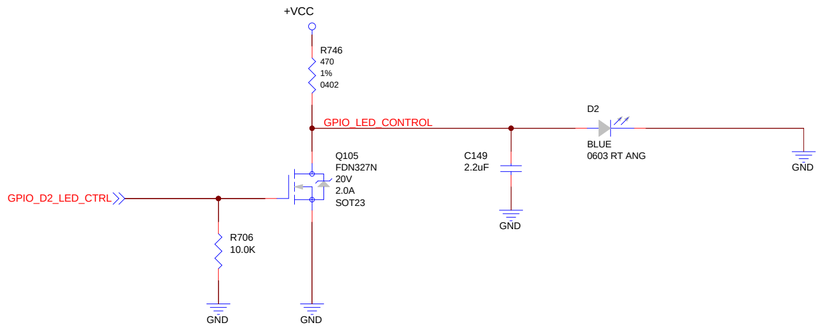
Prepared For:

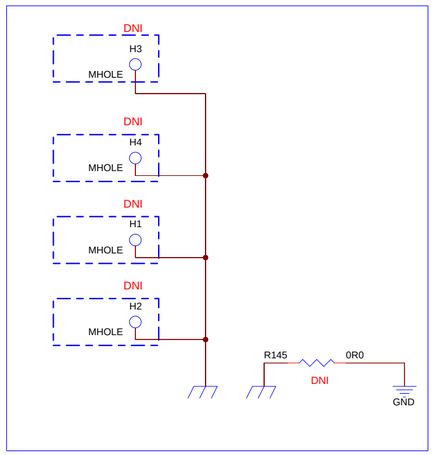
BY:
ADI ENGINEERING
1758 WORTH PARK
CHARLOTTESVILLE, VA 22911
WWW.ADIENGINEERING.COM

TITLE	Turbot B - i210 / Quad Core E3845		
SIZE C	DWG NO 80200-0139-G01		REV R200
DATE 10/27/2016		SHEET 20 of 29	









PWR BTN / LED / HOLES

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE C / DWG NO 80200-0139-G01 / REV R200	
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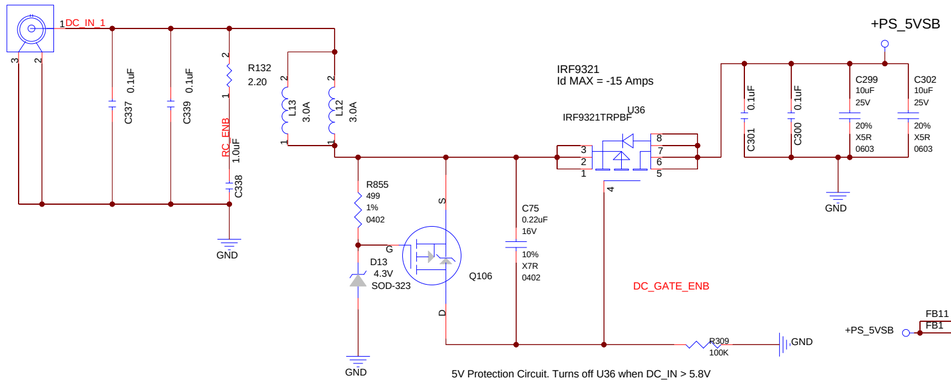
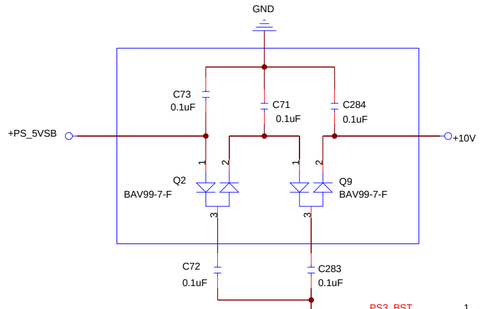
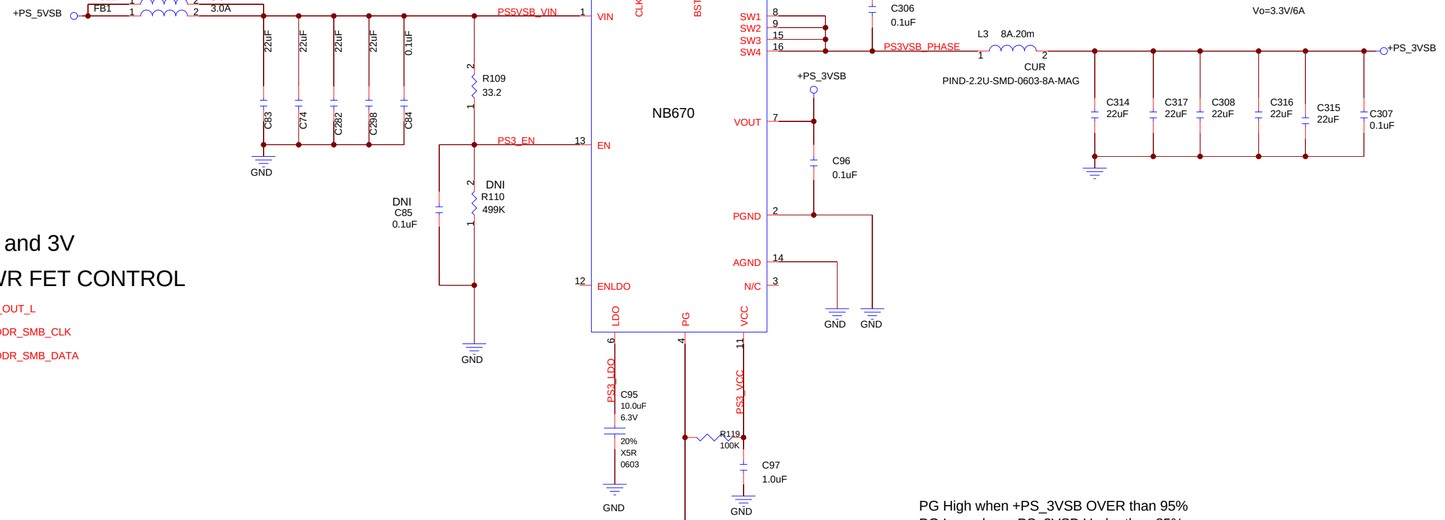
DC_IN 5V

J9 RAPC712



+3.3VSB / Boost +10V



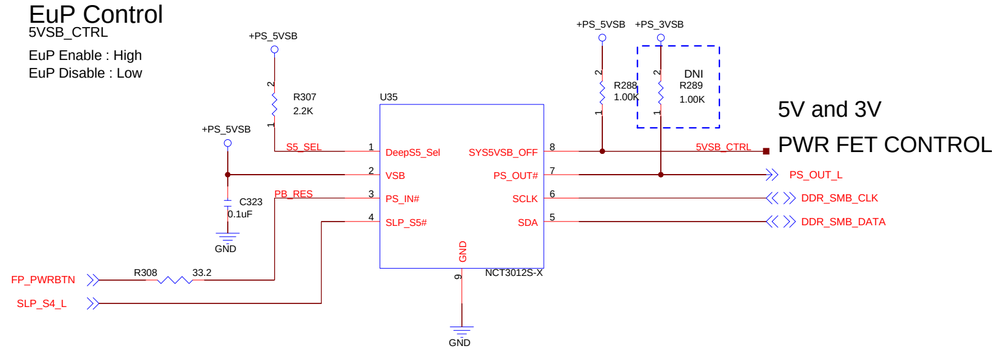


EuP Control

5VSB_CTRL

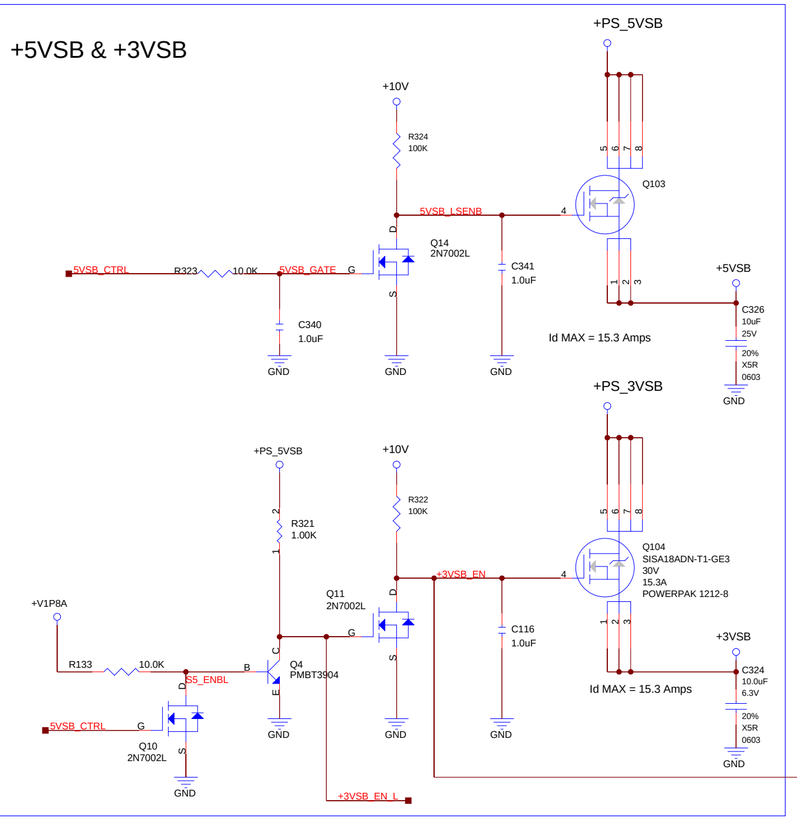
EuP Enable : High

EuP Disable : Low

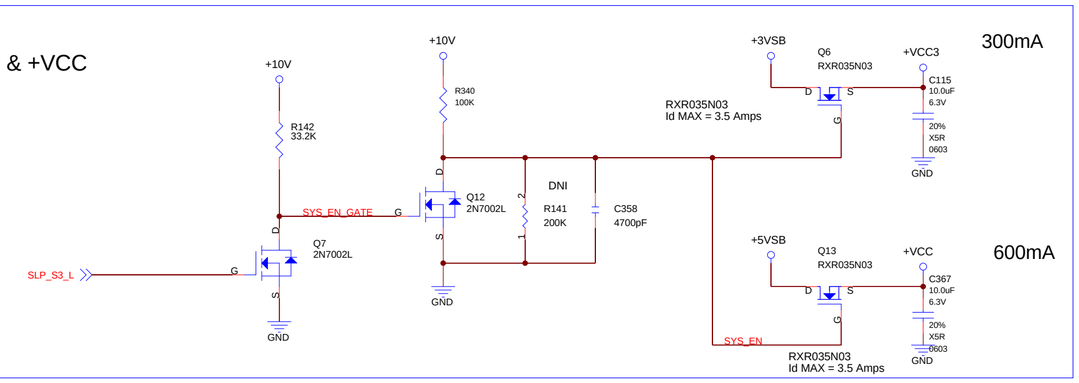


5V and 3V PWR FET CONTROL

+5VSB & +3VSB



+VCC3 & +VCC



+5V

+10V

D6 BAT54ALT1G

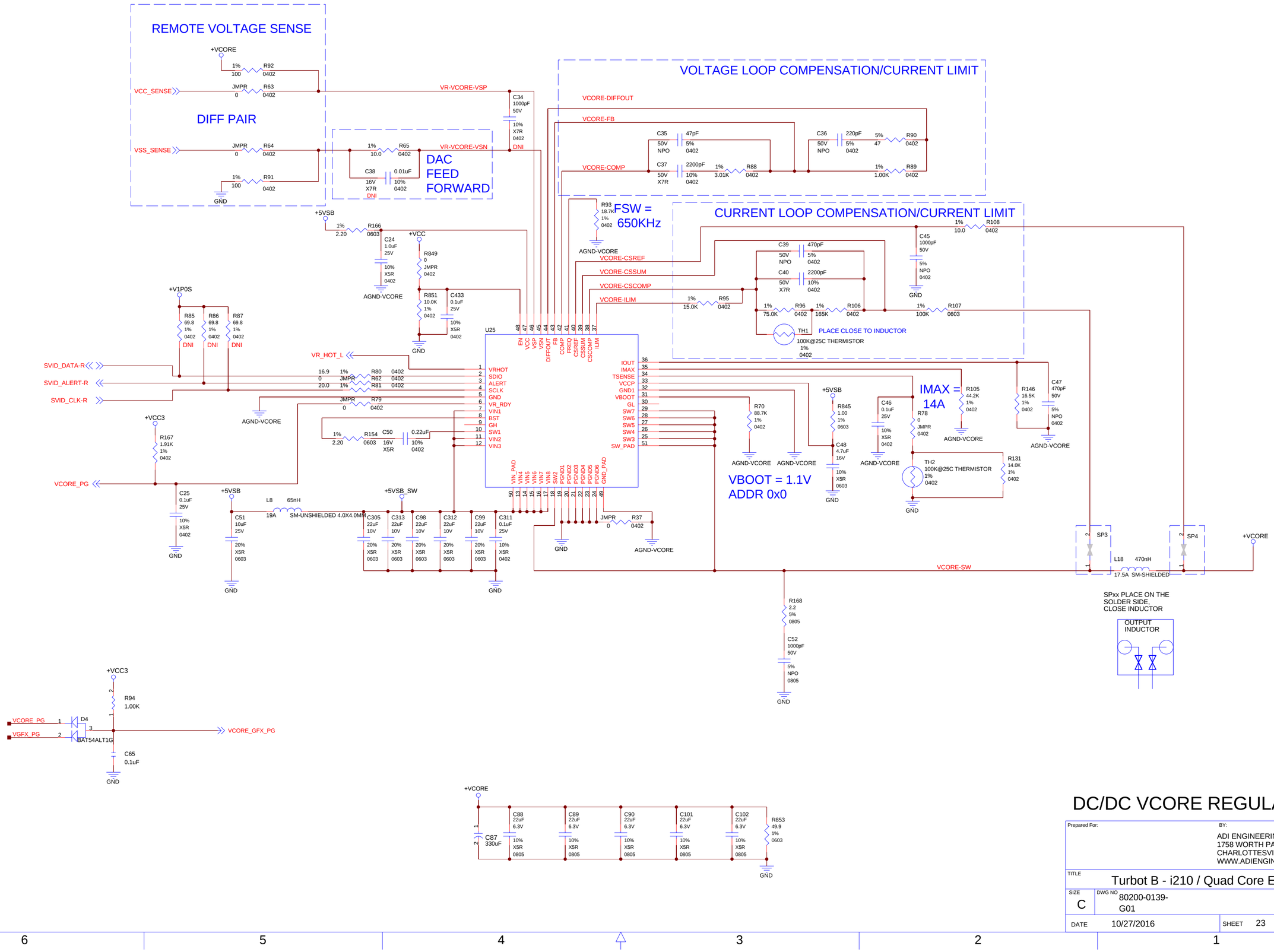
+3.3V

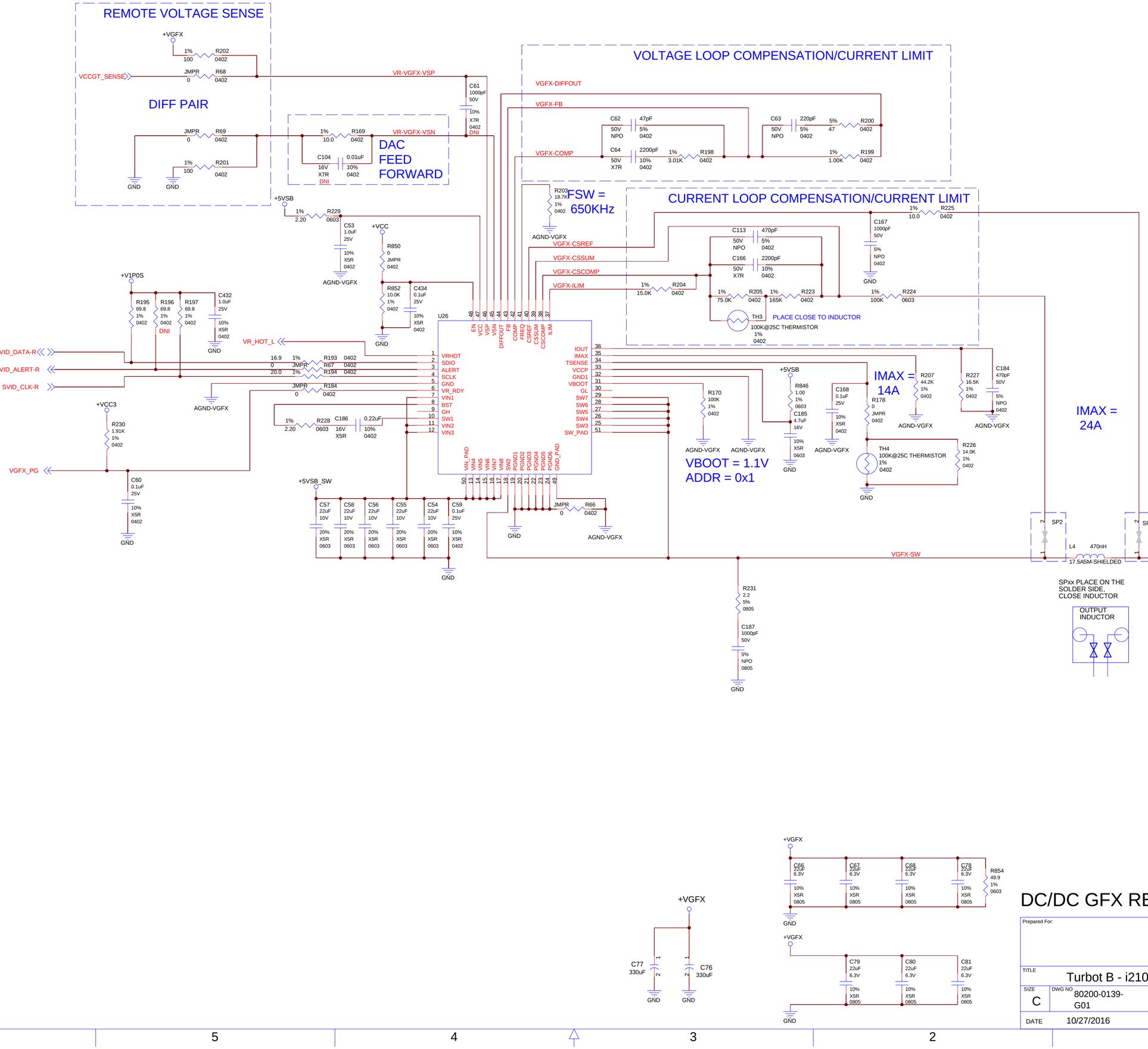
PMC_RSMRST

VRTC LEVEL (+3VSB)

DC-5VSB/3VSB / VCC / VCC3

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE C	DWG NO 80200-0139-G01
REV	R200
DATE 10/27/2016	SHEET 22 of 29


REMOTE VOLTAGE SENSE
+VCORE
VCC_SENSE
VSS_SENSE
DIFF PAIR
GND
DAC FEED FORWARD
VOLTAGE LOOP COMPENSATION/CURRENT LIMIT
VCORE-DIFFOUT
VCORE-FB
VCORE-COMP
FSW = 650KHz
CURRENT LOOP COMPENSATION/CURRENT LIMIT
VCORE-CSREF
VCORE-CSSUM
VCORE-CSCOMP
VCORE-ILIM
TH1
PLACE CLOSE TO INDUCTOR
100K@25C THERMISTOR
+5VSB
+VCC
+V1P0S
AGND-VCORE
U25
VR_HOT_L
SVID_DATA-R
SVID_ALERT-R
SVID_CLK-R
VRHOT
SDIO
ALERT
SCLK
GND
VR_RDY
VIN1
BST
GH
SW1
VIN2
VIN3
+VCC3
VCORE_PG
+5VSB_SW
L8 65nH
19A SM-UNSHIELDED 4.0X4.0MM
IOUT
IMAX
TSENSE
VCCP
GND1
VBOOT
GL
SW7
SW6
SW5
SW4
SW3
SW_PAD
IMAX = 14A
TH2
100K@25C THERMISTOR
VBOOT = 1.1V
ADDR 0x0
VCORE-SW
SP3
SP4
L18 470nH
17.5A SM-SHIELDED
+VCORE
SPxx PLACE ON THE SOLDER SIDE, CLOSE INDUCTOR
OUTPUT INDUCTOR
VCORE_PG
VGFX_PG
D4
BAT54ALT1G
VCORE_GFX_PG
+VCORE
DC/DC VCORE REGULATOR
Prepared For:
BY:
ADI ENGINEERING
1758 WORTH PARK
CHARLOTTESVILLE, VA 22911
WWW.ADIENGINEERING.COM
TITLE
Turbot B - i210 / Quad Core E3845
SIZE C
DWG NO 80200-0139-G01
REV R200
DATE 10/27/2016
SHEET 23 of 29



DC/DC GFX REGULATOR

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE: C	DWG NO: 80200-0139-G01
REV	R200
DATE	10/27/2016
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VDIMM

F= (Vin - 0.5) / 3.85p*Vin*Rton
Rton=806K , F=285KHz

RT8207M S3 and S5 truth table

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	on		on
S3	Lo	Hi	on		Off(Hi-Z)
S4/S5	Lo	Lo	Off Discharge	Off Discharge	Off Discharge

+VDIMM_VTT

Imax:0.6A

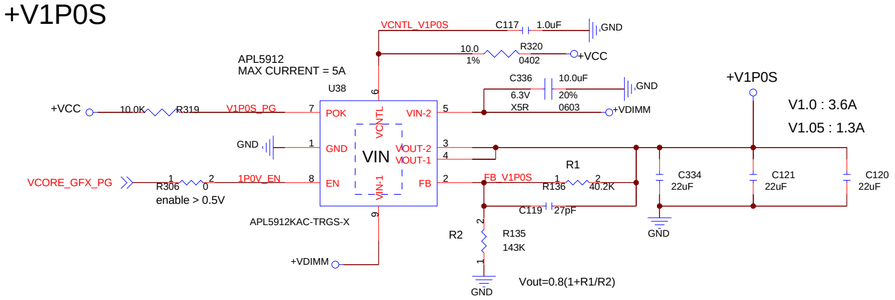
1.35V
Imax. 7.1A
OCP. 11A

DCR=10mohm
Idc= 11A

DC/DC-DIMM/DDR_VTT

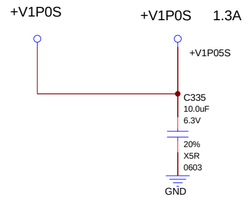
Prepared For:	BY: ADI ENGINEERING 1758 WORTH PARK CHARLOTTESVILLE, VA 22911 WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE: C	DWG NO: 80200-0139-G01
REV	R200
DATE: 10/27/2016	SHEET 25 of 29

+V1P0S

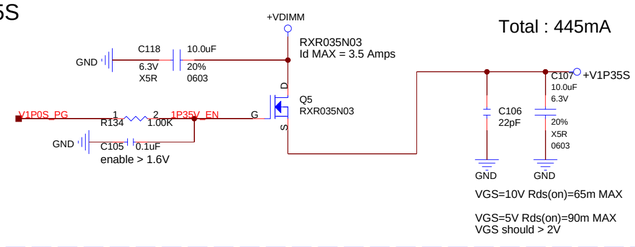


+V1P05S

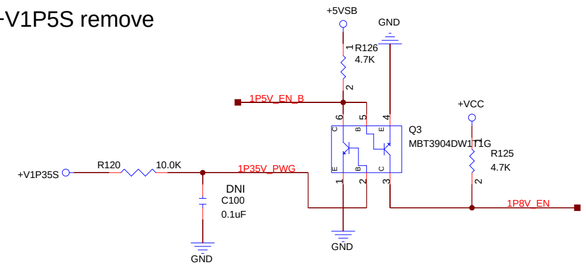
Combine +V1P0S and +V1P05S



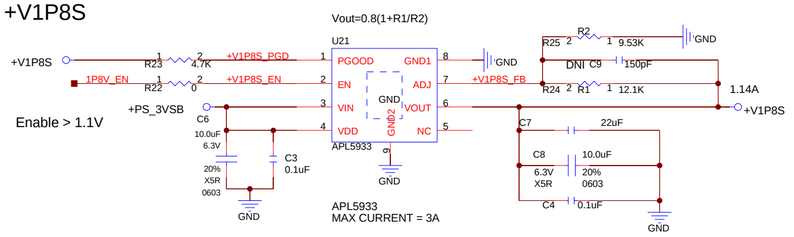
+V1P35S



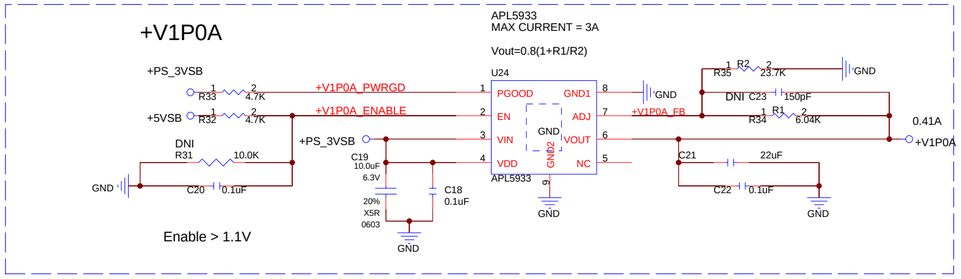
+V1P5S remove



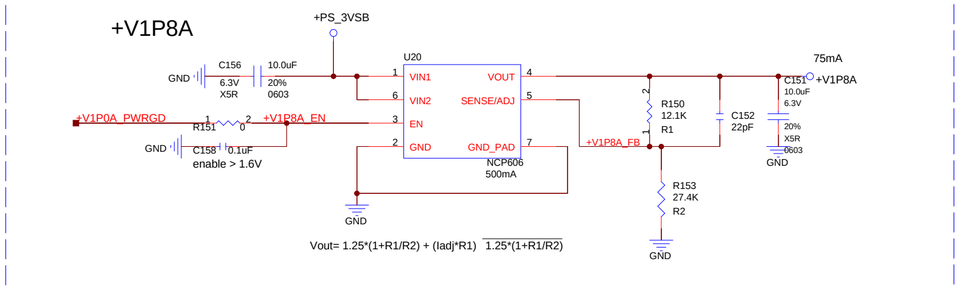
+V1P8S



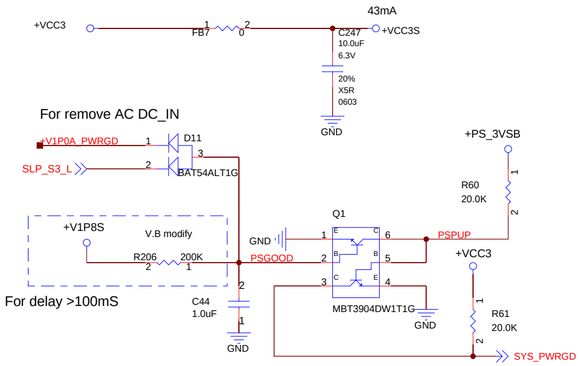
+V1P0A



+V1P8A



+VCC3S(For CPU)



DC-DC VOLTAGE

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	Turbot B - i210 / Quad Core E3845
SIZE: C	DWG NO: 80200-0139-G01
REV: R200	
DATE: 10/27/2016	SHEET 26 of 29

PCH-GPIO function

Pin Name	Power Well	Usage	Boot Set
GPIO_S5[00]	1P8VSB, 20k,H	SOC_GPIO_S5_0 (LSS CONN)	GPO
GPIO_S5[01]	1P8VSB, 20k,H	SOC_GPIO_S5_1 (LSS CONN)	GPO
GPIO_S5[02]	1P8VSB, 20k,H	SOC_GPIO_S5_2 (LSS CONN)	GPO
GPIO_S5[03]	1P8VSB, 20k,H	mPCIE_WAKEB	GPI
GPIO_S5[04]	1P8VSB, 20k,L	OPEN	GPO
GPIO_S5[05]	1P8VSB, 20k,L	BOM OPTION	GPI
GPIO_S5[06]	1P8VSB, 20k,L	BOM OPTION	GPI
GPIO_S5[07]	1P8VSB, 20k,L	BOM OPTION	GPI
GPIO_S5[08]	1P8VSB, 20k,H	HDMI_DC_DC ENABLE	GPO
GPIO_S5[09]	1P8VSB, 20k,H	HDMI LD SWITCH ENABLE	GPO
GPIO_S5[10]	1P8VSB, 20k,H	TXE UNLOCK control	GPO
GPIO_S0_SC[022]	1P8V, 20k,H	OPEN	GPO
GPIO_S0_SC[023]	1P8V, 20k,H	XDP_H_OBSDATA_A0	GPO
GPIO_S0_SC[024]	1P8V, 20k,H	XDP_H_OBSDATA_A1	GPO
GPIO_S0_SC[025]	1P8V, 20k,H	XDP_H_OBSDATA_A2	GPO
GPIO_S0_SC[026]	1P8V, 20k,H	XDP_H_OBSDATA_A3	GPO
GPIO_S0_SC[027]	1P8V, 20k,H	EXPANSION_BUS GPIO1	GPO
GPIO_S0_SC[028]	1P8V, 20k,H	EXPANSION_BUS GPIO2	GPO
GPIO_S0_SC[029]	1P8V, 20k,H	EXPANSION_BUS GPIO3	GPO
GPIO_S0_SC[030]	1P8V, 20k,H	EXPANSION_BUS GPIO4	GPO
GPIO_S0_SC[058]	1P8V, 20k,L	GPIO reserved	GPO
GPIO_S0_SC[059]	1P8V, 20k,L	GPIO reserved	GPO
GPIO_S0_SC[060]	1P8V, 20k,L	GPIO reserved	GPO
GPIO_S0_SC[057]	1P8V, 20k,H	Debug Port UART3 TXD	UART
GPIO_S0_SC[061]	1P8V, 20k,H	Debug Port UART3 RXD	UART

Interrupt mapping

Function	INT# port	PCIe*1 port	Device
LAN	INTC#	port 2	Intel i210/211

GPIO/HW MAPPING

Prepared For:

BY:
ADI ENGINEERING
1758 WORTH PARK
CHARLOTTESVILLE, VA 22911
WWW.ADIENGINEERING.COM

TITLE	Turbot B - i210 / Quad Core E3845	
SIZE C	DWG NO 80200-0139-G01	REV R200
DATE 10/27/2016	SHEET 27 of 29	

DC-IN: +5V

+PS_5VSB

EuP

N-MOS

Switching

7.5W max

+5VSB
8A max

Switching

+10V (VOLTAGE DBLR)

+PS_3VSB
4.8A max

+3VSB

N-MOS

DDR3L 1066MHz (SDRAM x4)	
+VDIMM	1.5A max
+VTT_DDR	0.5A max

0.27W*4 = 1.18W

+VTT_DDR:0.675V

LDO

N-MOS

1.917A max

Switching

1.35V 7.1A max

0.075A @V1P8A
1.14A @V1P8S

LDO

1.8V 0.075A max

1.8V

0.3A max
+VCC3

0.6A max
+VCC

N-MOS

N-MOS

LDO

1.8V 1.14A max

0.055A max

0.033A max

0.41A max

LDO

1.0V 410mA max

LDO

1.0V

2.75A max

LDO

1.05V

1.0A max

LDO

??? A max

0.75A max

1A max

0.2A max

0.07A max

??A max

1.4A max

EXPANSION SLOT	
+3.3V_AUX	??A

FRONT USB3 * 1PCS	
5V	0.9A

FRONT USB2 * 1PCS	
5V	0.5A

		Bay Trail - M	Bay Trail - I
VCORE	SVID	13A	
VNN	SVID	15A	
V1P35S	1.35V	1.3A	
V1P8A	1.8V	65mA	
V1P8S	1.8V	10mA	
V1P5S	1.8V	N/A	
V3P3A	3.3V	50mA	
V3P3S	3.3V	33mA	
V1P0A	1.0V	325mA	
V1P0S	1.0V	2.75A	
V1P05S	1.05V	1.0A	
V1P2A	N/A	N/A	
V1P2S	1.2V	21.3mA	0 mA
VRTC	RTC	160uA	

Can be grounded if MIPI CSI not used.

Battery
3V

ALC282		
AVDD	5.0V	N/A
DVDD	3.3V	N/A
PVDD	1.8V	N/A

LAN i210/211

VDD3P3	3.3V	225 mA

eMMC		
VCC	3.3V	200mA
VCCQ	1.8V	150mA

CSI Connector	
3.3V	70mA

POWER DELIVERY

Prepared For:

BY:
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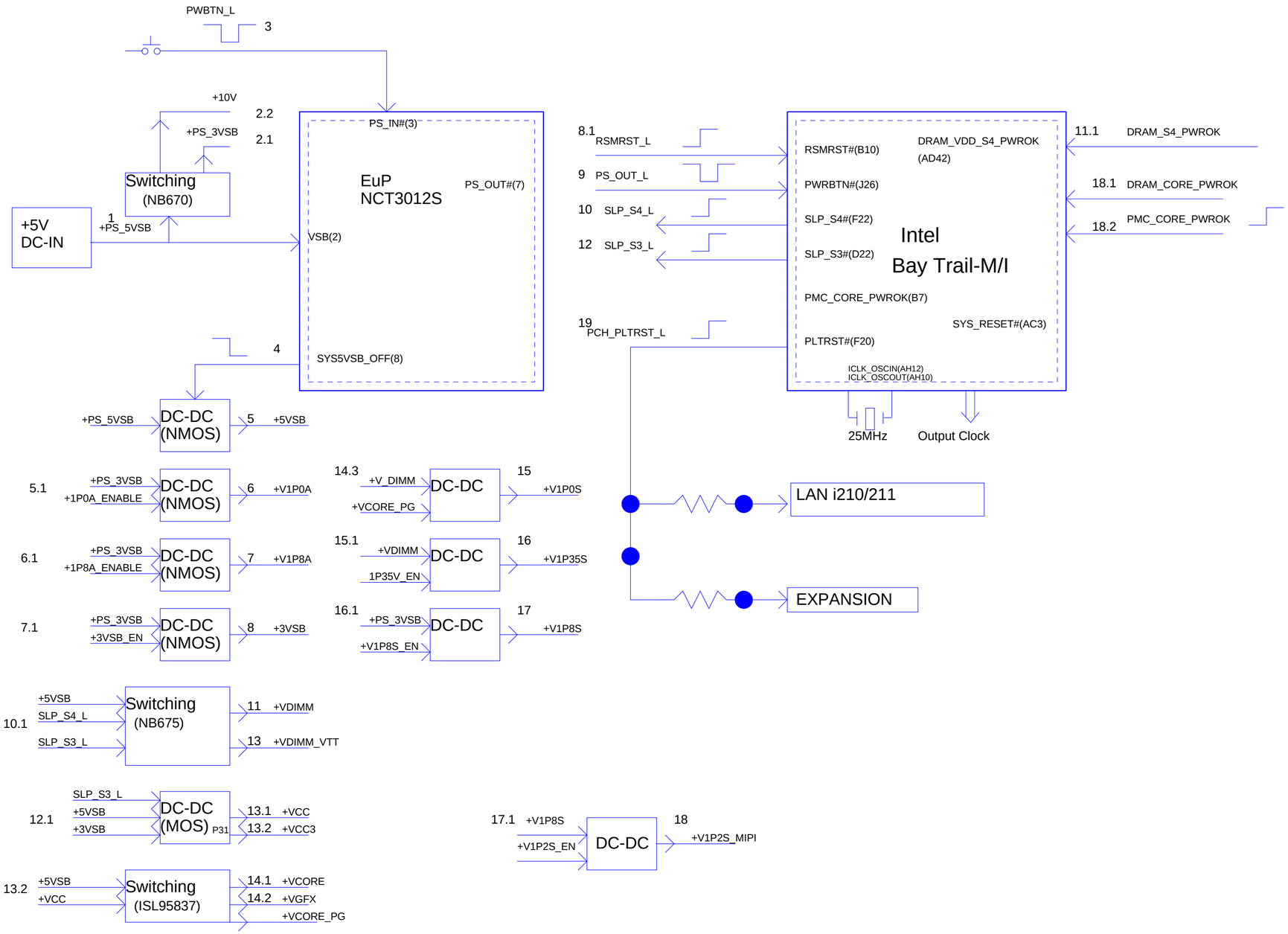
PWR Sequence & RST Diagram



POWER SEQUENCE

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