Minnow Project
Block Diagram – 3/20/2013

PROGRAM HEADER

SPI flash (BIOS)

SPI

Expansion Connector

POWER JACK

1GB DDR2 1.8V 4X256Mbx8

DDRM_BUS

5V_POWER → 5V BOARD PWR

LVDS — LVDS

HD Audio — HDA(1)

PCIe[1..2] — PCIE(2:1)

SMB — SMB_BUS

SATA Connector — SATA0_BUS

CAN — CAN BUS

SATA1 — SATA1_BUS

USB HOST[4] — USB[4]

UART[1, 2] — UART[2:1]

I2C0 — I2C0_BUS

SPI — SPI_BUS

GPIO[0..7] — GPIO[7:0]

SDIO[1] — SDIO[1]

Intel Atom E6xx

SDVO → Sil 1362 → DVI Connector

GPIO → Buffer → Header

GPIO/GPIO_SUS → Switches & LEDs

XDP_BUS → JTAG Connector

HDA(0)

AUDIO CHIP (ALC262) — AUD_OUT → , AUD_IN ←

PCIe[0]

Clocks

Power Management

DAC6011 ← 5V BOARD PWR

Intel Platform Controller Hub EG20T

SDIO[0] → microSD Connector

RGMII → PHY AR8031_AL1A → DP[3:0] → 10/100/1000 RJ-45 MAGJACK

USB_DEV_BUS → Micro USB-B Connector

USB[0,1] → 2x USB Connector

UART[0] → UART to USB FT230XS → Mini USB-B Connector

BOARD BLOCK DIAGRAM

minnowboard.org

CircuitCo — Printed Circuit Board Solutions

FOR ALL DESIGN FILES, INCLUDING BILL OF MATERIALS AND GERBER FILES, PLEASE VISIT WWW.MINNOWBOARD.ORG

INTEL MINNOW BOARD PRODUCTION

1380 Presidential Dr Ste#100 Richardson, TX 75081

Size	Date Modified	DWG NO	Rev
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Engineer(s)		Sheet	
MINNOW_TEAM		1 of 22	

ATOM DDR2 I/O - LOWER WORD (15:0)

INTEL_ATOM_Processor_E6XX

U5A

DDR2

1 OF 7

DDR_M_BA[2..0]   2,3
DDR_M_MA[14..0]   2,3
DDR_M_DQ[31..0]   2,3

U5A pin labels (left side):
DDR_M_MA14 AJ8 — M_MA14
DDR_M_MA13 AU10 — M_MA13
DDR_M_MA12 AD5 — M_MA12
DDR_M_MA11 AG8 — M_MA11
DDR_M_MA10 W10 — M_MA10
DDR_M_MA9 AF7 — M_MA9
DDR_M_MA8 AB7 — M_MA8
DDR_M_MA7 W8 — M_MA7
DDR_M_MA6 AH7 — M_MA6
DDR_M_MA5 AP7 — M_MA5
DDR_M_MA4 AN2 — M_MA4
DDR_M_MA3 Y7 — M_MA3
DDR_M_MA2 AN4 — M_MA2
DDR_M_MA1 AA10 — M_MA1
DDR_M_MA0 AA8 — M_MA0

DDR_M_BA2 AL2 — M_BS2
DDR_M_BA1 AM1 — M_BS1
DDR_M_BA0 AB5 — M_BS0

DDR_M_nRAS AJ10 — M_RASB   2,3
DDR_M_nCAS AP17 — M_CASB   2,3
DDR_M_nWE AT13 — M_WEB   2,3

DDR_M_nCS1 AJ12 — M_CSB1   3
DDR_M_nCS0 AN14 — M_CSB0   2,3

DDR_M_CKE1 AM7 — M_CKE1   3
DDR_M_CKE0 AK7 — M_CKE0   2,3

DDR_M_CKP AU8 — M_CKP   2,3
DDR_M_CKN AT7 — M_CKN   2,3

DDR_M_ODT1 AN12 — M_ODT1   3
DDR_M_ODT0 AK11 — M_ODT0   2,3

DDR_M_SRFWEN AT9 — M_SRFWEN
AL8 — NC45

U5A pin labels (DQ side):
AT15 M_DQ31 DDR_M_DQ31
AL10 M_DQ30 DDR_M_DQ30
AN10 M_DQ29 DDR_M_DQ29
AP11 M_DQ28 DDR_M_DQ28
AT11 M_DQ27 DDR_M_DQ27
AU12 M_DQ26 DDR_M_DQ26
AP9 M_DQ25 DDR_M_DQ25
AN8 M_DQ24 DDR_M_DQ24
AU24 M_DQ23 DDR_M_DQ23
AT19 M_DQ22 DDR_M_DQ22
AT23 M_DQ21 DDR_M_DQ21
AU22 M_DQ20 DDR_M_DQ20
AT21 M_DQ19 DDR_M_DQ19
AT17 M_DQ18 DDR_M_DQ18
AU18 M_DQ17 DDR_M_DQ17
AU16 M_DQ16 DDR_M_DQ16
AH5 M_DQ15 DDR_M_DQ15
AM5 M_DQ14 DDR_M_DQ14
AP5 M_DQ13 DDR_M_DQ13
AK5 M_DQ12 DDR_M_DQ12
AJ4 M_DQ11 DDR_M_DQ11
AR4 M_DQ10 DDR_M_DQ10
AU6 M_DQ9 DDR_M_DQ9
AC4 M_DQ8 DDR_M_DQ8
AA4 M_DQ7 DDR_M_DQ7
AE4 M_DQ6 DDR_M_DQ6
AG4 M_DQ5 DDR_M_DQ5
AH1 M_DQ4 DDR_M_DQ4
AJ2 M_DQ3 DDR_M_DQ3
AF1 M_DQ2 DDR_M_DQ2
AK1 M_DQ1 DDR_M_DQ1
M_DQ0 DDR_M_DQ0

AP13 M_DM3 DDR_M_DM3   3
AU20 M_DM2 DDR_M_DM2   3
AF5 M_DM1 DDR_M_DM1   2
AG2 M_DM0 DDR_M_DM0   2

AU14 M_DQS3 DDR_M_DQS3   3
AP15 M_DQS2 DDR_M_DQS2   3
AT5 M_DQS1 DDR_M_DQS1   2
Y5 M_DQS0 DDR_M_DQS0   2

AC8 M_RCVENIN DDR_M_RCVEN
AD7 M_RCVENOUT
AE8 M_RCOMPOUT DDR_M_RCOMPOUT   R26   49.9

DDR_M_DQ[31..0]   2,3

U26 (MT47H256M8):
DDR_M_MA0 H8 A0
DDR_M_MA1 H3 A1
DDR_M_MA2 H7 A2
DDR_M_MA3 J2 A3
DDR_M_MA4 J8 A4
DDR_M_MA5 J3 A5
DDR_M_MA6 J7 A6
DDR_M_MA7 K2 A7
DDR_M_MA8 K8 A8
DDR_M_MA9 K3 A9
DDR_M_MA10 H2 A10
DDR_M_MA11 K7 A11
DDR_M_MA12 L2 A12
DDR_M_MA13 L8 A13
DDR_M_MA14 L3 A14
DDR_M_BA0 G2 BA0
DDR_M_BA1 G3 BA1
DDR_M_BA2 G1 BA2

E8 CK — DDR_M_CKP   2,3
F8 CKn — DDR_M_CKN   2,3
F2 CKE — DDR_M_CKE0   2,3
G8 CSn — DDR_M_nCS0   2,3
F7 RASn — DDR_M_nRAS   2,3
G7 CASn — DDR_M_nCAS   2,3
F3 WEn — DDR_M_nWE   2,3

C8 DQ0 DDR_M_DQ0
C2 DQ1 DDR_M_DQ1
D7 DQ2 DDR_M_DQ2
D3 DQ3 DDR_M_DQ3
D1 DQ4 DDR_M_DQ4
D9 DQ5 DDR_M_DQ5
B1 DQ6 DDR_M_DQ6
B9 DQ7 DDR_M_DQ7

DDR_M_DQ[31..0]   2,3

F9 ODT — DDR_M_ODT0   2,3
B7 DQS A8 DQSn B3 DM — DDR_M_DQS0   2 / DDR_M_DM0   2

VDD_DDR_1V8
A1 E9 H9 L1 VDD
A9 C1 C3 C7 C9 VDDQ
A3 E3 J1 K9 VSS
A7 B2 B8 D2 D8 VSSQ
E1 VDDL
E7 VSSDL   A2 NU/RDQSn
E2 VREF   L7 RFU
DDR_VREF

C136 0.1uF   C15 0.1uF

U1 (MT47H256M8, lower):
DDR_M_MA[14..0]   2,3
DDR_M_MA0 H8 A0
DDR_M_MA1 H3 A1
DDR_M_MA2 H7 A2
DDR_M_MA3 J2 A3
DDR_M_MA4 J8 A4
DDR_M_MA5 J3 A5
DDR_M_MA6 J7 A6
DDR_M_MA7 K2 A7
DDR_M_MA8 K8 A8
DDR_M_MA9 K3 A9
DDR_M_MA10 H2 A10
DDR_M_MA11 K7 A11
DDR_M_MA12 L2 A12
DDR_M_MA13 L8 A13
DDR_M_MA14 L3 A14
DDR_M_BA0 G2 BA0
DDR_M_BA1 G3 BA1
DDR_M_BA2 G1 BA2

DDR_M_CKP   2,3   R277   191
DDR_M_CKN   2,3

E8 CK — DDR_M_CKP   2,3
F8 CKn — DDR_M_CKN   2,3
F2 CKE — DDR_M_CKE0   2,3
G8 CSn — DDR_M_nCS0   2,3
F7 RASn — DDR_M_nRAS   2,3
G7 CASn — DDR_M_nCAS   2,3
F3 WEn — DDR_M_nWE   2,3

C8 DQ0 DDR_M_DQ8
C2 DQ1 DDR_M_DQ9
D7 DQ2 DDR_M_DQ10
D3 DQ3 DDR_M_DQ11
D1 DQ4 DDR_M_DQ12
D9 DQ5 DDR_M_DQ13
B1 DQ6 DDR_M_DQ14
B9 DQ7 DDR_M_DQ15

DDR_M_DQ[31..0]   2,3

F9 ODT — DDR_M_ODT0   2,3
B7 DQS A8 DQSn B3 DM — DDR_M_DQS1   2 / DDR_M_DM1   2

VDD_DDR_1V8
A1 E9 H9 L1 VDD
A9 C1 C3 C7 C9 VDDQ
A3 E3 J1 K9 VSS
A7 B2 B8 D2 D8 VSSQ
E1 VDDL
E7 VSSDL   A2 NU/RDQSn
E2 VREF   L7 RFU

DDR_VREF
C133 0.1uF
MT47H256M8

VDD_DDR_1V8
R70 10K
DNI R63 1K

VDD_DDR_1V8
R10 10K
DDR_VREF
Etch needs plane
R11 10K

Decoupling caps (top):
VDD_DDR_1V8
C137 2700pF   C117 2700pF   C116 0.1uF   C134 0.1uF   C135 2.2uF   C1 10uF

Decoupling caps (bottom):
VDD_DDR_1V8
C7 2700pF   C13 2700pF   C14 0.1uF   C8 0.1uF   C16 2.2uF   C2 10uF

MINNOW - CPU DDR2   I/O - DDR CHIPS 1/2

ATOM DDR2 I/O - UPPER WORD (31:16)

2,3 DDR_M_MA[14..0]

DDR_M_MA0
DDR_M_MA1
DDR_M_MA2
DDR_M_MA3
DDR_M_MA4
DDR_M_MA5
DDR_M_MA6
DDR_M_MA7
DDR_M_MA8
DDR_M_MA9
DDR_M_MA10
DDR_M_MA11
DDR_M_MA12
DDR_M_MA13
DDR_M_MA14

2,3 DDR_M_BA[2..0]

DDR_M_BA0
DDR_M_BA1
DDR_M_BA2

U27

Pin	Signal
H8	A0
H3	A1
H7	A2
J2	A3
J8	A4
J3	A5
J7	A6
K2	A7
K8	A8
K3	A9
H2	A10
K7	A11
L2	A12
L8	A13
L3	A14
G2	BA0
G3	BA1
G1	BA2

Pin	Signal			
E8	CK		DDR_M_CKP	2,3
F8	CKn		DDR_M_CKN	2,3
G8	CKE		DDR_M_CKE0	2,3
F7	CSn		DDR_M_nCS0	2,3
G7	RASn		DDR_M_nRAS	2,3
F3	CASn		DDR_M_nCAS	2,3
	WEn		DDR_M_nWE	2,3

Pin	Signal	Net
C8	DQ0	DDR_M_DQ16
C2	DQ1	DDR_M_DQ17
D7	DQ2	DDR_M_DQ18
D3	DQ3	DDR_M_DQ19
D9	DQ4	DDR_M_DQ20
D5	DQ5	DDR_M_DQ21
B1	DQ6	DDR_M_DQ22
B9	DQ7	DDR_M_DQ23

DDR_M_DQ[31..0] 2,3

Pin	Signal	Net
B7	DQS	DDR_M_DQS2 2
B3	DQSn DM	DDR_M_DM2 2

2,3 DDR_M_ODT0 — F9 ODT

VDD_DDR_1V8
A1 VDD
E9 VDD
H9 VDD
L1 VDD

A9 VDDQ
C1 VDDQ
C3 VDDQ
C7 VDDQ
C9 VDDQ   VDD_DDR_1V8

A3 VSS
E3 VSS
J1 VSS
K9 VSS

E1 VDDL

A7 VSSQ
B2 VSSQ
B8 VSSQ
D2 VSSQ
D8 VSSQ

E7 VSSDL
A2 NU/RDQSn
E2 VREF
L7 RFU

DDR_VREF

MT47H256M8

C24 0.1uF

C34 2700pF   C35 2700pF   C33 0.1uF   C23 0.1uF   C25 2.2uF   C32 10uF

VDD_DDR_1V8

2,3 DDR_M_MA[14..0]

DDR_M_MA0 ... DDR_M_MA14

2,3 DDR_M_BA[2..0]

DDR_M_BA0
DDR_M_BA1
DDR_M_BA2

U4

Pin	Signal
H8	A0
H3	A1
H7	A2
J2	A3
J8	A4
J3	A5
J7	A6
K2	A7
K8	A8
K3	A9
H2	A10
K7	A11
L2	A12
L8	A13
L3	A14
G2	BA0
G3	BA1
G1	BA2

Pin	Signal			
E8	CK		DDR_M_CKP	2,3
F8	CKn		DDR_M_CKN	2,3
G8	CKE		DDR_M_CKE0	2,3
F7	CSn		DDR_M_nCS0	2,3
G7	RASn		DDR_M_nRAS	2,3
F3	CASn		DDR_M_nCAS	2,3
	WEn		DDR_M_nWE	2,3

Pin	Signal	Net
C8	DQ0	DDR_M_DQ24
C2	DQ1	DDR_M_DQ25
D7	DQ2	DDR_M_DQ26
D3	DQ3	DDR_M_DQ27
D9	DQ4	DDR_M_DQ28
D5	DQ5	DDR_M_DQ29
B1	DQ6	DDR_M_DQ30
B9	DQ7	DDR_M_DQ31

DDR_M_DQ[31..0] 2,3

Pin	Signal	Net
B7	DQS	DDR_M_DQS3 2
B3	DQSn DM	DDR_M_DM3 2

2,3 DDR_M_ODT0 — F9 ODT

VDD_DDR_1V8
A1 VDD
E9 VDD
H9 VDD
L1 VDD

A9 VDDQ
C1 VDDQ
C3 VDDQ
C7 VDDQ
C9 VDDQ   VDD_DDR_1V8

A3 VSS
E3 VSS
J1 VSS
K9 VSS

E1 VDDL

A7 VSSQ
B2 VSSQ
B8 VSSQ
D2 VSSQ
D8 VSSQ

E7 VSSDL
A2 NU/RDQSn
E2 VREF
L7 RFU

DDR_VREF

MT47H256M8

C267 0.1uF

VDD_DDR_1V8

C266 2700pF   C268 2700pF   C173 0.1uF   C172 0.1uF   C171 2.2uF   C22 10uF

Make sure all ref caps, PLL's are
X5R's and X7R's not Y5V's

Test Points on all nets and
rails for ICT when possible

0V9_S

56.2	R22	DDR_M_BA0
56.2	R23	DDR_M_BA1
56.2	R39	DDR_M_BA2

DDR_M_BA[2..0] 2,3

56.2	R35	DDR_M_nRAS	2,3
56.2	R24	DDR_M_nCAS	2,3
56.2	R36	DDR_M_nWE	2,3

0V9_S

39.2	R20	DDR_M_nCS0	2,3
39.2	R37	DDR_M_nCS1	2
39.2	R38	DDR_M_ODT0	2,3
39.2	R55	DDR_M_ODT1	2

VDD_DDR_1V8

| 10K | R31 | 39.2 | R33 | DDR_M_CKE1 | 2 |
| 10K | R32 | 39.2 | R34 | DDR_M_CKE0 | 2,3 |

0V9_S

56.2	R8	DDR_M_MA0
56.2	R21	DDR_M_MA1
56.2	R18	DDR_M_MA2
56.2	R3	DDR_M_MA3
56.2	R16	DDR_M_MA4
56.2	R19	DDR_M_MA5
56.2	R17	DDR_M_MA6
56.2	R4	DDR_M_MA7
56.2	R1	DDR_M_MA8
56.2	R7	DDR_M_MA9
56.2	R9	DDR_M_MA10
56.2	R6	DDR_M_MA11
56.2	R2	DDR_M_MA12
56.2	R5	DDR_M_MA13
56.2	R15	DDR_M_MA14

DDR_M_MA[14..0] 2,3

INTEL MINNOW BOARD PRODUCTION

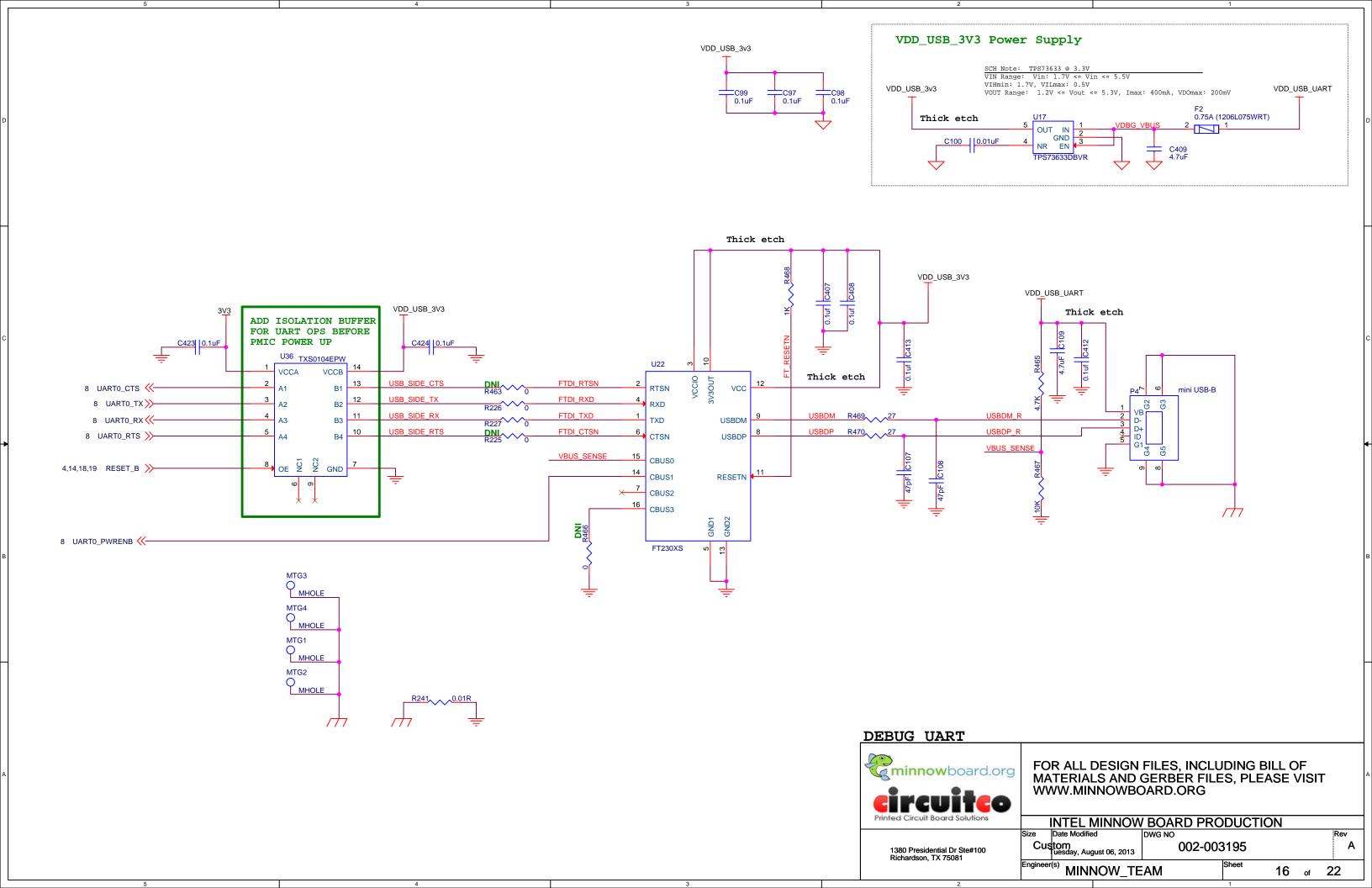| Size	Date Modified	DWG NO	Rev
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Engineer(s) MINNOW_TEAM

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ATOM JTAG & SPI BIOS I/O

U5D — INTEL_ATOM_Processor_E6XX — 4 OF 7

GPIO
- GPIO_SUS8 H1 11,19 E6XX_GPIO_SUS8
- GPIO_SUS7 J4 8,19 E6XX_GPIO_SUS7
- GPIO_SUS6 L2 19 E6XX_GPIO_SUS6
- GPIO_SUS5 M1 19 E6XX_GPIO_SUS5
- GPIO_SUS4 K11 20 E6XX_GPIO_SUS4
- GPIO_SUS3 M3 20 E6XX_GPIO_SUS3
- GPIO_SUS2 P1 20 E6XX_GPIO_SUS2
- GPIO_SUS1 N4 20 E6XX_GPIO_SUS1
- GPIO_SUS0 L10 19 E6XX_GPIO_SUS0
- GPIO4 B5 19,21 E6XX_GPIO_4
- GPIO3 D5 19 E6XX_GPIO_3
- GPIO2 A6 19 E6XX_GPIO_2
- GPIO1 C4 19 E6XX_GPIO_1
- GPIO0 E6 19 E6XX_GPIO_0

SPI
- SPI_SCK F5 18 E6XX_SPI_SCK
- SPI_MOSI F1 18 E6XX_SPI_MOSI
- SPI_MISO E2 18 E6XX_SPI_MISO
- SPI_CS_B H5 18 E6XX_SPI_CS_B

SMBUS
- SMB_CLK E4 R56 0 SMB_CLK_R 4,14,18,20
- SMB_DATA G14 R57 0 SMB_DATA_R 4,14,18,20
- SMB_ALERT_B F7 SMB_ALERT_B 4

POWER MANAGMENT
- PWROK Y1 J2 14,19,20 PWROK
- SUSCLK TP2 SUSCLK
- SLPRDY_B K1 14 SLPRDY_B
- SLPMODE M5 14 SLPMODE
- RESET_B K5 4,14,16,18,19 RESET_B
- RSTWARN L4 14 RSTWARN
- RSTRDY_B K7 14 RSTRDY_B
- RSMRST_B V1 14 RSMRST_B
- GPE_B N2 4,14 GPE_N
- WAKE_B H11 WAKE_N_BUF 11,14,18,20 R156 0 WAKE_N_PROC

RTC
- RTCRST_B AA2 RTCRST_N
- RTCX1 L8 4 RTCX1
- RTCX2 M7 4 RTCX2

UNUSED
- NC42 L36
- NC43 K37
- RCOMP H37 R141 249 RCOMP

CLOCKS
- PWRMODE2 AL24 R332 56.2 PWRMODE_R_2 14,18
- PWRMODE1 AN26 R333 56.2 PWRMODE_R_1 14,18
- PWRMODE0 AK23 R334 56.2 PWRMODE_R_0 14,18

CPU VOLTAGE
- VID6 AT31 14 VID_6
- VID5 AT33 14 VID_5
- VID4 AR34 14 VID_4
- VID3 AP29 14 VID_3
- VID2 AL28 14 VID_2
- VID1 AT29 14 VID_1
- VID0 AU32 14 VID_0
- VIDEN1 AL26 14 VID_EN1
- VIDEN0 AK27 14 VID_EN0

CPU JTAG
- TCK AN22 CPU_TCK 4,18
- TMS AL16 CPU_TMS 18
- TDI AN16 CPU_TDI 18
- TDO AN18 CPU_TDO 18
- TRST_B AL14 CPU_TRST_N 4,18

NC JTAG
- NCTCK AN28
- NCTMS AP27
- NCTDI AL22
- NCTDO AU30

OVLY JTAG
- IO_TCK T1 AB1 IO_TCK 4,18
- IO_TMS AC2 IO_TMS 4,18
- IO_TDI AD1 IO_TDI 4,18
- IO_TDO R2 IO_TDO 18
- IO_TRST IO_TRST_N 4,18

BPM
- BPM_B3 AN36 BPM_B3 18
- BPM_B2 AN34 BPM_B2 18
- BPM_B1 AP35 BPM_B1 18
- BPM_B0 AP33 BPM_B0 18
- PREQ_B AM37 PREQ_B 18
- PRDY_B AM33 PRDY_B 18
- NC38 E34
- GPIO_B AP19
- NC40 AK17
- NC41 AN30

- NC6 AP31
- NC1 AN24
- NC44 AL18
- NC57 AL20
- NC56 AK21

LEGACY
- TEST_B H3 TEST_N 4
- HIGHZ_B W2 HIGHZ_N 4
- NC3 G4 NCLK_TTL 18
- SMI_B H7 SMI_N 4
- SPKR G2 TP3
- CLK14 J8 REFCLK_14MHz 15

- BSEL2 AP25 BSEL2 4
- BSEL1 AP21 BSEL1 4
- BSEL0 AM31 BSEL0 4

- BCLKN AU26 BCLK_100MHz_N 15
- BCLKP AT25 R309 100 BCLK_100MHz_P 15
- NC2 R4
- HPLL_REFCLK W4 HPLL_REFCLK_100MHz_N 15
- HPLL_REFCLK_P V5 R283 100 HPLL_REFCLK_100MHz_P 15

THERMAL
- THERMTRIP_B AU28 THRMTRIP_B 14
- THRM_B G10 R338 22 PROCHOT_B 14,19
- PROCHOT_B AT27 PROCHOT_B_ATOM
- THRMDA P33 CPU_THRMDA R136 0
- THRMDC N34 CPU_THRMDC R139 0

U5B — INTEL_ATOM_Processor_E6XX — 2 OF 7

CDMI
- NC20 AE36, NC19 AE34, NC18 AC30, NC17 AD31, NC16 AF33, NC15 AF37, NC14 AF35, NC13 AG34
- NC28 AH33, NC27 AJ36, NC26 AJ34, NC25 AK35, NC24 AH31, NC23 AK33, NC22 AK31, NC21 AG30
- NC36 AD37, NC33 AD33, NC30 AC36, NC4 AB31
- NC35 AL36, NC32 AK37, NC31 AF31, NC5 AE30
- NC12 W34, NC11 W36, NC10 Y37, NC9 AA36, NC8 AA34, NC7
- NC37 W30, NC34 Y31, NC59 AA30, NC58 V35, NC29 V37

CDVO
- COMP01 AL34 R363 54.9 COMP01
- COMP00 AJ30 R362 27.4 COMP00
- COMP11 AB33 R361 35.7 COMP11
- COMP10 AB35 R360 18.2 COMP10
- IOCOMP11 R6 R275 35.7 IOCOMP11
- IOCOMP10 T5 R47 18.2 IOCOMP10

LVDS
- IOCOMP00 N30 R357 27.4 IOCOMP00
- IOCOMP01 L34 R356 54.9 IOCOMP01
- LVD_CLKP U36 LVDS_CLK_P 20
- LVD_CLKN T37 LVDS_CLK_N 20
- LVD_DATAP_3 T33 LVDS_DATA_P_3 20
- LVD_DATAN_3 R34 LVDS_DATA_N_3 20
- LVD_DATAP_2 P37 LVDS_DATA_P_2 20
- LVD_DATAN_2 R36 LVDS_DATA_N_2 20
- LVD_DATAP_1 U30 LVDS_DATA_P_1 20
- LVD_DATAN_1 V31 LVDS_DATA_N_1 20
- LVD_DATAP_0 V33 LVDS_DATA_P_0 20
- LVD_DATAN_0 U34 LVDS_DATA_N_0 20
- LVD_IBG R30 R359 2.43K LVD_IBG
- LVD_VREFH M37 R138 0 LVD_VREFH
- LVD_VREFL N36 R137 0 LVD_VREFL

U28 — LM95245CIMM
- VDD 1, D+ 2, D- 3, SMB_DAT 7, SMB_CLK 8, OS_A0 6, T_CRIT 4, GND 5
- THRMDA, THRMDC
- SMB_DAT 4,14,18,20 R103 0 U29_DAT
- SMB_CLK 4,14,18,20 R102 0 U29_CLK
- R104 0 OS_A0
- R105 0 THRMT_N 4   DNI
- THRM_N 4

Crystal
- THT XTAL Y5 32.768KHz, CITIZEN XTAL_CFS-145 CFS308-32.768KDZF-UB
- SMT XTAL DNI Y6 32.768KHz, CITIZEN 2-SMD CM21232768DZFT
- C156 12pF, C157 12pF
- 4 RTCX1, 4 RTCX2
- R27 10M
- CRYSTAL SPECS
- FREQUENCY - 32.768KHz
- TOLERANCE - 20PPM

- 3V3 R272 1K TEST_N 4 R273 0 DNI
- 1V05_S R45 1K HIGHZ_N 4 R44 1K DNI
- R90 1K, R71 1K, R107 1K BSEL2 4, BSEL1 4, BSEL0 4
- R280 10K THRM_N 4
- R281 10K R58 0 SMI_N_EG20T 11
- 4 SMI_N R282 0 DNI SMB_ALERT_B 4

INTEL MINNOW BOARD PRODUCTION

1380 Presidential Dr Ste#100
Richardson, TX 75081

Size: Custom
Date Modified: Tuesday, August 06, 2013
DWG NO: 002-003195
Rev: A
Engineer(s): MINNOW_TEAM

INTEL_ATOM_Processor_E6XX

U5C

PCIe*

NOT USED PCIE3_RX BUS ON MINNOW

NOT USED PCIE3 TX BUS ON MINNOW

Pin	Signal
D33	PCIE_PERP3
C34	PCIE_PERN3
A32	PCIE_PERP2
B33	PCIE_PERN2
E30	PCIE_PERP1
D29	PCIE_PERN1
A30	PCIE_PERP0
B31	PCIE_PERN0
B25	PCIE_ICOMPO
B23	PCIE_ICOMPI
A24	PCIE_RCOMPO
A22	NC47
D21	NC46
E22	PCIE_RBIAS

PCIE_R_IO_COMP — R74 49.9

R304 750 PCIE_RBIAS

Pin	Signal
H31	PCIE_PETP3
G32	PCIE_PETN3
D31	PCIE_PETP2
E32	PCIE_PETN2
E28	PCIE_PETP1
D27	PCIE_PETN1
D25	PCIE_PETP0
E26	PCIE_PETN0
B27	PCIE_CLKINP
A26	PCIE_CLKINN
E24	NC51
D23	NC50
B29	NC49
A28	NC48

20 PCIe2_RX_P   C44 0.1uf   PCIe2_RX_P_C
20 PCIe2_RX_N   C45 0.1uf   PCIe2_RX_N_C
20 PCIe1_RX_P   C285 0.1uf   PCIe1_RX_P_C
20 PCIe1_RX_N   C286 0.1uf   PCIe1_RX_N_C
9 PCIe0_RX_P
9 PCIe0_RX_N

PCIe2_TX_P_C C52 0.1uf   PCIe2_TX_P 20
PCIe2_TX_N_C C53 0.1uf   PCIe2_TX_N 20
PCIe1_TX_P_C C55 0.1uf   PCIe1_TX_P 20
PCIe1_TX_N_C C54 0.1uf   PCIe1_TX_N 20
PCIe0_TX_P_C C235 0.1uf   PCIe0_TX_P 9
PCIe0_TX_N_C C236 0.1uf   PCIe0_TX_N 9

E6XX_PCIe_CLK_P 15
R331 100
E6XX_PCIe_CLK_N 15

SDVO

Pin	Signal
B15	SDVO_TVCLKINP
A14	SDVO_TVCLKINN
B21	SDVO_INTP
A20	SDVO_INTN
E20	SDVO_STALLP
D19	SDVO_STALLN
E14	SDVO_CTRLCLK
B7	SDVO_CTRLDATA
D15	NC53
E16	NC52
B9	NC55
A8	NC54

DNI R65 0 SDVO_TVCLKINP
DNI R64 0 SDVO_TVCLKINN
SDVO_INT+ SDVO_INTP
SDVO_INT- SDVO_INTN
DNI R306 0 SDVO_STALLP
DNI R305 0 SDVO_STALLN
SDVO_CTRLCLK
SDVO_CTRLDATA

3V3_S
DNI R278 10K   DNI R279 10K

Pin	Signal
B17	SDVO_REDP
A16	SDVO_REDN
A18	SDVO_GREENP
B19	SDVO_GREENN
E18	SDVO_BLUEP
D17	SDVO_BLUEN
B13	SDVO_CLKP
A12	SDVO_CLKN
B11	SDVO_REFCLKP
A10	SDVO_REFCLKN

SDVO_RED+   C31 0.1uf   SDVO_RED+_C
SDVO_RED-   C36 0.1uf   SDVO_RED-_C
SDVO_GREEN+   C37 0.1uf   SDVO_GREEN+_C
SDVO_GREEN-   C38 0.1uf   SDVO_GREEN-_C
SDVO_BLUE+   C189 0.1uf   SDVO_BLUE+_C
SDVO_BLUE-   C188 0.1uf   SDVO_BLUE-_C
SDVO_CLK+   C30 0.1uf   SDVO_CLK+_C
SDVO_CLK-   C29 0.1uf   SDVO_CLK-_C

R288 100 SDVO_REFCLK_96MHz_P 15
SDVO_REFCLK_96MHz_N 15

LPC / High Definition Audio

Pin	Signal
D11	LPC_FRAME_B
G12	LPC_AD3
G8	LPC_AD2
D3	LPC_AD1
D13	LPC_AD0
E8	LPC_SERIRQ
D7	LPC_CLKRUN_B
E10	LPC_CLKOUT2
D9	LPC_CLKOUT1
E12	LPC_CLKOUT0

Pin	Signal
E36	HDA_CLK
P31	HDA_RST_B
F35	HDA_SYNC
G36	HDA_SDI1
N32	HDA_SDI0
J36	HDA_SDO
F37	HDA_DOCKEN_B
D35	HDA_DOCKRST_B

HDA_CLK_R R142 33 HDA_CLK 17,20
HDA_RST_N_R R358 33 HDA_RST_N 17,20
HDA_SYNC_R R355 33 HDA_SYNC 17,20
HDA_SDI1 20
HDA_SDI0 17
HDA_SDO_R R140 33 HDA_SDO 17,20

LPC_SERIRQ
LPC_CLKRUN_N

3 OF 7

5V Protection

30OHM_4A_MLB_0805
MLB_201209-0030P-N1
DNI L1
DC_IN_5V
DNI F1
32V_2A_LITTELFUS 0467002_NR_2A_LF
DNI D1 SCS0520P SCHOTTKY_SECOS
0.1uF DNI C3
RT1 PTC,0ZCE0010FF2G

DVI_TX2-   1   4   L5   DVI_TX2-_sec
DVI_TX2+   2   3   DVI_TX2+_sec
R255 2.2K   R254 2.2K
90 ohm_130mA_PANASONIC EXC24CG900U

DVI_TX1-   1   4   L4   DVI_TX1-_sec
DVI_TX1+   2   3   DVI_TX1+_sec
90 ohm_130mA_PANASONIC EXC24CG900U

DVI_HTPLG R256 10K
D6 MMSZ5226B-7-F
R12 51K
DNI C9 0.1uf

DVI_TX0-   1   4   L3   DVI_TX0-_sec
DVI_TX0+   2   3   DVI_TX0+_sec
90 ohm_130mA_PANASONIC EXC24CG900U

DVI_TXC+   2   3   DVI_CLK+_sec
DVI_TXC-   1   4   L2   DVI_CLK-_sec
EXC24CG900U
90 ohm_130mA_PANASONIC

FOR ESD AND CONDUCTED IMMUNITY

J1 HDMIConnA
NOVA CAP 1808

Pin	Signal
3	DAT2-
1	DAT2+
2	DAT2_S
15	SCL
16	SDA
6	DAT1-
4	DAT1+
5	DAT1_S
18	+5V
17	DDC/CEC GND
19	HPLG
9	DAT0-
7	DAT0+
8	DAT0_S
11	CLK_S
10	CLK+
12	CLK-
13	CEC
14	NC

MTG1 MTG2 MTG3 MTG4
SMTG3
DVI_DDC_SCL
DVI_DDC_SDA
DC_IN_5V_DVI

DNI C4 8200pF 1000V
DNI C5 150pF 1000V

Avoid placing GND Copper or traces adjacent to TMDS Trace

Route traces with 100 Ohm Differential Impedance

Put these 4 resistors and 4 capacitors as close as possible to the TMDS output pins of the Sil1362

R253 300 DVI_TX2R   C130 0.1uf   DVI_TX2-
DVI_TX2+
DVI_TX1+
R252 300 DVI_TX1R   C129 0.1uf   DVI_TX1-
DVI_TX0+
R251 300 DVI_TX0R   C128 0.1uf   DVI_TX0-
DVI_TXC+
R250 300 DVI_TXCR   C127 0.1uf   DVI_TXC-

SDVO_INT+   C40 0.1uf   SDVO_INT+_C
SDVO_INT-   C39 0.1uf   SDVO_INT-_C
DNI R265 49.9   DNI R264 49.9

U2 SII1362

Pin	Signal
23	TX2+
22	TX2-
20	TX1+
19	TX1-
17	TX0+
16	TX0-
14	TXC+
13	TXC-
25	EXT_SWING
32	SDI+
33	SDI-
37	SDR+
38	SDR-
40	SDG+
41	SDG-
43	SDB+
44	SDB-
46	SDC+
47	SDC-
35	EXT_RES
2	RESET#
3	SDSCL
4/5	SDSDA
6	A1
9	SDADDC
8	SCLDDC
30	TEST
29	HTPLG
10	VCC1
28	VCC2
34	VCC3
31	GND1
7	GND2
1	OVCC
15	AVCC1
21	AVCC2
18	AGND1
24	AGND2
11	PVCC1
12	AGND3
26	PVCC2
27	PGND2
36	SVCC1
42	SVCC2
39	GND3
45	GND4
48	SPVCC
3	SPGND

DVI_HTPLG
SDVO_RED+_C 37 / SDVO_RED-_C 38
SDVO_GREEN+_C 40 / SDVO_GREEN-_C 41
SDVO_BLUE+_C 43 / SDVO_BLUE-_C 44
SDVO_CLK+_C 46 / SDVO_CLK-_C 47
DVI_EXT_RES R271 1K
R260 10K
SII1362_RESET_B
SDVO_CTRLCLK
SDVO_CTRLDATA
SII1362_ADDR
DVI_DDC_SDA
DVI_DDC_SCL

VDD_3V3 VCC_1V8
DNI R261 1K
R262 1K
C147 0.1uf

3V3_S
1K R267
R54 3.16K   C28 0.1uf
SDVO_CTRLCLK_PU R268 5.6K SDVO_CTRLCLK
3V3_S
1K R270
SDVO_CTRLDATA_PU R269 5.6K SDVO_CTRLDATA
R53 3.16K   C27 0.1uf

VCC_1V8   VDD_1V8   VDD_3V3   VDD_PVCC2

L8 FERRITE, MMZ1608R301A   VDD_AVCC   C20 4.7uF
L7 FERRITE, MMZ1608R301A   C17 1uF
L6 FERRITE, MMZ1608R301A   VDD_OVCC   C10 4.7uF
VDD_SVCC
L11 FERRITE, MMZ1608R301A   VDD_PVCC1   C160 4.7uF
L9 FERRITE, MMZ1608R301A   C26 4.7uF
L18 FERRITE, MMZ1608R301A   VDD_SPVCC
VDD_AVCC   C125 1uF
L10 FERRITE, MMZ1608R301A
R263 300   C163 1uF
VDD_OVCC

VCC_1V8
C151 100pF   C155 0.01uf   C154 0.1uf   C144 0.01uf   C146 0.1uf   C152 0.01uf   C153 0.1uf
C145 0.1uf

VDD_AVCC VDD_PVCC1
C148 100pF   C149 0.01uf   C150 0.1uf
VDD_PVCC2
C124 0.1uf   C126 0.1uf
C131 0.1uf   C132 0.01uf

VDD_SVCC
C165 100pF   C166 0.01uf   C167 0.1uf
VDD_SPVCC
C161 100pF   C162 0.01uf   C164 0.1uf

ATOM SDVO AND DVI I/O

INTEL MINNOW BOARD PRODUCTION

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INTEL_ATOM_Processor_E6XX

U5E

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14

VNN1 VNN2 VNN3 VNN4 VNN5 VNN6 VNN7 VNN8 VNN9 VNN10 VNN11 VNN12 VNN13 VNN14

All SMT Electrolytic has double footprint for THT

All SMT Electrolytic has double footprint for THT

NC39
VCCPQ
VCCF
VCCA1 VCCA2 VCCA3
VCCP1 VCCP2 VCCP3 VCCP4 VCCP5 VCCP6 VCCP7 VCCP8
VCCPA1 VCCPA2
VCCPDDR1 VCCPDDR2 VCCPDDR3 VCCPDDR4 VCCPDDR5
VCCQ1 VCCQ2 VCCQ3
LVD_VBG
VMM
GTLREF
DLIOGTLREF
IOGTLREF
IO_RX_GVREF

VCCD180
VCCA180
VCC180_1 ... VCC180_17
VCC180SR
VCCDSUS
VCCD1 VCCD2 VCCD3 VCCD4 VCCD5 VCCD6 VCCD7
VCCD_DPL
VCCA_PEG1 VCCA_PEG2 VCCA_PEG3 VCCA_PEG4 VCCA_PEG5 VCCA_PEG6 VCCA_PEG7
VCCQHPLL
VCCFHV
VCCP33_1 VCCP33_2 VCCP33_3
VCCP33SUS
VCCPSUS
VCC33RTC
VCCRTCEXT
VCCSFRDPLL
VCCSFR_EXP
VCCSFRHPLL
CMREF
DLIOCMREF
IOCMREF
IO_RX_CVREF
GTLPREF
GTLVREF

5 OF 7

DNI R405 0
DNI R153 0

Thick etch

U29 TPS22922
A1 VOUT1 VIN1 A2
B1 VOUT2 VIN2 B2
C1 GND ON C2

CTRL_V1P8_S 14

Thick etch

Shielded Ferrite X5R,X7R,NPO caps TANT bulk

FB1 BEAD
FB10 BEAD
FB8 BEAD
FB9 BEAD

1V8_S
1V8
1V05
1V05_S
3V3_S
3V3
3V3_RTC

ATOM CPU POWER I

INTEL_ATOM_Processor_E6XX

U5G

INTEL_ATOM_Processor_E6XX

U5F

6 OF 7

7 OF 7

SENSE PINS

VCC_S — R308 100
13 VCC_SENSE
13 VCC_VSS_SENSE
R307 100

Run as differential pair

VNN_S — R72 100
12 VNN_SENSE
12 VNN_VSS_SENSE
R73 0

Run as differential pair

Connect VNN_VSS_SENSE to GND close to E6XX

VCCSENSE
VCC_VSSSENSE
VNNSENSE

VCCDSENSE
VCCD_VSSSENSE

VCCD_SENSE 13
VCCD_VSS_SENSE

1V05_S
R401 100
R400 100

Run as differential pair

ATOM CPU POWER II

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INTEL MINNOW BOARD PRODUCTION

1380 Presidential Dr Ste#100
Richardson, TX 75081

Size	Date Modified	DWG NO	Rev
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EMI Place holders

SENDING OUT USB4
to EXPANSION HEADER

FOR ESD AND
CONDUCTED
IMMUNITY

FOR ESD AND
CONDUCTED
IMMUNITY

PULLUP LOW-ACTIVE
CURRENT MONITOR
USB PORTS (0,1,4)

DISABLE UNUSED
USB PORTS (2,3,5)

POPULATE IF YOU WANT
TO DISABLE USB PORTS
(0,1,4) UPON POWER UP

NOVA CAP 1808

USB HOST & Client and UART

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SDIO, SATA, CAN, I2C

FOR ESD AND
CONDUCTED
IMMUNITY

FOR ESD AND
CONDUCTED
IMMUNITY

UPDATED
SATA
CONNECTOR
SYMBOL

RIGHT ANGLE
SATA CONNECTOR

X7R caps

Only if this is an eSATA port; Otherwise, GND pins
8 and 0 to GND.

U6C   PCH EG20T

NOVA CAP 1808

NOVA CAP 1808

ALL SMT ELECTROLYTIC HAS THT DOUBLE FOOTPRINT

ALL SMT ELECTROLYTIC HAS THT DOUBLE FOOTPRINT

1V2
3V3
2V5_A
1V2_A

Thick etch
1V2_AVD
FB3
BEAD
C346 47uF

U6F   PCH EG20T

3V3_AVD
FB4
BEAD
C345 47uF
Thick etch

3V3

1V2_S

FB1
BEAD
C175 47uF
ALL SMT ELECTROLYTIC HAS THT DOUBLE FOOTPRINT

Thick etch
1V2_S_VDNS

U6G   PCH EG20T

3V3_S

Thick etch

3V3_S_VDP
FB2
BEAD
C174 47uF ALL SMT ELECTROLYTIC HAS THT DOUBLE FOOTPRINT

U6D   PCH EG20T

1V2_A
3V3_A

U6E   PCH EG20T

EG20T POWER

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1380 Presidential Dr Ste#100
Richardson, TX 75081

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INTEL MINNOW BOARD PRODUCTION

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For EMI place holder

U6A   PCH EG20T

15 SYSCLK_25MHz   AB9   sys_25mhz_i

20,21 GPIO0   AB20   gpio0
20,21 GPIO1   AB19   gpio1
20,21 GPIO2   AB18   gpio2
20,21 GPIO3   AA18   gpio3
20,21 GPIO4   Y18   gpio4
20,21 GPIO5   AB17   gpio5
20,21 GPIO6   AA17   gpio6
20,21 GPIO7   Y17   gpio7
21 GPIO8   A9   gpio8
21 GPIO9   B9   gpio9
21 GPIO10   A8   gpio10
20 GPIO11   B8   gpio11

14 IO_PWROK   Y20   pwrgd
14 IO_SLP_PLB_B   AA22   slp_plb_n
14 IO_SLP_PLC_B   W20   slp_plc_n
                    Y21

11,14 IO_RST_PLA_B   AA21   rst_pla_n
14 IO_RST_PLB_B   AB21   rst_plb_n
14 IO_RST_PLC_B   AB22   rst_plc_n
4 SMI_N_EG20T   AA9   smi_n
                    AA8   TEST1H
R325 0   TEST2H   AA9
R326 0

11 WAKE_OUT_N   Y19   wake_out_n

gmii_col   Y10   GMII_COL
gmii_crs   AA10   GMII_CRS
gmii_mdc   W10   GMII_MDC   R330 22   GMII_MDC_R
gmii_mdio   V10   GMII_MDIO
gmii_phyint   AB10   GMII_PHYINT
gmii_rxclk   AB16   GMII_RXCLK_R
gmii_rxd0   AA16   GMII_RXD0_R
gmii_rxd1   Y16   GMII_RXD1_R
gmii_rxd2   W16   GMII_RXD2_R
gmii_rxd3   AB15   GMII_RXD3_R
gmii_rxd4   AA15   GMII_RXD4
gmii_rxd5   Y15   GMII_RXD5
gmii_rxd6   Y16   GMII_RXD6
gmii_rxd7   Y14   GMII_RXD7
gmii_rxdv   AB14   GMII_RXDV_R
gmii_rxer   AA14   GMII_RXER
gmii_rxer   AA13   GMII_TXCLKI
gmii_txclki   AB13   GMII_TXCLK   R352 22   GMII_TXCLK_R
gmii_txclko   Y13   GMII_TXD0   R353 22   GMII_TXD0_R
gmii_txd0   W13   GMII_TXD1   R354 22   GMII_TXD1_R
gmii_txd1   AB12   GMII_TXD2   R351 22   GMII_TXD2_R
gmii_txd2   AA12   GMII_TXD3   R346 22   GMII_TXD3_R
gmii_txd3   Y12
gmii_txd4   W12
gmii_txd5   Y11
gmii_txd6   W11   GMII_TXEN   R329 22   GMII_TXEN_R
gmii_txd7   AB11
gmii_txen   AA11
gmii_txer

THT XTAL
Y3
ECS-250-20-46X-TR HC-46X

SMT XTAL
Y4
ECS-250-20-30-TR ECX-53

CRYSTAL SPECS
FREQUENCY - 25.0MHz
TOLERANCE - 30PPM

DNI R440 0   PHY_CLK_25M
DNI R441 0   PHY_PPS

R435 2.37K   ETH_RBIAS

10K R422

GMII_PHYINT

ETH_INT

DNI 10K R328   R91 0

3V3_RTC   NPO caps

10K R417

10K R324 GMII_COL
10K R327 GMII_CRS
10K R350 GMII_RXD4
10K R387 GMII_RXD5
10K R345 GMII_RXD6
10K R349 GMII_RXD7
10K R348 GMII_RXER
10K R347 GMII_TXCLKI
10K R108 GPIO11

ETH_WOL_INT

U9   AR8031_AL1A

GMII_TXD0_R 36 TXD0
GMII_TXD1_R 37 TXD1
GMII_TXD2_R 38 TXD2
GMII_TXD3_R 39 TXD3

GMII_RXD0_R R189 22 GMII_RXD0 31 RXD0
GMII_RXD1_R R190 22 GMII_RXD1 30 RXD1
GMII_RXD2_R R91 22 GMII_RXD2 28 RXD2
GMII_RXD3_R R92 22 GMII_RXD3 27 RXD3

GMII_TXEN_R 34 TX_EN
GMII_RXDV_R R180 22 GMII_RXDV 32 RX_DV
GMII_RXCLK_R R179 22 GMII_RXCLK 33 RX_CLK
GMII_TXCLK_R 35 GTX_CLK

25 CLK_25M
22 PPS
2 RST
6 XTLO
7 XTLI
9 RBIAS
5 INT
40 WOL_INT

11 TRXP0   ETH_DP0
12 TRXN0   ETH_DN0
14 TRXP1   ETH_DP1
15 TRXN1   ETH_DN1
17 TRXP2   ETH_DP2
18 TRXN2   ETH_DN2
20 TRXP3   ETH_DP3
21 TRXN3   ETH_DN3

46 SIP
45 SIN
43 SOP
42 SON
41 SD
1 MDC   GMII_MDC_R
48 MDIO   GMII_MDIO
23 LED_ACT   LED_ACT_B
24 LED_LINK1000   LED_1000_B
26 LED_LINK10_100   LED_10_100

49 EP

ETH_RESETn

x5r and x7r. NO Y5V   THICK ETCH

FB13 BEAD   VDD_3V3

C365 10uF   C366 0.1uF
C351 1uF   C368 0.1uF   R434 0
C370 1uF   C364 0.1uF

C57 0.1uF   C369 0.1uF   C371 0.1uF   C367 0.1uF
C58 1uF, TANTALUM
C59 0.1uF   C347 10uF   C60 0.1uF

Bcase TANT placeholder

L21 4.7uH
FB12 BEAD
DNI FB5 BEAD   VDD_3V3

ETH_AVDDL ETH_DVDDL ETH_LX ETH_AVDD_3V3 VDD_3V3
ETH_AVDD_3V3 ETH_DVDDH ETH_VDDIO ETH_DVDDL
ETH_DVDDH ETH_VDDIO

J12   RJ-45 Gigabit

DB0- 10
DB0+ 9
DB1- 8
DB1+ 7
DB2- 6
DB2+ 5
DB3- 4
DB3+ 3

VDD_3V3

U18 74LVC1G08DBVR
LED_1000 1
LED_ACT_B 2   5
                4 ELL R238 220 LED_LEFT

U19 74LVC1G08DBVR
LED_100_10 1
LED_ACT_B 2   5
                4 ELR R237 220 LED_RIGHT

C415 0.1uF C414 0.1uF C411 0.1uF C410 0.1uF

U15 SN74LVC1G14DBVR
LED_1000_B 2   4 LED_1000

U16 SN74LVC1G14DBVR
LED_10_100 2   4 LED_100_10

DNI C110 8200pF 1000V

FOR ESD AND CONDUCTED IMMUNITY
DOUBLE VIA
NOVA CAP 1808

VDD_3V3 10K R224
10K R430 GMII_RXD0
10K R431 GMII_RXD1
DNI 10K R223 LED_ACT_B
10K R416 GMII_RXDV
10K R432 GMII_RXD2
10K R415 GMII_RXCLK
10K R433 GMII_RXD3
DNI 10K R456 LED_1000_B
VDD_3V3 10K R457

AR8031 ETHERNET PHY STRAPPINGS
RXD0 - PHYADDRESS0
RXD1 - PHYADDRESS1
LED_ACT - PHYADDRESS2 (PHYADDRESS4/3=00)
RX_DV - MODE[0]
RXD2 - MODE[1]
RX_CLK - MODE[2]
RXD3 - MODE[3]
LED_1000 - External Interrupt Select
          1 = INT RGMII IBM,
          0 = EXT Interrupt
NOTE : PHY ADDRESS = 00001
(since I need LED_ACT TO BE LOW ACTIVE)

LED OPERATION
10MBIT - NO LEDS
100MBIT - D3 RIGHT LED - GREEN
1GBIT - D1 LEFT LED - GREEN
ACTIVITY WILL MAKE LED FLASH ON/OFF

2V5_A   R426 10K   R421 1.5K

C62 0.1uF
U30 74LVC1G08DBVR
4,19 E6XX_GPIO_SUS8
11,14 IO_RST_PLA_B   E6XX_GPIO_SUS8
ETH_RESETn
2V5_A VDD_3V3
DNI R419 0   R418 0
C63 100pF C61 100pF C64 100pF

3V3_S   R395 1K
3V3_S   C340 0.1uF
U7 74LVC1G07DCK
11 WAKE_OUT_N   WAKE_N_BUF 4,14,18,20

GIGABIT ETHERNET - EG20T HUB/AR8031 PHY

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1380 Presidential Dr Ste#100
Richardson, TX 75081

INTEL MINNOW BOARD PRODUCTION

Size: Custom
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BUCKS WITH INTERNAL FETs   U13G DA6011

VDD_5V

THICK ETCH   H1   VSUP_G

BUCK_GRAPHIC
0.3V-1.2V/1600mA

VLX_VMIN

C81
10uF

K1   VSS_G

VNN_SENSE   G4

VNN_VSS_SENSE   G3

VDD_5V

THICK ETCH   E13   VSUP_3P3

BUCK_V3P3
3.3V/1000mA

VLX_3P3

C391
10uF

G13   VSS_3P3

V3P3   F10

PD_V3P3_S
3.3V/250mA

V3P3_IN   C13

V3P3_S   B13

VDD_5V

THICK ETCH   H13   VSUP_1P2

BUCK_V1P2_A
1.2V/1400mA

VLX_1P2

C349
10uF

K13   VSS_1P2

V1P2_A   H12

PD_V1P2
1.2V/150mA

V1P2_IN   G12

V1P2   G11

C348
10uF

L16
VNN_S_VLX_VMIN   J1
THICK ETCH
1.5uH
THICK ETCH

VNN_S

+ C384
220uF

VNN_SENSE_PMIC 374   R443   VNN_SENSE_R
10R   R442

VNN_SENSE   7

VNN_VSS_SENSE   7

Route these 2 signals differential

C388
1000pF

L12
3V3_VLX_3P3   F13
THICK ETCH
4.7uH
THICK ETCH

3V3

+ C350
220uF

3V3_S

C79
10uF

L15
1V2_A_VLX_1P2   J13
THICK ETCH
1.5uH
THICK ETCH

1V2_A

+ C372
220uF

1V2

DC_IN_5V

J15   RAPC712

3   2   1

D7
SMCJ5.0CA

DNI
D8   MBRS410LT3G

VDD_5V

R184   470   5V_LED_ON

+ C418
220uF

D13
LTST-S270GKT
GRN

3V3   VDD_3V3

DNI
R464   0

DC_IN_5V   3V3   U34

C422
2.2uF

2   IN   OUT   3
1   EN   ADJ   4
5   GND1   GND3   6
7   GND2   GND4   8
TL5209   500mA

VDD_3V3

470K   R471   280K   R472

VDD_3V3_FB

C419
470pF

C420
0.1uf

C421
2.2uF

VDD_5V

J4
1
2   1
3   2
4   3
    4
HEADER_4

DC_IN_5V   VDD_3V3   U35

C106
2.2uF

1   IN   OUT   5
3   EN
4   NR   GND   2
TPS79318   200mA

DNI
C103
0.1uf

VDD_1V8

C105   C104
0.1uf   2.2uF

TP20

DC_IN_5V

J13
JUMPER
1
2

DIALOG DA6011 PMIC PART I
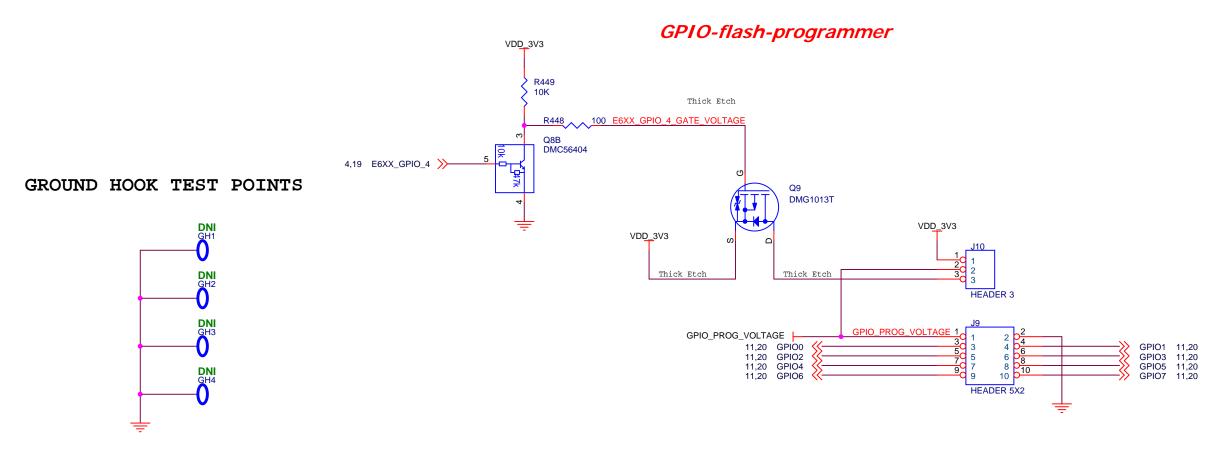
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VDD_5V

NOTE: The FOLLOWING IS CRUCIAL TO PMIC OPERATION. RESISTORS

R196, R186, R212, R197, R185, R175 are 0.56 OHMS for the EXTERNAL FETS and need to be verified if the Power supply has any Stability issues.

R187, R211, R176 are 0.01 OHM Current SENSE Resistors. Again They need to be checked if PS VOLTAGES ARE NOT CORRECT

VDD_5V
Thick Etch A8
VSUP_C

BUCKS WITH EXTERNAL FETS U13C

C361 10uF

BUCK_CORE 0.3V-1.2V/3500mA

A5 VSS_C

C390 10uF

VCC_S

A6 VHS_VCC   VHS_VCC   R196   0R56   VHS_VCC_G   4   G2   U32   S2 3
A7 VLS_VCC   VLS_VCC   R186   0R56   VLS_VCC_G   2   G1
SI7540DP
D22 6
D21 5
D12 7
D11 8
U6_D   L14 1.5uH   R187   0.01R
S1 1

C417 220uF

B5 CS_VCC   CS_VCC
B4 VCC_S   VCC_S
B6 VCC_SENSE   VCC_SENSE_R   R407   10R   VCC_SENSE 7
B7 VCC_VSS_SENSE   VCC_VSS_SENSE_R   R406   10R   VCC_VSS_SENSE 7

Route these 2 signals differential

VDD_5V

VDD_5V
Thick Etch A4
VSUP_1P8

BUCK_V1P8 1.8V/3500mA

C380 10uF

A1 VSS_1P8

C406 22uF

1V8   VDD_DDR_1V8

A2 VHS_1P8   VHS_1V8   R212   0R56   VHS_1V8_G   4   G2   U33   S2 3
A3 VLS_1P8   VLS_1V8   R197   0R56   VLS_1V8_G   2   G1
SI7540DP
D22 6
D21 5
D12 7
D11 8
U7_D   L17 1.5uH   R211   0.01R
S1 1

R462   0

C405 22uF   C91 22uF   C92 22uF   C87 22uF

SMT THT Double Footprint

B3 CS_1P8   CS_1V8
B2 V1P8   1V8

C1 V1P8_IN   PD_V1P8_S 1.8V/250mA   1V8_S
B1 V1P8_S

C90 10uF

BUCK_V1P05_S 1.05V/3500mA

VDD_5V
Thick Etch A12
VSUP_1P05

C82 10uF

A9 VSS_1P05

VDD_5V

C362 22uF

1V05_S

A10 VHS_1P05   VHS_1V05   R185   0R56   VHS_1V05_G   4   G2   U31   S2 3
A11 VLS_1P05   VLS_1V05   R175   0R56   VLS_1V05_G   2   G1
SI7540DP
D22 6
D21 5
D12 7
D11 8
U12_D   L13 1.5uH   R176   0.01R
S1

SMT THT Double Footprint

C360 22uF   C71 22uF

B8 CS_1P05   CS_1V05
B9 V1P05_S   VCCD_SENSE 7

DA6011

DIALOG DA6011 PMIC PART II

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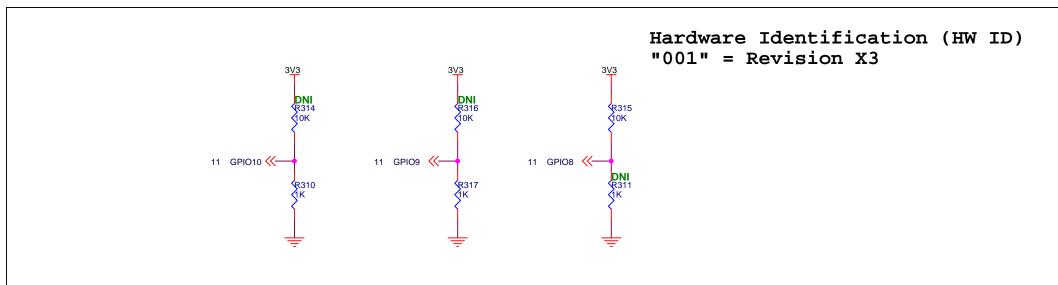
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1380 Presidential Dr Ste#100
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DNI
BT1

COIN BATTERY, BR-1225
PANASONIC

3V3_S

LDO   U13A

VDD_5V
Thick Etch   E12   VSUP1   LDO_VINT 2.65V/100mA   VINT   D13   Thick Etch   VINT
C379 4.7uF   C355 0.1uF

VDD_5V
Thick Etch   D12   VSUP2   LDO_VLP 2.5V/5mA   VLP   D11   Thick Etch   VLP
C377 4.7uF   C358 0.1uF   C357 1uF

VDD_5V
Thick Etch   F12   VSUP3   LDO_RTC_3P3 3.3V/5mA   V3P3_RTC   E10   3V3_RTC_D
C389 4.7uF   C354 0.1uF   C378 0.22uF

R236 1K VBAT_R   VBAT   D9 BAT54C, SOT23
BH1   BATT HOLDER, BS-1225-PC

3V3_A
C80 1uF   3V3_A

3V3_RTC
3V3_RTC   2
1   3V3_RTC   1

3V3_A
Thick Etch   E11   V3P3_A   LDO_V3P3A 3.3V/100mA   V3P3_A   3V3_A
C356 1uF

2V5_A
Thick Etch   F11   V2P5_A   LDO_V2P5A 2.5V/50mA   V2P5_A   2V5_A
C56 1uF

1V2_A
DNI R460   0   1V2_A_1V8_V0P9
1V8   R461   0   E1   VDD_V0P9   LDO_V0P9S 0.9V/+/-200mA   V0P9_S   D1   0V9_S
C404 0.1uF   C6 1uF   C88 10uF

0V9_R
E2   V0P9R   LDO_V0P9R 0.9V/25mA   V0P9_R   C402 1uF

1V2_S
1V8   G1   VDD_VUNI   LDO_VUNI V3P3S: 2.5V/250mA V1P8_S:1.2V/290mA   VUNI   G2   Thick Etch
F4   VDDC_VUNI   C399 0.1uF   C398 4.7uF

1V5_S
F1   VDD_V1P8   LDO_V1P5_S 1.5V/150mA   V1P5_S   F3   C400 1uF
E4   VDDC_V1P8   C83 0.1uF

1V25_S
LDO_V1P25_S 1.25V/5mA   V1P25_S   E3   C403 0.22uF

1V05
LDO_V1P05 1.05V/100mA   V1P05   V1P05   F2   C401 1uF

DA6011

DIGITAL INTERFACE   U13F

3V3_RTC   DNI R166   0
3V3_A   DNI R424   0
R423   0   3V3_A_RTC_S_VDDIO   N13   VDDIO
R164 10K   R165 10K   R178 10K (DNI)   C352 1uF

4   GPE_N   R177   0   GPE_N_R   D3   IRQ_B
4,18,20   SMB_DAT   R163   0   U5_DAT   G10   SMBDAT
4,18,20   SMB_CLK   R162   0   U5_CLK   D8   SMBCLK

4   VID_6   R124   0   VID_6_R   D10   VID[6]
4   VID_5   R150   0   VID_5_R   C12   VID[5]
4   VID_4   R151   0   VID_4_R   D9   VID[4]
4   VID_3   R147   0   VID_3_R   C10   VID[3]
4   VID_2   R123   0   VID_2_R   C11   VID[2]
4   VID_1   R148   0   VID_1_R   B11   VID[1]
4   VID_0   R149   0   VID_0_R   B10   VID[0]

4   VID_EN1   R120   0   VID_EN1_R   C3   VIDEN[1]
4   VID_EN0   R125   0   VID_EN0_R   C2   VIDEN[0]

1mm hole 2mm space with etch between holes top side

R231 10K

4,11,18,20   WAKE_N_BUF   R129   0   WAKE_N_PMIC   L12   WAKE_B
3V3   19   PWRBTN_B   R233   0   PWRBTN_B_R   J11   PWRBTN_B
4   SLPRDY_B   R126   0   SLPRDY_B_R   H11   SLPRDY_B
4   SLPMODE   R127   0   SLPMODE_R   D6   SLPMODE
18,19   RESET_IN_B   R230   0   RESET_IN_B_R   C9   RESET_IN_B
IO_PWROK_EN   R219   0   IO_PWROK_EN_R   J4   IO_PWROK_EN
4   RSTRDY_B   R154   0   RSTRDY_B_R   K12   RSTRDY_B
4   THRMTRIP_B   R121   0   THRMTRIP_B_R   C5   THRMTRIP_B
TEST_PMIC   C8   TEST

R444 10K

DA6011

K11   PWROK   PWROK_R   R160   0   PWROK   4,19,20
M12   RESET_B   RESET_B_R   R128   0   RESET_B   4,16,18,19
H3   RSTWARN   RSTWARN_R   R155   0   RSTWARN   4
K3   RSMRST_B   RSMRST_B_R   R170   0   RSMRST_B   4
H2   IO_PWROK   IO_PWROK_R   R221   0   IO_PWROK   11
L11   IO_SLP_PLC_B   IO_SLP_PLC_B_R   R220   0   IO_SLP_PLC_B   11
D4   IO_SLP_PLB_B   IO_SLP_PLB_B_R   R222   0   IO_SLP_PLB_B   11
C4   IO_RST_PLC_B   IO_RST_PLC_B_R   R218   0   IO_RST_PLC_B   11
D5   IO_RST_PLB_B   IO_RST_PLB_B_R   R232   0   IO_RST_PLB_B   11
H4   IO_RST_PLA_B   IO_RST_PLA_B_R   R217   0   IO_RST_PLA_B   11
L13   CTRL_V1P8_S   CTRL_V1P8_S_R   R152   0   CTRL_V1P8_S   6
D2   PROCHOT_B   PROCHOT_B_R   R161   0   PROCHOT_B   4,19
J3   PWRMODE[0]   PWRMODE_R_0_R   R159   0   PWRMODE_R_0   4,18
J2   PWRMODE[1]   PWRMODE_R_1_R   R158   0   PWRMODE_R_1   4,18
K4   PWRMODE[2]   PWRMODE_R_2_R   R157   0   PWRMODE_R_2   4,18

3V3
R213 10K   R214 10K   R188 10K   R216 10K

L2   TMS   TMS_PMIC
L1   TCK   TCK_PMIC
J12   TDO   TDO_PMIC
K2   TDI   TDI_PMIC

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DIALOG DA6011 PMIC PART III

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DIALOG DA6011 PMIC CLOCKS

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1380 Presidential Dr Ste#100
Richardson, TX 75081

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VDD_USB_3v3

C99 0.1uF
C97 0.1uF
C98 0.1uF

VDD_USB_3V3 Power Supply

SCH Note: TPS73633 @ 3.3V
VIN Range: Vin: 1.7V <= Vin <= 5.5V
VIHmin: 1.7V, VILmax: 0.5V
VOUT Range: 1.2V <= Vout <= 5.3V, Imax: 400mA, VDOmax: 200mV

VDD_USB_3v3

Thick etch

U17
5 OUT   IN 1
2
GND
4 NR   EN 3
TPS73633DBVR

C100 0.01uF

VDBG_VBUS

C409 4.7uF

F2
0.75A (1206L075WRT)
2   1

VDD_USB_UART

3V3

C423 0.1uF

ADD ISOLATION BUFFER
FOR UART OPS BEFORE
PMIC POWER UP

VDD_USB_3V3

C424 0.1uF

U36 TXS0104EPW

1 VCCA   VCCB 14
2 A1   B1 13
3 A2   B2 12
4 A3   B3 11
5 A4   B4 10
8 OE   GND 7
   NC1 NC2
   6   9

8 UART0_CTS
8 UART0_TX
8 UART0_RX
8 UART0_RTS

4,14,18,19 RESET_B

8 UART0_PWRENB

USB_SIDE_CTS   DNI R463 0   FTDI_RTSN
USB_SIDE_TX   R226 0   FTDI_RXD
USB_SIDE_RX   R227 0   FTDI_TXD
USB_SIDE_RTS   DNI R225 0   FTDI_CTSN

VBUS_SENSE

Thick etch

R468 1K

C407 0.1uf
C408 0.1uf

FT_RESETN

Thick etch

VDD_USB_3V3

C413 0.1uf

U22
2 RTSN   VCC 12
4 RXD
1 TXD   USBDM 9
6 CTSN   USBDP 8
15 CBUS0
14 CBUS1   RESETN 11
7 CBUS2
16 CBUS3
   VCCIO 3V3OUT
   3   10
   GND1 GND2
   5   13
FT230XS

DNI R466 0

USBDM R469 27   USBDM_R
USBDP R470 27   USBDP_R
                  VBUS_SENSE

C107 47pF
C108 47pF

VDD_USB_UART

Thick etch

R465 4.7K

C109 4.7uF
C412 0.1uf

R467 10K

P47 mini USB-B
   G2   G3
7   6
1 VB
2 D-
3 D+
4 ID
5 G1
   G4   G5
9   8

MTG3
MHOLE
MTG4
MHOLE
MTG1
MHOLE
MTG2
MHOLE

R241 0.01R

DEBUG UART

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ADD SELECTION
FOR AUDIO IC
PWR

3V3   VDD_3V3

DNI
R621   R622
0   0

VDD_AUD3V3

0.1uf C159
1uF C158
0.1uf C142

AGND_AUD   AGND_AUD

FB6
150OHM800mA
1   2   TP15   1

U3

12 BEEP
33 DC_VOL
20 CD_R
19 CD_GND
18 CD_L

TP18
TP4
TP5
TP7
TP9

1 DVDD_CORE
9 DVDD_CORE
25 AVDD_DAC
38 AVDD2_DAC

TP21

43 GPIO0
44 GPIO1
2 GPIO2
3 GPIO3

TP22
TP12
TP17
TP19

5,20 HDA_SDO   5 SDOUT
5,20 HDA_CLK   6 BCLK
5   HDA_SDI0   8 SDIN
5,20 HDA_SYNC   10 SYNC

TP14
TP6
TP16
TP8

5,20 HDA_RST_N   11 RESET

TP10

45 NC1
46 NC2

TP23
TP13

4 DVSS_CORE
7 DVSS_CORE

26 AVSS_DAC
42 AVSS2_DAC

TP11

FB7
1   2
150OHM800mA

AGND_AUD

R266
20K

C140
1uF

AGND_AUD

40 JDREF
27 VREF

ALC262

30 MIC2_VREFO
32 MIC1_VREFO_R
28 MIC1_VREFO_L
48 SPDIFO
47 SPDIF/EAPD

39 HPOUT_L
41 HPOUT_R

37 MONO_OUT
16 MIC2_L
17 MIC2_R
21 MIC1_L
22 MIC1_R

13 SENSE_A
34 SENSE_B

35 LINEOUT_L
36 LINEOUT_R

23 LINE1_IN_L
24 LINE1_IN_R
14 LINE2_L
15 LINE2_R

29 LINE1_VREFO
31 LINE2_VREFO

SENSE_A   R249   5.1K
SENSE_B   DNI R257 5.1K
AGND_AUD

AUD1_IN_SENSE

LINEOUT_L   R259 100   AUD_OUT_L
LINEOUT_R   R258 100   AUD_OUT_R

LINE1_IN_L   C122 0.1uf   AUD1_IN_L
LINE1_IN_R   C123 0.1uf   AUD1_IN_R

DNI
C11
100uF
10V

DNI
C12
100uF
10V

DNI R13 4.7K
DNI R14 4.7K

L1 VREF RR
L1 VREF RL
L1 VREF D1
L1 VREF DL

DNI
D10
RB717F

LINE1_VREF

DNI C120 47nF
DNI C121 47nF
C143 47nF
C141 47nF

AGND_AUD

D2 D3   D4 D5
PGB0010603MR

1 SLEEVE
R
S
TS
3
5
4
2
P3 AUDIO_OUT
SJ1-3515-SMT-TR-GR

1 SLEEVE
R
S
TS
3
5
4
2
P2 AUDIO_IN
SJ1-3515-SMT-TR-BE

AGND_AUD

AUDIO

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Engineer(s) MINNOW_TEAM

VDD_5V

THICK ETCH

NOTE: WHEN VERIFY OR PROGRAM OCCURS
DEDIPROG ACTIVATES 3V3_DEDIPROG (3.3V)
AND GNDS DEDIPROG_IO3 (GND) FOR FLASH
PROGRAMING DURING BOARD ACTIVITY

R203 49.9K   R199 49.9K   R206 49.9K   R202 49.9K   R207 49.9K

3V3_DEDIPROG

18 DEDIPROG_IO3_N
THICK ETCH

R204 499 E6XX_SPI_SCK_G THICK ETCH
R200 499 E6XX_SPI_MOSI_G
R205 499 E6XX_SPI_CS_B_G   THICK ETCH   THICK ETCH
R201 499 BIOS_SPI_MISO_G
R208 499 BIOS_SPI_WP_N_G

3V3_S   Q3 BSS138

THICK ETCH

C382 0.1uF   C381 4.7uF   R437 4.7K

R436 4.7K

Q6 BSS138   Q4 BSS138

4 E6XX_SPI_SCK
4 E6XX_SPI_CS_B

BIOS_SPI_SCK 18   BIOS_SPI_CS 18

U11
18 BIOS_SPI_SCK   R438 33 BIOS_SPI_SCK_R   6 CLK   VCC 8
18 BIOS_SPI_MOSI R439 33 BIOS_SPI_MOSI_R 5 DI
18 BIOS_SPI_MISO R414 33 BIOS_SPI_MISO_R 2 DO
                                                  CS   HOLD 7 BIOS_SPI_HOLD_N
18 BIOS_SPI_CS   R413 33 BIOS_SPI_CS_R   1
                       BIOS_SPI_WP_N   3 WP   GND 4
W25Q32CV

Q7 BSS138   Q5 BSS138

4 E6XX_SPI_MOSI

BIOS_SPI_MOSI 18   E6XX_SPI_MISO 4

18 BIOS_SPI_MISO

At least 0.1" on the pin 1-2 side
and the pin 7-8 side to allow
space for the DediProg connector

3V3_DEDIPROG

R412 4.7K   J11

3/8" Minimum on all sides
of the JTAG port (ITP) connector
and 1" of vertical clearance
above the connector is required

18 BIOS_SPI_CS   1 2
18 BIOS_SPI_MISO   3 4   BIOS_SPI_SCK 18
                       5 6   BIOS_SPI_MOSI 18
                       7 8   DEDIPROG_IO3_N 18
HEADER 4x2

Ensure the odd numbered pins
are facing the PCB edge

1V05_S

R146 R145 R392 R117 R391 R116
49.9 49.9 49.9 49.9 49.9 49.9

Ensure the odd numbered pins
are facing the PCB edge

DNI J7

1V05_S   3V3_S

R409 10R PREQ_B_R   NCLK_TTL 4
R408 10R PRDY_B_R

4 PREQ_B
4 PRDY_B

4 BPM_B3
4 BPM_B2

4 BPM_B1
4 BPM_B0

18 XDP_TCK   DNI R82 0   IO_TCK 4   18 XDP_TCK   R83 0   CPU_TCK 4
18 XDP_TMS   DNI R85 0   IO_TMS 4   18 XDP_TMS   R68 0   CPU_TMS 4
18 XDP_TDO   DNI R41 0   IO_TDO 4   18 XDP_TDO   R93 0   CPU_TDO 4,18
18 XDP_TRST_N DNI R79 0   IO_TRST_N 4   18 XDP_TRST_N R80 0   CPU_TRST_N 4
18 XDP_TDI   DNI R276 0   IO_TDI 4,18   18 XDP_TDI   R81 0   CPU_TDI 4
                                              4,18 IO_TDI   DNI R42 0 CPU_TDO 4,18

CONN_ITP_XDP

DNI R112 49.9
R109 0   XDP_CLK_P_R 15

R111 100

DNI R97 49.9
R94 0   XDP_CLK_N_R 15

4,14 PWRMODE_R_0   R115 1K XDP_PWRMODE0   XDP_CLK_P
4,14 PWRMODE_R_1   R114 1K XDP_PWRMODE1   XDP_CLK_N

4,14 PWRMODE_R_2   R101 1K XDP_PWRMODE2   XDP_CPU_RST_N R113 0   RESET_B 4,14,16,19
4,11,14,20 WAKE_N_BUF R366 0 XDP_CB_WAKE_N   XDP_CB_SYS_RST R110 0   RESET_IN_B 14,19

ATOM JTAG & BIOS FLASH

4,14,20 SMB_DAT   R100 0 XDP_SDAT   XDP_TDO_R   R78 0
4,14,20 SMB_CLK   R99   0 XDP_SCLK   XDP_TRST_N_R R95 0   XDP_TRST_N 18
                                        XDP_TDI_R   R96 0   XDP_TDI 18
18 XDP_TCK   R98   0 XDP_TCK_R XDP_TMS_R   R69 0   XDP_TMS 18
                                        XDP1_PRSNT_N R77 1K 3V3_S
                                                                 XDP_TDO 18
1V05_S   56.2 R40

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ATOM BOOTSTRAP DEFINITIONS

```
GPIO(0)       = BOOT FLASH SRC (1=SPI)
GPIO(1)       = N/A
GPIO(3:2)     = CMA BADDR (00=0xFFFB0000)
GPIO(4)       = LPCCLK STRENGTH (0=1Load)
GPIO_SUS(0)   = SPI MEM_WIDTH (1=x8)
GPIO_SUS(6:5) = SPI MEM SIZE (11=2Gb)
GPIO_SUS(7)   = E6xx B1 REV Silicon
GPIO_SUS(8)   = DDR2 Mem Rank(1=1Rank)
```

3V3 R451 10K E6XX_GPIO_0 4,19 DN R450 1K
3V3 R92 10K E6XX_GPIO_1 4,19 DN R76 1K
3V3 DN R453 10K E6XX_GPIO_2 4,19 R452 10K
3V3 DN R455 10K E6XX_GPIO_3 4,19 R454 10K
3V3 DN R446 10K E6XX_GPIO_4 4,21 R447 1K

3V3_S R51 10K E6XX_GPIO_SUS0 4,19 DN R52 1K
3V3_S R182 10K E6XX_GPIO_SUS5 4,19 DN R183 1K
3V3_S R171 10K E6XX_GPIO_SUS6 4,19 DN R172 1K
3V3_S R229 10K E6XX_GPIO_SUS7 4,8 DN R228 1K
3V3_S R411 10K E6XX_GPIO_SUS8 4,11 DN R410 1K

ADDED PULLUPS FOR SWITCHES TO BE ABLE TO USE FOR GPIO TOGGLING AFTER BOOTUP

R473 1K 3V3 E6XX_GPIO_S0 19
TL3320AF100Q

PULLED UP ON BOOT UP
E6XX_GPIO_1 4,19
TL3320AF100Q

R474 1K 3V3 E6XX_GPIO_S2 19
TL3320AF100Q

R475 1K 3V3 E6XX_GPIO_S3 19
TL3320AF100Q

DNI R476 10K 3V3 RESET_IN_B 14,18 PULLED UP PMIC INTERNAL
TL3320AF100Q

VDD_5V R215 10K PWRBTN_B 14
TL3320AF100Q

3V3_S U37 C1043 0.1uF VCC 14
R624 1K UNA A3 6 B3 9 ONA 1K R627 DNI
R625 1K UNB A2 5 B3 10 ONB 1K R628 DNI
4,14 PROCHOT_B A1 3 B2 12 PROCHOT_B_3V3
THERMTRIP_B A0 2 B1 13 THERMTRIP_B_3V3
B0
1V05_S DIR 1 GND1 7
R623 1K GTLREF 4 GND2 8
GTL_REFA GND3 11
GTL2005PW
R626 2.2K C1044 1uF

GREEN LED R173 330 D11 LTST-S270GKT GRN Q1A DMC56404
4,19 E6XX_GPIO_SUS5 10k 47k 3V3_S

GREEN LED R174 330 D12 LTST-S270GKT GRN Q1B DMC56404
4,19 E6XX_GPIO_SUS6 10k 47k 3V3_S

GREEN LED R210 330 D15 LTST-S270GKT GRN Q2A DMC56404
4,14,20 PWROK 10k 47k 3V3_S

RED LED R195 330 D14 LTST-S270KRKT RED Q2B DMC56404
3V3_S R629 10k 10k 47k 3V3_S
C78 0.1uF U12 PROCHOT_B_3V3 PROCHOT_3V3
SN74LVC1G06

U14 TXS0104EPW
C392 0.1uF 3V3 VCCA 1 VCCB 14 3V3 C393 0.1uF
4,19 E6XX_GPIO_0 A1 2 B1 13 E6XX_GPIO_S0 19
4,19 E6XX_GPIO_2 A2 3 B2 12 E6XX_GPIO_S2 19
4,19 E6XX_GPIO_3 A3 4 B3 11 E6XX_GPIO_S3 19
4,19 E6XX_GPIO_SUS0 A4 5 B4 10 E6XX_GPIO_SUS0_BUF 20
4,14,16,18 RESET_B OE 8 NC1 NC2 GND 7

ATOM BOOTSTRAP - GPIO LED - SWITCHES

VDD_3V3   VDD_3V3

R193 1K   R209 1K

PCIe2_CLK_REQ
PCIe1_CLK_REQ

4,14,19   PWROK

15   PCIe_REFCLK_N
Differential pair   DNI   R194   100
15   PCIe_REFCLK_P

Differential pair   5   PCIe1_RX_N
5   PCIe1_RX_P

Differential pair   5   PCIe1_TX_N
5   PCIe1_TX_P

4,14,18   SMB_CLK
4,14,18   SMB_DAT

9   SATA1_RX_N
9   SATA1_RX_P

9   SATA1_TX_N
9   SATA1_TX_P

Differential pair   8   USB_HOST_DM4
8   USB_HOST_DP4
VBUS4

20   WAKE_EXP_N   UART1_TX
8   UART1_TX   UART1_RX
8   UART1_RX   UART2_TX
8   UART2_TX   UART2_RX
8   UART2_RX   I2C0_SCL
9   I2C0_SCL   I2C0_SDA
9   I2C0_SDA

9   EG20T_SPI_CLK   EG20T_SPI_CLK
9   EG20T_SPI_nCS   EG20T_SPI_nCS
9   EG20T_SPI_MOSI   EG20T_SPI_MOSI
9   EG20T_SPI_MISO   EG20T_SPI_MISO
  GPIO0
11,21   GPIO0   GPIO1
11,21   GPIO1   GPIO2
11,21   GPIO2   GPIO3
11,21   GPIO3   GPIO4
11,21   GPIO4   GPIO5
11,21   GPIO5   GPIO6
11,21   GPIO6   GPIO7
11,21   GPIO7
GPIO_PROG_VOLTAGE

J8
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
31 32
33 34
35 36
37 38
39 40
41 42
43 44
45 46
47 48
49 50
51 52
53 54
55 56
57 58
59 60
61 62
63 64
65 66
67 68
69 70
71 72
73 74
75 76
77 78
79 80
81 82
83 84
85 86
87 88
89 90
91 92
93 94
95 96
97 98
99 100

DC_IN_5V   DC_IN_5V

CONN PLUG 50x2/SM

Differential pair
LVDS_DATA_N_0
LVDS_DATA_P_0
Differential pair
LVDS_DATA_N_1
LVDS_DATA_P_1
Differential pair
LVDS_DATA_N_2
LVDS_DATA_P_2
Differential pair
LVDS_CLK_N
LVDS_CLK_P
Differential pair
LVDS_DATA_N_3
LVDS_DATA_P_3

HDA_CLK   5,17
HDA_RST_N   5,17
HDA_SYNC   5,17
HDA_SDO   5,17
HDA_SDI1   5

PCIe2_RX_N   5
PCIe2_RX_P   5   Differential pair

PCIe2_TX_N   5
PCIe2_TX_P   5   Differential pair

CAN_TX   9
CAN_RX   9

LVDS_DATA_N_0   4
LVDS_DATA_P_0   4

LVDS_DATA_N_1   4
LVDS_DATA_P_1   4

LVDS_DATA_N_2   4
LVDS_DATA_P_2   4

LVDS_CLK_N   4
LVDS_CLK_P   4

LVDS_DATA_N_3   4
LVDS_DATA_P_3   4

E6XX_GPIO_SUS0_BUF   19
E6XX_GPIO_SUS1   4
E6XX_GPIO_SUS3   4
E6XX_GPIO_SUS4   4
E6XX_GPIO_SUS2   4
GPIO11   11
SDIO1_CD_N   9
SDIO1_WP   9
SDIO1_CLK_R   9
SDIO1_CMD_R   9
SDIO1_DATA0_R   9
SDIO1_DATA1_R   9
SDIO1_DATA2_R   9
SDIO1_DATA3_R   9

LVDS CONTROLS
E6XX_GPIO_SUS0_BUF = LVDS_VDD_EN
E6XX_GPIO_SUS1 = LVDS_BKLTEN
E6XX_GPIO_SUS2 = LVDS_BLKCTRL
E6XX_GPIO_SUS3 = LVDS_DDC_CLK
E6XX_GPIO_SUS4 = LVDS_DDC_DAT
GPIO11 = LVDS_DETECT
    0 = NO LVDS PRESENT
    1 = LVDS PRESENT

3V3_S   3V3_S

C339 0.1uF   R394 1K

U8
5
4
1
2
3
74LVC1G07DCK

4,11,14,18   WAKE_N_BUF   WAKE_EXP_N   20

EXPANSION BUS I/O

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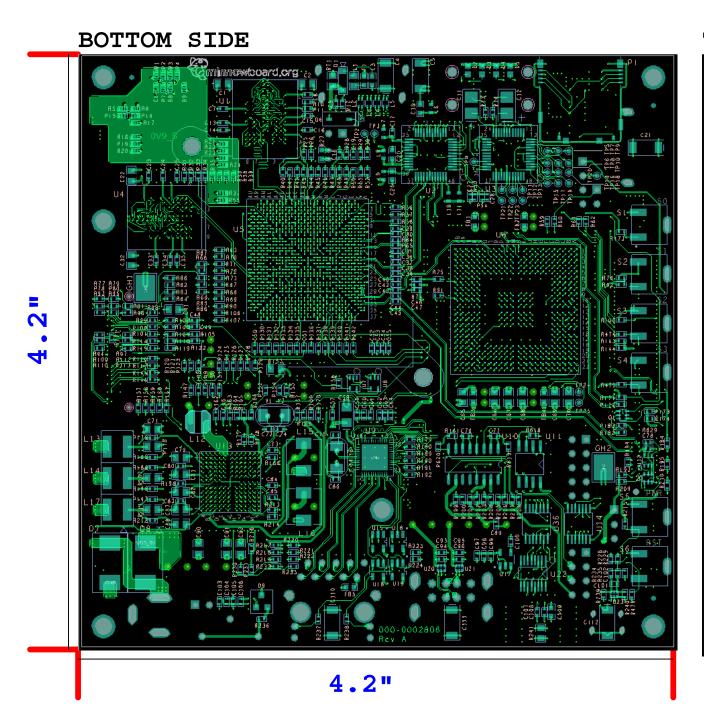
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GPIO-flash-programmer

VDD_3V3

R449
10K

Thick Etch

R448   100   E6XX_GPIO_4_GATE_VOLTAGE

3

Q8B
DMC56404

4,19   E6XX_GPIO_4

5

10k

47k

4

G

Q9
DMG1013T

VDD_3V3

S

D

Thick Etch   Thick Etch

VDD_3V3

J10
1
2
3
HEADER 3

GROUND HOOK TEST POINTS

DNI
GH1

DNI
GH2

DNI
GH3

DNI
GH4

GPIO_PROG_VOLTAGE   GPIO_PROG_VOLTAGE

J9
1   2   2
3   3   4   4
5   5   6   6
7   7   8   8
9   9   10   10
HEADER 5X2

11,20   GPIO0
11,20   GPIO2
11,20   GPIO4
11,20   GPIO6

GPIO1   11,20
GPIO3   11,20
GPIO5   11,20
GPIO7   11,20

**Hardware Identification (HW ID)
"001" = Revision X3**

3V3   3V3   3V3

DNI
R314
10K

DNI
R316
10K

R315
10K

11   GPIO10   11   GPIO9   11   GPIO8

R310
1K

R317
1K

DNI
R311
1K

MINNOW GPIO BUS PROGRAMMER

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BOTTOM SIDE

TOP SIDE

4.2"

4.2"

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