

TURBOT Dual-E

Rev : R200

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REVISION HISTORY:

Rev	Date	Notes
X100	2016/04/29	Prototype Release
R100	2016/10/19	Production Release
R200	2016/12/16	Changed M.2 RESET# from 3.3V to 1.8V

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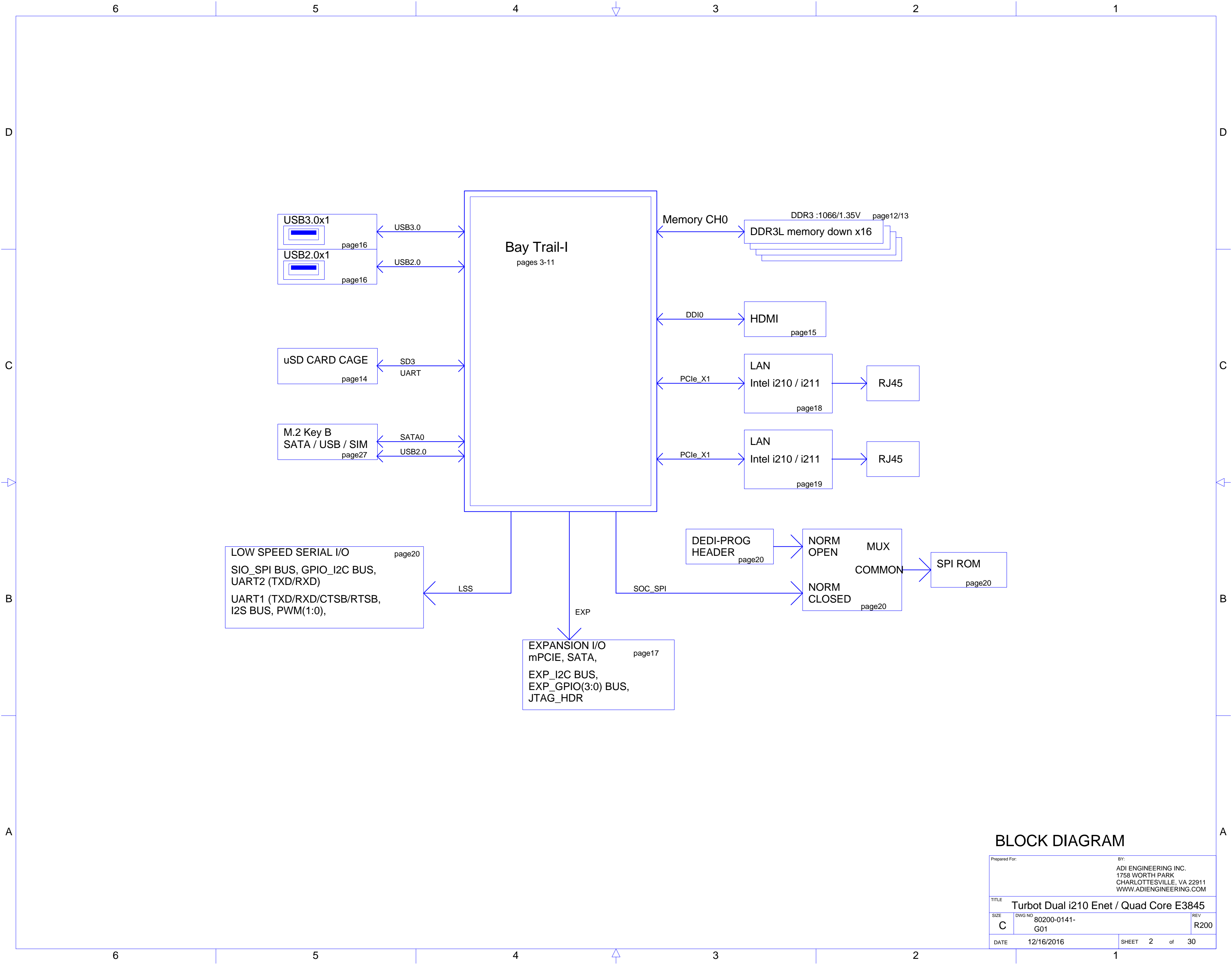
Minnowboard Turbot Dual-E design derived from Minnowboard Turbot B as Designed by ADI Engineering, A Division of Silicom and Minnowboard MAX as designed by CircuitCo LLC.

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For all design files, including bill of materials and gerber files, please visit www.minnowboard.org

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TITLE Turbot Dual i210 Enet / Quad Core E3845			
SIZE C	DWG NO 80200-0141-G01	REV R200	
DATE 04/17/2017		SHEET 1	of 30



BLOCK DIAGRAM

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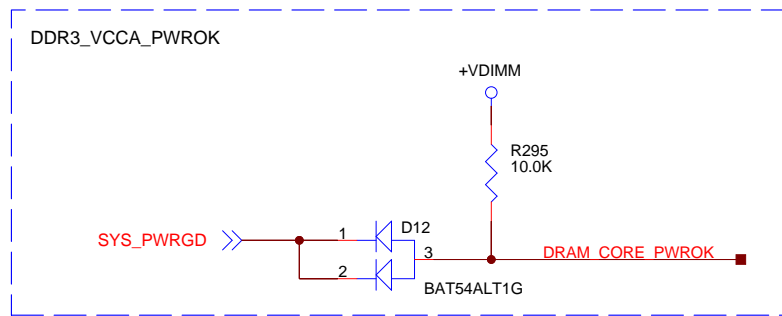
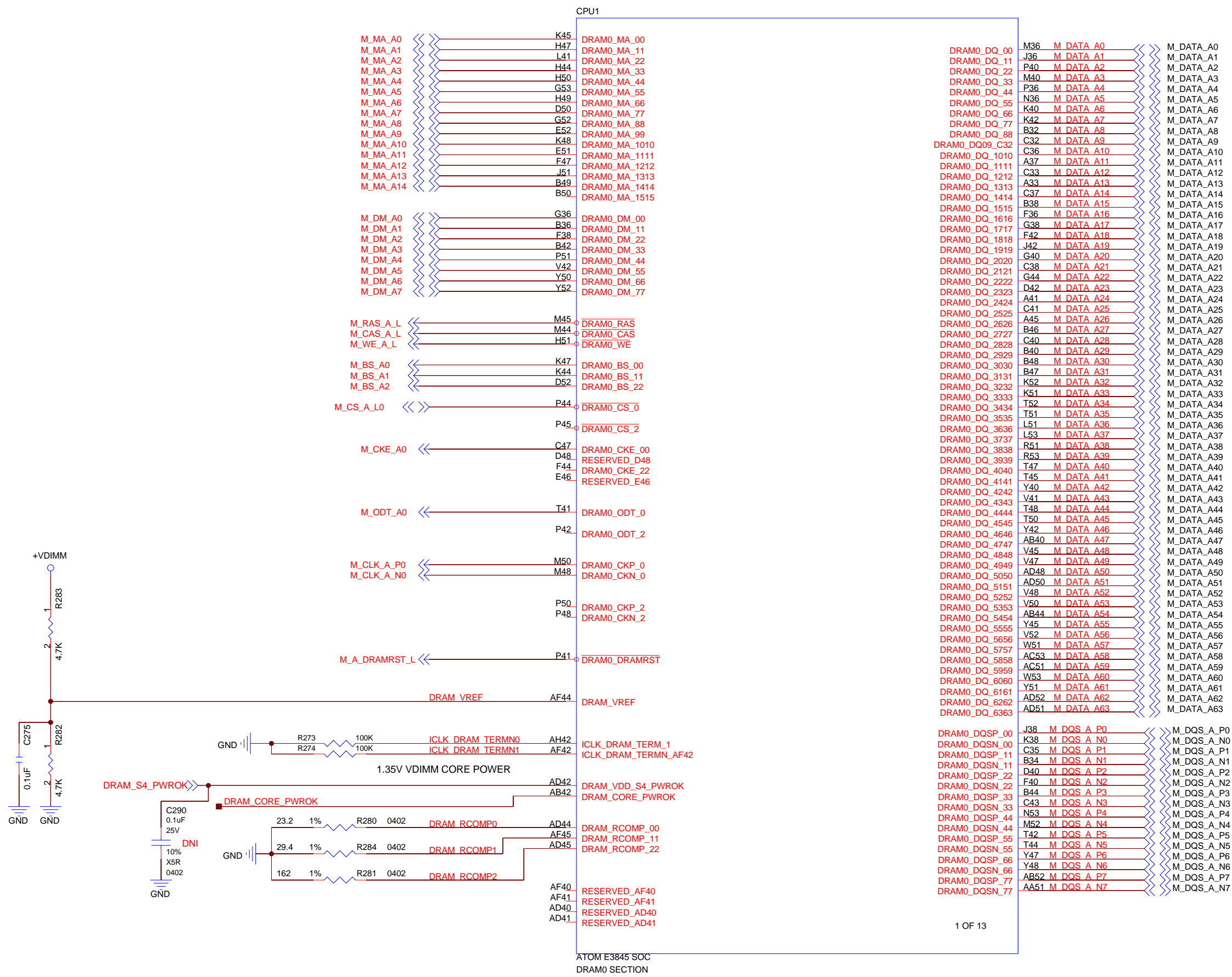
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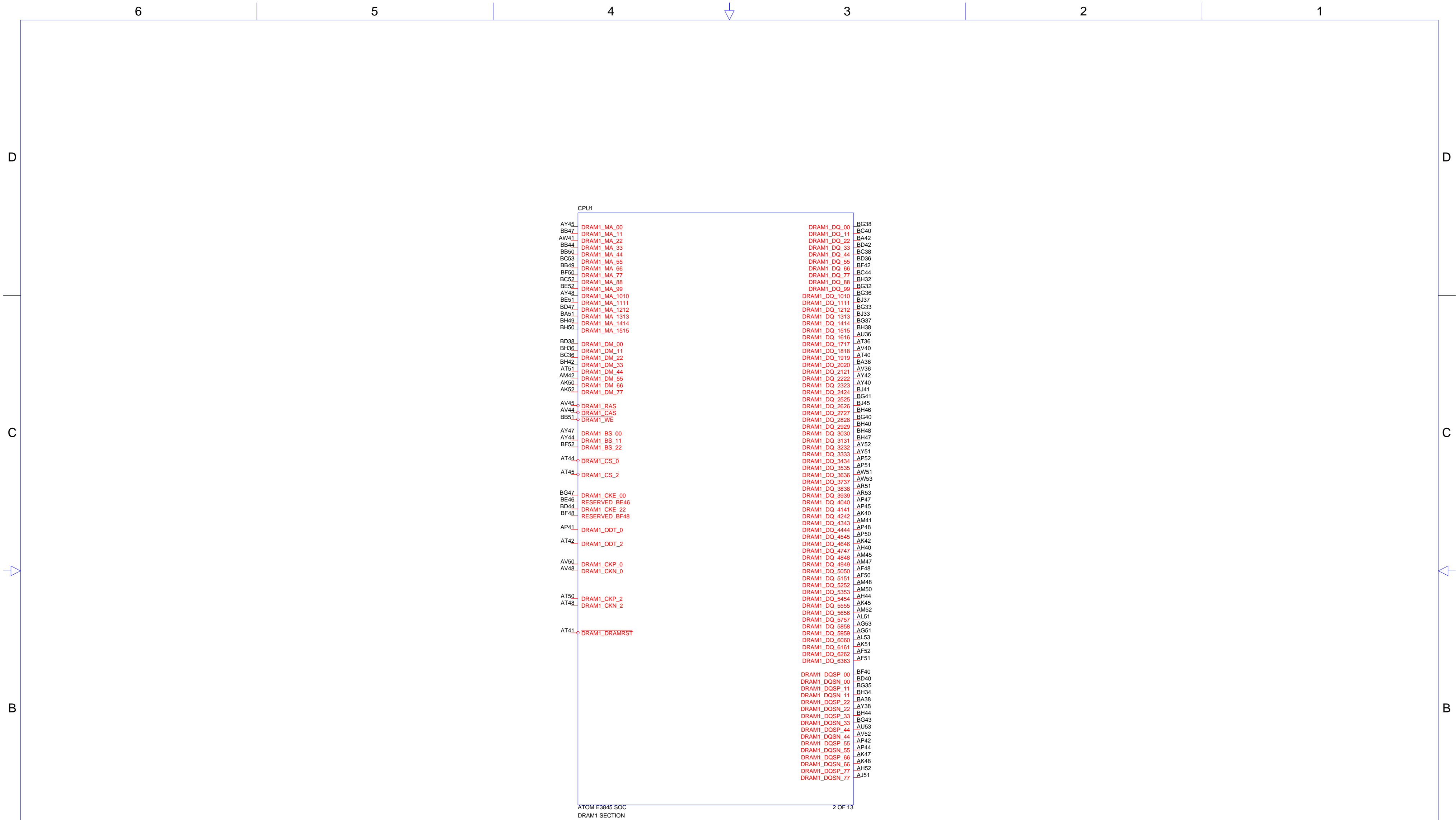
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CPU-DDR3-CHA

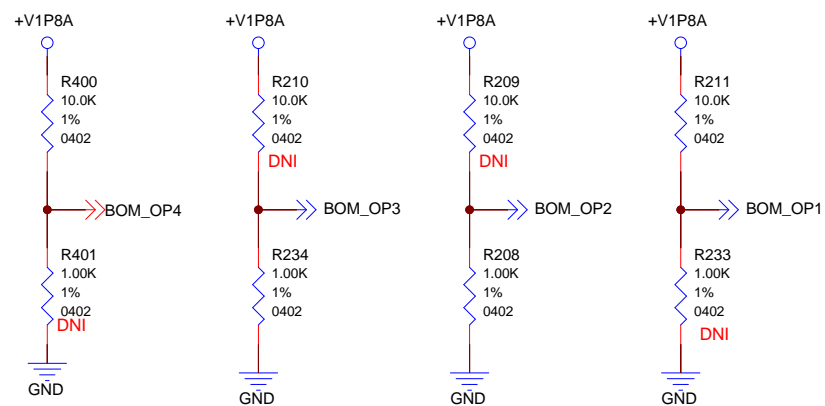
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CPU-DDR3-CHB

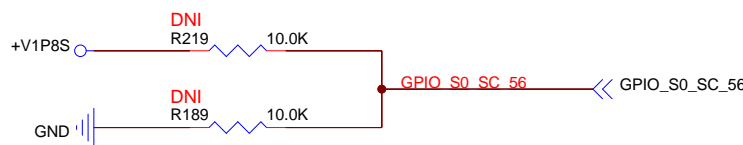
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BOM Option
Hardware Identification (HW ID)
"1001"



HW STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC



Top Swap(A16 Override)

H	Top address bit is unchanged
L	Top address bit is inverted

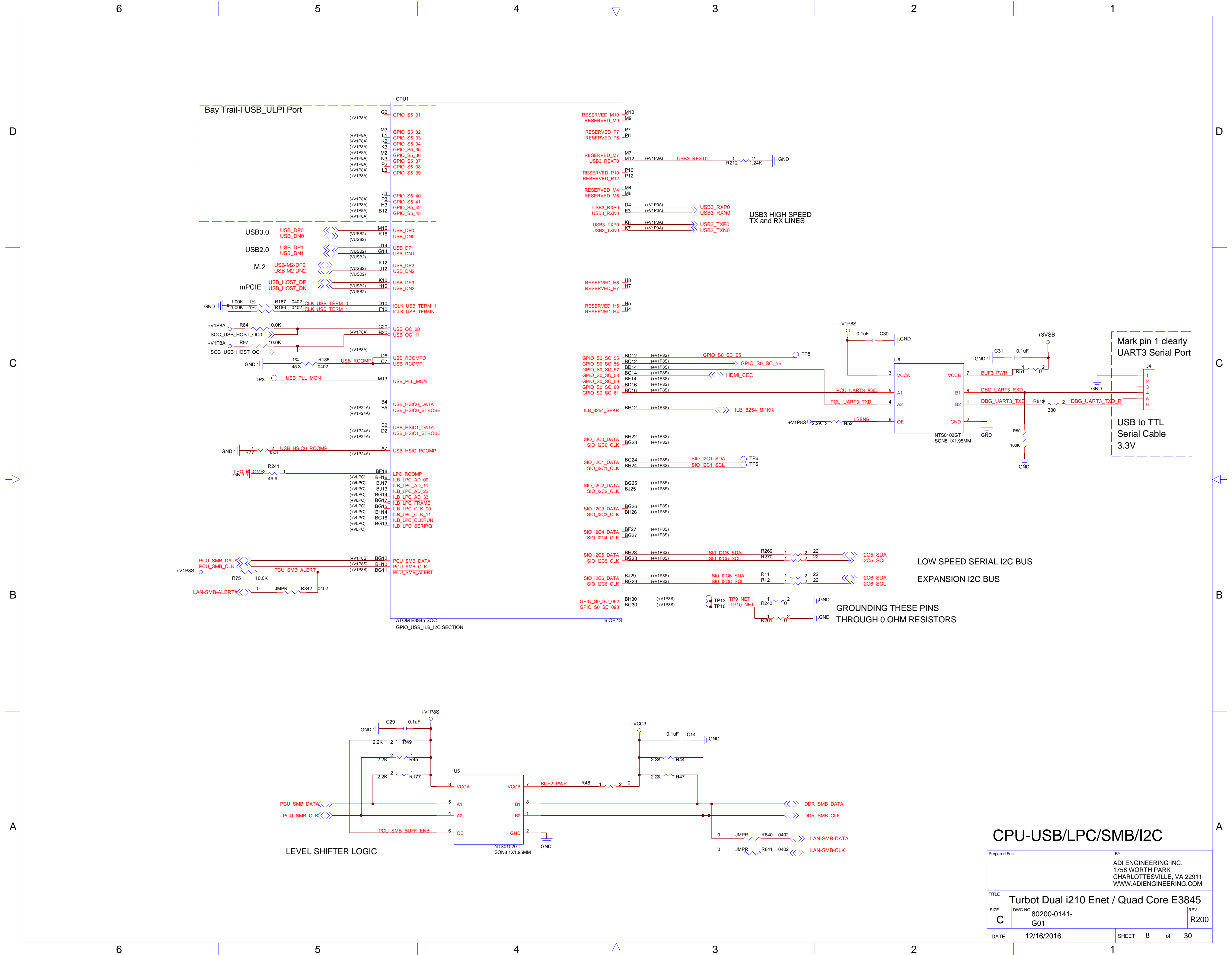
Strap Pin	Function
GPIO_S0_SC63 (LPE_I2S_FRM)	BIOS Boot Selection 0=LPC *1=SPI
GPIO_S0_SC65 (LPE_I2S_DATAOUT)	Security Flash Descriptors 0=Override *1=Normal Operation

CPU-PE/HDA/SD/eMMC/Strap

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CPU-USB/LPC/SMB/I2C

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CPU-PWR1/TPM/LPC

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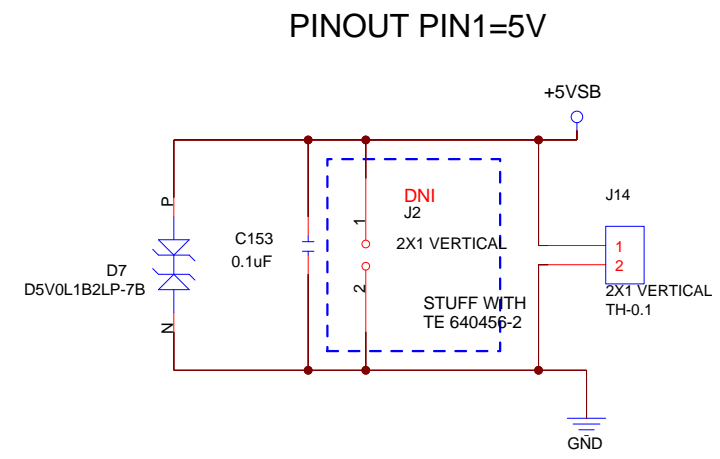
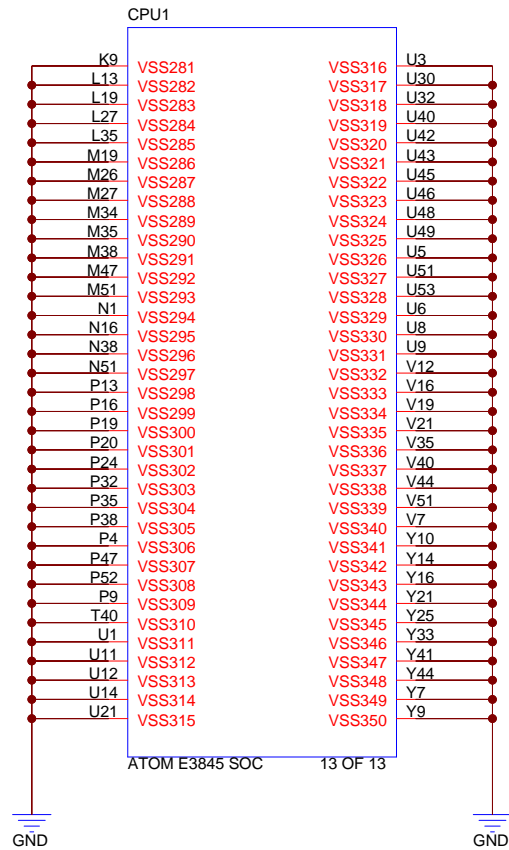
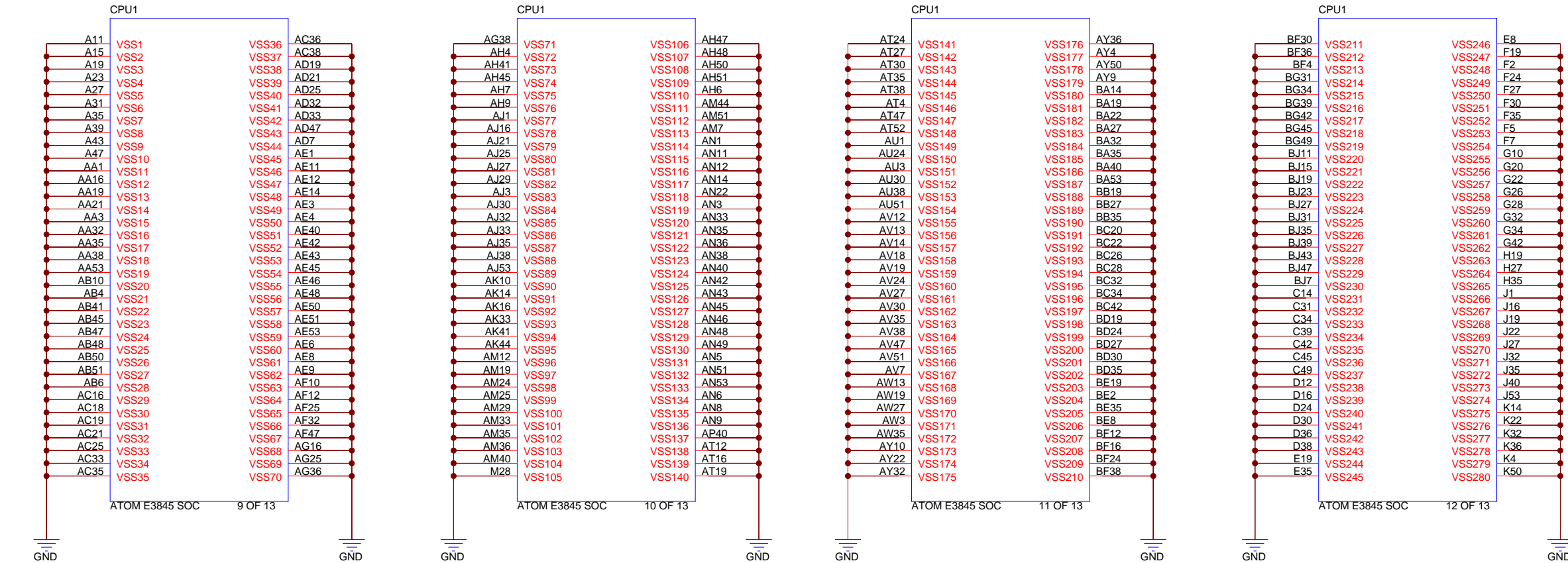
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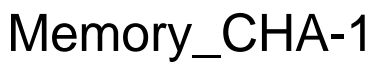
A



Note: Do not Populate J2 and J14 at same time as they occupy the same space. J2 is 2.54 mm pitch and J14 is 2.00 mm pitch.

CPU-GND

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TITLE			
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SIZE:	DWG NO	REV	
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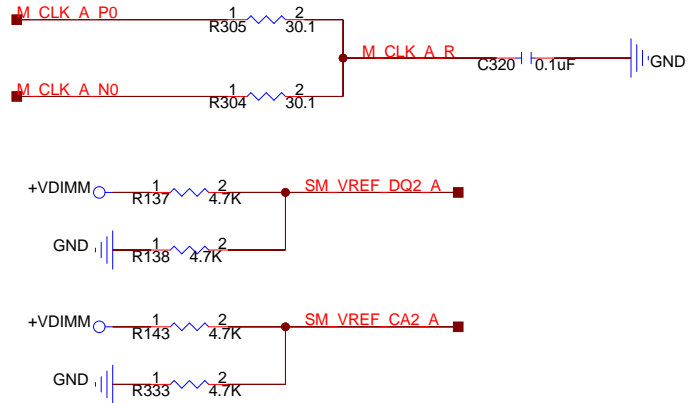
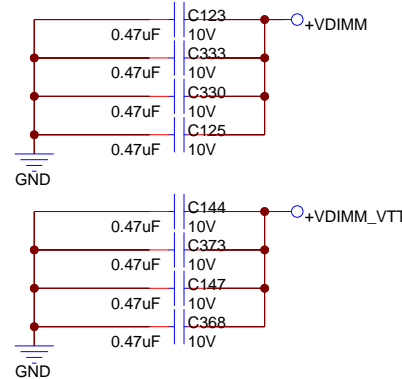
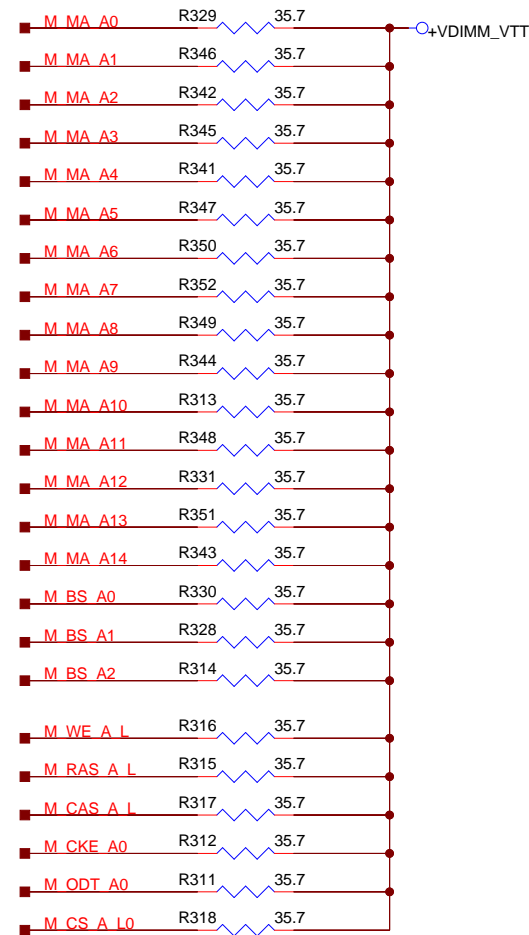
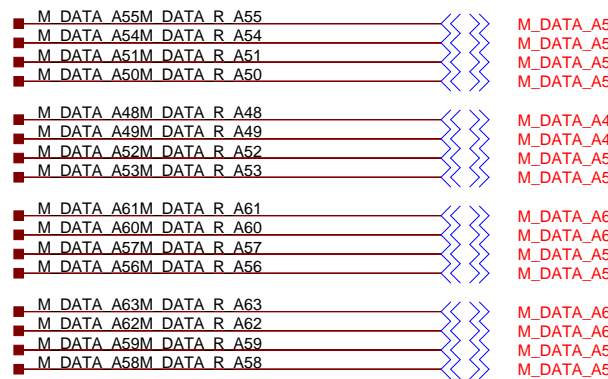
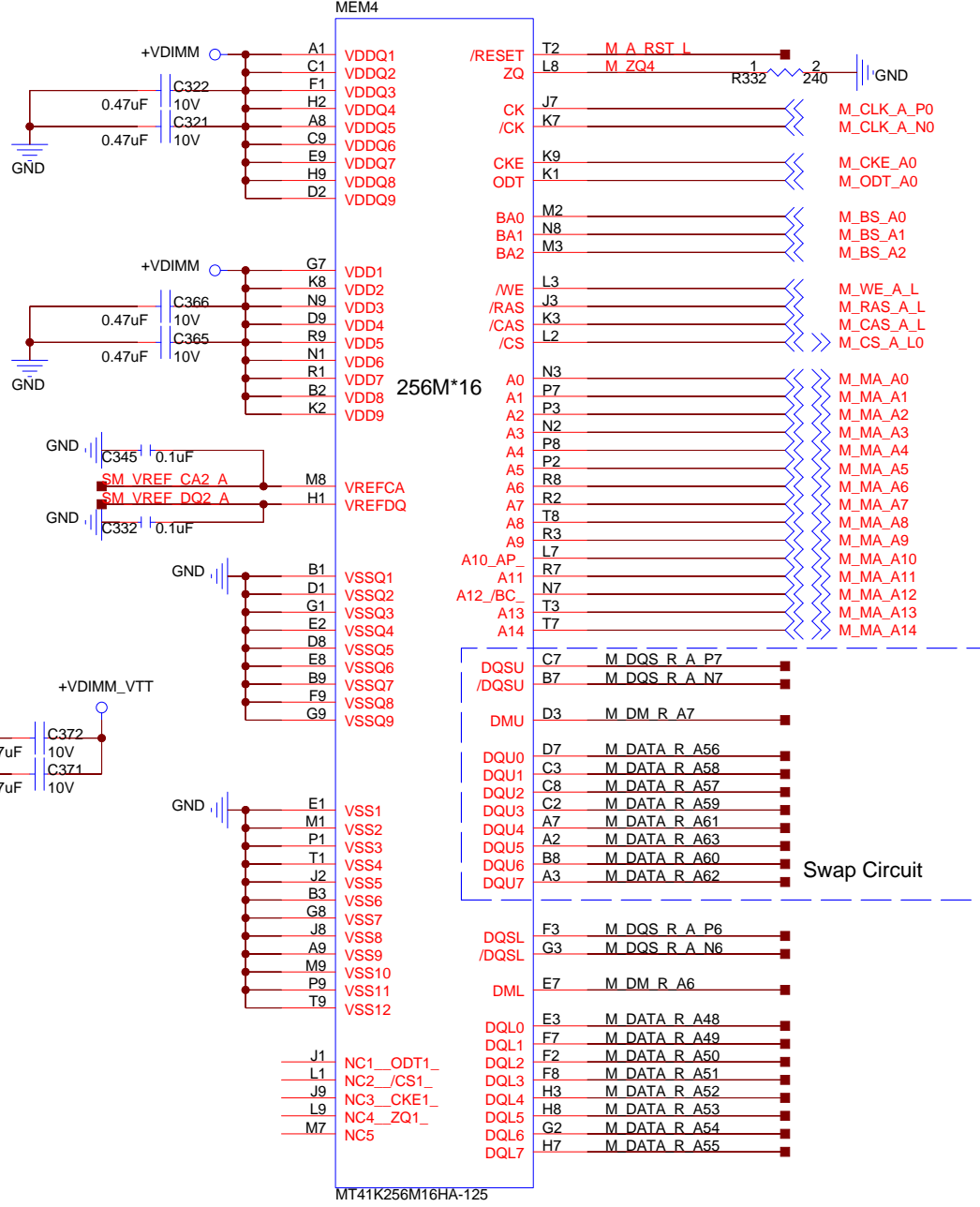
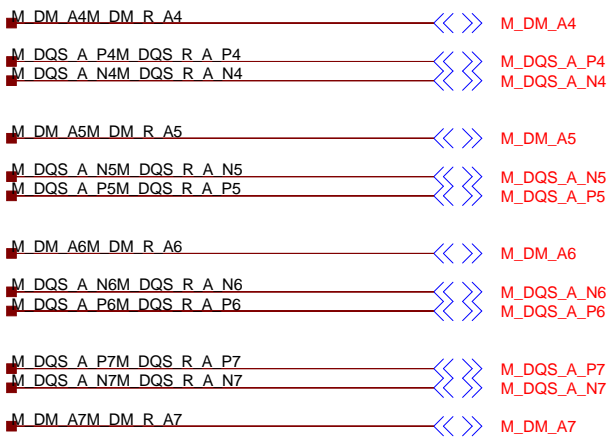
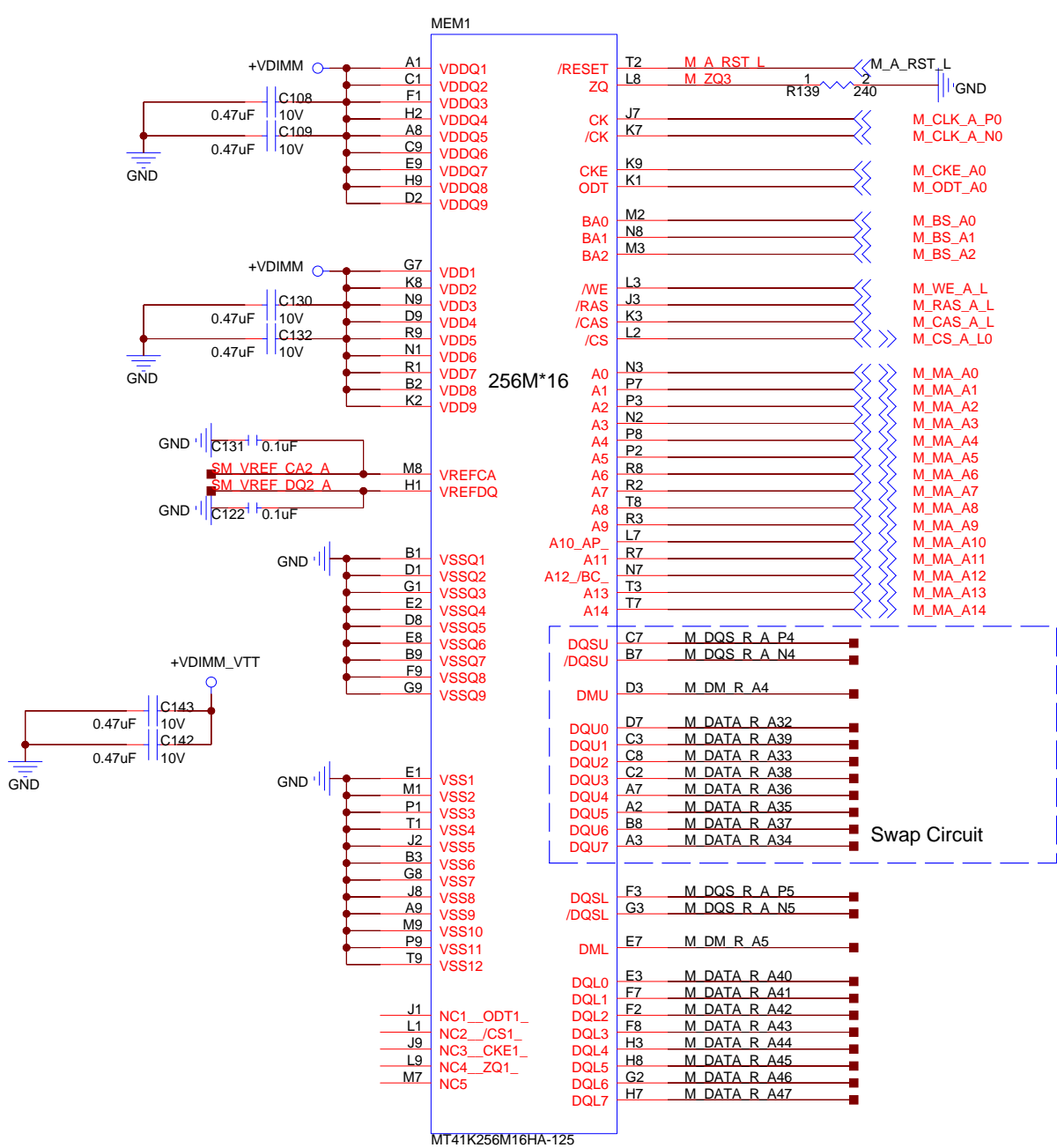
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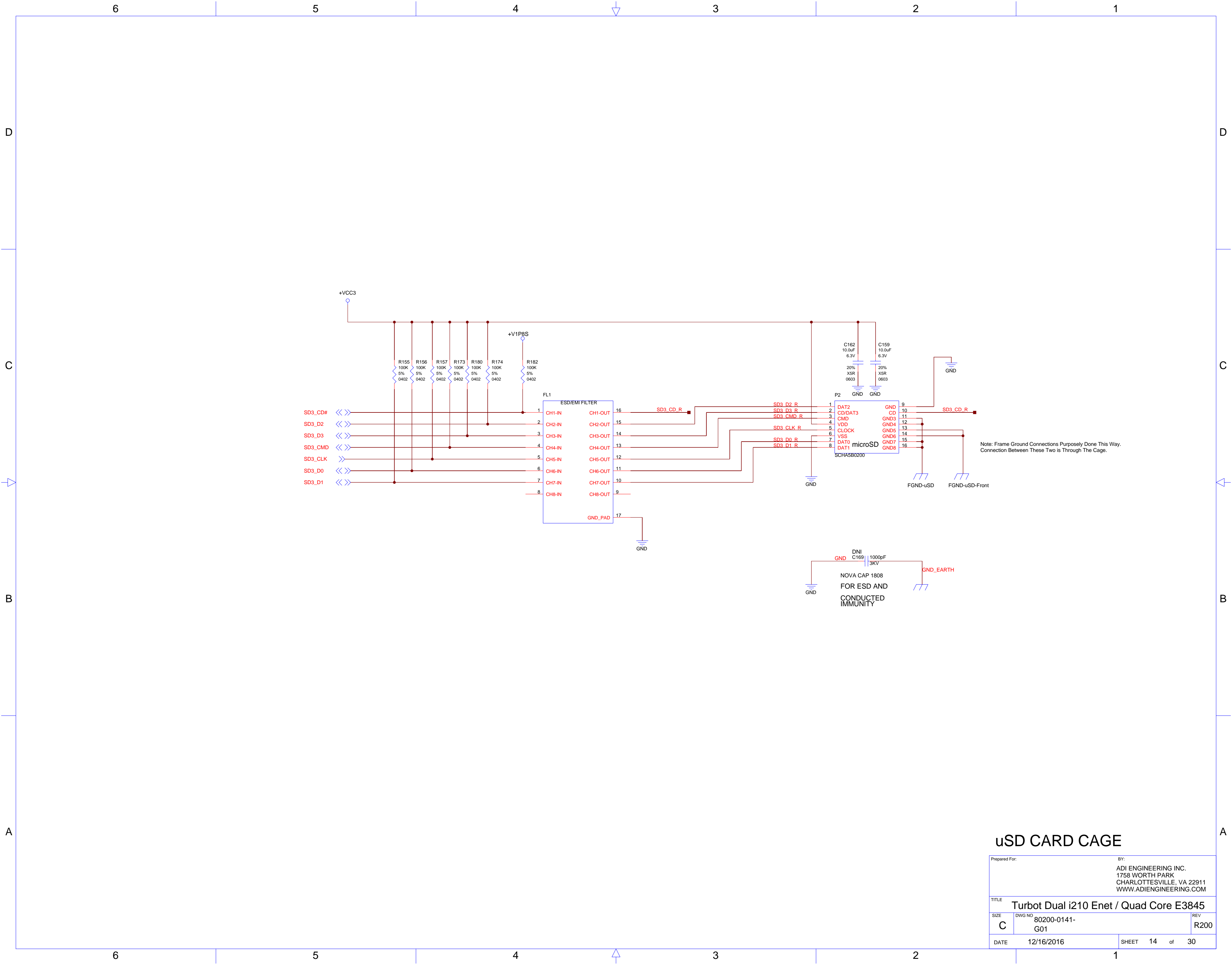
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NOTE: COMPATIBLE DDR3L MEMORIES
FOR THE MINNOWMAX
ARE THE FOLLOWING:
MICRON MT41K128M16HA-125:D,
MICRON MT41K512M16HA-125:E,
MICRON MT41K512M16HA-125:X

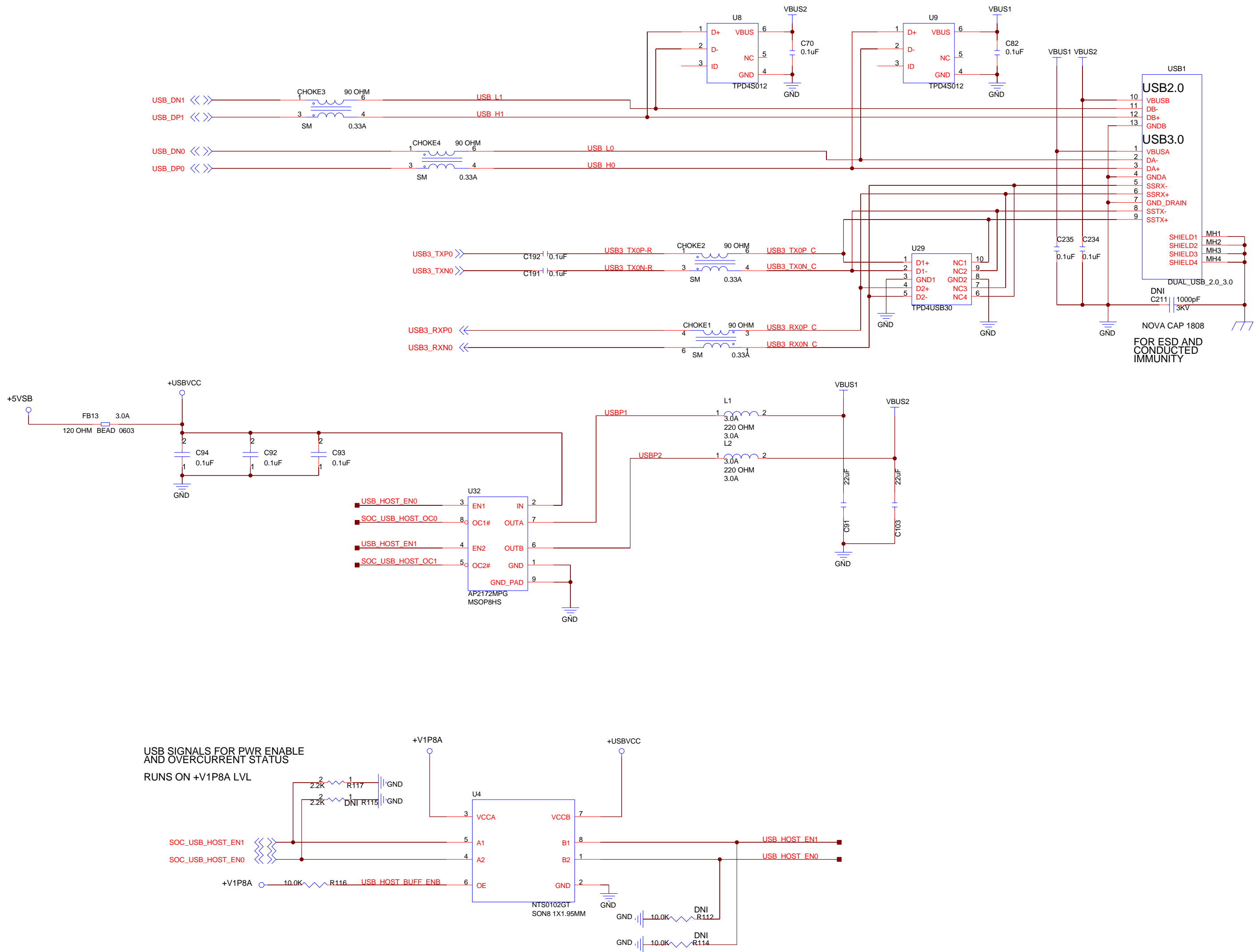
Memory_CHA-2

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SIZE	DWG NO. 80200-0141- G01
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REV	R200



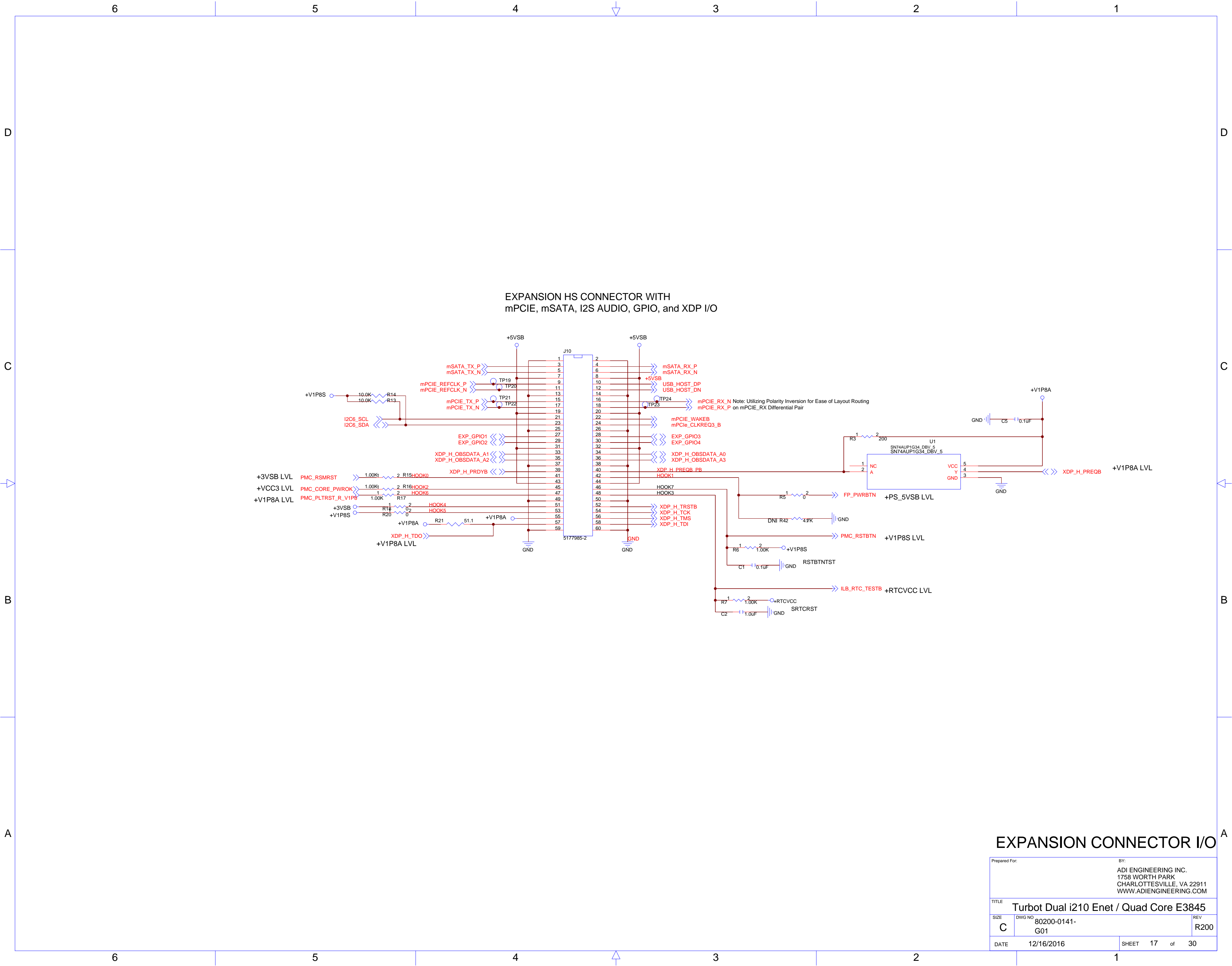
uSD CARD CAGE

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SIZE C	DWG NO 80200-0141- G01	REV R200	
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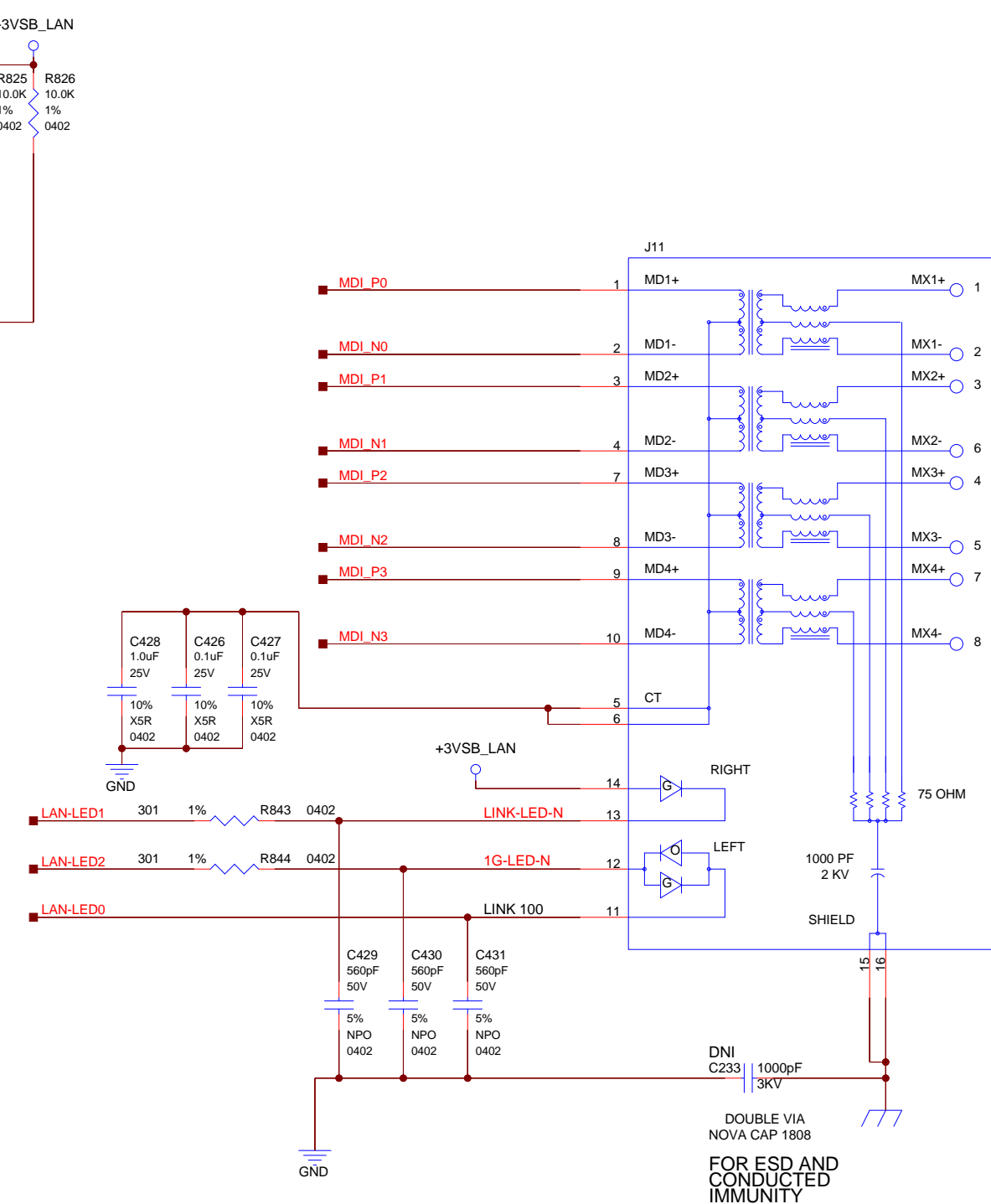
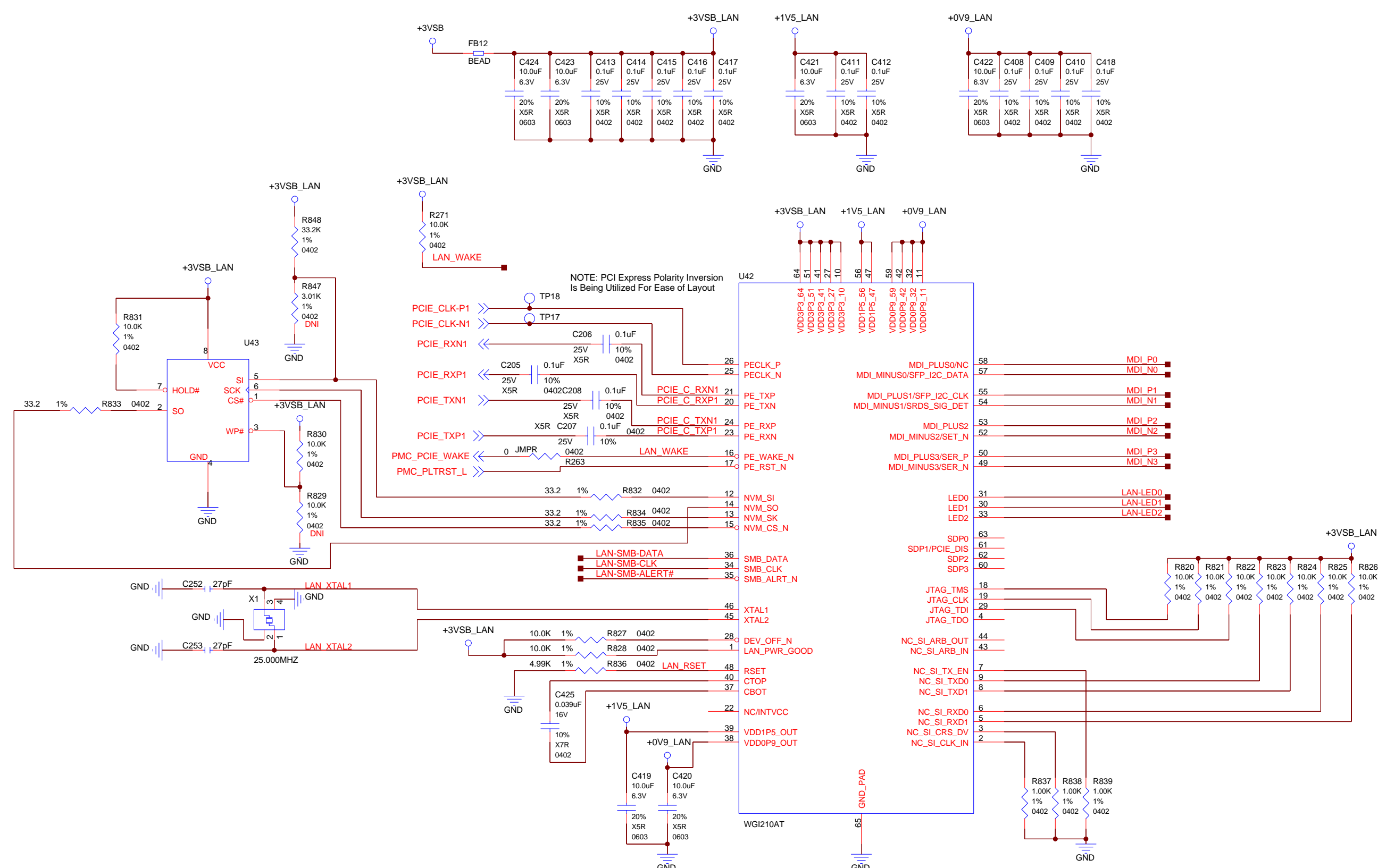
USB3+USB2

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EXPANSION CONNECTOR I/O

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LAN #1 i210/i211

D

C

B

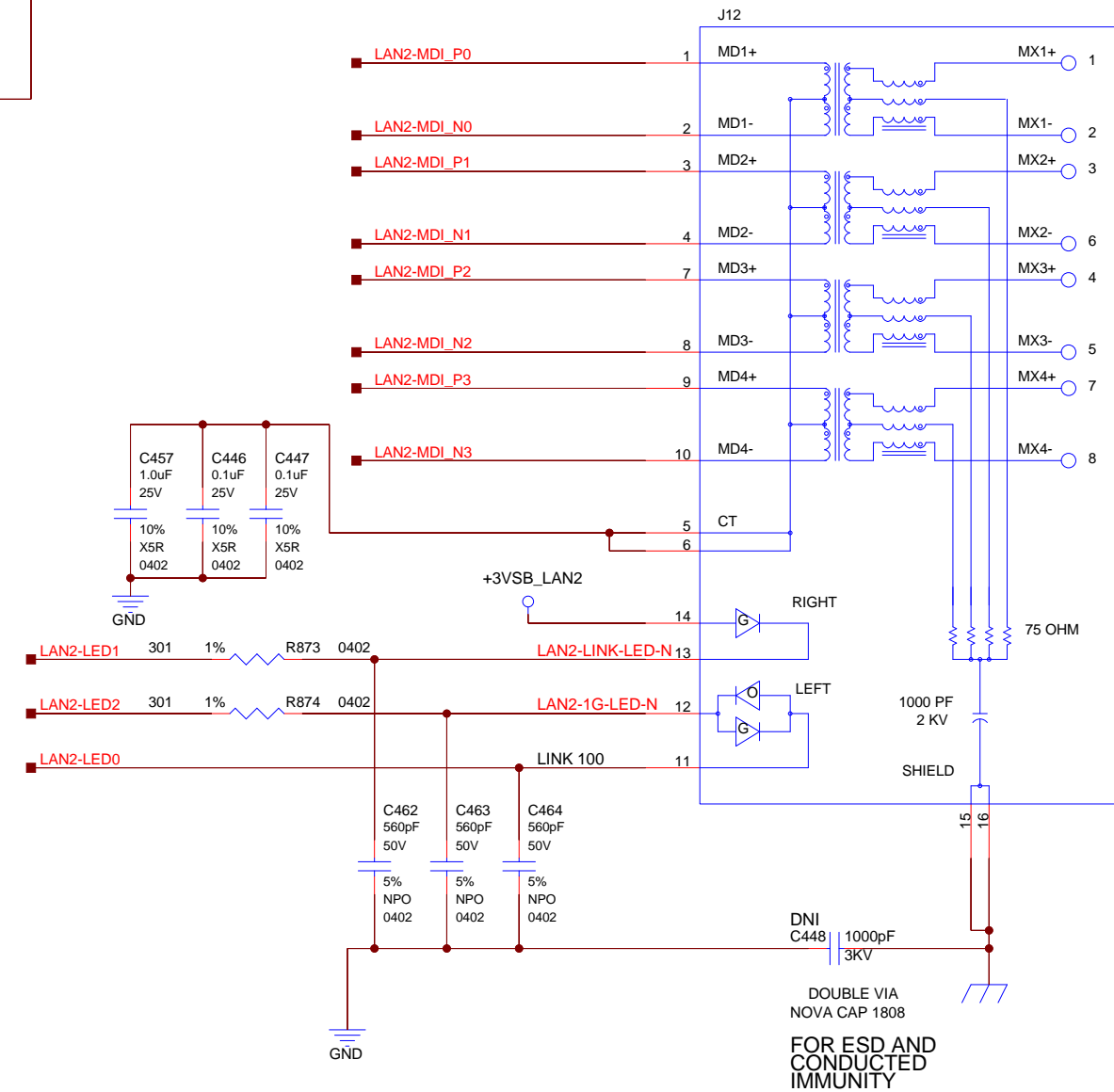
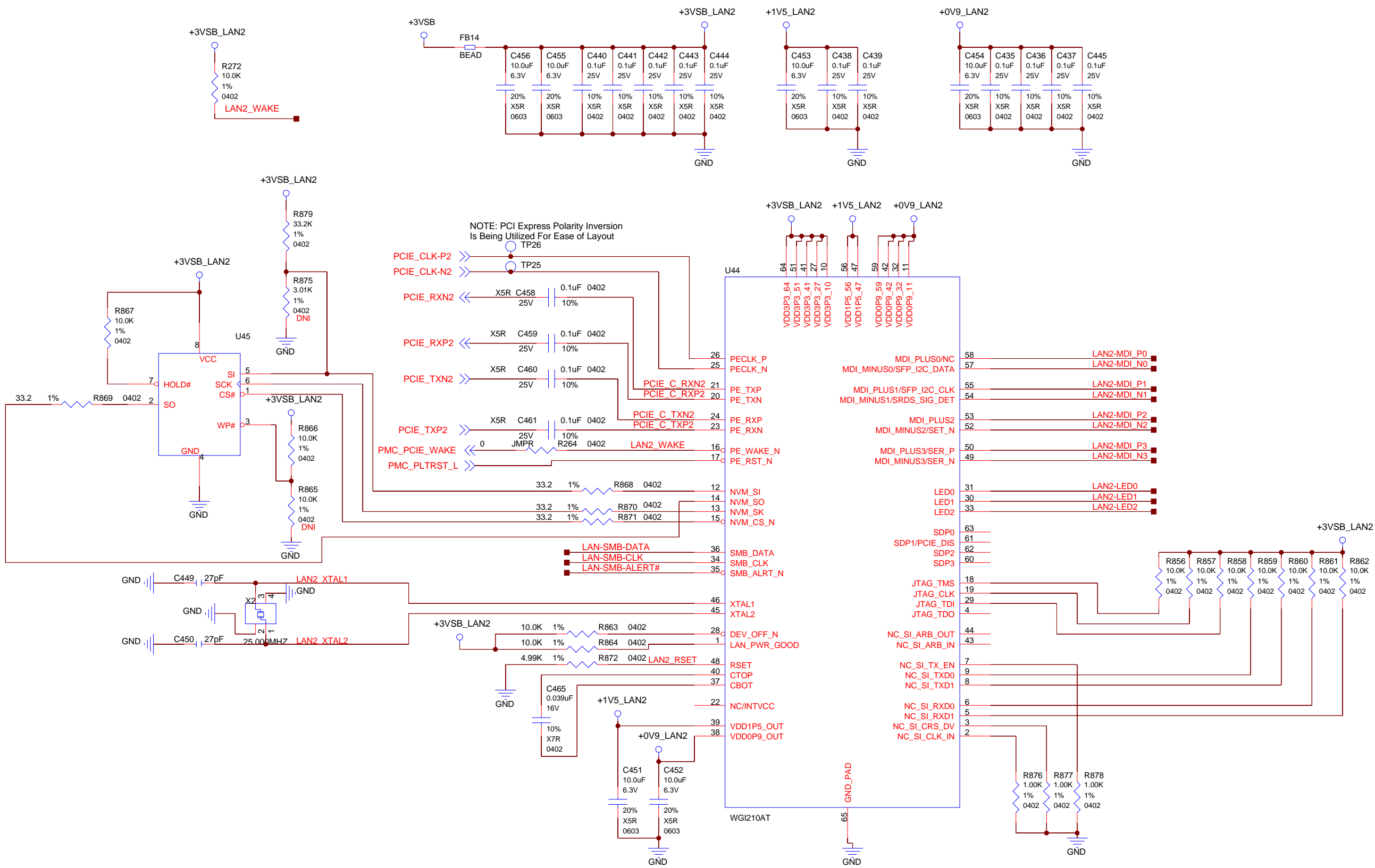
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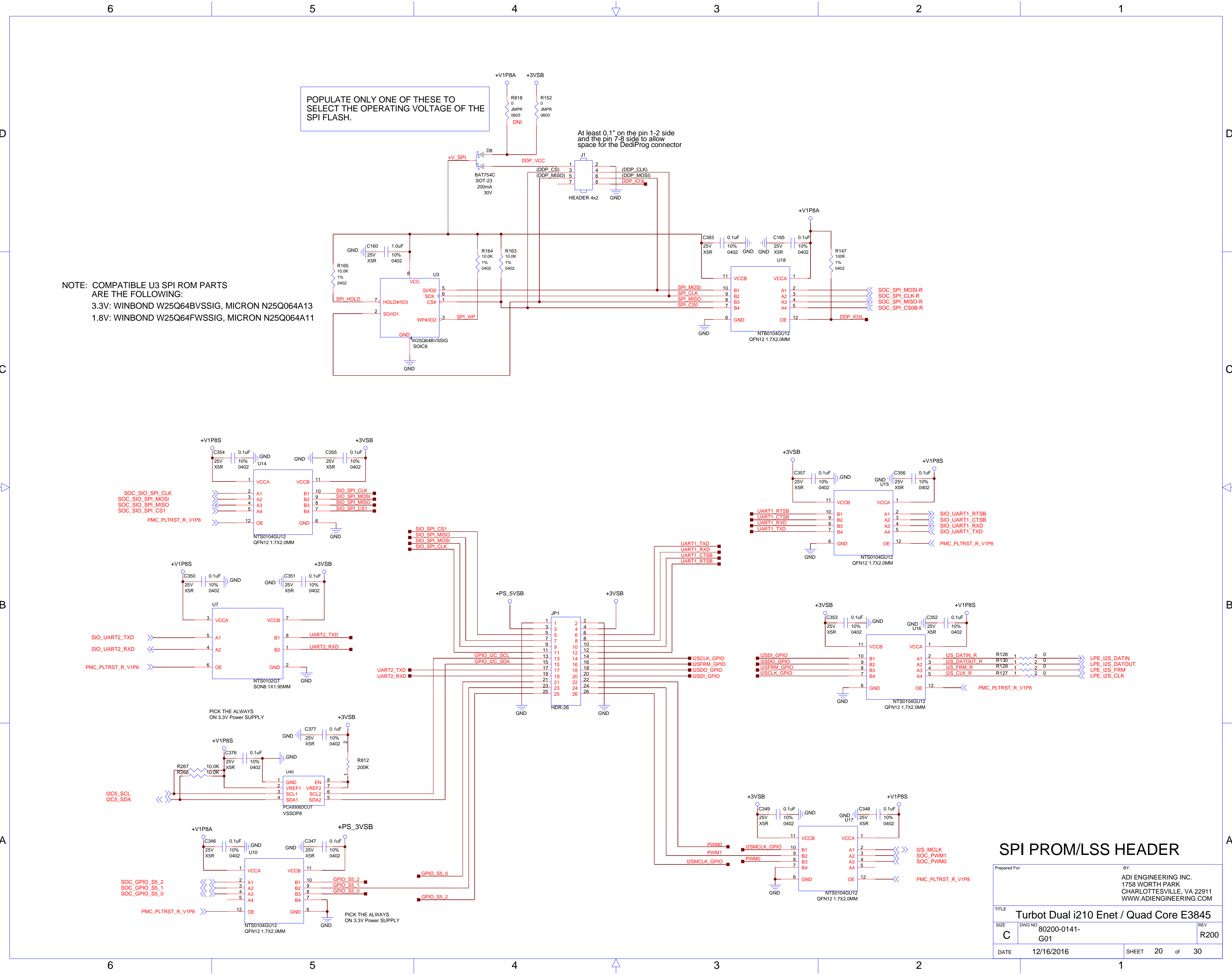
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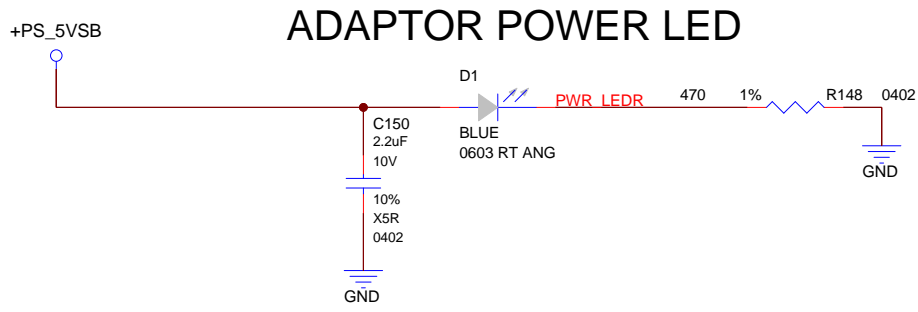
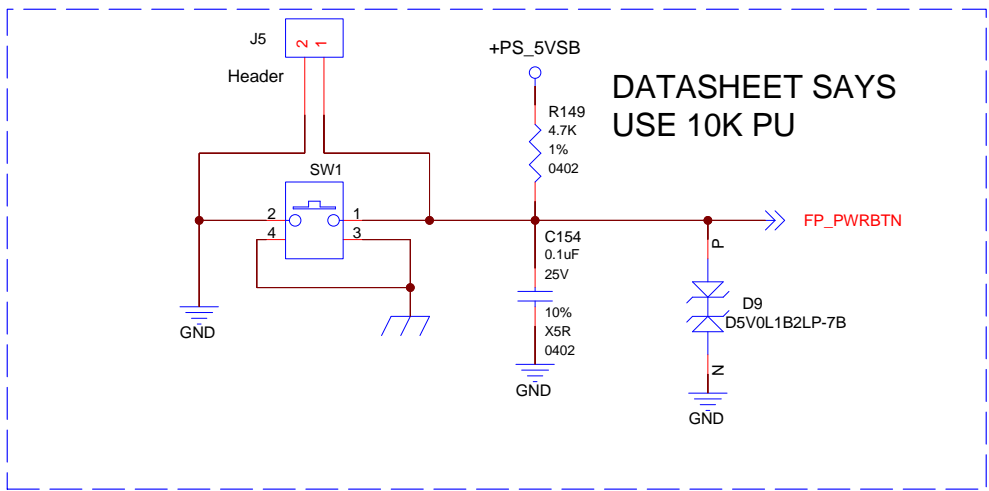
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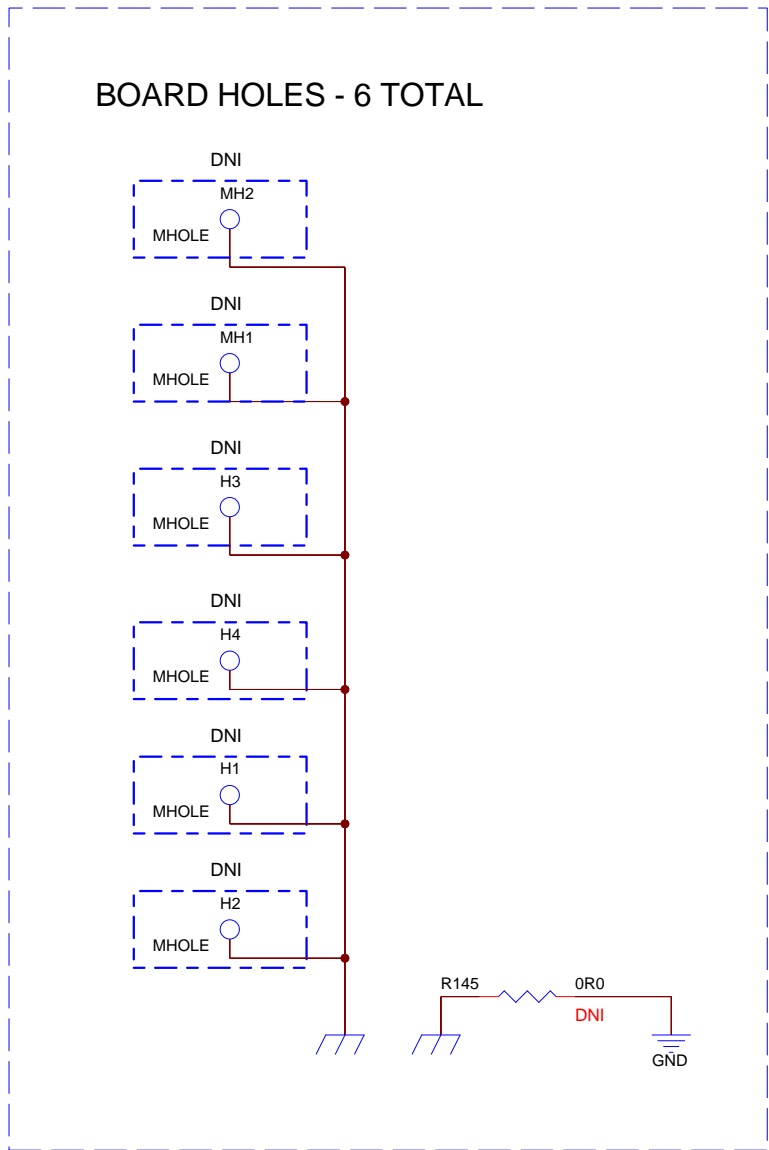
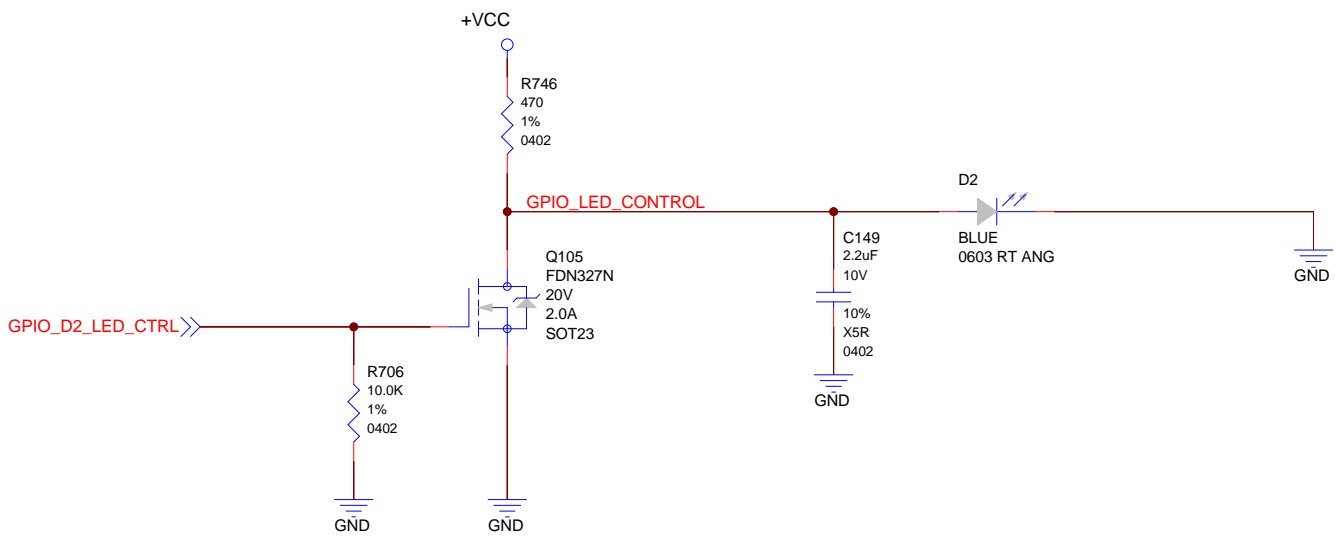
LAN #2 i210/i211

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C	80200-0141-G01	R200	
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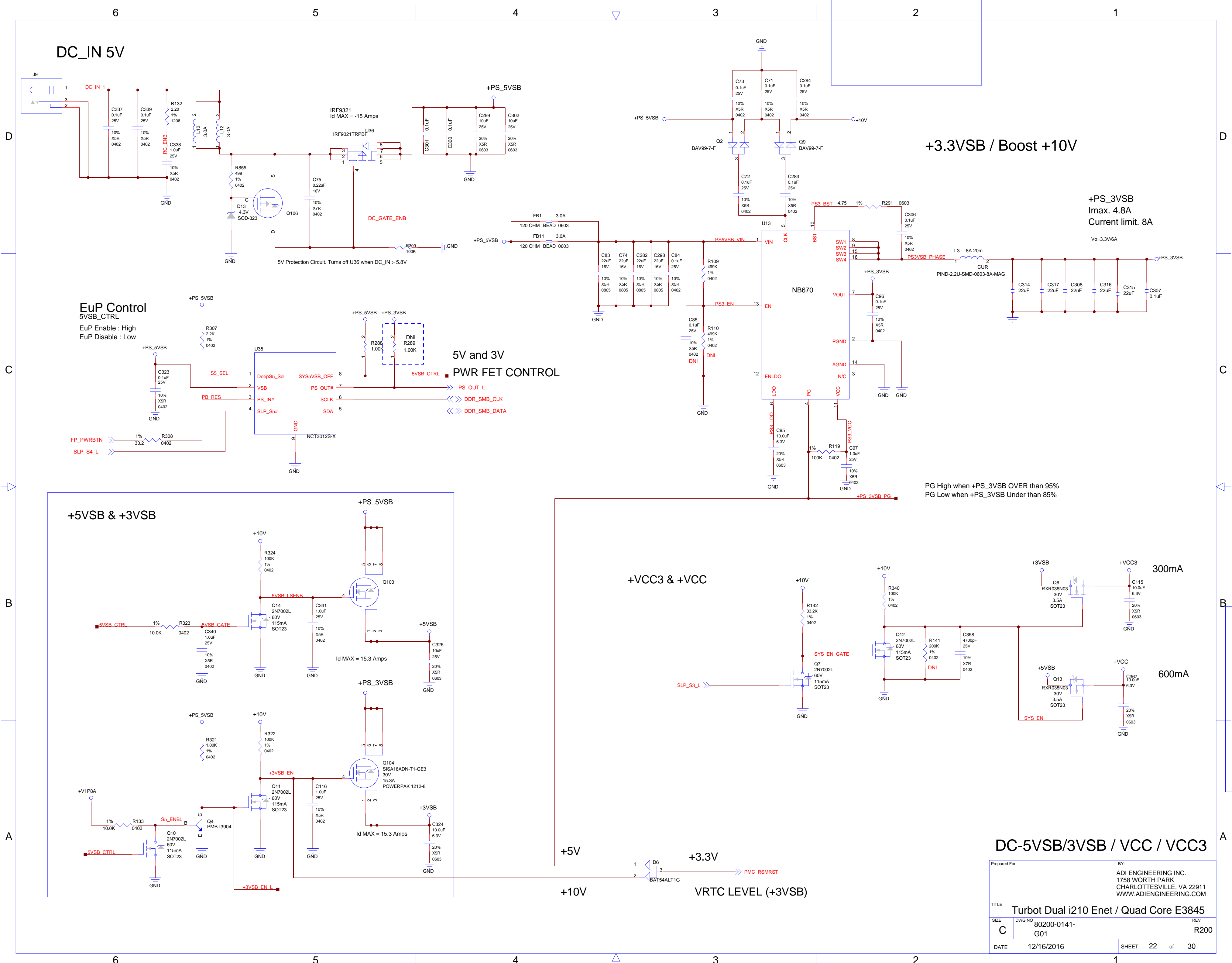


SYSTEM POWER LED - GPIO CONTROLLED



PWR BTN / LED / HOLES

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SIZE	DWG NO	REV	
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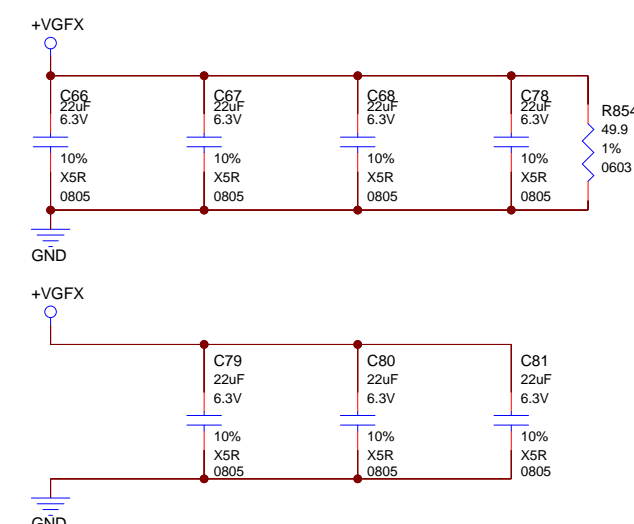
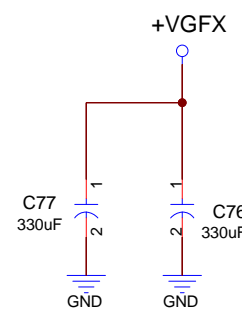
+3.3VSB / Boost +10V

+PS_3VSB
Imax. 4.8A
Current limit. 8A
V_{ov}=3.3V/6A

PG High when +PS_3VSB OVER than 95%
PG Low when +PS_3VSB Under than 85%

DC-5VSB/3VSB / VCC / VCC3

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DATE 12/16/2016		SHEET 24 of 30	

6

5

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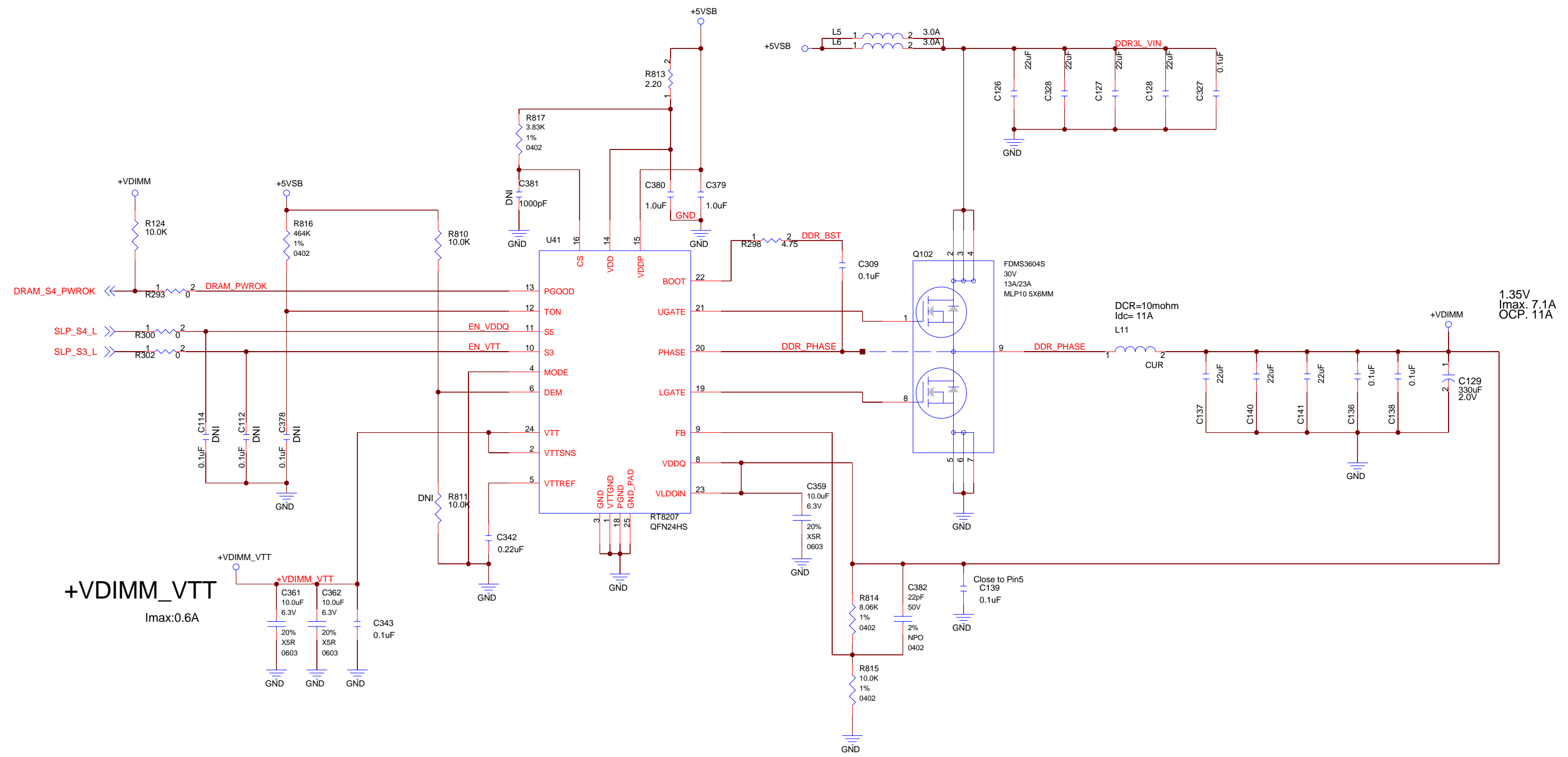
VDIMM

$F = (V_{in} - 0.5) / 3.85p \cdot V_{in} \cdot R_{ton}$
 $R_{ton} = 806K, F = 285KHz$

on

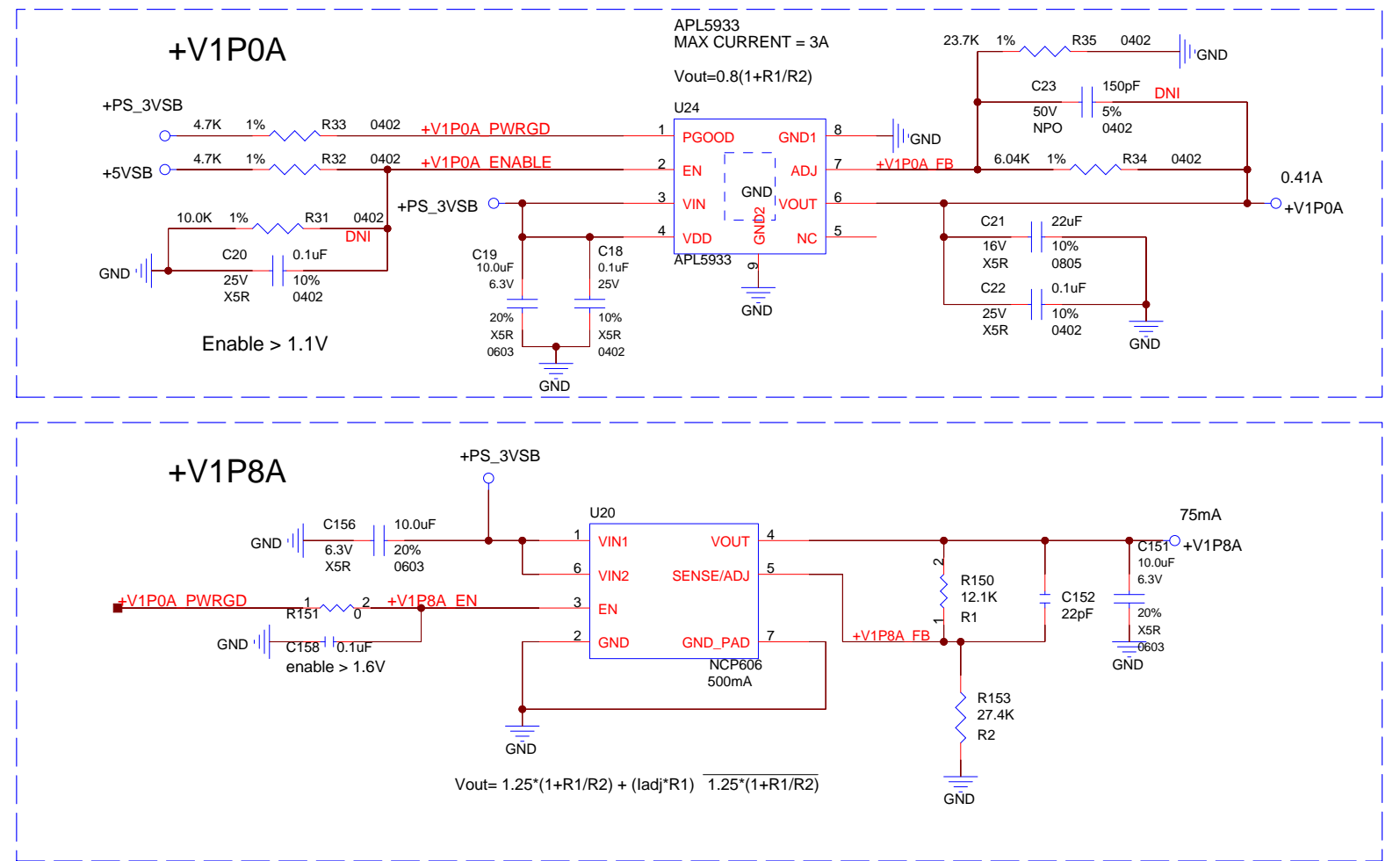
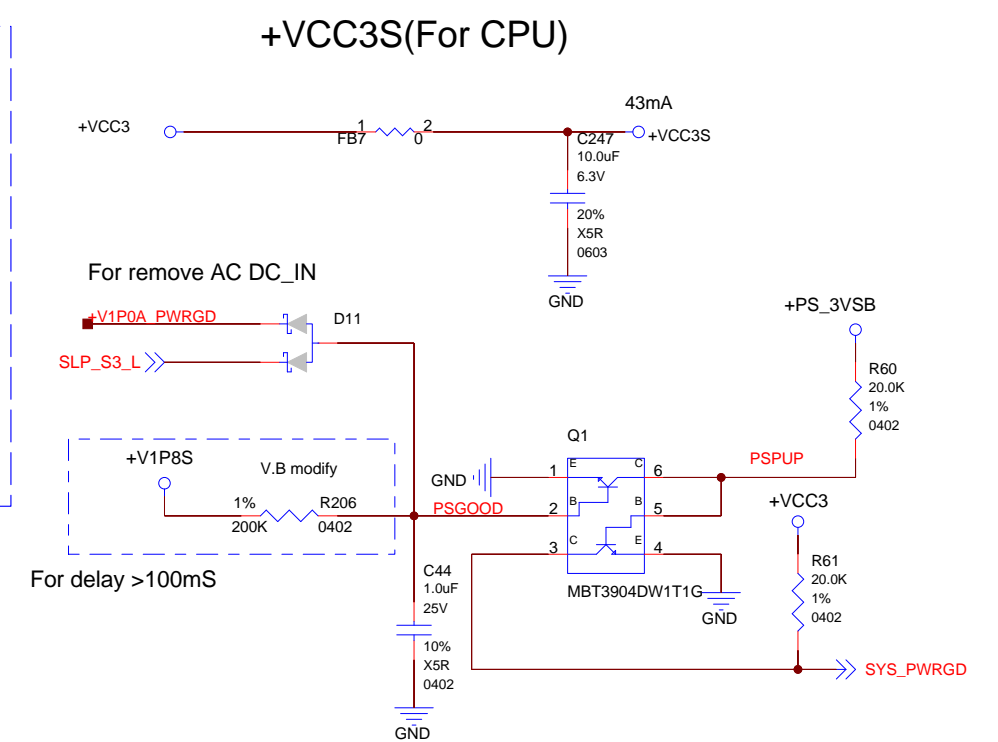
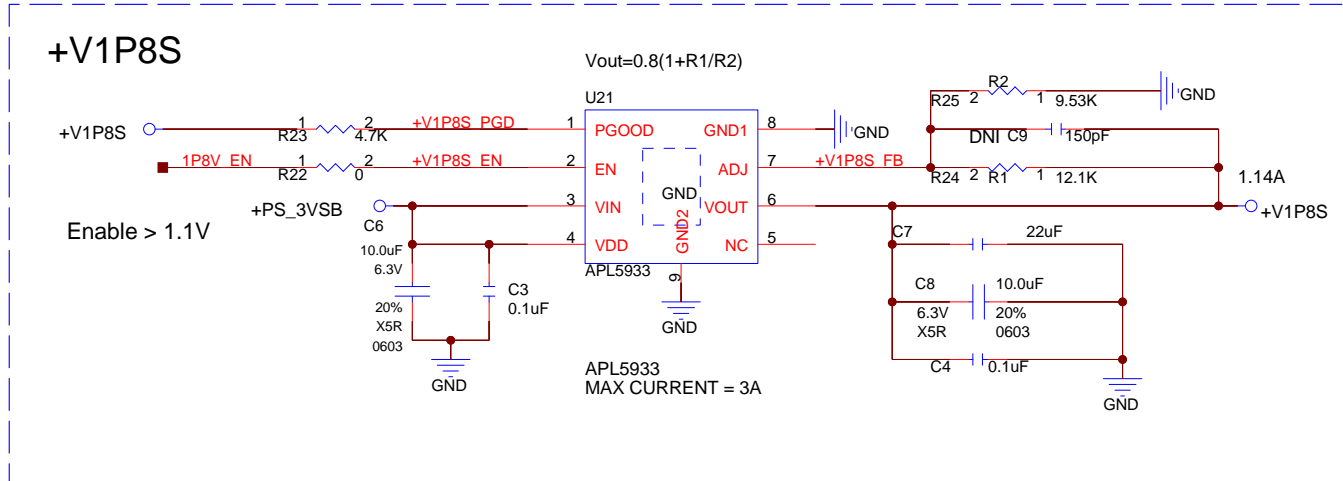
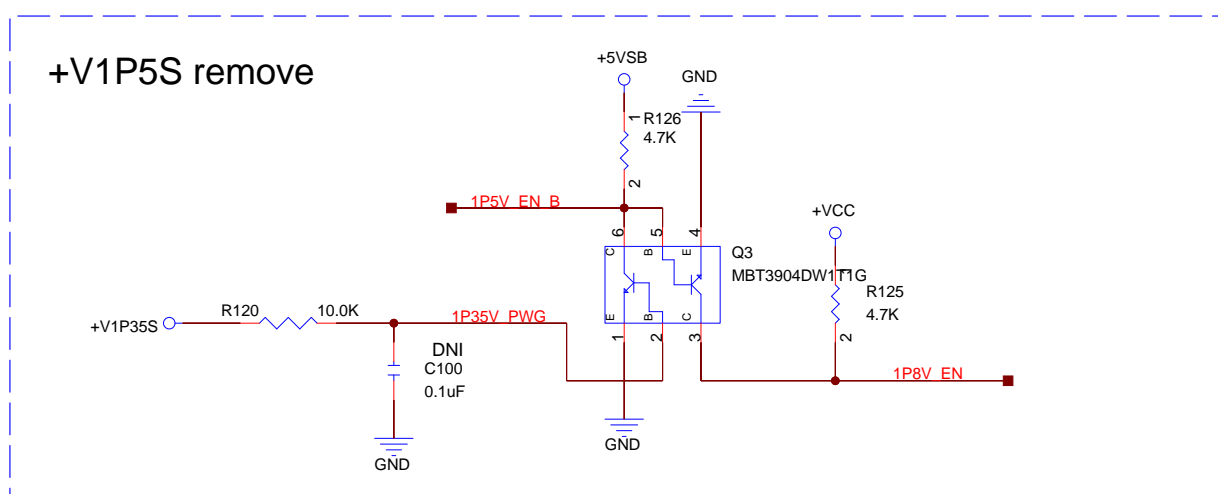
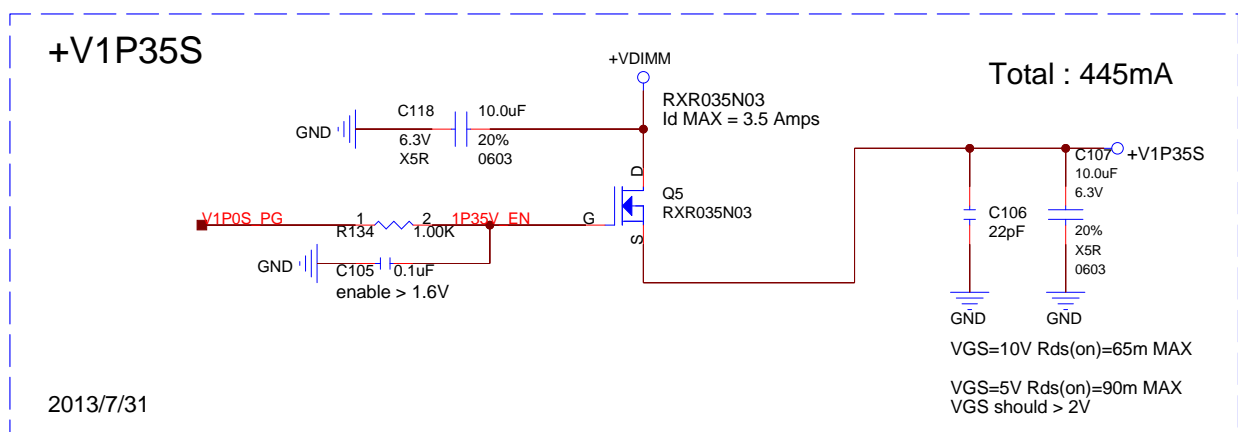
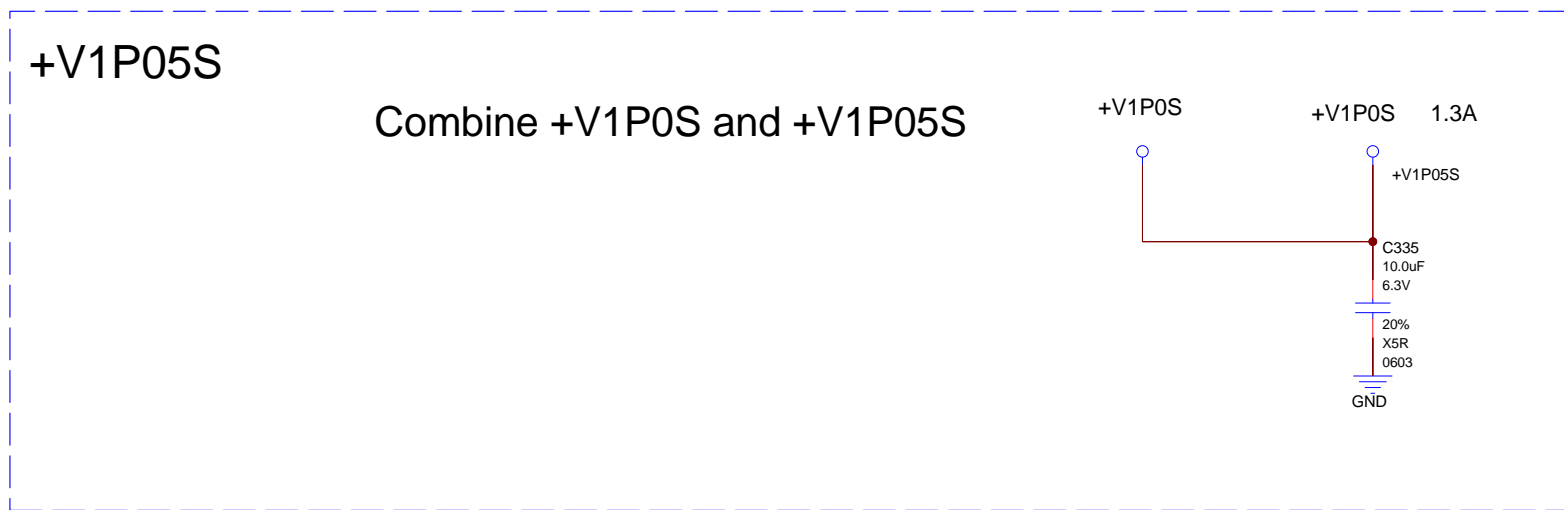
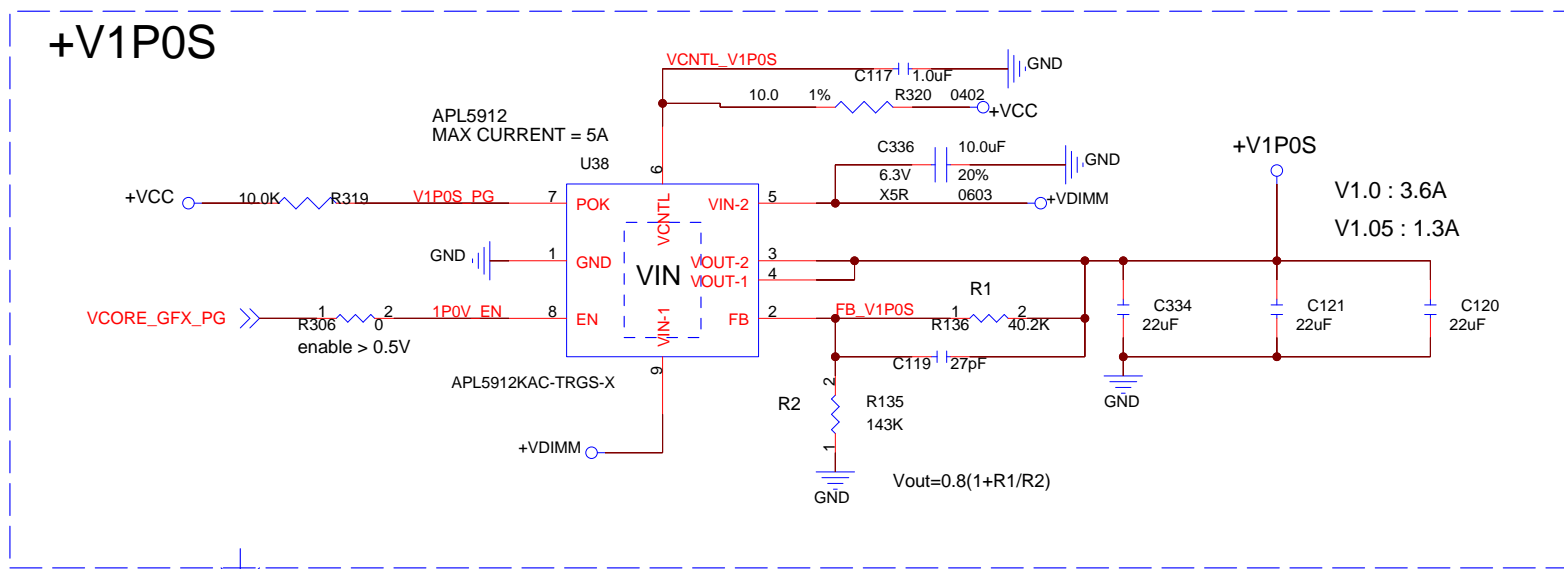
STATE	S3/S5/VDDQ	VTTREF/VTT
S0	Hi/Hi	on
S3	Lo/Hi	on
S4/S5	Lo/Lo	Off

Off Discharge



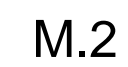
DC/DC-DIMM/DDR_VTT

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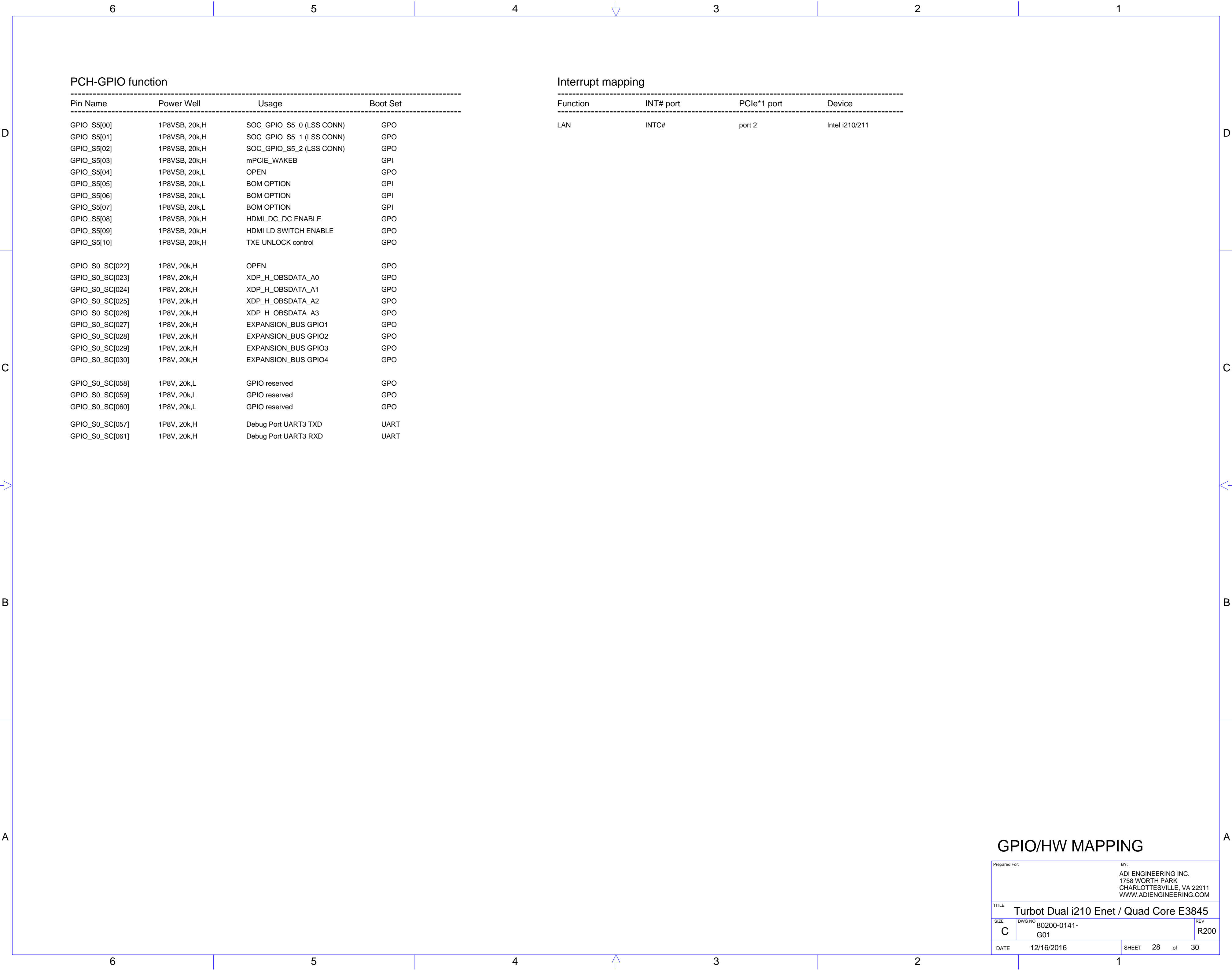


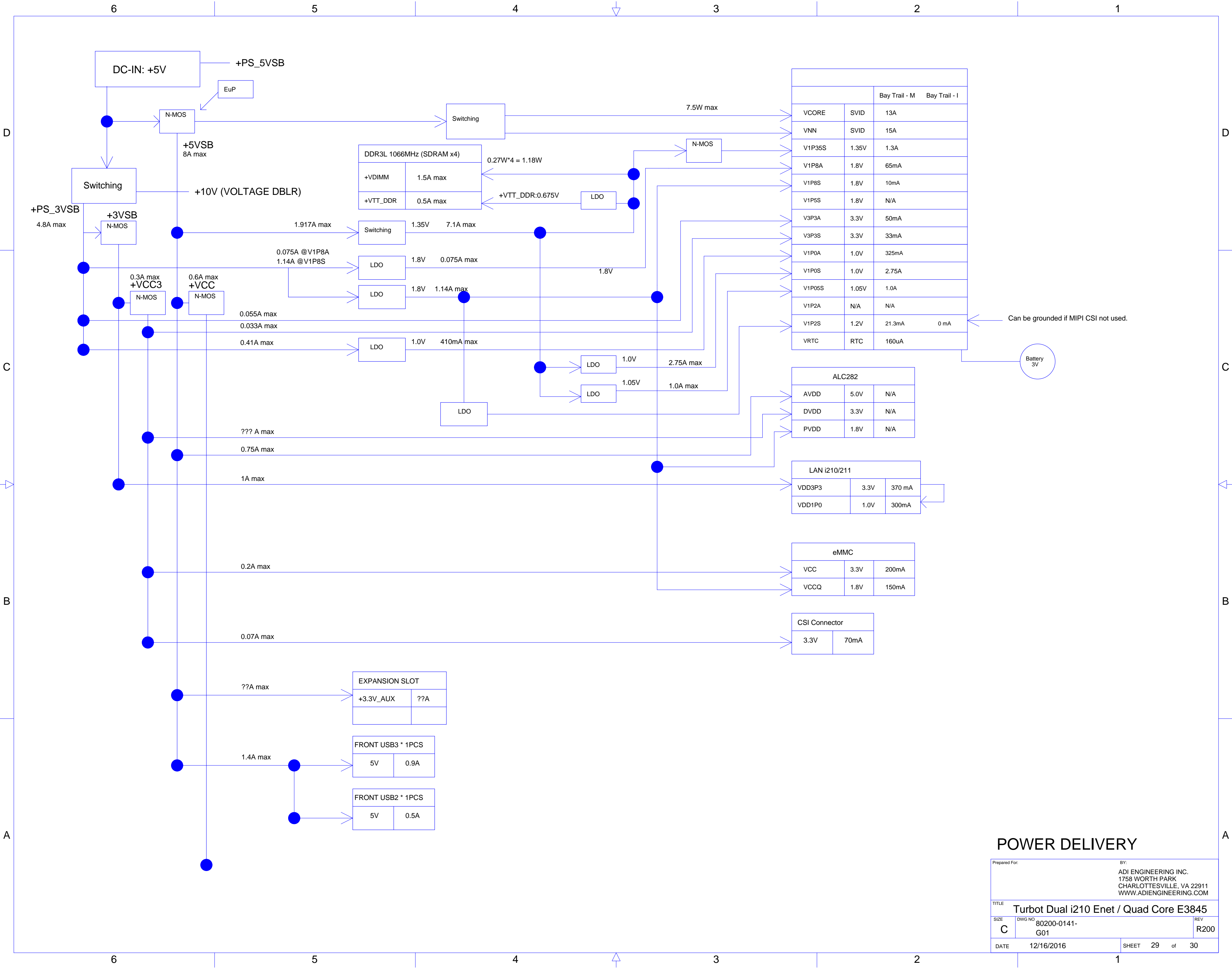
DC-DC VOLTAGE

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POWER DELIVERY

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Turbot Dual i210 Enet / Quad Core E3845			
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The diagram illustrates the power management system for the Intel Bay Trail-M/I processor. It shows the flow of power from a +5V DC-IN source through various DC-DC converters and switching regulators to the processor and other components.

Power Management Components:

- +5V DC-IN:** The primary power source.
- Switching (NB670):** A switching regulator that takes +5V DC-IN and outputs +PS_5VSB (pin 1) and +PS_3VSB (pin 2.2).
- EuP NCT3012S:** A power controller that takes +PS_5VSB (pin 1) and +PS_3VSB (pin 2.2) and outputs VSB(2) (pin 2.1) and PS_OUT#(7) (pin 7).
- DC-DC (NMOS):** Multiple DC-DC converters that take +PS_5VSB and +PS_3VSB and output various voltages: +5VSB (pin 5), +V1P0A (pin 6), +V1P8A (pin 7), +3VSB (pin 8), +V1P0S (pin 15), +V1P35S (pin 16), and +V1P8S (pin 17).
- DC-DC (MOS):** A DC-DC converter that takes +PS_3VSB and +3VSB and outputs +VCC (pin 13.1) and +VCC3 (pin 13.2).
- Switching (ISL95837):** A switching regulator that takes +5VSB and +VCC and outputs +VCCORE (pin 14.1), +VGFX (pin 14.2), and +VCCORE_PG (pin 14.3).

Processor and System Components:

- Intel Bay Trail-M/I:** The central processor, showing internal power management blocks and external connections for DRAM, LAN, and expansion modules.
- DRAM:** Connected to the processor via DRAM_VDD_S4_PWROK (AD42) and DRAM_S4_PWROK (pin 11.1).
- LAN i210/211:** A LAN controller connected to the processor via LAN_VDD_S4_PWROK (AD42) and LAN_S4_PWROK (pin 11.1).
- EXPANSION:** An expansion module connected to the processor via EXPANSION_VDD_S4_PWROK (AD42) and EXPANSION_S4_PWROK (pin 11.1).
- M.2:** An M.2 module connected to the processor via M2_VDD_S4_PWROK (AD42) and M2_S4_PWROK (pin 11.1).

Signal Connections:

- RSMRST_L (pin 8.1):** Reset signal for the processor.
- PS_OUT_L (pin 9):** Power status output.
- SLP_S4_L (pin 10):** Sleep signal for S4 state.
- SLP_S3_L (pin 12):** Sleep signal for S3 state.
- PCH_PLTRST_L (pin 19):** Processor control host reset signal.
- ICLK_OSCIN(AH12) and ICLK_OSCOUT(AH10):** Clock signals for the processor.

Prepared For:		BY:	
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TITLE			
Turbot Dual i210 Enet / Quad Core E3845			
SIZE	DWG NO	REV	
C	80200-0141-G01	R200	
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