X20(c)AI4632-1

1 General information

The module is equipped with 4 inputs with 16-bit digital converter resolution. It is possible to select between the current and voltage signal using different terminals.

- 4 analog inputs
- Either current or voltage signal possible
- Extended signal range
- 16-bit digital converter resolution
- Simultaneous input conversion
- Very fast conversion time

2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, method 4, exposure 21 days

3 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI4632-1	X20 analog input module, 4 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	
X20cAI4632-1	X20 analog input module, coated, 4 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20AI4632-1, X20cAI4632-1 - Order data

4 Technical data

Model number	X20AI4632-1	X20cAI4632-1
Short description		
I/O module	4 analog inputs ±11 V or 0 to 22 mA	
General information		
B&R ID code	0xA29D	0xD57A
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Inputs	Yes, using status LED and software	
Channel type	Yes, using software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.5 W [1)]	
Additional power dissipation caused by actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certifications		
CE	Yes	
KC	Yes	-
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see user's manual) FTZÚ 09 ATEX 0083X	
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (Bridge and open deck)	
LR	ENV1	
GOST-R	Yes	
Analog inputs		
Input	±11 V or 0 to 22 mA, via different terminal connections	
Input type	Differential input	
Digital converter resolution		
Voltage	±15-bit	
Current	15-bit	
Conversion time	50 µs for all inputs	
Output format	INT	
Output format		
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 335.693 µV	
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 671.387 nA	
Input impedance in signal range		
Voltage	20 MΩ	
Current	-	
Load		
Voltage	-	
Current	<400 Ω	
Input protection	Protection against wiring with supply voltage	
Permissible input signal		
Voltage	Max. ±30 V	
Current	Max. ±50 mA	
Output of digital value during overload		
Undershoot		
Voltage	0x8001	
Current	0x0000	
Overshoot		
Voltage	0x7FFF	
Current	0x7FFF	
Conversion procedure	SAR	
Input filter	Hardware - 3rd-order low pass / cutoff frequency 10 kHz	

Table 2: X20AI4632-1, X20cAI4632-1 - Technical data

Model number	X20AI4632-1	X20cAI4632-1
Max. error at 25°C		
Voltage		
Gain	0.08% 2)	
Offset	0.01% 3)	
Current		
Gain	0.08% 2)	
Offset	0.02% 4)	
Max. gain drift		
Voltage	0.01 %/°C 2)	
Current	0.01 %/°C 2)	
Max. offset drift		
Voltage	0.001 %/°C 3)	
Current	0.002 %/°C 4)	
Common-mode rejection		
DC	70 dB	
50 Hz	70 dB	
Common-mode range	±12 V	
Crosstalk between channels	<-70 dB	
Nonlinearity		
Voltage	<0.01% 3)	
Current	<0.015% 4)	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
Degree of protection per EN 60529	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm	

Table 2: X20AI4632-1, X20cAI4632-1 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Based on the current measured value.
3) Based on the 22 V measurement range.
4) Based on the 22 mA measurement range.

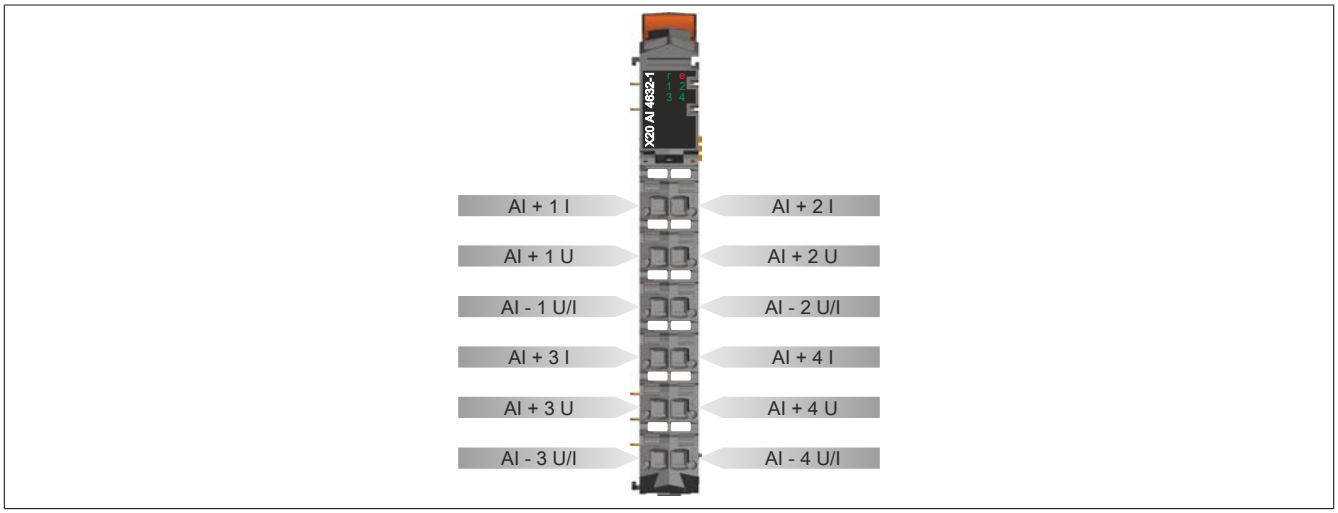
5 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" of the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the scan time • Synchronization error
	1 - 4	Green	Off	Open line[2] or sensor is disconnected
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

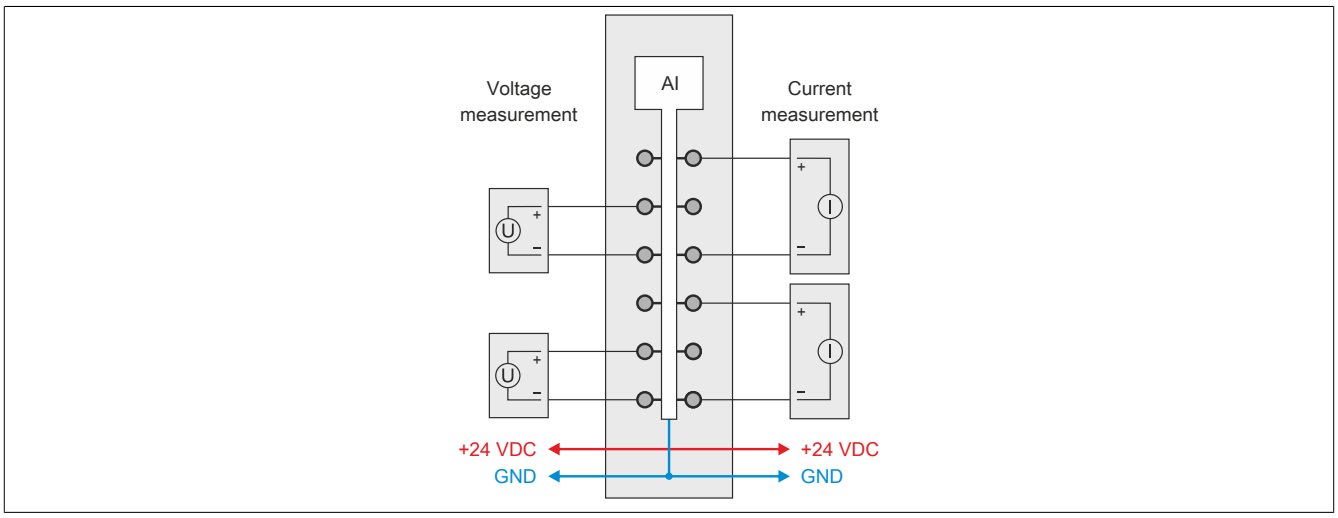
6 Pinout



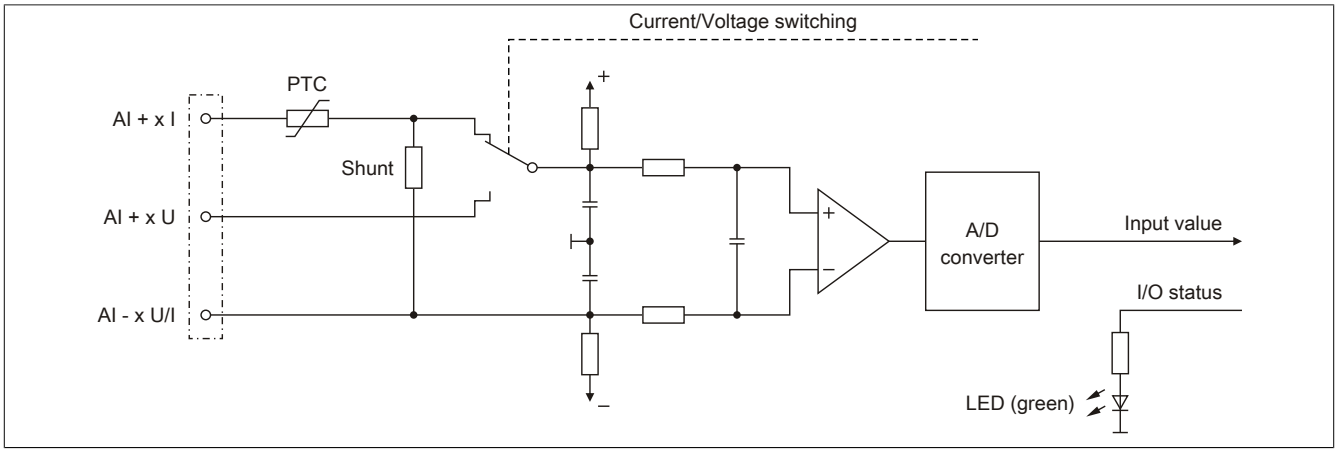
7 Connection example

To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Supply module X20PS9500/X20PS9502
- CPU modules



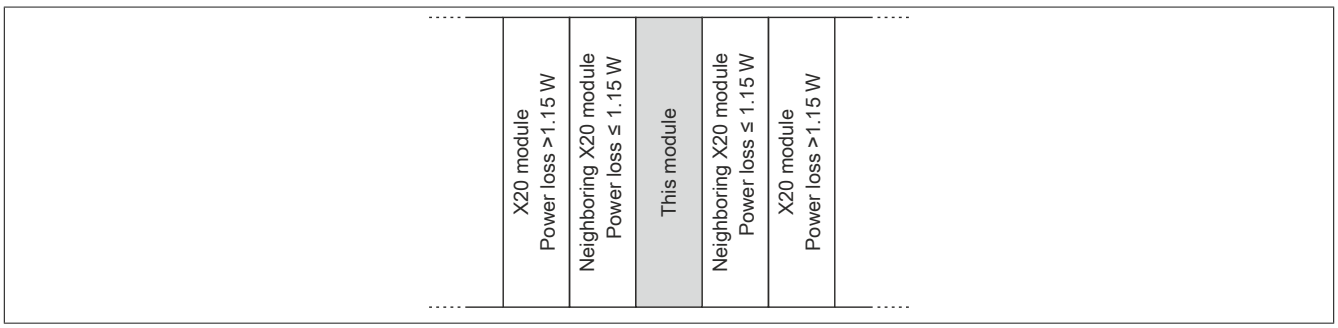
8 Input circuit diagram



9 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



10 Register description

10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

General data points are described in section "Additional information - General data points" of the X20 system user's manual.

10.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size						
-	AsynSize	-				
Configuration						
257 289 321 353	ConfigOutput01 (channel configuration) ConfigOutput06 ConfigOutput11 ConfigOutput16	USINT				•
	Sampling time					
390	ConfigOutput24 (sampling time)	UINT				•
	Filtering					
259 291 323 355	ConfigOutput26 (order for low-pass filter) ConfigOutput28 ConfigOutput30 ConfigOutput32	USINT				•
262 294 326 358	ConfigOutput27 (cutoff frequency of low-pass filter) ConfigOutput29 ConfigOutput31 ConfigOutput33	UINT				•
	Scaling					
276 308 340 372	ConfigOutput04 (user-defined gain) ConfigOutput09 ConfigOutput14 ConfigOutput19	DINT				•
284 316 348 380	ConfigOutput05 (user-defined offset) ConfigOutput10 ConfigOutput15 ConfigOutput20	DINT				•
	User-defined limit values					
266 298 330 362	ConfigOutput02 (minimum limit value) ConfigOutput07 ConfigOutput12 ConfigOutput17	UINT				•
270 302 334 366	ConfigOutput03 (maximum limit value) ConfigOutput08 ConfigOutput13 ConfigOutput18	UINT				•
Communication						
0 + (N-1) * 4	AnalogInput0N (index N = 1 to 4	INT	•			
650	SampleCycleCounter	UINT		•		
	Error monitoring and counters					
641	Channel status	USINT	•			
	Channel01OK	Bit 0				
	...	...				
	Channel04OK	Bit 3				
	SyncStatus	Bit 6				
	ConvertionCycle	Bit 7				
654	SampleCycleViolationErrorCounter	UINT		•		
658	Synchronization error counter	UINT		•		
2097	Range violation (neg. and pos.)	USINT	•			
	Channel01underflow	Bit 0				
	Channel01overflow	Bit 1				
	...	...				
	Channel04underflow	Bit 6				
	Channel04overflow	Bit 7				
2099	Working range violation (pos.)	USINT	•			
	Channel01OutofRange	Bit 0				
	...	...				
	Channel04OutofRange	Bit 3				
518 + (N-1) * 32	Ch0NOverflow (index N = 1 to 4)	UINT		•		
522 + (N-1) * 32	Ch0NUnderflow (index N = 1 to 4)	UINT		•		

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
526 + (N-1) * 32	Ch0NOutofRange (index N = 1 to 4)	UINT		•		
Additional analysis functions						
133	ConfigOutput21 (trigger reaction on falling edge)	USINT				•
135	ConfigOutput22 (trigger reaction on rising edge)	USINT				•
129	Analysis control byte	USINT			•	
	TraceTrigger01	Bit 0				
	MinMaxStart01	Bit 4				
	...	...				
	MinMaxStart04	Bit 7				
129	Analysis status byte	USINT	•			
	MinMaxStart01Readback	Bit 4				
	...	...				
	MinMaxStart04Readback	Bit 7				
	Limit values					
530 + (N-1) * 32	MinInput0N (index N = 1 to 4)	INT	•			
534 + (N-1) * 32	MaxInput0N (index N = 1 to 4)	INT	•			
538 + (N-1) * 32	Ch0NMinMaxLatchCounter (index N = 1 to 4)	UINT		•		
	Trace configuration					
1026	TraceChannelEnable	USINT				•
1030	TraceSampleDepth	UINT				•
4157	ConfigOutput25 (trace priority)	USINT				•
1037	Starting a recording	USINT			•	
	TraceEnable01	Bit 0				
1089	Recording status	USINT	•			
	TraceEnabled	Bit 0				
	TraceWriteActive	Bit 2				
	TraceReadActive	Bit 3				
	ReadyForTrigger	Bit 4				
	TriggerActive	Bit 5				
	TraceOK	Bit 6				
	TraceError	Bit 7				
1094	FreeBufferSize	UINT	•			
1098	TriggerCount	UINT	•			
1102	TriggerFailCount	UINT	•			
	Comparator					
450 + (N-1) * 8	cfgComp_LowLimitCh0N (index N = 1 to 4)	INT			(•)	•
454 + (N-1) * 8	cfgComp_HighLimitCh0N (index N = 1 to 4)	INT			(•)	•
662	CompStateCollection	UINT	•			
490	cfgComp_NominalState	UINT				•
482	cfgComp_EnableMask	UINT				•
486	cfgComp_ConditionTypeMask	UINT				•
	Time-offset trace					
1042	TraceTriggerStart	INT				•
1046	TraceTriggerStop	UINT				•

10.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size							
-	-	AsynSize	-				
Configuration							
257 289 321 353	-	ConfigOutput01 (channel configuration) ConfigOutput06 ConfigOutput11 ConfigOutput16	USINT				•
	Sampling time						
390	-	ConfigOutput24 (sampling time)	UINT				•
	Filtering						
259 291 323 355	-	ConfigOutput26 (order for low-pass filter) ConfigOutput28 ConfigOutput30 ConfigOutput32	USINT				•
262 294 326 358	-	ConfigOutput27 (cutoff frequency of low-pass filter) ConfigOutput29 ConfigOutput31 ConfigOutput33	UINT				•
	Scaling						
276 308 340 372	-	ConfigOutput04 (user-defined gain) ConfigOutput09 ConfigOutput14 ConfigOutput19	DINT				•
284 316 348 380	-	ConfigOutput05 (user-defined offset) ConfigOutput10 ConfigOutput15 ConfigOutput20	DINT				•
	User-defined limit values						
266 298 330 362	-	ConfigOutput02 (minimum limit value) ConfigOutput07 ConfigOutput12 ConfigOutput17	UINT				•
270 302 334 366	-	ConfigOutput03 (maximum limit value) ConfigOutput08 ConfigOutput13 ConfigOutput18	UINT				•
Communication							
0 + (N-1) * 4	0 + (N-1) * 2	AnalogInput0N (index N = 1 to 4)	INT	•			
650	-	SampleCycleCounter	UINT		•		
	Error monitoring and counters						
641	-	Channel status	USINT		•		
		Channel01OK	Bit 0				
		...	...				
		Channel04OK	Bit 3				
		SyncStatus	Bit 6				
		ConvertionCycle	Bit 7				
654	-	SampleCycleViolationErrorCounter	UINT		•		
658	-	Synchronization error counter	UINT		•		
2097	-	Range violation (neg. and pos.)	USINT		•		
		Channel01underflow	Bit 0				
		Channel01overflow	Bit 1				
		...	...				
		Channel04underflow	Bit 6				
		Channel04overflow	Bit 7				
2099	-	Working range violation (pos.)	USINT		•		
		Channel01OutofRange	Bit 0				
		...	...				
		Channel04OutofRange	Bit 3				
518 + (N-1) * 32	-	Ch0NOverflow (index N = 1 to 4)	UINT		•		
522 + (N-1) * 32	-	Ch0NUnderflow (index N = 1 to 4)	UINT		•		
526 + (N-1) * 32	-	Ch0NOutofRange (index N = 1 to 4)	UINT		•		
Additional analysis functions							
133	-	ConfigOutput21 (trigger reaction on falling edge)	USINT				•
135	-	ConfigOutput22 (trigger reaction on rising edge)	USINT				•
129	-	Analysis control byte	USINT				•
		MinMaxStart01	Bit 4				
		...	...				
		MinMaxStart04	Bit 7				

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
129	-	Analysis status byte	USINT		•		
		MinMaxStart01Readback	Bit 4				
		...	...				
		MinMaxStart04Readback	Bit 7				
	Limit values						
530 + (N-1) * 32	-	MinInput0N (index N = 1 to 4)	INT		•		
534 + (N-1) * 32	-	MaxInput0N (index N = 1 to 4)	INT		•		
538 + (N-1) * 32	-	Ch0NMinMaxLatchCounter (index N = 1 to 4)	UINT		•		

1) The offset specifies the position of the register within the CAN object.

10.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

10.4 Configuration

This module is equipped with analog inputs with connected 16-bit A/D converters. Each of the inputs can be configured separately from one another either on the voltage or current input for the following areas:

- Permitted voltage: ±11 V at 20 Ω
- Permitted current: 22 mA (maximum 40 mA) (<400 Ω)

10.4.1 Channel configuration

Name:
ConfigOutput01 for channel 01
ConfigOutput06 for channel 02
ConfigOutput11 for channel 03
ConfigOutput16 for channel 04

The individual inputs for processing the current or voltage signal are configured in these registers. This configuration must be made in addition to using suitable terminals.

Filtering, analysis and error monitoring (bits 4 to 6) can only be used if the channel is enabled (bit 7 = 0).

Data type	Values	Bus controller default setting
USINT	See bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Terminal selector	0	Voltage terminal for ±11 VDC (bus controller default setting)
		1	Current terminal for 0 to 22 mA
1	Gain selector	0	Voltage ±11 VDC (bus controller default setting)
		1	Current 0 to 22 mA
2 - 3	Reserved	-	
4	Filtering active (only if bit 7 = 0)	0	Inactive (bus controller default setting)
		1	Active
5	Minimum/Maximum analysis active (only if bit 7 = 0)	0	Inactive (bus controller default setting)
		1	Active
6	Error monitoring active (only if bit 7 = 0)	0	Inactive (bus controller default setting)
		1	Active
7	Enables channel	0	Channel enabled (bus controller default setting)
		1	Channel disabled

10.4.2 Sampling and conversion

The analog signal is sampled in 2 steps.

- **Conversion task**
  The A/D converter digitalizes the inputs signals for the enabled inputs once per conversion cycle. Then the results are available internally in the module. To ensure that this process is executed without delays, the corresponding task will be handled with very high priority.
  The timespan needed for conversion results from the set sampling time.
- **Processing task**
  The converted A/D converter values are further processed according to the user settings (filtering, scaling, limit values, error statistics, min/max analysis, hysteresis comparison). The task for this process has low priority. The timespan needed for further processing depends on the configured functions and is the second portion of the sampling time.

Cycle time violation

In normal operation, further processing is triggered after each conversion. The conversion and sampling tasks run synchronous to one another. If the predefined sampling time is not sufficient to convert all enabled channels and complete the configured functions, a cycle time violation occurs.

10.4.2.1 Sampling time

Name:
ConfigOutput24

The sampling time is set to µs in this register. This makes it possible to improve the sampling cycle (resolution = 1 µs). The lowest configurable cycle time is 50 µs.

Data type	Value	Information
UINT	50 to 10,000	Bus controller default setting: 100

Information:

Values that are too low for the cycle time will result in cycle time violations.

10.4.3 Filtering (optional)

If filtering is enabled in the "Channel configuration" on page 9 register, the basic data of the A/D converter is filtered per channel. The following registers are available to specify the filter order and respective cutoff frequency for configuring the low-pass filter:

- "Filter order" on page 11
- "Filter cutoff frequency" on page 11

10.4.3.1 Filter order

Name:
ConfigOutput26 for channel 1
ConfigOutput28 for channel 2
ConfigOutput30 for channel 3
ConfigOutput32 for channel 4

The filter order is specified in this register. The "Filter cutoff frequency" on page 11 register is used to configure the respective cutoff frequency of the filter.

Data type	Value	Information
USINT	1 to 4	Bus controller default setting: 0

Internal filter orders greater than 1 are implemented as cascaded first-order filters. Since the filter is calculated in the sampling cycle, the filter characteristics are directly related to the settings for the sampling cycle time.

Calculating the cutoff frequency of an nth-order filter:

yn = a * xn + b * y(n-1)

Approximate calculation

a = Sampling time / (Sampling time + 1/Cutoff frequency)

b = 1 - a

10.4.3.2 Filter cutoff frequency

Name:
ConfigOutput27 for channel 1
ConfigOutput29 for channel 2
ConfigOutput31 for channel 3
ConfigOutput33 for channel 4

The cutoff frequency of the respective filter is configured in these registers.

Data type	Value	Information
UINT	1 to 65,535	Cutoff frequency in hertz. Bus controller default setting: 0

Information:

The highest cutoff frequency is limited by the Nyquist Shannon sampling theorem (based on the sampling cycle time). The system does not check for violations of this sampling theorem.

10.4.4 User-defined scaling

The raw and filtered A/D converter data is compared and normalized (gain = k, offset = d). In addition, user-defined normalization is available using the following registers:

- "User-defined gain" on page 12 (= ku)
- "User-defined offset" on page 12 (= du)

The execution time is optimized by grouping the factors together.

System scaling calculation:

nom = k * RawValue + d

k = k * ku

d = k * d + du

The value has to be limited since it can exceed the 16-bit constraints. To provide the greatest degree of flexibility, limiting is possible using the registers "Minimum limit value" on page 13 and "Maximum limit value" on page 13.

10.4.4.1 User-defined gain

Name:
ConfigOutput04 for channel 1
ConfigOutput09 for channel 2
ConfigOutput14 for channel 3
ConfigOutput19 for channel 4

The user-defined gain for the A/D converter data of the respective physical channel can be specified in these registers.

The value 65,536 (0x10000) corresponds to a gain of 1.

Data type	Values	Information
DINT	-2,147,483,648 to 2,147,483,647	Bus controller default setting: 65,536

10.4.4.2 User-defined offset

Name:
ConfigOutput05 for channel 1
ConfigOutput10 for channel 2
ConfigOutput15 for channel 3
ConfigOutput20 for channel 4

The user-defined offset for the A/D converter data of the respective physical channel can be specified in this register.

The value 65,536 (0x10000) corresponds to an offset of 1.

Data type	Values	Information
DINT	-2,147,483,648 to 2,147,483,647	Bus controller default setting: 0

10.4.5 Limit values

If the application requires a limitation of the range of values, then the user can define his own limit values. These values will also be use for the module's error statistics. The following registers are available for this:

- "Minimum limit value" on page 13
- "Maximum limit value" on page 13

Information:

32-bit numbers are used inside the module. A limit value violation can therefore also be determined if the permitted range of values was defined from -32768 to 32767.

10.4.5.1 Minimum limit value

Name:
ConfigOutput02 for channel 1
ConfigOutput07 for channel 2
ConfigOutput12 for channel 3
ConfigOutput17 for channel 4

The minimum limit value is configured in this register. This limit value is also used as the lower value in the error statistics (see register "CH0xUnderflow" on page 16).

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: -32768

10.4.5.2 Maximum limit value

Name:
ConfigOutput03 for channel 1
ConfigOutput08 for channel 2
ConfigOutput13 for channel 3
ConfigOutput18 for channel 4

The maximum limit value is configured in this register. This limit value is also used as the upper value in the error statistics (see register "CH0xOverflow" on page 16).

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: 32767

10.5 Communication - General

The module's analog inputs convert current and voltage values with 16-bit resolution. This information can be used by the application with the help of the registers listed here.

10.5.1 Analog input channels

Name:
AnalogInput01 to AnalogInput04

The analog input value is mapped in this register depending on the configured operating mode.

Data type	Value	Input signal:
INT	-32,768 to 32,767	Voltage signal ±11 VDC
	0 to 32,767	Current signal 0 to 22 mA

10.5.2 Sampling cycle counter

Name:
SampleCycleCounter

The number of times the input signal has been sampled is provided in this register.

Data type	Values
UINT	0 to 65,535

10.5.3 Error monitoring and counters

10.5.3.1 Channel status

Name:
Channel01OK to Channel04OK
SyncStatus
ConvertionCycle

This register collects error messages synchronously with the network cycle. Temporary error states that were registered in a conversion cycle remain active for at least 2 network cycles. In order to receive detailed error information, the corresponding error counters and X2X network events should also be observed.

Data type	Values
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OK	0	OK
		1	Errors • Range overshot • Range undershot • Working range overshot
...		...	
3	Channel04OK	0	OK
		1	Errors See description for bit 0.
4 - 5	Reserved	-	
6	SyncStatus[1)]	0	OK
		1	Not synchronized
7	ConvertionCycle[2)]	0	OK
		1	Errors

1) Identical to bit 0 of the registers "SynchronizationViolationErrorCounter" on page 14.
2) Identical to bit 0 of the registers "SampleCycleViolationErrorCounter" on page 14.

10.5.3.2 Synchronization error counter

Name:
SynchronizationViolationErrorCounter

This register counts how often the conversion task was triggered more than 5 µs after the next-coming X2X cycle. In this case, the module is considered being no longer synchronized with X2X Link.

The counters in this register follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

10.5.3.3 Counter for faulty sampling cycles

Name:
SampleCycleViolationErrorCounter

This register is used to indicate the number of cycle time violations that have occurred thus far. A cycle time violation occurs if the conversion tasks initiates a sampling task before the last sampling cycle has finished. See "Sampling and conversion" on page 10.

The counters in this register follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

10.5.3.4 Range violation (neg. and pos.)

Name:
Channel01underflow to Channel04underflow
Channel01overflow to Channel04overflow

This register indicates whether a range violation (pos. and/or neg.) of the limit values defined in the registers "Minimum limit value" on page 13 and "Maximum limit value" on page 13 has occurred. The individual bits in this register are identical to the values of the lowest bits in the registers "CH0xUnderflow" on page 16 and "CH0xOverflow" on page 16.

Data type	Values
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01underflow	0	No error
		1	Range exceeded (.neg) on channel 1
...		...	
3	Channel04underflow	0	No error
		1	Range exceeded (.neg) on channel 4
4	Channel01overflow	0	No error
		1	Range exceeded (.pos) on channel 1
...		...	
7	Channel04overflow	0	No error
		1	Range exceeded (.pos) on channel 4

10.5.3.5 Working range violation (pos.)

Name:
Channel01OutofRange to Channel04OutofRange

This register indicates whether the input value exceeds the module's maximum measurement range. The individual bits in this register are identical to the values of the lowest bits in the register "CH0xOutofRange" on page 15.

Data type	Values
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OutofRange	0	No error
		1	Working range violation (pos.) of channel 1
...		...	
3	Channel04OutofRange	0	No error
		1	Working range violation (pos.) of channel 4
4 - 7	Reserved	-	

10.5.3.6 Counter for work range violations (pos.)

Name:
CH01OutofRange to CH04OutofRange

Errors outside of the module's maximum possible measurement range are indicated in this register. These errors lead to full-scale deflection of the A/D converter.

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register "Channel configuration" on page 9).

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

10.5.3.7 Counter for range exceeded violations (neg.)

Name:
CH01Underflow to CH04Underflow

This register indicates range exceeded violations (neg.) of the value configured in the register "Minimum limit value" on page 13.

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register "Channel configuration" on page 9).

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

10.5.3.8 Counter for range exceeded violations (pos.)

Name:
CH01Overflow to CH04Overflow

This register indicates range exceeded violations (pos.) of the value configured in the register "Maximum limit value" on page 13.

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register "Channel configuration" on page 9).

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

10.6 Additional analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

- **Limit value analysis**
  If limit value analysis has been enabled for a channel, the sampled minimum and maximum values are latched internally in the module. A measurement period can be triggered using the control byte. When the respective configured edge is generated by the application, the limit values from the previous measurement period are displayed and the internal latch register is reset.
- **Recording sampled values**
  If recording sampled values has been enabled for a channel, then the sampled values are additionally recorded in the module's internal FIFO memory. If the configured event occurs, the contents of the FIFO memory are transmitted to the application.

Information:

It is only possible to use the recording of sampled values if the module is operated on an X2X master that is an SG4 CPU.

10.6.1 Trigger condition on falling edge

Name:
ConfigOutput21

This register configures whether the falling edge is used to trigger the trace and determination of the input value in the register "Analysis control byte" on page 18.

Data type	Values	Bus controller default setting
USINT	See bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	No trigger (bus controller default setting)
		1	Falling edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination (bus controller default setting)
		1	Falling edge determines input value of channel 1
...	...	...	
7	MinMaxStart04	0	No determination (bus controller default setting)
		1	Falling edge determines input value of channel 4

10.6.2 Trigger condition on rising edge

Name:
ConfigOutput22

This register configures whether the rising edge is used to trigger the trace and determination of the input value in the register "Analysis control byte" on page 18.

Data type	Values	Bus controller default setting
USINT	See bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Trigger not initiated on positive edge (bus controller default setting)
		1	Rising edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination (bus controller default setting)
		1	Rising edge determines input value of channel 1
...	...	...	
7	MinMaxStart04	0	No determination (bus controller default setting)
		1	Rising edge determines input value of channel 4

10.6.3 Analysis control byte

Name:
TraceTrigger01
MinMaxStart01 to MinMaxStart04

The trace function and determination of the minimum/maximum input values can be started in this register. Whether the rising and/or falling edge is used to trigger the functions can be configured using the registers "Trigger condition on falling edge" on page 17 and "Trigger condition on rising edge" on page 17.

Data type	Values	Bus controller default setting
USINT	See bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Trigger/Trace not triggered (bus controller default setting)
		1	Initiates trigger/trace
1 - 3	Reserved	-	
4	MinMaxStart01	0	Determination not triggered (bus controller default setting)
		1	Initiates determination of input value of channel 1
...	...	...	
7	MinMaxStart04	0	Determination not triggered (bus controller default setting)
		1	Initiates determination of input value of channel 4

Information:

To reduce the cyclic data transfer, this register combines the trace and limit value determination functions.

10.6.4 Analysis status byte

Name:
MinMaxStart01Readback to MinMaxStart04Readback

The currently requested module-internal analyses can be checked in this register.

Data type	Values
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	MinMaxStart01Readback	0 or 1	Current state of the trigger bits for determining the limit values on the channel
...	...	...	
7	MinMaxStart04Readback	0 or 1	Current state of the trigger bits for determining the limit values on the channel

10.7 Limit values

Limit value analysis must be enabled for the desired channel (see "Channel configuration" on page 9). The sampled value of the channel is then compared to the minimum and maximum values that are stored internally in the module. If a new measurement period is initiated with the "Analysis control byte" on page 18 register, then the values determined from the previous measurement period can be taken from the respective registers intended for this.

10.7.1 Minimum input values

Name:
MinInput01 to MinInput04

The minimum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

10.7.2 Maximum input values

Name:
MaxInput01 to MaxInput04

The maximum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

10.7.3 Limit value trigger counter

Name:
CH01MinMaxLatchCounter to CH04MinMaxLatchCounter

The number of valid events that trigger a new measurement period for the limit value analysis is counted in this register.

Data type	Value
UINT	0 to 65535

10.8 Trace

If the module is operated on a SG4 CPU, the digitalized input values are recorded by the module. The module must be operated in "Supervised" mode in order to use the trace function.

Recording must be enabled for the desired channel. The enable bits can then control the recording at runtime. The sampled values are recorded in the module's internal FIFO memory.

If the previously defined state occurs on the channel, the contents of the FIFO memory are transmitted to the application. Whether the FIFO memory continued to be filled depends on how recording is configured.

> **Information:**
>
> **The trace mechanism can only be used if the module is connected directly to the CPU, not if it is operated behind a bus controller.**

10.8.1 Enable recording

Name:
TraceChannelEnable

The respective channel is enabled for the trace with this register.

Data type	Values
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Channel disabled
		1	Channel enabled
...	...	...	
3	Channel 4	0	Channel disabled
		1	Channel enabled
4 - 7	Reserved	-	

10.8.2 Number of values to be recorded

Name:
TraceSampleDepth

16 kB are available on the module for the trace. The FIFO memory limitation means that a maximum of 8192 analog values can be recorded. This memory is divided up equally among the enabled channels. The actual number of maximum possible recordings therefore depends on the number of channels enabled for trace:

1 channel enabled: Up to 8192 recordings
2 channels enabled: Up to 4096 recordings per channel
3 channels enabled: Up to 2730 recordings per channel
4 channels enabled: Up to 2048 recordings per channel

Data type	Value
UINT	2 to 8192

10.8.3 Recording priority

Name:
ConfigOutput25

The priority of the trace can be increased with this register.

Data type	Value	Function
USINT	3	Standard
	6	Trace priority higher than X2X Link communication

10.8.4 Starting a recording

Name:

TraceEnable01

This register starts the recording according to the specifications for edge control or the comparator.

Data type	Values
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceEnable01	0	Disables the trace function
		1	Enables the trace function
1 - 7	Reserved	-	

10.8.5 Recording status

Name:
TraceEnabled
TraceWriteActive
TraceReadActive
ReadyForTrigger
TriggerActive
TraceOk
TraceError

The status of the trace is represented in this register.

Data type	Values
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	TraceEnabled	0	Trace inactive
		1	Trace active
1	Reserved	-	
2	TraceWriteActive	0	Data not recorded
		1	Data recorded
3	TraceReadActive	0	Data not output/read
		1	Data output/read
4	ReadyForTrigger	0	Not ready for triggering
		1	Ready for triggering
5	TriggerActive	0	No trigger active or already executed
		1	Trigger active
6	TraceOk	0	Overflow or inactive
		1	No overflow
7	TraceError	0	No error or inactive
		1	Trace buffer full

10.8.6 Free trace buffer

Name:
FreeBufferSize

Specifies the available FIFO memory area in bytes for the trace

Data type	Values
UINT	0 to 65,535

10.8.7 Counter for trace triggers

Name:
TriggerCount

This register indicates the number of triggers that have occurred since starting the trace.

Data type	Values
UINT	0 to 65,535

10.8.8 Counter for faulty recording triggers

Name:
TriggerFailCount

Counts the trigger events for which the trace could not be performed.

Data type	Values
UINT	0 to 65,535

10.8.9 Comparator for trigger conditions

In order to adapt the trace as closely as possible to the requirements of the application, the trace function can also be controlled using the comparator. Threshold values (hysteresis) can be defined within the permitted range of values to do so. 2 status bits are then generated for each enabled channel:

- **InRange bit**
  The InRange status is "1" if the measured value falls within the defined limits.
  The InRange status is "0" if the measured value falls outside the defined limits.
- **Threshold value bit**
  The threshold value bit is "1" if the measured value exceeds the upper threshold value.
  The threshold value bit is "0" if the measured value falls below the lower threshold value.

The InRange and threshold value bits for all channels are grouped together in the lower-value byte of the "CompStateCollection" on page 23 register. In addition, the states of the previous sampling are stored in the higher-value byte.

The 4 status messages of each channel can be linked according to the following logic via a logical connective mask using AND or OR operators and used as a trace trigger:

```
delta = (Current_HysteresisStatus ^ NominalValues)// Different between current status and preset
cond = delta & Selected_HysteresisStatusBits// Eliminate irrelevant status messages
ccond = Selected_HysteresisStatusBits (Current_HysteresisStatus ^ NominalValues)
if((0==(cond & ~LogicalOperators)) &&
(0!=(~cond & LogicalOperators))) {=> Generate trigger event}
```

	Corresponds to register:
Selected_HysteresisStatusBits	"cfgComp_EnableMask" on page 24
Current_HysteresisStatus	"CompStateCollection" on page 23
Nominal values	"cfgComp_NominalState" on page 23
Logical operators	"cfgComp_ConditionTypeMask" on page 24

10.8.9.1 Lower limit value for hysteresis

Name:
cfgComp_LowLimitCh01 to cfgComp_LowLimitCh04

The lower limit value for hysteresis is configured in this register.

Data type	Values
INT	-32768 to 32767

10.8.9.2 Upper limit value for hysteresis

Name:
cfgComp_HighLimitCh01 to cfgComp_HighLimitCh04

The upper limit value for hysteresis is configured in this register.

Data type	Values
INT	-32768 to 32767

10.8.9.3 Hysteresis status of the channels

Name:
CompStateCollection

The hysteresis status of the input channels for the current and last cycle are represented in this register.

Data type	Values
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
7	Channel04 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
15	Channel04 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values

10.8.9.4 Comparison state of the channels

Name:
cfgComp_NominalState

The desired comparison state for the hysteresis status is indicated in this register.

Data type	Values
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
7	Channel04 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
15	Channel04 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values

Information:

This is a "whitelist", i.e. the trace starts as soon as the current status message takes on the state predefined here.

One or more matches will be necessary depending on the selection of the relevant hysteresis status bits and logical connective operators.

10.8.9.5 Selecting the relevant hysteresis status bits

Name:
cfgComp_EnableMask

This register selects which status bits of the hysteresis comparison should be used to generate the trigger.

For more information about using this register, see "Comparator for trigger conditions" on page 22.

Data type	Values
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
1	Channel01 InRange status in the current cycle	0	Do not use
		1	Use for generation
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
7	Channel04 InRange status in the current cycle	0	Do not use
		1	Use for generation
8	Channel01 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
9	Channel01 InRange status in the last cycle	0	Do not use
		1	Use for generation
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
15	Channel04 InRange status in the last cycle	0	Do not use
		1	Use for generation

10.8.9.6 Logical connective operators for hysteresis status bits

Name:
cfgComp_ConditionTypeMask

The desired state operators with which the respective status bit is linked to others to generate a trigger are selected in this register.

At least one OR operation must be configured, but it does not necessarily have to be located on a channel configured with "1" in the "cfgComp_EnableMask" on page 24 register.

Data type	Values
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
1	Channel01 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
7	Channel04 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
8	Channel01 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
9	Channel01 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
15	Channel04 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation

10.8.10 Time-offset trace

Additional conditions for shifting the starting and stopping points can be defined if the trace should be chronologically offset to the trigger.

10.8.10.1 Starting the trace

Name:
TraceTriggerStart

The starting position is defined relative to the configured trigger condition (rising/falling edge) in this register. Positive values mean that the trace takes place x samples after the trigger condition. Negative values mean that the trace takes place x samples before the trigger condition.

The value -32768 performs the trace without regard for the configured trigger condition. If the trace memory is completely full, then the oldest recorded value is overwritten (FIFO principle).

"Trace start" in the I/O configuration or the registers "Trigger condition on falling edge" on page 17 and "Trigger condition on rising edge" on page 17 determine whether a positive, negative or any edge must be triggered.

Data type	Values
INT	-32768 to 32767

10.8.10.2 Stopping the trace

Name:
TraceTriggerStop

The stopping position is defined relative to the configured trigger condition in this register.

- When configuring an early trigger event, this value refers to the trigger event.
- When configuring a delayed trigger event, this value refers to the starting event.

Data type	Values
UINT	0 to 65,535

10.9 Acyclic frame size

Name:
AsynSize

When the stream is used, data is exchanged internally between the module and CPU. For this purpose, a defined amount of acyclic bytes is reserved for this slot.
Increasing the acyclic frame size leads to increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Value	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

10.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. Note that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Standard priority	200 µs
High priority with trace function	300 µs

10.11 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.