# X20(c)MM2436

## 1 General information

The motor bridge module is used to control 2 DC motors with a nominal voltage of 24 to 39 VDC ±25% at a nominal current up to 3 A. The module can be reconfigured and used in current controller mode for controlling inductive loads. The module is also equipped with 4 digital inputs, which can be used as incremental counters. Each motor is controlled with a full-bridge (H-bridge). This enables the motors to be moved in both directions.

- 2x outputs (H bridge) with PWM control and 24 to 39 VDC ±25% supply
- 3 A nominal current (3.5 A max current)
- 15 Hz to 50 kHz frequency, 16-bit
- Frequency mode with 10 to 6553.5 Hz or 1 to 655.35 Hz resolution.
- PWM resolution, 15-bit + sign, minimum 10 ns
- Configurable dither
- 2x 2 inputs 24V, can be configured as AB
- Sink connection
- 1-wire connections

## 2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

**For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.**

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, exposure 21 days

## 3 Order data

| Model number | Short description | Figure |
|---|---|---|
| | **Motor controllers** |  |
| X20MM2436 | X20 PWM motor module, 24 to 39 VDC ±25%, 2 PWM motor bridges, 3 A continuous current, 3.5 A peak current, 4 digital inputs 24 VDC, sink, configurable as incremental encoder | |
| X20cMM2436 | Coated X20 PWM motor module, 24 to 39 VDC ±25%, 2 PWM motor bridges, 3 A continuous current, 3.5 A peak current, 4 digital inputs 24 VDC, sink, configurable as incremental encoder | |
| | **Required accessories** | |
| | **Bus modules** | |
| X20BM31 | X20 bus module for double-width modules, 24 VDC keyed, internal I/O supply continuous | |
| X20cBM31 | X20 bus module, coated, for double-width modules, 24 VDC keyed, internal I/O supply continuous | |
| | **Terminal blocks** | |
| X20TB12 | X20 terminal block, 12-pin, 24 VDC keyed | |

Table 1: X20MM2436, X20cMM2436 - Order data

# 4 Technical data

| Model number | X20MM2436 | X20cMM2436 |
|---|---|---|
| **Short description** | | |
| I/O module | 2-channel PWM motor bridge, 2 AB incremental encoders | |
| **General information** | | |
| B&R ID code | 0x26B5 | 0xE752 |
| Status indicators | I/O function per channel, operating state, module status | |
| Diagnostics | | |
| Module run/error | Yes, using status LED and software | |
| Output | Yes, using status LED and software | |
| I/O power supply | Yes, using software | |
| Power consumption | | |
| Bus | 0.01 W | |
| Internal I/O | - | |
| External I/O | | |
| 24 VDC | 2.45 W | |
| 48 VDC | 3.15 W | |
| Additional power dissipation caused by the actuators (resistive) [W] | - | |
| Electrical isolation | | |
| Channel - Bus | Yes | |
| Channel - Channel | No | |
| Certification | | |
| CE | Yes | |
| KC | Yes | - |
| UL | cULus E225616<br>Power conversion equipment | - |
| HazLoc | cCSAus 244665<br>Process control equipment<br>for hazardous locations<br>Class I, Division 2, Groups ABCD, T5 | - |
| ATEX | Zone 2, II 3G Ex nA nC IIA T5 Gc<br>IP20, Ta = 0 - Max. 60°C<br>FTZÚ 09 ATEX 0083X | |
| GOST-R | Yes | |
| **Digital inputs** | | |
| Quantity | 4 | |
| Nominal voltage | 24 VDC | |
| Input voltage | 24 VDC (-15% / +20%) | |
| Input current at 24 VDC | Approx. 1.3 mA | |
| Input filter | | |
| Hardware | <5 µs | |
| Software | - | |
| Connection type | 1-wire connections | |
| Input circuit | Sink | |
| Additional functions | 2x AB incremental encoder, 1x ABR counter, 2x event counter, 2x period duration/gate measurement | |
| Input resistance | Typ. 18 kΩ | |
| Switching threshold | | |
| Low | <5 VDC | |
| High | >15 VDC | |
| Isolation voltage between channel and bus | 500 $V_{eff}$ | |
| **AB incremental encoder** | | |
| Quantity | 2 | |
| Encoder inputs | 24 V, asymmetrical | |
| Counter size | 16-bit | |
| Input frequency | Max. 50 kHz | |
| Evaluation | 4x | |
| Signal form | Square wave pulse | |
| **PWM output** | | |
| Quantity | 2 | |
| Nominal voltage | 24 to 39 VDC ±25% | |
| Nominal current | 3 A | |
| Maximum current | 3.5 A (2 s) | |
| PWM frequency | | |
| Standard operating mode (PWM/current) | 15 Hz to 50 kHz | |
| Frequency operating mode | 1 Hz to 6553.5 Hz | |
| Actuator power supply | | |
| Supply | External | |
| Fuse | Required line fuse: Max. 10 A, slow-blow | |
| Output protection | Thermal cutoff for overcurrent and short circuit | |
| Design | H bridge | |
| Configurable dither | Amplitude, frequency | |

Table 2: X20MM2436, X20cMM2436 - Technical data

| Model number | X20MM2436 | X20cMM2436 |
|---|---|---|
| Period duration resolution (PWM/current operating mode) | 16-bit, min. 20 µs | |
| Frequency resolution (frequency operating mode) | | |
| 0.1 Hz scaling | <3000 Hz: 0.1 Hz, 3000 Hz to 6553.5 Hz: 0.1 Hz to 0.4 Hz | |
| 0.01 Hz scaling | <300 Hz: 0.01 Hz, 300 Hz to 655.35 Hz: 0.01 Hz to 0.04 Hz | |
| Phase shift PWM1 to PWM2 | 180° - if possible (according to operating mode) | |
| DC bus capacitance | 100 µF | |
| PWM pulse width | | |
| PWM mode | 15-bit + sign ≥10 ns | |
| Current mode | 15-bit + sign ≥10 ns | |
| Frequency mode | 15-bit + sign ≥10 ns | |
| Isolation voltage between channel and bus | 500 $V_{eff}$ | |
| **Operating conditions** | | |
| Mounting orientation | | |
| Horizontal | Yes | |
| Installation at elevations above sea level | | |
| 0 to 2000 m | No limitations | |
| >2000 m | Reduction of ambient temperature by 0.5°C per 100 m | |
| EN 60529 protection | IP20 | |
| **Environmental conditions** | | |
| Temperature | | |
| Operation | | |
| Horizontal installation | 0 to 50°C | |
| Vertical installation | Not permitted | |
| Derating | See section "Derating" | |
| Storage | -25 to 70°C | |
| Transport | -25 to 70°C | |
| Relative humidity | | |
| Operation | 5 to 95%, non-condensing | Up to 100%, condensing |
| Storage | 5 to 95%, non-condensing | |
| Transport | 5 to 95%, non-condensing | |
| **Mechanical characteristics** | | |
| Note | Order 1x terminal block X20TB12 separately<br>Order 1x X20BM31 bus module separately | Order 1x terminal block X20TB12 separately<br>Order 1x bus module X20cBM31 separately |
| Spacing | $25^{+0.2}$ mm | |

Table 2: X20MM2436, X20cMM2436 - Technical data

# 5 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" of the X20 system user's manual.

| Figure | LED | Color | Status | Description |
|---|---|---|---|---|
|  | r | Green | Off | No power to module |
| | | | Single flash | RESET mode |
| | | | Double flash | BOOT mode (during firmware update)[1)] |
| | | | Blinking | PREOPERATIONAL mode |
| | | | On | RUN mode |
| | e | Red | Off | No power to module or everything OK |
| | | | On | Error or reset status |
| | e + r | Red on / Green single flash | | Invalid firmware |
| | 1 - 4 | Green | | Input state of the corresponding digital input |
| | M1, M2 | Orange | On | Output 1 or 2 is active |

1) Depending on the configuration, a firmware update can take up to several minutes.

# 6 Pinout

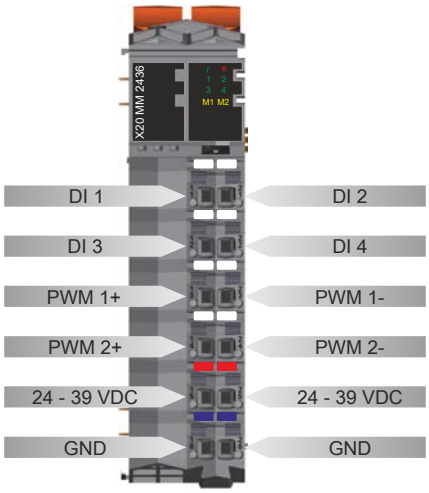
In accordance with the EN 60204-1 standard, a cable cross section of 0.75 mm² or larger must be used for the motor outputs in order to handle the maximum motor current of 3.5 A. To ensure full motor power, voltage drops that could result from the cable length and the electrical connections must also be taken into consideration when selecting the attachment cable.

## Warning!

**The terminal block is not permitted to be plugged in or unplugged during operation.**

## Information:

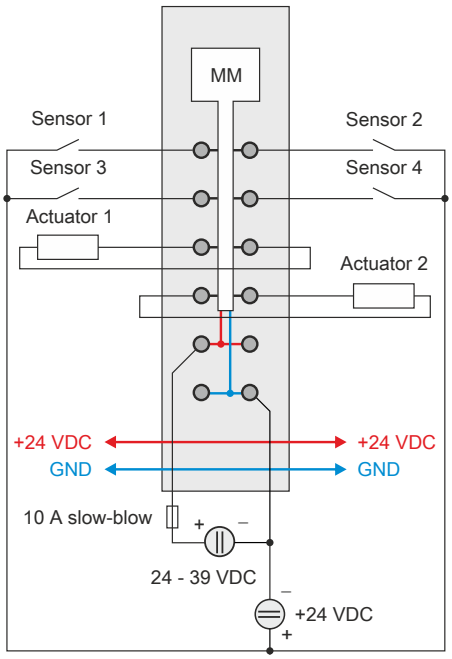
**Shielded motor cables must be used in order to meet the limits according to the EN 55011 standard (emissions).**



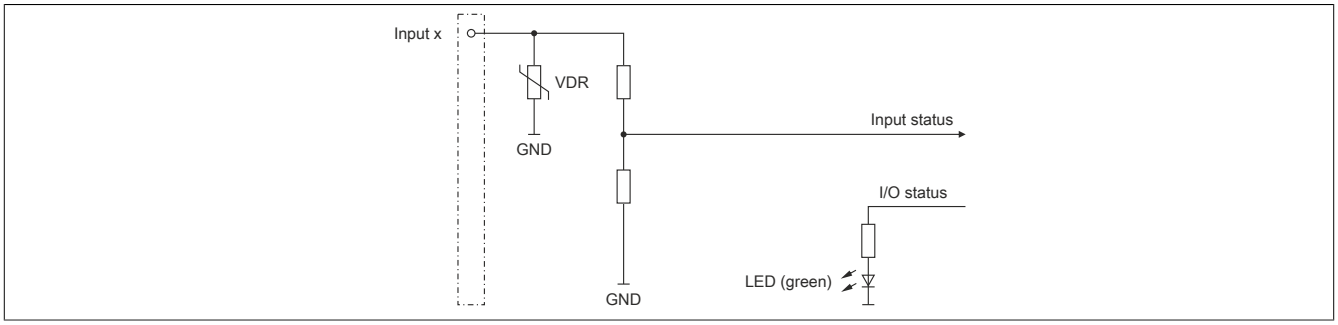

# 7 Connection example

## Information:

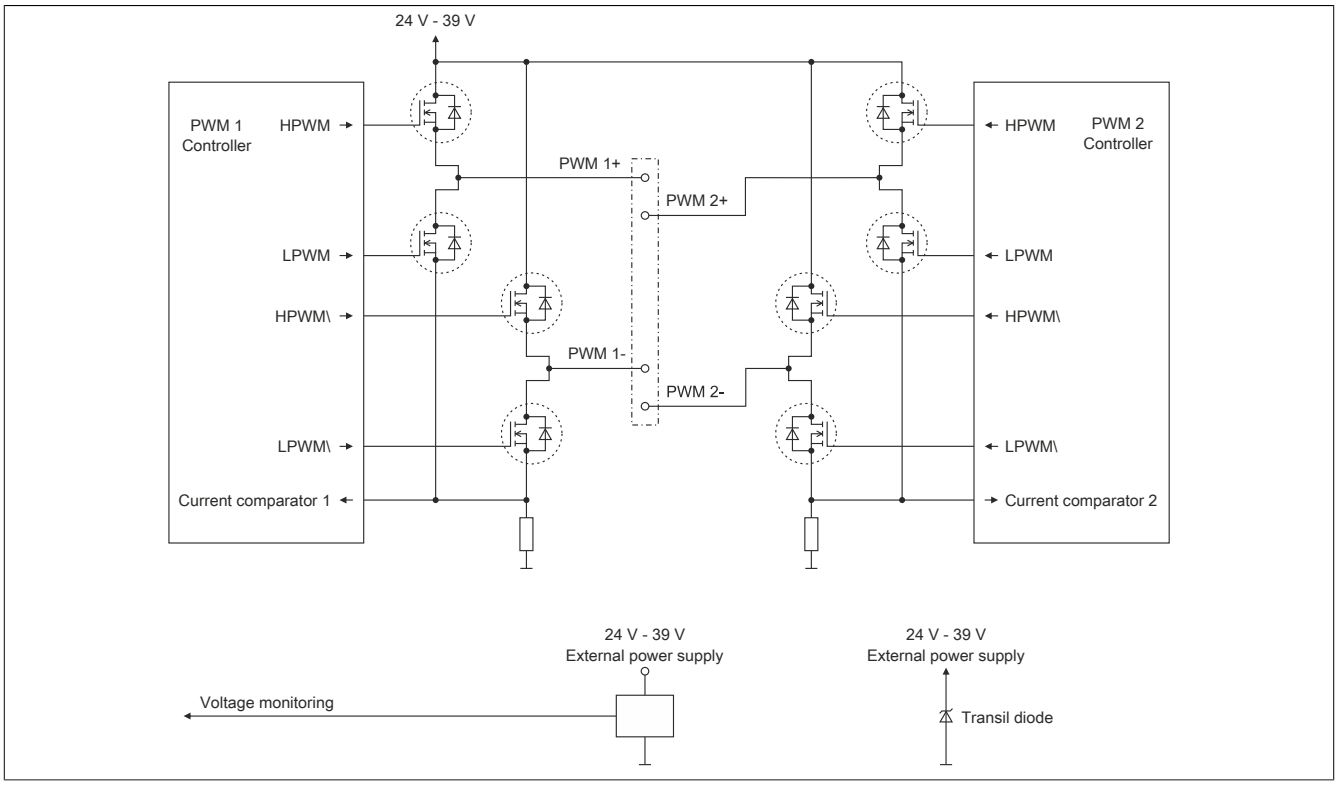
**This module can only be operated if supplied with power via the terminal block.**



# 8 Input circuit diagram




# 9 Output circuit diagram



# 10 Protection

The power supply line should be protected by a circuit breaker or a fuse. In general, dimensioning the supply line and overcurrent protection depends on the structure of the power supply (modules can be connected individually or in groups).

## Information:

**The effective current for the power supply depends on the load but is always less than the motor current. Make sure the maximum nominal current of 7 A is not exceeded on the power supply terminals of the power element.**

When choosing a suitable fuse, the user must also account for characteristics such as aging effects, temperature derating, overcurrent capacity and the definition of the rated current, which can vary by manufacturer and type. In addition, the fuse that is selected must also be able to handle application-specific characteristics (e.g. overcurrent that occurs in acceleration cycles).

The cross section of the power mains and the rated current of the overcurrent protection used are chosen according to the current load so that the maximum current load for the cable cross section selected (based on the type of wiring, see table) is greater than or equal to the current load in the power mains. The rated current of the overcurrent protection must be less than or equal to the maximum current load for the cable cross section selected (based on the type of wiring, see table):

| $I_{Mains}$ | ≤ | $I_b$ | ≤ | $I_Z$ |
|---|---|---|---|---|
| Mains | ≤ | Fuse | ≤ | Line/cable |

| Wire cross section [mm²] | Maximum current load for cable cross section $I_Z$ / rated current for overcurrent protection $I_b$ [A] depending on the type of wiring at an ambient air temperature of 40°C in accordance with EN 60204-1 | | | |
|---|---|---|---|---|
| | B1 | B2 | C | E |
| 1.5 | 13.5 / 13 | 13.1 / 10 | 15.2 / 13 | 16.1 / 16 |
| 2.5 | 18.3 / 16 | 16.5 / 16 | 21 / 20 | 22 / 20 |

Table 3: Cable cross section of the mains supply line depending on the type of wiring

The tripping current of the fuse must not exceed the rated current for overcurrent protection $I_b$.

| Type of wiring | Description |
|---|---|
| B1 | Wires in conduit or cable duct |
| B2 | Cables in conduit or cable duct |
| C | Cables or wires on walls |
| E | Cables or wires on open-ended cable tray |

Table 4: Type of wiring used for the mains supply line

# 11 Derating

To ensure proper operation, the following items must be taken into consideration:

- The sum of the square of both effective currents ($I_N$ , peak value must not exceed 3 A) must not exceed 9 A². The boost current of 3.5 A for 2 seconds is an exception.
- Modules next to the motor module can have a maximum power consumption of 1 W.
- The derating values listed below must be taken into consideration

### Example calculations

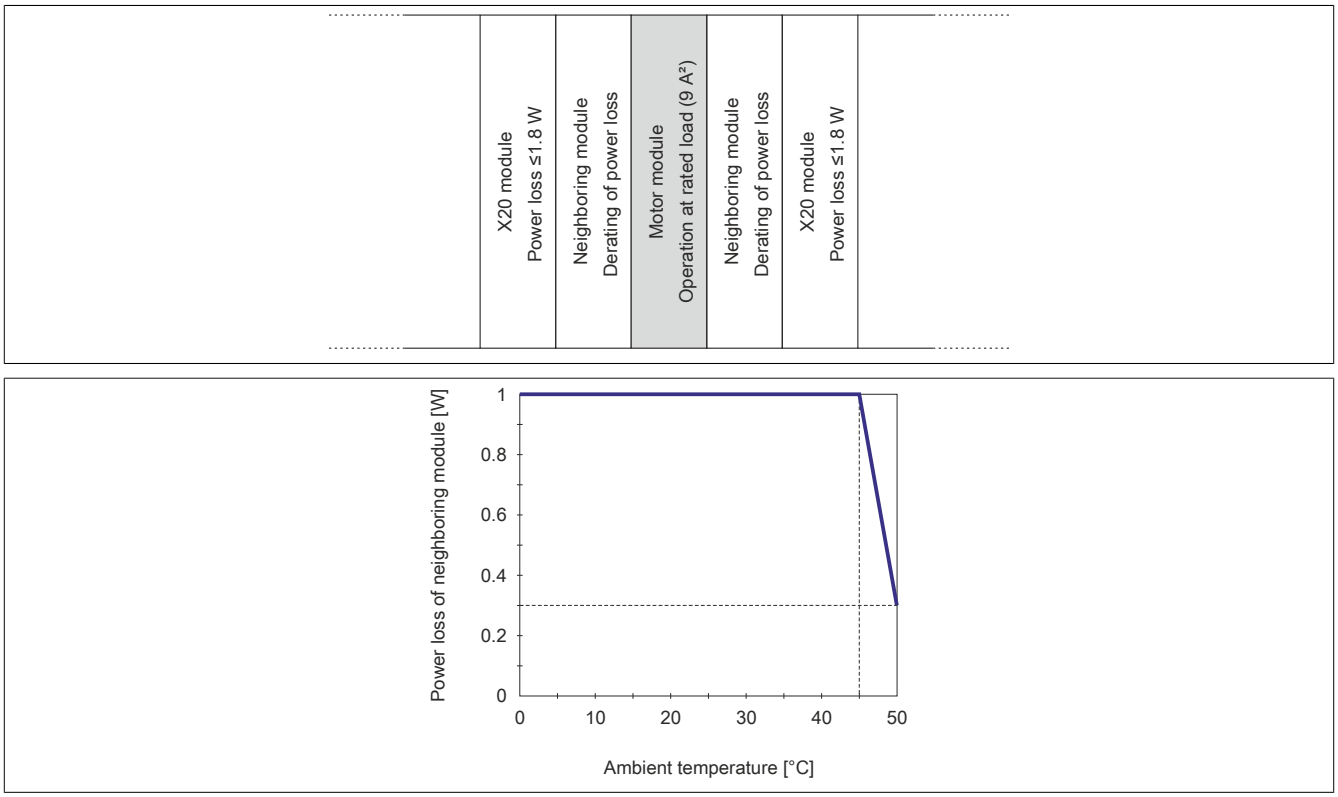
In the following examples, the calculation of $I_N^2$ is used to check if the current operating state is permitted.

| Output current | | $I_N^2$ | Operating state permitted |
|---|---|---|---|
| PWM 1 | PWM 2 | | |
| 3 A | 0 A | $I_N^2 = 3\ A \cdot 3\ A + 0\ A \cdot 0\ A = 9\ A^2$ | Yes |
| 2.1 A | 2.1 A | $I_N^2 = 2.1\ A \cdot 2.1\ A + 2.1\ A \cdot 2.1\ A = 8.82\ A^2$ | Yes |
| 2.8 A | 2 A | $I_N^2 = 2.8\ A \cdot 2.8\ A + 2\ A \cdot 2\ A = 11.84\ A^2$ | for max. 2 s[1)] |

1) The cooling time, which means operation <9 A², must be at least 5 times as long as the time of the overload.

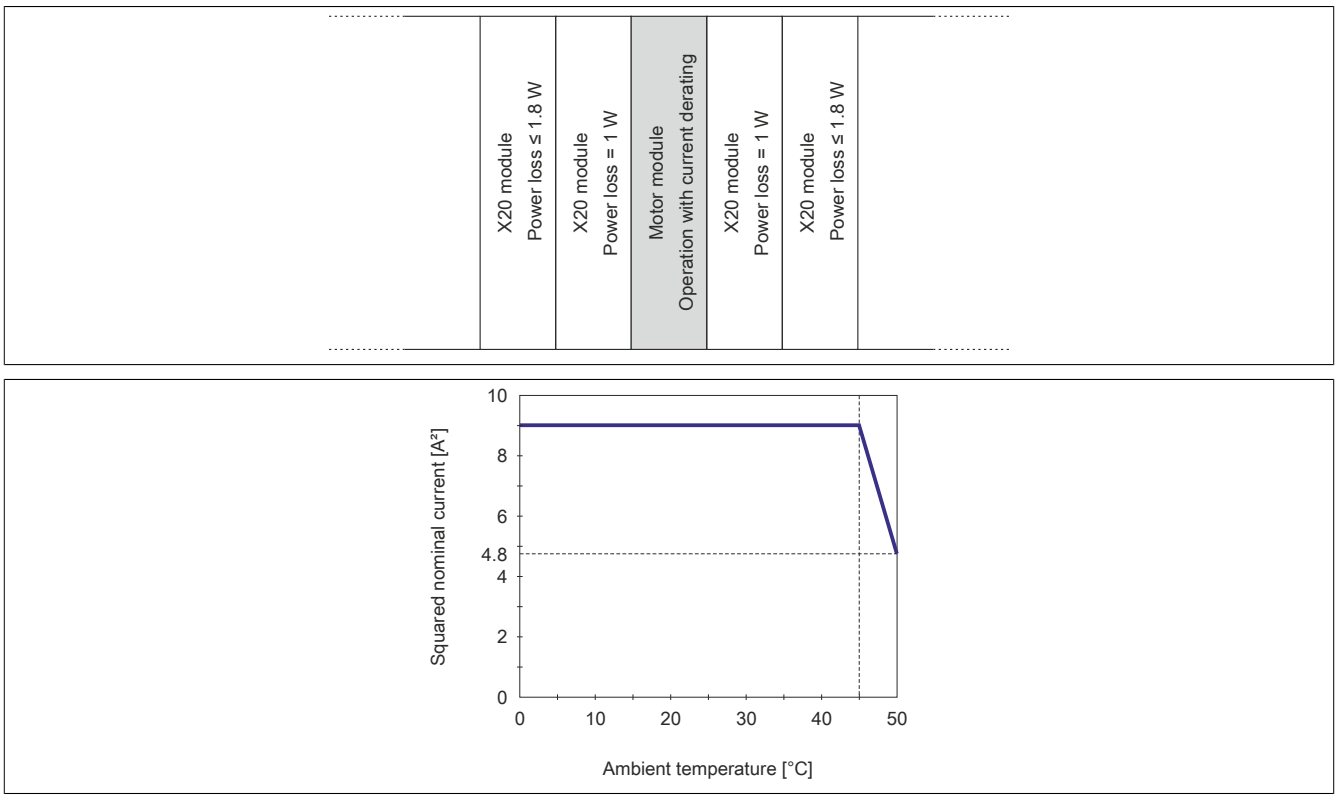
### Power loss derating for neighboring modules

Modules directly next to the motor module can have a power loss of 1 W. If the motor module is operated with the rated load over the entire temperature range (9 A²), a derating for power loss of the neighboring modules must be adhered to starting at 45°C.



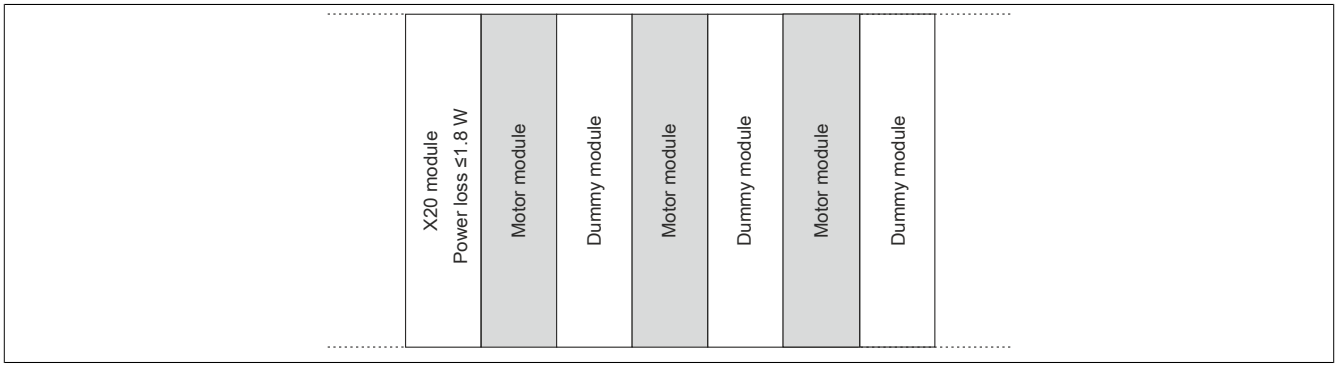

### Current derating of the motor module

If the power loss of the neighboring modules to the motor module is 1 W, then the current of the motor module must be derated starting at 45°C.



**Hardware configuration for multiple motor modules**

If three or more motor modules are operated in a cluster, a dummy module must be inserted between the motor modules. There is no derating in this configuration.




## 12 Monitoring the module supply

The module supply is continually monitored (with firmware Version 3 or higher). If the following limits are exceeded in either direction, an error bit is set.

Upper limit: >50 V
Lower limit: <18 V

## 13 Overvoltage cutoff

If the supply voltage on the module exceeds 50V (e.g. through feedback during generator operation), then both PWM outputs are disabled (PWM output pins are shorted). The outputs are reactivated as soon as the supply voltage is back in the valid range. Switching the outputs on again can cause an open load error in current mode (depending on the current setpoint and load inductance) as well as with any other abrupt change to the current setpoint value.

## 14 Overtemperature cutoff (at 85°C)

If the module temperature reaches or exceeds the limit value of 85°C, then the module executes the following actions:

- Setting the "overtemperature" error bit
- The PWM outputs are disabled (short-circuited)

Once the module temperature sinks to 83°C, the error bit is automatically cleared by the module and the outputs become operational again.

# 15 Register description

## 15.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

These general data points are listed in section "Additional information - General data points" of the X20 system user's manual.

## 15.2 Function model 0 - Standard

| Register | Name | Data type | Read | | Write | |
|---|---|---|---|---|---|---|
| | | | Cyclic | Acyclic | Cyclic | Acyclic |
| **Configuration** | | | | | | |
| **"Standard PWM/current mode" operating mode only** | | | | | | |
| 12 | PeriodDurationPWM01PWM02 | UINT | | | • | |
| 14 | PulseWidthCurrentPWM01 | INT | | | • | |
| 16 | PulseWidthCurrentPWM02 | INT | | | • | |
| 18 | ConfigOutput01 | USINT | | | | • |
| 20 | ConfigOutput02 | USINT | | | | • |
| 31 | DecayConfig[1] | USINT | | | | • |
| **"Frequency mode 1 and 2" operating mode only**[2] | | | | | | |
| 12 | FrequencyPWM01PWM02 | UINT | | | • | |
| | DutyCyclePWM01PWM02 | INT | | | | |
| 14 | DutyCyclePWM01 | INT | | | • | |
| | FrequencyPWM01 | UINT | | | | |
| 16 | DutyCyclePWM02 | INT | | | • | |
| | FrequencyPWM02 | UINT | | | | |
| **All operating modes** | | | | | | |
| 30 | ConfigOutput03 | USINT | | | | • |
| 38 | CounterConfig01[3] | USINT | | | | • |
| 39 | CounterConfig02[3] | USINT | | | | • |
| **Communication** | | | | | | |
| **All operating modes** | | | | | | |
| 0 | Counter01 | INT | • | | | |
| 2 | Counter02 | INT | • | | | |
| 10 | Input status[3] | USINT | • | | | |
| | StatusInput01 | Bit 0 | | | | |
| | ... | ... | | | | |
| | StatusInput04 | Bit 3 | | | | |
| | CounterOverflow01 | Bit 4 | | | | |
| | CounterOverflow02 | Bit 5 | | | | |
| | RefToggle01 | Bit 6 | | | | |
| 32 | Error status | USINT | • | | | |
| | UnderVoltageError | Bit 0 | | | | |
| | OverVoltageError | Bit 1 | | | | |
| | OvertemperaturError | Bit 2 | | | | |
| | OperatingError | Bit 3 | | | | |
| | CurrentError01 | Bit 4 | | | | |
| | OverCurrentError01 | Bit 5 | | | | |
| | CurrentError02 | Bit 6 | | | | |
| | OverCurrentError02 | Bit 7 | | | | |
| 34 | Error acknowledgment, dither switch-off[3] and FrequencyPrescale[2] | USINT | | | • | |
| | ClearError01 | Bit 0 | | | | |
| | ClearError02 | Bit 1 | | | | |
| | CounterOverflowDetectEnable01 | Bit 2 | | | | |
| | CounterOverflowDetectEnable02 | Bit 3 | | | | |
| | CounterReset01 | Bit 4 | | | | |
| | CounterReset02 | Bit 5 | | | | |
| | DitherDisable01<br>FrequencyPrescale01 | Bit 6 | | | | |
| | DitherDisable02<br>FrequencyPrescale02 | Bit 7 | | | | |
| 36 | Temperature01 | SINT | | • | | |

1) Firmware version 3 or higher.
2) Firmware version 7.00 or higher.
3) Firmware version 4 or higher.

## 15.3 Function model 254 - Bus controller

| Register | Offset[1] | Name | Data type | Read | | Write | |
|---|---|---|---|---|---|---|---|
| | | | | Cyclic | Acyclic | Cyclic | Acyclic |
| **Configuration** | | | | | | | |
| **"Standard PWM/current mode" operating mode only** | | | | | | | |
| 12 | 0 | PeriodDurationPWM01PWM02 | UINT | | | ● | |
| 14 | 2 | PulseWidthCurrentPWM01 | INT | | | ● | |
| 16 | 4 | PulseWidthCurrentPWM02 | INT | | | ● | |
| 18 | - | ConfigOutput01 | USINT | | | | ● |
| 20 | - | ConfigOutput02 | USINT | | | | ● |
| 31 | - | DecayConfig[2] | USINT | | | | ● |
| **"Frequency mode 1 and 2" operating mode only[3]** | | | | | | | |
| 12 | 0 | FrequencyPWM01PWM02 | UINT | | | ● | |
| | | DutyCyclePWM01PWM02 | INT | | | | |
| 14 | 2 | DutyCyclePWM01 | INT | | | ● | |
| | | FrequencyPWM01 | UINT | | | | |
| 16 | 4 | DutyCyclePWM02 | INT | | | ● | |
| | | FrequencyPWM02 | UINT | | | | |
| **All operating modes** | | | | | | | |
| 30 | - | ConfigOutput03 | USINT | | | | ● |
| 38 | - | CounterConfig01[4] | USINT | | | | ● |
| 39 | - | CounterConfig02[4] | USINT | | | | ● |
| **Communication** | | | | | | | |
| **All operating modes** | | | | | | | |
| 0 | 0 | Counter01 | INT | ● | | | |
| 2 | 2 | Counter02 | INT | ● | | | |
| 10 | 4 | Input status[4] | USINT | ● | | | |
| | | StatusInput01 | Bit 0 | | | | |
| | | ... | ... | | | | |
| | | StatusInput04 | Bit 3 | | | | |
| | | CounterOverflow01 | Bit 4 | | | | |
| | | CounterOverflow02 | Bit 5 | | | | |
| | | RefToggle01 | Bit 6 | | | | |
| 32 | 6 | Error status | USINT | ● | | | |
| | | UnderVoltageError | Bit 0 | | | | |
| | | OverVoltageError | Bit 1 | | | | |
| | | OvertemperaturError | Bit 2 | | | | |
| | | OperatingError | Bit 3 | | | | |
| | | CurrentError01 | Bit 4 | | | | |
| | | OverCurrentError01 | Bit 5 | | | | |
| | | CurrentError02 | Bit 6 | | | | |
| | | OverCurrentError02 | Bit 7 | | | | |
| 34 | 6 | Error acknowledgment, dither switch-off[4] and FrequencyPrescale[3] | USINT | | | ● | |
| | | ClearError01 | Bit 0 | | | | |
| | | ClearError02 | Bit 1 | | | | |
| | | CounterOverflowDetectEnable01 | Bit 2 | | | | |
| | | CounterOverflowDetectEnable02 | Bit 3 | | | | |
| | | CounterReset01 | Bit 4 | | | | |
| | | CounterReset02 | Bit 5 | | | | |
| | | DitherDisable01<br>FrequencyPrescaled01 | Bit 6 | | | | |
| | | DitherDisable02<br>FrequencyPrescaled02 | Bit 7 | | | | |
| 36 | - | Temperature01 | SINT | | ● | | |

1) The offset specifies the position of the register within the CAN object.
2) Firmware version 3 or higher.
3) Firmware version 7.00 or higher.
4) Firmware version 4 or higher.

### 15.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

## 15.4 Operating mode description

Beginning with firmware version 7.00, the module is equipped with the "Frequency mode 1" and "Frequency mode 2" operating modes in addition to "Standard PWM/current mode".
The following table lists the differences between the different operating modes:

| | Operating mode | | |
|---|---|---|---|
| | Standard PWM/current mode | Frequency mode 1 | Frequency mode 2 |
| **Frequency setting** | 1x period duration in µs (see register "PWM period duration" on page 13) | 1x In 2/10 or 1/100 Hz (see register "Frequency" on page 18) | 1x In 1/10 or 1/100 Hz (see register "Frequency" on page 18) |
| **Duty cycle / Current setting** | 2x -100 to 100% (see register "PWM pulse width" on page 14) | 1x -100 to 100% (see register "Duty cycle" on page 18) | 2x -100 to 100% (see register "Duty cycle" on page 18) |
| **Dithering** | Yes | No | No |
| **Decay mode setting** | Yes | No | No |
| **PWM/current mode selection** | Yes | No | No |
| **Other** | PWM start from channel 2 offset 180° compared to channel 1 | Due to a different frequency, a fixed phase relationship between channel 1 and channel 2 is not possible. | PWM start from channel 2 offset 180° compared to channel 1 |
| | 3.5 A per channel | 1 A per channel | 3.5 A per channel |

## 15.5 Configuration

### 15.5.1 Counter configuration 1

Name:
CounterConfig01

This register can be used to configure counter 1.

**This function is available beginning with firmware Version 4.**

| Data type | Value |
|---|---|
| SINT | See bit structure. |

Bit structure:

| Bit | Description | Value | Information |
|---|---|---|---|
| 0 - 2 | Sets the type of counter. | 000 | AB counter with 4x evaluation (A = DI 1, B = DI 2) |
| | | 001 | Event counter (DI 1) |
| | | 010 | Period measurement (DI 1) |
| | | 011 | Gate measurement (DI 1) |
| | | 100 | ABR counter with 4x evaluation (A = DI 1, B = DI 2, R = DI 3, Reference enable = DI 4). Copies counter 1 to counter 2 on a reference pulse. Counter 2 is shown in the I/O map, even if it is disabled in counter configuration 2. |
| | | 101 to 111 | No counter. Counter is disabled and not shown in the I/O map. |
| 3 | Measurement starts | 0 | At rising edge on DI 1<br>Referencing at rising edge on DI 3 (only for ABR counters) |
| | | 1 | At falling edge on DI 1<br>Referencing at falling edge on DI 3 (only for ABR counters) |
| 4 - 5 | Set the counter frequency for gate or period measurement | 00 | 4 MHz |
| | | 01 | External via DI 2 |
| | | 10 | 31.25 kHz |
| | | 11 | Reserved |
| 6 - 7 | Set the reference input | 00 | Reference input always enabled (DI 3) |
| | | 01 | Reserved |
| | | 10 | Enable for reference input (DI 3) if DI 4 = 0 |
| | | 11 | Enable for reference input (DI 3) if DI 4 = 1 |

### 15.5.2 Counter configuration 2

Name:
CounterConfig02

This register can be used to configure counter 2. Unlike counter 1, this counter cannot be configured as an ABR counter.

**This function is available beginning with firmware Version 4.**

| Data type | Value |
|---|---|
| SINT | See bit structure. |

Bit structure:

| Bit | Description | Value | Information |
|---|---|---|---|
| 0 - 2 | Sets the type of counter. | 000 | AB counter with 4x evaluation (A = DI 3, B = DI 4) |
| | | 001 | Event counter (DI 3) |
| | | 010 | Period measurement (DI 3) |
| | | 011 | Gate measurement (DI 3) |
| | | 100 to 111 | No counter. Counter is disabled and not shown in the I/O map. |
| 3 | Measurement starts | 0 | At rising edge on DI 3 |
| | | 1 | At falling edge on DI 3 |
| 4 - 5 | Set the counter frequency for gate or period measurement | 00 | 4 MHz |
| | | 01 | External via DI 4 |
| | | 10 | 31.25 kHz |
| | | 11 | Reserved |
| 6 - 7 | Reserved | - | |

### 15.5.3 Module configuration

Name:
ConfigOutput03

The output control for each motor can be configured separately in this register.

| Data type | Values |
|---|---|
| USINT | See bit structure. |

Bit structure:

| Bit | Description | Value | Information |
|---|---|---|---|
| 0 | Output 1 | 0 | PWM control |
| | | 1 | Current control |
| 1 | Output 2 | 0 | PWM control |
| | | 1 | Current control |
| 2 - 3 | Operating mode[1)] | 00 | Standard PWM/current mode |
| | | 01 | Frequency mode 1 (bit 0 to 1 ignored) |
| | | 10 | Frequency mode 2 (bit 0 to 1 ignored) |
| | | 11 | Reserved |
| 4 - 7 | Reserved | - | |

1) Firmware version 7.00 or higher.

## Information:

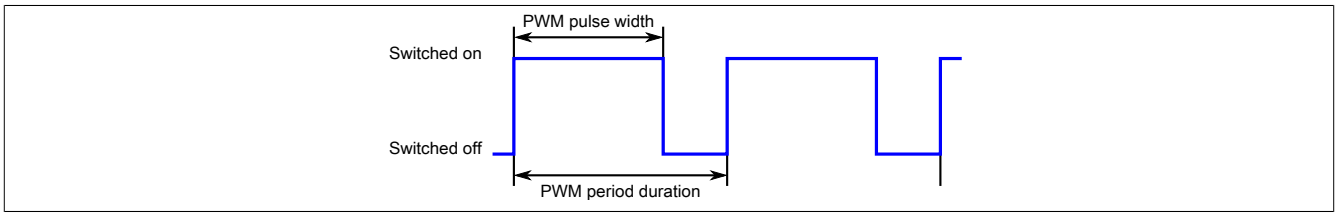
**After switching on or resetting, only one switchover from the default "Standard PWM/current mode" is allowed after "Frequency mode 1" or "Frequency mode 2". Later reconfigurations into another mode are ignored by the module's firmware.**

### 15.5.4 Registers for "Standard PWM/current mode" operating mode

This module provides both "PWM mode" and "current mode".
The following images illustrate how the current curves for the outputs are affected by registers "PWM period duration" on page 13 and "PWM pulse width" on page 14.

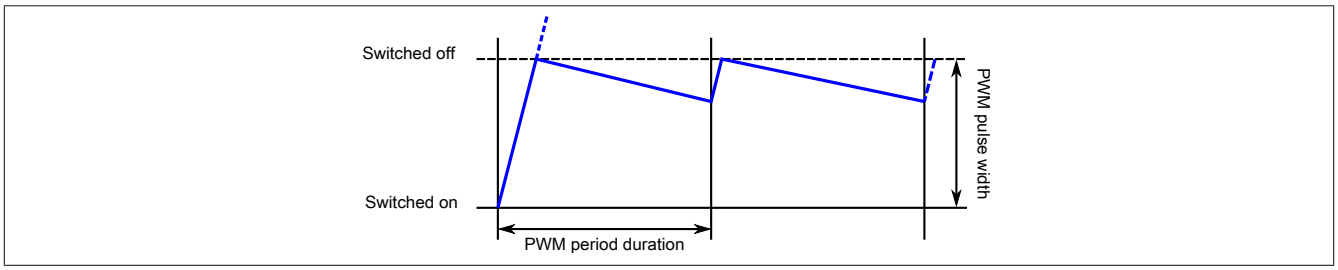
**PWM mode**

At the beginning of each period, the output is switched on for the percentage of time set in the PWM pulse width.




**Current mode**

At the beginning of each period, the current output is switched on. After reaching the value set in "PulseWidthCurrentPWM" on page 14, the output is switched off and the voltage drops according to the decay configuration until switched back on.




#### 15.5.4.1 PWM period duration

Name:
PeriodDurationPWM01PWM02

This register can be used to set the period duration between 20 µs (50 kHz) and 65535 µs (15 Hz). See also "Registers for "Standard PWM/current mode" operating mode" on page 13.

| Data type | Value | Information |
|---|---|---|
| UINT | 20 to 65535 | Time in µs |

### 15.5.4.2 PWM pulse width

Name:
PulseWidthCurrentPWM01 to PulseWidthCurrentPWM02

The PWM pulse width (PWM mode) or current setting (in current mode) is entered in this register according to the setting in the module configuration register. (see also "Registers for "Standard PWM/current mode" operating mode" on page 13.) A negative value changes the output polarity.

## Information:

**This module uses the same scaling as the X67MM2436 module to maintain software compatibility. Current values larger than 3.5 A are limited to 3.5 A.**

**Derating must also be taken into consideration when using both channels (see "Derating" on page 6).**

**PWM mode**

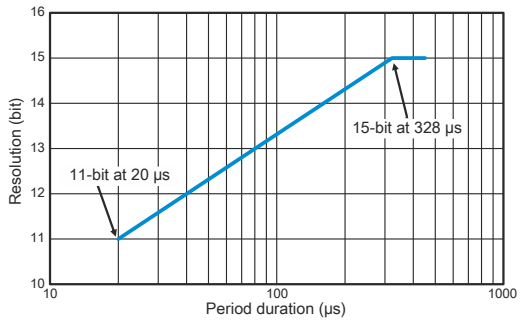
| Data type | Value | Output + | Output - |
|---|---|---|---|
| INT | 32767 | High | Low |
| | 16384 | PWM 50/50 | Low |
| | 0 | Low | Low |
| | -16384 | Low | PWM 50/50 |
| | -32767 | Low | High |

**Current mode**

| Data type | Value | Current mode | Note |
|---|---|---|---|
| INT | 22937 to 32767 | +3.5 A (max. 2 s) | Limited internally, check derating |
| | 22936 | 3.5 A (max. 2 s) | Derating must be taken into consideration. |
| | 19660 | +3 A | |
| | 0 | 0 A | |
| | -19660 | -3 A | |
| | -22936 | -3.5 A (max. 2 s) | Derating must be taken into consideration. |
| | -22937 to -32767 | -3.5 A (max. 2 s) | Limited internally, check derating |

**Resolution/Derating**

As mentioned earlier in the technical data, the PWM resolution is 15-bit (+ sign). This value is derated for a period duration of less than 328 µs because of the minimal PWM timing resolution (10 ns) (see following diagram). With the minimum PWM period duration of 20 µs, the PWM has 11-bit resolution (+ sign):



### 15.5.4.3 Decay configuration

Name:
DecayConfig

The decay configuration determines the method and dynamics of current reduction for inductive loads or motors.

"Slow decay" is configured by default. In this mode, the current is automatically reduced relatively slowly with resistance in the load. No energy is regenerated into the module.

"Mixed decay" mode is recommended for applications that require a dynamic and linear reduction of current. In this mode, energy is regenerated into the module during part of the PWM cycle (fast decay).

**This function is available beginning with firmware version 3.**

| Data type | Values |
|---|---|
| USINT | See bit structure. |

Bit structure:

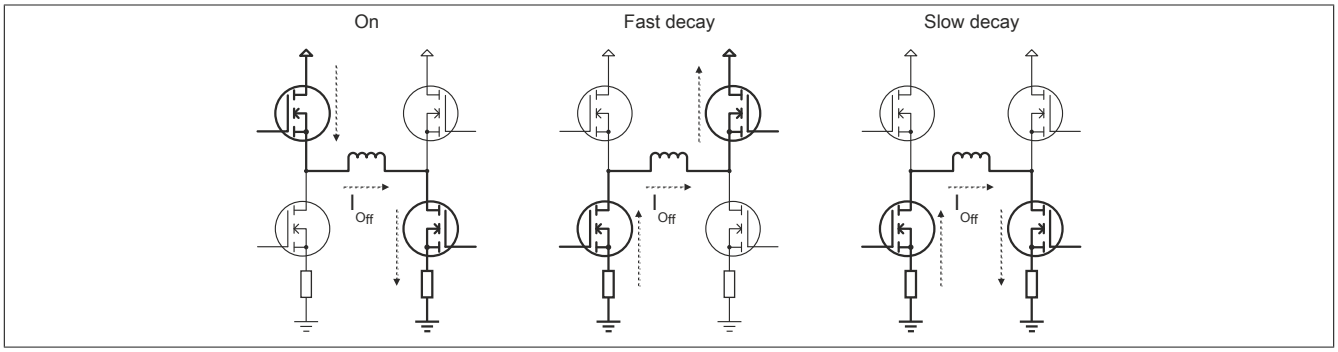
| Bit | Description | Value | Information |
|---|---|---|---|
| 0 - 1 | PWM 1 | 00 | Slow decay (default setting) |
| | | 01 | Mixed decay |
| | | 10 to 11 | Reserved |
| 2 - 3 | Reserved | 0 | |
| 4 - 5 | PWM 2 | 00 | Slow decay (default setting) |
| | | 01 | Mixed decay |
| | | 10 to 11 | Reserved |
| 6 - 7 | Reserved | 0 | |

**Mixed decay**

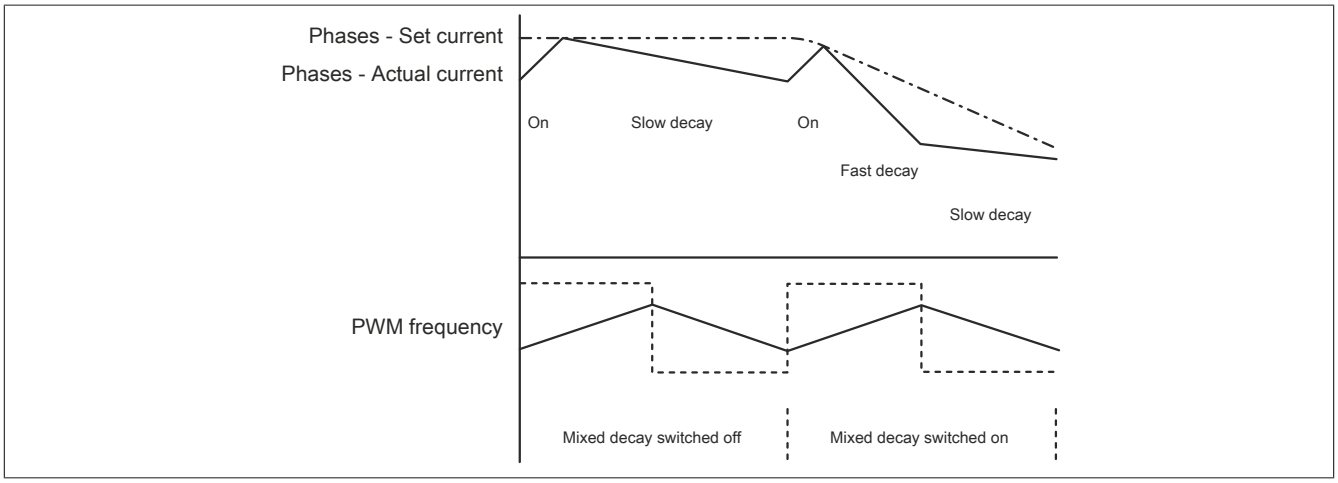
As its name suggests, mixed decay mode is a mix of "slow decay" and "fast decay". This occurs as follows:

A check is made at the beginning of each PWM cycle to determine if the actual current for the phases is below the current setpoint. If this is the case, PWM is enabled (On) until the set current is reached. The system switches to fast decay mode for the rest of the first half of the PWM cycle. If the current setpoint has already been exceeded at the beginning of the PWM cycle (generator operation), the system immediately switches to fast decay mode. The second half of the PWM cycle always takes place in slow decay mode.

This also permits generator operation as long as the valid range for the supply voltage has not been exceeded due to the regeneration into the DC circuit.




**Mixed decay - Set / actual current, PWM frequency**



### Operating DC motors

In PWM mode, the motor current is limited to the maximum current (3.5 A), independent of the supply voltage.

However, the motor switches to generator operation when braking. Because of the counter EMF, which is dependent on the rotary speed, a current is generated in the module that is only limited by the internal resistance of the motor. This is not permitted to exceed 7 A (maximum 2 seconds).

The counter EMF closely corresponds to the voltage needed to achieve this speed. Therefore, the maximum brake current is very easy to calculate with the following formula.

$$I_{Brake} = U_e * \frac{Pulse\ width}{100\%} * \frac{1}{R_{Motor}}$$

Example:

| Module supply | 38 V |
|---|---|
| Pulse width | 16364 (equal to 50%) |
| Internal resistance of motor | 3.5 Ω |

$$I_{Brake} = 38V * \frac{50}{100\%} * \frac{1}{3.5\Omega} = 5.4A$$

### 15.5.4.4 Dither

When the position setpoint for valves remains constant for a long period of time, especially in fluids, there is a risk that a valve will stick. This is normally prevented using "dithering". When doing so, the value is permitted to slightly oscillate around the position setpoint.

In the module, this dithering is implemented in the form of a triangle wave.

- In PWM mode, the pulse width (duty cycle) of the PWM signal oscillates.
- In current mode, the current setpoint oscillates.

Concrete values for the dither amplitude and dither frequency to be set must be either taken from the valve data sheet or determined empirically.

By default, the dither is active for both outputs as soon as the dither amplitude and dither frequency are set to a value >0. If necessary, the dither can be deactivated for each output individually or simultaneously (see "Error acknowledgment, dither switch-off and FrequencyPrescale" on page 21).

#### 15.5.4.4.1 Dither amplitude

Name:
ConfigOutput01

This register can be used to configure the amplitude value or pulse width.

| Data type | Value | Information |
|---|---|---|
| USINT | 0 to 255 | Current mode: 0 to 25.5% of the module's nominal current[1)]<br>PWM mode: 0 to 25.5% of the period duration |

1) See the technical data for the module.

#### 15.5.4.4.2 Dither frequency

Name:
ConfigOutput02

This register can be used to set the frequency in 2 Hz steps.

| Data type | Value | Information |
|---|---|---|
| USINT | 0 to 255 | Corresponds to 0 to 510 Hz |

#### 15.5.4.4.3 Dither example

The values specified in the data sheet for a valve should be used to calculate Dither amplitude and Dither frequency.

**Data sheet for the valve**

The data sheet for a valve manufacturer recommends the following dithering:

Dither amplitude in percent ($A_{Dither}$): 20 to 35% (peak value) of the valves 2 A nominal current

Dither frequency in Hertz ($F_{Dither}$): 40 to 70 Hz

**Selected values**

These values correspond to the average values on the value data sheet.

$A_{Dither}$ = 27% of the valve's nominal current (peak values)

$F_{Dither}$ = 56 Hz

**Formulas**

Dither amplitude = ($A_{Dither}$ / 2) * (Nominal $current_{Valve}$ / Nominal $current_{Module}$) * 10
**Information:** ($A_{Dither}$ / 2) = conversion of the peak values to amplitude; " * 10" = scaling of the dither amplitude to 1/10%

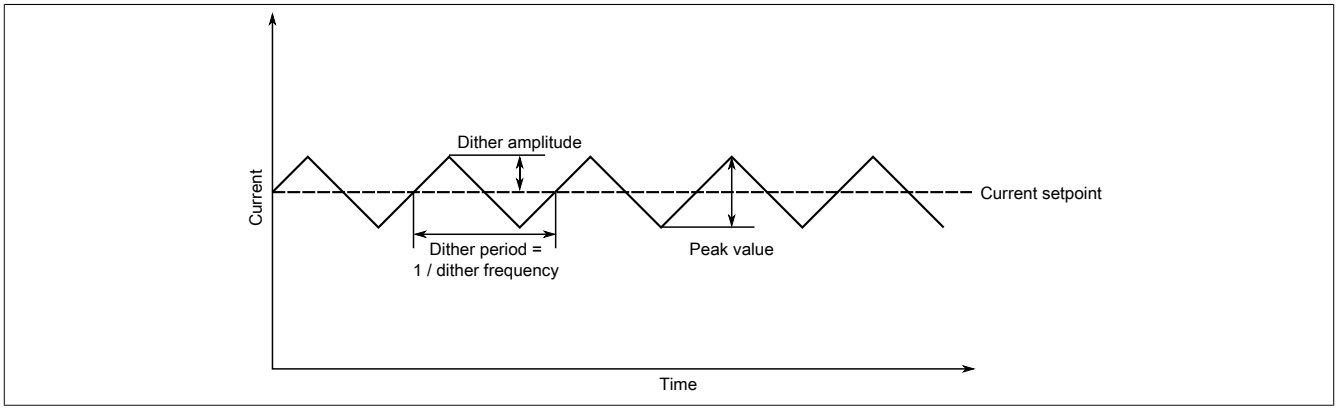
Dither frequency = $F_{Dither}$ / 2 Hz
**Info:** Dither frequency is configured in 2 Hz steps

**Calculation**

By using the selected values in the formulas.

Dither amplitude = 27% / 2 * (2 A / 3 A) * 10 = 90

Dither frequency = 56 Hz / 2 Hz = 28



### 15.5.5 Registers for "Frequency mode 1 and 2" operating mode

#### 15.5.5.1 Frequency

Name:
FrequencyPWM01 to FrequencyPWM02 (frequency mode 1)
FrequencyPWM01PWM02 (frequency mode 2)

The frequency for PWM01 or PWM02 (depends on the frequency mode) can be set individually or together in these registers. The unit is 1/10 or 1/100 Hz depending on how the "FrequencyPrescale" settings are configured. For more information, see the "Error acknowledgment, dither switch-off and FrequencyPrescale" on page 21 registers.

| Data type | Value | Information |
|---|---|---|
| DINT | 0 | Disabled |
| | 1 to 99 | FrequencyPrescale 1/10: 10 Hz<br>FrequencyPrescale 1/100: 1 Hz |
| | 100 to 65535 | FrequencyPrescale 1/10: 1/10 * Value = 10 to 6553.5 Hz<br>FrequencyPrescale 1/100: 1/100 * Value = 1 to 655.35 Hz |

#### 15.5.5.2 Duty cycle

Name:
DutyCyclePWM01PWM02 (frequency mode 1)
DutyCyclePWM01 to DutyCyclePWM02 (frequency mode 2)

The duty cycle for the PWM outputs is set individually or separately depending on the frequency mode.

For information about scaling, derating, etc. see the "PWM pulse width" on page 14 registers (PWM mode).

## Important!

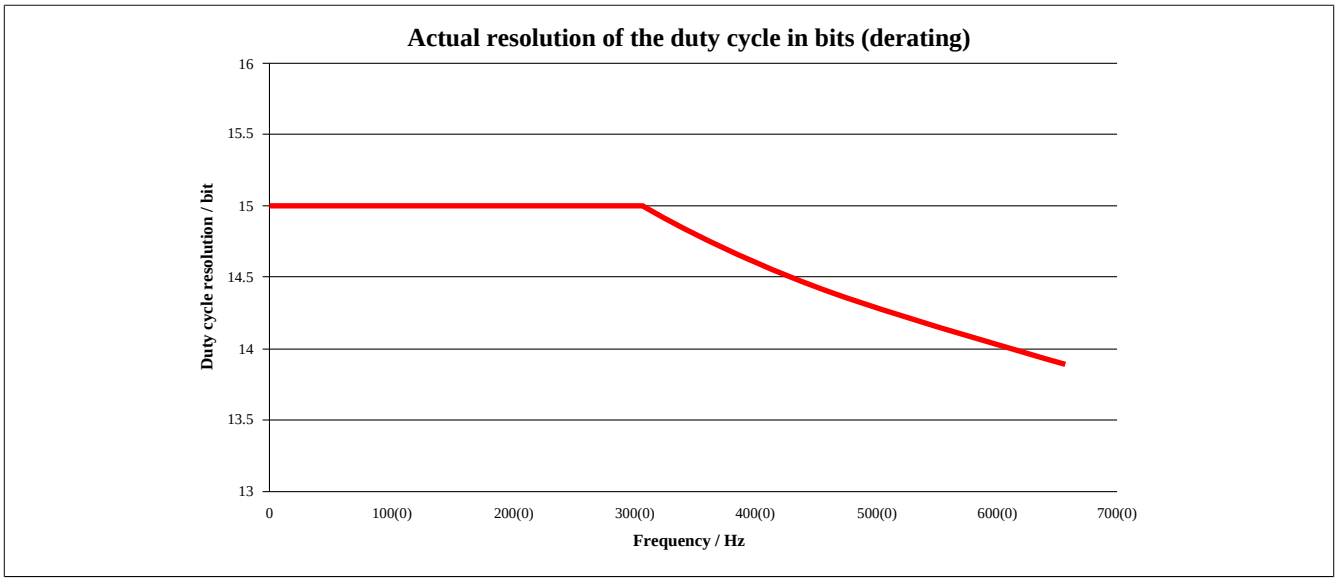
**A negative duty cycle can also be configured. In this case, the frequency is output to "PWM1/2" (identical to "Standard PWM/current mode") instead of the "PWM1/2+" output. It is especially important to take this into consideration with actuators that are only able to process positive input values.**

| Data type | Value |
|---|---|
| INT | -32768 to 32767 |

**Derating the duty cycle**

As with "Standard PWM/current mode", the predefined duty cycle in the frequency modes cannot be implemented over the entire frequency domain with full 15-bit resolution; instead, it is subject to derating.

It is possible to achieve the full 15-bit resolution until about 305 (frequency domain 1) or 3050 Hz (frequency domain 2).



## 15.6 Communication

### 15.6.1 Numerator

Name:
Counter01 to Counter02

This register indicates the status of counters 1 and 2. Configuration of the counters is described in sections "Counter configuration 1" on page 11 and "Counter configuration 2" on page 12. The following counter types or measurements can be configured:

- AB counter
- ABR counter
- Event counter
- Period measurement
- Gate measurement

If counter 1 is configured as an ABR counter, then the register for counter 2 is assigned the current value of counter 1 when the reference pulse occurs.

| Data type | Value |
|---|---|
| INT | -32768 to 32767 |

Counter function - Assignment of the digital inputs:

| Counter function | Counter number | A | B | R | Enable reference | Counter input | Period duration and gate signal | External measuring frequency |
|---|---|---|---|---|---|---|---|---|
| Incremental counter | 1 | DI 1 | DI 2 | DI 3 | DI 4 | | | |
| | 2 | DI 3 | DI 4 | | | | | |
| Event counter | 1 | | | | | DI 1 | | |
| | 2 | | | | | DI 3 | | |
| Period duration and gate measurement | 1 | | | | | | DI 1 | DI 2 |
| | 2 | | | | | | DI 3 | DI 4 |

### 15.6.2 Input status

Name:
StatusInput01 to StatusInput04
CounterOverflow01 to CounterOverflow02
RefToggle01

The status of the inputs and counters is mapped in this register.

**This function is available beginning with firmware Version 4.**

| Data type | Values |
|---|---|
| USINT | See bit structure. |

Bit structure:

| Bit | Description | Value | Information |
|---|---|---|---|
| 0 | StatusInput01 | 0 or 1 | Logical state of input 1 |
| ... | | ... | |
| 3 | StatusInput0 | 0 or 1 | Logical state of input 4 |
| 4 | CounterOverflow01 | 0 | Period duration or gate measurements of counter 1 are within the valid range (0x0 - 0xFFFF). The bit is only valid if overflow detection is enabled (bit 2 = 1 in the "Error acknowledgment, dither switch-off and FrequencyPrescale" on page 21 register). |
| | | 1 | Overflow during period duration or gate measurement (reset with bit 2 = 0 in the "Error acknowledgment, dither switch-off and FrequencyPrescale" on page 21 register). |
| 5 | CounterOverflow02 | 0 | Period duration or gate measurements of counter 2 are within the valid range (0x0 - 0xFFFF). The bit is only valid if overflow detection is enabled (bit 3 = 1 in the "Error acknowledgment, dither switch-off and FrequencyPrescale" on page 21 register). |
| | | 1 | Overflow during period duration or gate measurement (reset with bit 3 = 0 in the "Error acknowledgment, dither switch-off and FrequencyPrescale" on page 21 register). |
| 6 | RefToggle01 | x | Bit 6 changes value each time the counter state is latched from counter 1 to counter 2. After the module boots, bit 6 = 0. |
| 7 | Reserved | - | |

### 15.6.3 Temperature

Name:
Temperature01

The module temperature is displayed in this register.

| Data type | Value | Information |
|---|---|---|
| SINT | -40 to 125 | Module temperature in °C |

### 15.6.4 Error status

Name:
UnderVoltageError
OverVoltageError
OvertemperatureError
OperatingError
CurrentError01 to CurrentError02
OverCurrentError01 to OverCurrentError02

If an error is detected, the corresponding error bit remains set in this register until the error is acknowledged (see "Error acknowledgment, dither switch-off and FrequencyPrescale" on page 21).

| Data type | Values |
|---|---|
| USINT | See bit structure. |

Bit structure:

| Bit | Description | Value | Information |
|---|---|---|---|
| 0 | UnderVoltageError | 0 | No error |
| | | 1 | Module supply lower limit <18 V |
| 1 | OverVoltageError | 0 | No error |
| | | 1 | Module supply upper limit >50 V |
| 2 | OvertemperatureError | 0 | No error |
| | | 1 | Overtemperature |
| 3 | OperatingError[1)] | 0 | No error |
| | | 1 | Faulty operation |
| 4 | CurrentError01 | 0 | No error |
| | | 1 | Open load error Output 1 |
| 5 | OverCurrentError01 | 0 | No error |
| | | 1 | Overcurrent error Output 1 |
| 6 | CurrentError02 | 0 | No error |
| | | 1 | Open load error Output 2 |
| 7 | OverCurrentError02 | 0 | No error |
| | | 1 | Overcurrent error Output 2 |

1) Firmware version 7.00 or higher.

#### Faulty operation

This warning indicates faulty operation of the module. The following table lists possible causes, the module's reaction and how to correct/acknowledge the error.

| Cause | Reaction | Correction/Acknowledgment |
|---|---|---|
| Default value for "PeriodDuration" on page 13 or "Frequency" on page 18 outside of specified range | Default value limited to the specified range | Automatic acknowledgment as soon as the default value is back within specifications |
| Later reconfiguration of the operating mode (see bits 2 to 3 of the "Module configuration" on page 12 register) | The new configuration is ignored. The module continues to work in the original operating mode. | The original configuration is restored. |

#### Overcurrent error

An overcurrent error is registered if one of the following conditions is met:

- ≥3.5 or 1 A (frequency mode 1) flow from a PWM output for at least 2 seconds
- ≥5 A flow for 3 consecutive PWM cycles

In both cases, the affected PWM output is deactivated by the firmware (i.e. the pins on the PWM output are short-circuited). The user must acknowledge the error (see "Error acknowledgment, dither switch-off and FrequencyPrescale" on page 21) before a PWM output disabled in this manner can be made operational again.

### Open load error

An open load error is only registered in current control mode (see "configuration register" on page 12) if the current setpoint is not reached. In some cases this can be caused by an open line, although usually the impedance of the load is too high.

### 15.6.5 Error acknowledgment, dither switch-off and FrequencyPrescale

Name:
ClearError01 to ClearError02
CounterOverflowDetectEnable01 to CounterOverflowDetectEnable02
CounterReset01 to CounterReset02
DitherDisable01 to DitherDisable02
FrequencyPrescale01 to FrequencyPrescale02

This register can be used to acknowledge errors; to enable/disable overflow detection, counters and dither; and to set a prescaler for the frequency domains.

**This function is available beginning with firmware Version 4.**

| Data type | Values |
|---|---|
| USINT | See bit structure. |

Bit structure:

| Bit | Description | Value | Information |
|---|---|---|---|
| 0 | ClearError01 | 0 | No effect |
| | | 1 | Error acknowledgment on output 1 (overcurrent or open load) or acknowledgment from limit switch 1 |
| 1 | ClearError02 | 0 | No effect |
| | | 1 | Error acknowledgment on output 2 (overcurrent or open load) or acknowledgment from limit switch 2 |
| 2 | CounterOverflowDetectEnable01 | 0 | Overflow detection disabled. Bit 4 in the counter status register is reset (see "Input status" on page 19) |
| | | 1 | Counter 1: Overflow detection enabled. |
| 3 | CounterOverflowDetectEnable02 | 0 | Overflow detection disabled. Bit 5 in the counter status register is reset (see "Input status" on page 19) |
| | | 1 | Counter 2: Overflow detection enabled. |
| 4 | CounterReset01 | 0 | Counter 1 is enabled (default). |
| | | 1 | Counter 1 is set to 0 and disabled. If counter 1 is configured as an ABR counter (see "Counter configuration 1" on page 11), then latch 2 is also set to 0. In this mode, the latched value from counter 1 is stored in counter 2. |
| 5 | CounterReset02 | 0 | Counter 2 is enabled (default). |
| | | 1 | Counter 2 is set to 0 and disabled (no effects if counter 1 is configured as an ABR counter) |
| 6 | DitherDisable01 | 0 | Dither for PWM output 1 is enabled (default). The dither frequency and dither amplitude must be >0 (see "Dither" on page 16). |
| | | 1 | Dither for PWM output 1 is disabled. |
| | FrequencyPrescale01[1)] | 0 | Unit in 1/10 Hz, frequency domain: 10 to 6553.5 Hz |
| | | 1 | Unit in 1 Hz, frequency domain: 1 to 655.35 Hz |
| 7 | DitherDisable02 | 0 | Dither for PWM output 2 is enabled (default). The dither frequency and dither amplitude must be >0 (see "Dither" on page 16). |
| | | 1 | Dither for PWM output 2 is disabled. |
| | FrequencyPrescale02[1)] | 0 | Unit in 1/10 Hz, frequency domain: 10 to 6553.5 Hz |
| | | 1 | Unit in 1 Hz, frequency domain: 1 to 655.35 Hz |

1) Firmware version 7.00 or higher.

### FrequencyPrescale

Beginning with firmware version 7.00, bits 6 to 7 in the "Frequency mode 1 and 2" operating mode have a different meaning.

Instead of enabling/disabling dithering for channel 1 or 2, it toggles the prescaler for the frequency setting between 1/10 and 1/100 Hz.

In "Frequency mode 2" operating mode, only bit 6 (FrequencyPrescale01) is used since both channels are operated with the same frequency.

## Information:

**The frequency domain can be toggled at any time, but it also results in the frequency jumping by a factor of 10. If this frequency jump is not tolerated in the application, then the value set in the "Frequency" on page 18 register must be adjusted accordingly.**

## 15.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. Note that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

| Minimum cycle time |
|---|
| 250 µs |

## 15.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

| Minimum I/O update time |
|---|
| 250 µs |