

TLV916x 16-V, 11-MHz, Rail-to-Rail Input/Output, Low Offset Voltage, Low Noise Op Amp

1 Features

- Low offset voltage: $\pm 210 \mu\text{V}$
- Low offset voltage drift: $\pm 0.25 \mu\text{V}/^\circ\text{C}$
- Low noise: $6.8 \text{nV}/\sqrt{\text{Hz}}$ at 1 kHz, $4.2 \text{nV}/\sqrt{\text{Hz}}$ broadband
- High common-mode rejection: 110 dB
- Low bias current: $\pm 10 \text{ pA}$
- Rail-to-rail input and output
- MUX-friendly/comparator inputs
 - Amplifier operates with differential inputs up to supply rails
 - Amplifier can be used in open-loop or as comparator
- Wide bandwidth: 11-MHz GBW, unity-gain stable
- High slew rate: $33 \text{ V}/\mu\text{s}$
- Low quiescent current: 2.4 mA per amplifier
- Wide supply: $\pm 1.35 \text{ V}$ to $\pm 8 \text{ V}$, 2.7 V to 16 V
- Robust EMIRR performance

2 Applications

- Professional microphones and wireless systems
- Multiplexed data-acquisition systems
- Test and measurement equipment
- Factory automation and control
- High-side and low-side current sensing

3 Description

The TLV916x family (TLV9161, TLV9162, and TLV9164) is a family of 16-V, general-purpose operational amplifiers. These devices offer exceptional DC precision and AC performance, including rail-to-rail input/output, low offset ($\pm 210 \mu\text{V}$, typical), low-offset drift ($\pm 0.25 \mu\text{V}/^\circ\text{C}$, typ), and low noise ($6.8 \text{nV}/\sqrt{\text{Hz}}$ at 1 kHz, $4.2 \text{nV}/\sqrt{\text{Hz}}$ at 10 kHz).

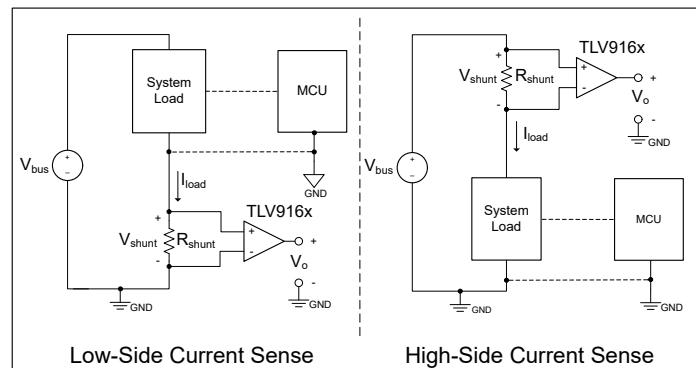
Features such as differential and common-mode input voltage ranges to the supply rails, high short-circuit current ($\pm 73 \text{ mA}$), and high slew rate ($33 \text{ V}/\mu\text{s}$) make the TLV916x a flexible, robust, and high-performance op amp for industrial applications.

The TLV916x family of op amps is available in *micro*-size packages (such as WSON), as well as standard packages (such as SOT-23, SOIC, and TSSOP), and is specified from -40°C to 125°C .

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)
TLV9161	SOT-23 (5)	2.90 mm \times 1.60 mm
	SOT-23 (6)	2.90 mm \times 1.60 mm
	SC70 (5)	2.00 mm \times 1.25 mm
TLV9162	SOIC (8)	4.90 mm \times 3.90 mm
	SOT-23 (8)	2.90 mm \times 1.60 mm
	TSSOP (8)	3.00 mm \times 4.40 mm
	VSSOP (8)	3.00 mm \times 3.00 mm
	WSON (8)	2.00 mm \times 2.00 mm
TLV9164	SOIC (14)	8.65 mm \times 3.90 mm
	TSSOP (14)	5.00 mm \times 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



TLV916x in Current-Sensing Applications



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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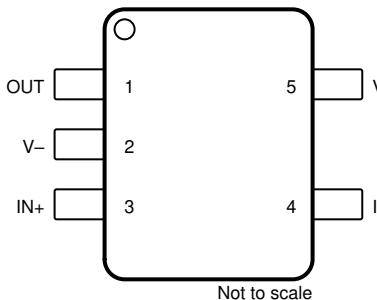
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4 Revision History

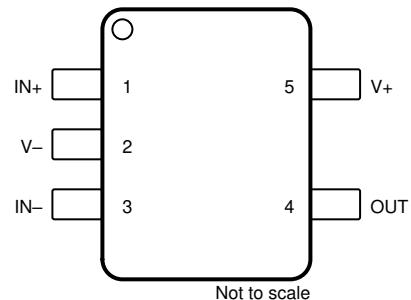
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2021) to Revision A (December 2021)	Page
• Removed preview notation from TLV9164 SOIC (14) package from <i>Device Information</i> table.....	1
• Removed preview notation from TLV9164 TSSOP (14) package from <i>Device Information</i> table.....	1
• Removed preview notation from TLV9164 D package (SOIC) in the <i>Pin Configuration and Functions</i> section... 3	
• Removed preview notation from TLV9164 PW package (TSSOP) in the <i>Pin Configuration and Functions</i> section.....	3
• Removed preview notation from TLV9164 D package (SOIC) in the <i>Thermal Information for Quad Channel</i> section.....	7
• Removed preview notation from TLV9164 PW package (TSSOP) in the <i>Thermal Information for Quad Channel</i> section.....	7
• Added PSRR specification for TLV9164 release in <i>Electrical Characteristics</i> section.....	8
• Added clarification to $V_S = 2.7\text{ V}$ to 16 V PSRR specification noting that specification is for all channel variants.....	8

5 Pin Configuration and Functions



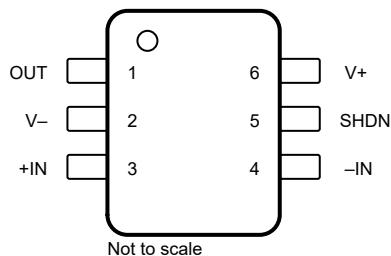
**Figure 5-1. TLV9161 DBV Package
5-Pin SOT-23
(Top View)**



**Figure 5-2. TLV9161 DCK Package
5-Pin SC70
(Top View)**

Table 5-1. Pin Functions: TLV9161

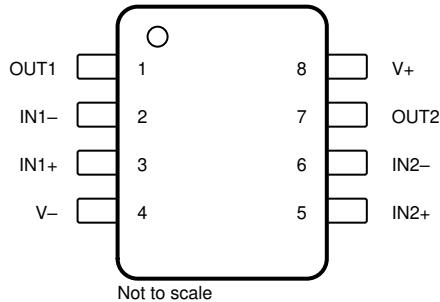
PIN			I/O	DESCRIPTION
NAME	SOT-23	SC70		
IN+	3	1	I	Noninverting input
IN-	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V-	2	2	—	Negative (lowest) power supply



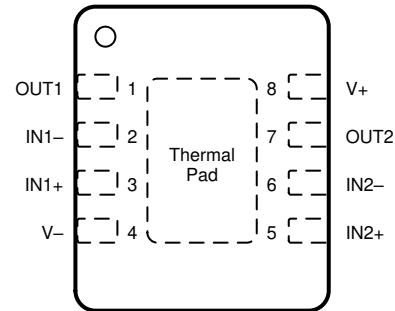
**Figure 5-3. TLV9161S DBV Package
6-Pin SOT-23
(Top View)**

Table 5-2. Pin Functions: TLV9161S

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting input
-IN	4	I	Inverting input
OUT	1	O	Output
SHDN	5	I	Shutdown: low = amplifier enabled, high = amplifier disabled
V+	6	—	Positive (highest) power supply
V-	2	—	Negative (lowest) power supply



**Figure 5-4. TLV9162 D, DDF, PW, and DGK Package
8-Pin SOIC, SOT-23, TSSOP, and VSSOP
(Top View)**

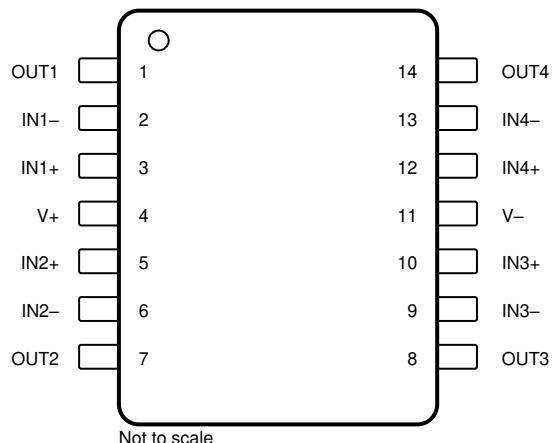


- A. Connect thermal pad to V-. See [Section 7.3.10](#) for more information.

**Figure 5-5. TLV9162 DSG Package(A)
8-Pin WSON With Exposed Thermal Pad
(Top View)**

Table 5-3. Pin Functions: TLV9162

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1-	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2-	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V-	4	—	Negative (lowest) power supply



**Figure 5-6. TLV9164 D and PW Package
14-Pin SOIC and TSSOP
(Top View)**

Table 5-4. Pin Functions: TLV9164

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1-	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2-	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3-	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4-	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V-	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		0	20	V
Signal input pins	Common-mode voltage ⁽³⁾	$(V-) - 0.5$	$(V+) + 0.5$	V
	Differential voltage ⁽³⁾		$V_S + 0.2$	V
	Current ⁽³⁾	-10	10	mA
Shutdown pin voltage		V_-	V_+	
Output short-circuit ⁽²⁾		Continuous		
Operating ambient temperature, T_A		-55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
- (2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
- (3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	± 1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, $(V+) - (V-)$	2.7	16	V
V_I	Common mode voltage range	V_-	V_+	V
V_{IH}	High level input voltage at shutdown pin (amplifier disabled)	$(V-) + 1.1$	V_+	V
V_{IL}	Low level input voltage at shutdown pin (amplifier enabled)	V_-	$(V-) + 0.2$	V
T_A	Specified temperature	-40	125	°C

6.4 Thermal Information for Single Channel

THERMAL METRIC ⁽¹⁾		TLV9161, TLV9161S			Unit
		DBV (SOT-23)		DCK (SC70)	
		5 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.4	166.9	198.1	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	83.9	83.9	94.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.5	47.1	45.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.4	25.9	16.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	52.1	47.0	45.0	°C/W

6.4 Thermal Information for Single Channel (continued)

THERMAL METRIC ⁽¹⁾		TLV9161, TLV9161S			Unit
		DBV (SOT-23)		DCK (SC70)	
		5 PINS	6 PINS	5 PINS	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Thermal Information for Dual Channel

THERMAL METRIC ⁽¹⁾		TLV9162					Unit
		D (SOIC)	DDF (SOT-23)	DGK (VSSOP)	DSG (WSON)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	131.0	149.6	174.2	74.8	183.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	73.0	85.3	65.9	93.6	72.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	74.5	68.6	95.9	42.1	114.0	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	25.0	7.9	11.0	3.8	12.1	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	73.8	68.4	94.4	41.9	112.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	17.0	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.6 Thermal Information for Quad Channel

THERMAL METRIC ⁽¹⁾		TLV9164		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	99.0	118.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	55.1	47.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	54.8	61.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	16.7	5.5	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	54.4	61.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.7 Electrical Characteristics

For $V_S = (V+) - (V-) = 2.7 \text{ V}$ to 16 V ($\pm 1.35 \text{ V}$ to $\pm 8 \text{ V}$) at $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	V _{CM} = V ₋	T _A = -40°C to 125°C	± 0.21	± 1	μV	
dV _{OS} /dT	Input offset voltage drift	V _{CM} = V ₋	T _A = -40°C to 125°C	± 0.25		$\mu\text{V}/^\circ\text{C}$	
PSRR	Input offset voltage versus power supply	TLV9161, TLV9162, V _{CM} = V ₋ , V _S = 5 V to 16 V	T _A = -40°C to 125°C	± 0.45	± 2	$\mu\text{V/V}$	
		TLV9164, V _{CM} = V ₋ , V _S = 5 V to 16 V					
		TLV9161, TLV9162, TLV9164, V _{CM} = V ₋ , V _S = 2.7 V to 16 V ⁽¹⁾	T _A = -40°C to 125°C	± 0.45	± 2.2		
		T _A = -40°C to 125°C	T _A = -40°C to 125°C	± 0.45	± 3.8		
	DC channel separation			± 2		± 12	
INPUT BIAS CURRENT							
I _B	Input bias current			± 10		pA	
I _{OS}	Input offset current			± 10		pA	
NOISE							
E _N	Input voltage noise	f = 0.1 Hz to 10 Hz	T _A = -40°C to 125°C	2.7		μV_{PP}	
				0.49		μV_{RMS}	
e _N	Input voltage noise density	f = 1 kHz	T _A = -40°C to 125°C	6.8		$\text{nV}/\sqrt{\text{Hz}}$	
		f = 10 kHz		4.2			
i _N	Input current noise density	f = 1 kHz		55		$\text{fA}/\sqrt{\text{Hz}}$	
INPUT VOLTAGE RANGE							
V _{CM}	Common-mode voltage range			(V ₋)		(V ₊)	V
CMRR	Common-mode rejection ratio	V _S = 16 V, V ₋ < V _{CM} < (V ₊) – 2 V (PMOS pair)	T _A = -40°C to 125°C	85		110	dB
		V _S = 5 V, V ₋ < V _{CM} < (V ₊) – 2 V (PMOS pair) ⁽¹⁾		75		98	
		V _S = 2.7 V, V ₋ < V _{CM} < (V ₊) – 2 V (PMOS pair)		90			
		V _S = 2.7 – 16 V, (V ₊) – 1 V < V _{CM} < V ₊ (NMOS pair)		78			
		(V ₊) – 2 V < V _{CM} < (V ₊) – 1 V		See Figure 6-6			
INPUT IMPEDANCE							
Z _{ID}	Differential			100 9		$\text{M}\Omega \text{pF}$	
Z _{ICM}	Common-mode			6 1		$\text{T}\Omega \text{pF}$	
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	V _S = 16 V, V _{CM} = V _S / 2, (V ₋) + 0.1 V < V _O < (V ₊) – 0.1 V	T _A = -40°C to 125°C	120		136	dB
				136			
		V _S = 5 V, V _{CM} = V _S / 2, (V ₋) + 0.1 V < V _O < (V ₊) – 0.1 V ⁽¹⁾	T _A = -40°C to 125°C	104		125	
				125			
		V _S = 2.7 V, V _{CM} = V _S / 2, (V ₋) + 0.1 V < V _O < (V ₊) – 0.1 V ⁽¹⁾	T _A = -40°C to 125°C	90		105	
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product			11		MHz	
SR	Slew rate	V _S = 16 V, G = +1, V _{STEP} = 10 V, C _L = 20 pF ⁽³⁾		33		V/μs	

6.7 Electrical Characteristics (continued)

For $V_S = (V+) - (V-) = 2.7 \text{ V}$ to 16 V ($\pm 1.35 \text{ V}$ to $\pm 8 \text{ V}$) at $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_S	Settling time	To 0.1%, $V_S = 16 \text{ V}$, $V_{STEP} = 10 \text{ V}$, $G = +1$, $C_L = 20 \text{ pF}$	0.70			μs
		To 0.1%, $V_S = 16 \text{ V}$, $V_{STEP} = 2 \text{ V}$, $G = +1$, $C_L = 20 \text{ pF}$	0.22			
		To 0.01%, $V_S = 16 \text{ V}$, $V_{STEP} = 10 \text{ V}$, $G = +1$, $C_L = 20 \text{ pF}$	0.89			
		To 0.01%, $V_S = 16 \text{ V}$, $V_{STEP} = 2 \text{ V}$, $G = +1$, $C_L = 20 \text{ pF}$	0.42			
	Phase margin	$G = +1$, $R_L = 10 \text{ k}\Omega$, $C_L = 20 \text{ pF}$	64			°
	Overload recovery time	$V_{IN} \times \text{gain} > V_S$	120			ns
THD+N	Total harmonic distortion + noise	$V_S = 16 \text{ V}$, $V_O = 3 \text{ V}_{RMS}$, $G = 1$, $f = 1 \text{ kHz}$	0.00005%			
			126			dB
		$V_S = 10 \text{ V}$, $V_O = 3 \text{ V}_{RMS}$, $G = 1$, $f = 1 \text{ kHz}$, $R_L = 128 \Omega$	0.0032%			
			90			dB
		$V_S = 10 \text{ V}$, $V_O = 0.4 \text{ V}_{RMS}$, $G = 1$, $f = 1 \text{ kHz}$, $R_L = 32 \Omega$	0.00032%			
			110			dB

6.7 Electrical Characteristics (continued)

For $V_S = (V+) - (V-) = 2.7 \text{ V}$ to 16 V ($\pm 1.35 \text{ V}$ to $\pm 8 \text{ V}$) at $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT						
Voltage output swing from rail	Positive and negative rail headroom	$V_S = 16 \text{ V}, R_L = \text{no load}$ $V_S = 16 \text{ V}, R_L = 10 \text{ k}\Omega$ $V_S = 16 \text{ V}, R_L = 2 \text{ k}\Omega$ $V_S = 2.7 \text{ V}, R_L = \text{no load}$ $V_S = 2.7 \text{ V}, R_L = 10 \text{ k}\Omega$ $V_S = 2.7 \text{ V}, R_L = 2 \text{ k}\Omega$	6	mV		
			25	60		
			85	300		
			0.5			
			5	20		
			20	50		
I_{SC}	Short-circuit current			± 73		mA
C_{LOAD}	Capacitive load drive			See Figure 6-33		pF
Z_O	Open-loop output impedance	$I_O = 0 \text{ A}$		See Figure 6-30		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	TLV9162, TLV9164, $I_O = 0 \text{ A}$		2.4	2.8	mA
			$T_A = -40^\circ\text{C}$ to 125°C		2.84	
		TLV9161, $I_O = 0 \text{ A}$		2.48	2.92	
			$T_A = -40^\circ\text{C}$ to 125°C		2.98	
SHUTDOWN						
I_{QSD}	Quiescent current per amplifier	$V_S = 2.7 \text{ V}$ to 16 V , all amplifiers disabled, SHDN = $V_- + 2 \text{ V}$		36	45	μA
Z_{SHDN}	Output impedance during shutdown	$V_S = 2.7 \text{ V}$ to 16 V , amplifier disabled		$10 \parallel 2$		$\text{G}\Omega \parallel \text{pF}$
V_{IH}	Logic high threshold voltage (amplifier disabled)	For valid input high, the SHDN pin voltage should be greater than the maximum threshold but less than or equal to V_+		$(V_-) + 1.1 \text{ V}$		V
V_{IL}	Logic low threshold voltage (amplifier enabled)	For valid input low, the SHDN pin voltage should be less than the minimum threshold but greater than or equal to V_-	$(V_-) + 0.2 \text{ V}$			V
t_{ON}	Amplifier enable time (from shutdown) ⁽²⁾	$V_S = \pm 8 \text{ V}$, $G = +1$, $V_{CM} = V_S/2$, $R_L = 10 \text{ k}\Omega$ connected to V_-		5		μs
t_{OFF}	Amplifier disable time ⁽²⁾	$V_S = \pm 8 \text{ V}$, $G = +1$, $V_{CM} = V_S/2$, $R_L = 10 \text{ k}\Omega$ connected to V_-		3		μs
	SHDN pin input bias current (per pin)	$V_S = 2.7 \text{ V}$ to 16 V , $V_+ \geq \text{SHDN} \geq (V_-) + 0.9 \text{ V}$		500	nA	
		$V_S = 2.7 \text{ V}$ to 16 V , $(V_-) \leq \text{SHDN} \leq (V_-) + 0.7 \text{ V}$		400		

(1) Specified by characterization only.

(2) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the SHDN pin and the point at which the output voltage reaches 10% (disable) or 90% (enable) of its final value.

(3) See Figure 6-15 for more information.

6.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ (unless otherwise noted)

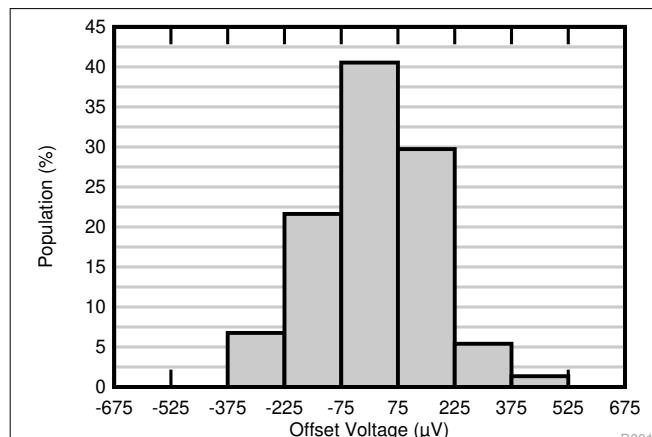


Figure 6-1. Offset Voltage Production Distribution

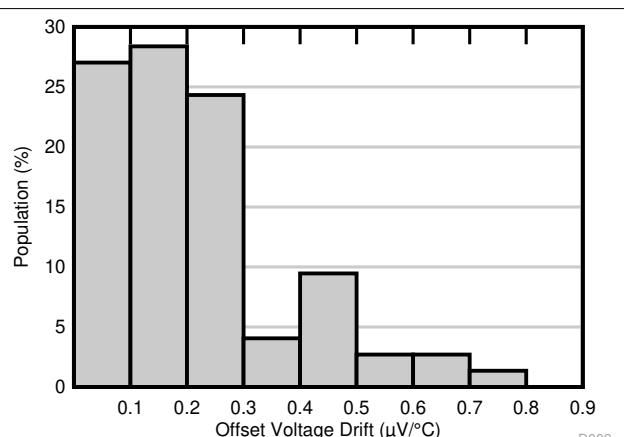


Figure 6-2. Offset Voltage Drift Distribution

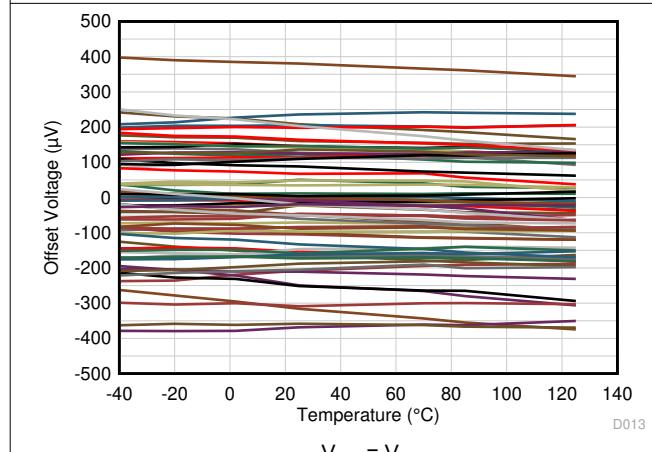


Figure 6-3. Offset Voltage vs Temperature

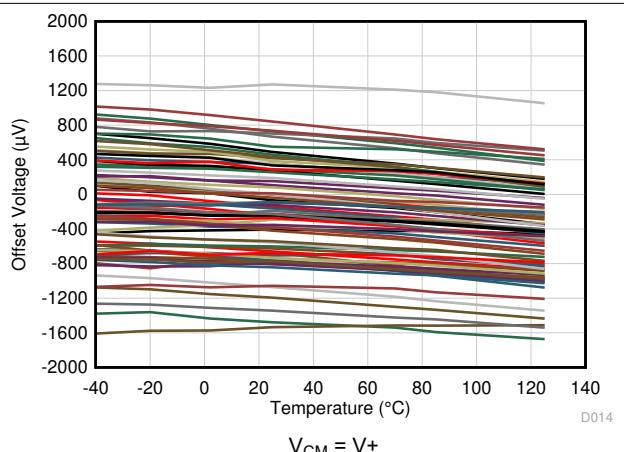


Figure 6-4. Offset Voltage vs Temperature

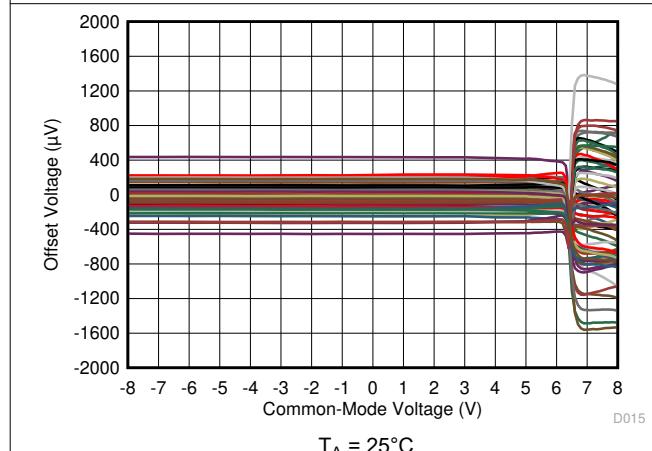


Figure 6-5. Offset Voltage vs Common-Mode Voltage

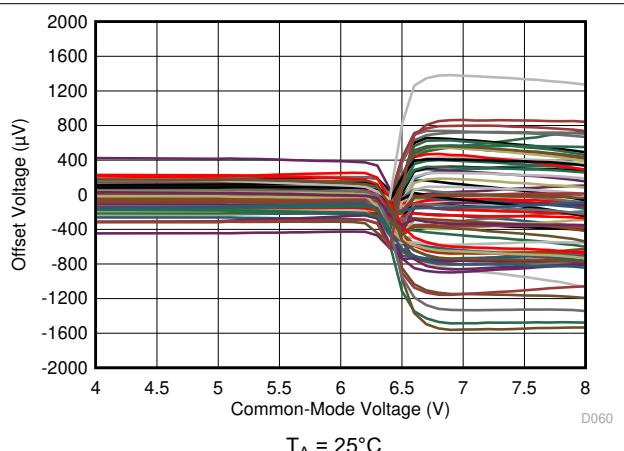


Figure 6-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8 \text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10 \text{ k}\Omega$ (unless otherwise noted)

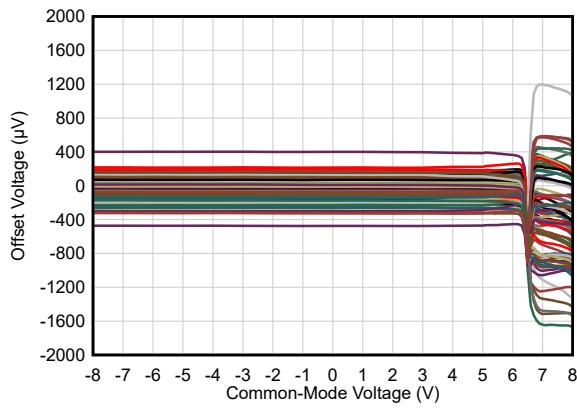


Figure 6-7. Offset Voltage vs Common-Mode Voltage

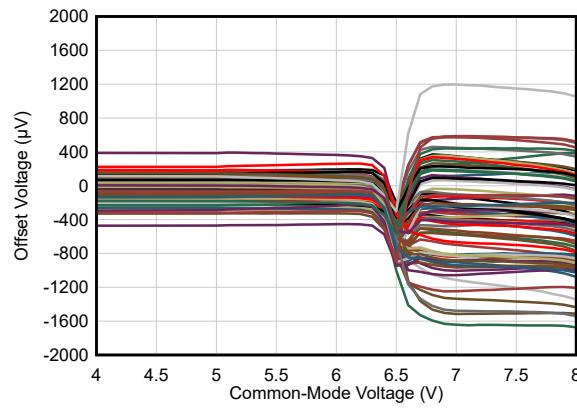


Figure 6-8. Offset Voltage vs Common-Mode Voltage (Transition Region)

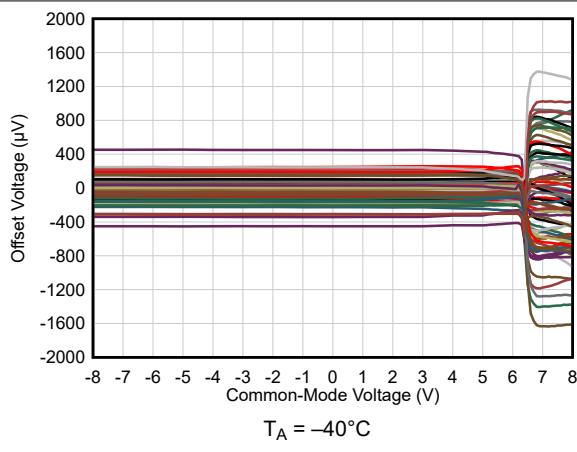


Figure 6-9. Offset Voltage vs Common-Mode Voltage

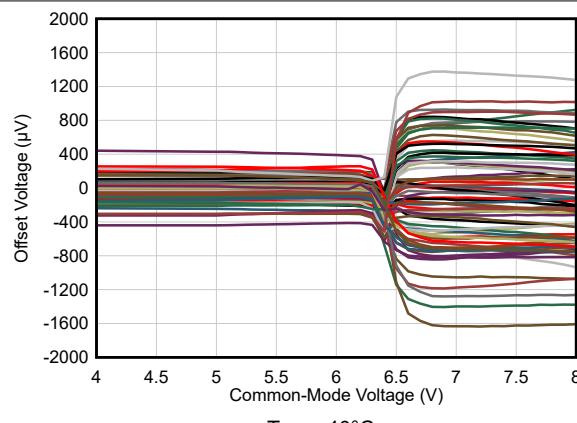


Figure 6-10. Offset Voltage vs Common-Mode Voltage (Transition Region)

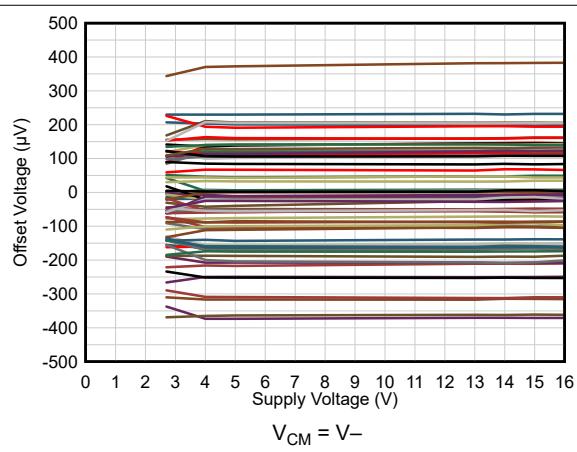


Figure 6-11. Offset Voltage vs Power Supply

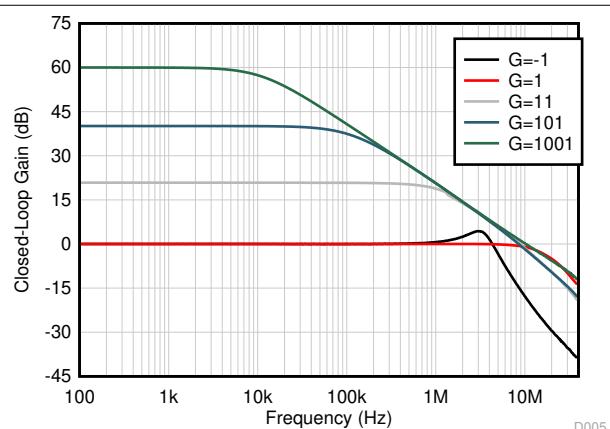


Figure 6-12. Closed-Loop Gain vs Frequency

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ (unless otherwise noted)

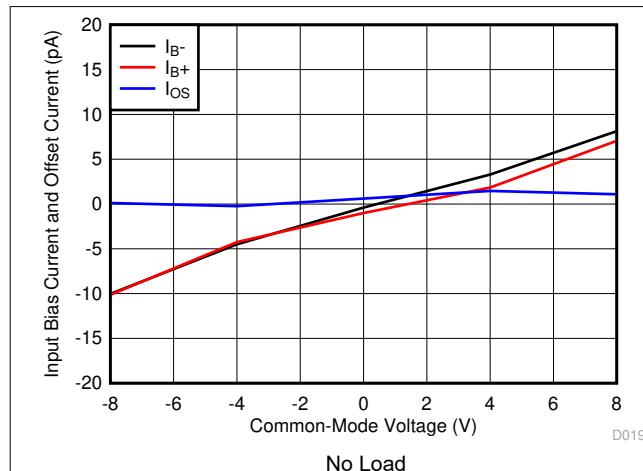


Figure 6-13. Input Bias Current and Offset Current vs Common-Mode Voltage

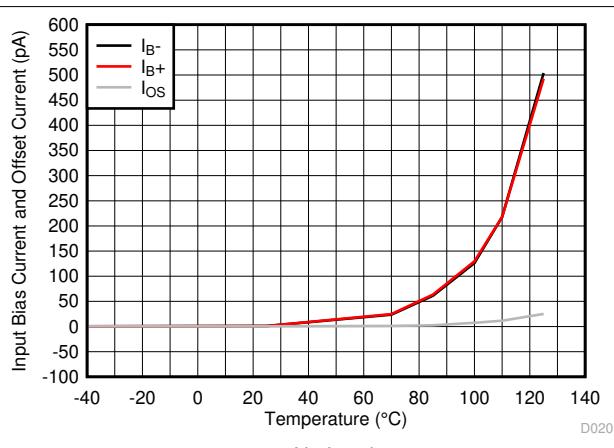


Figure 6-14. Input Bias Current and Offset Current vs Temperature

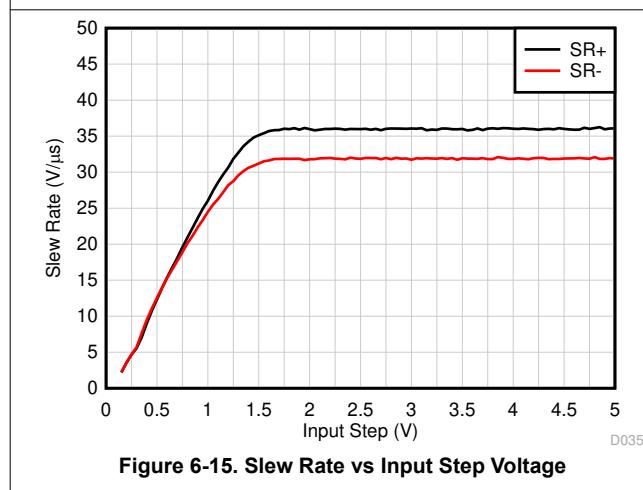


Figure 6-15. Slew Rate vs Input Step Voltage

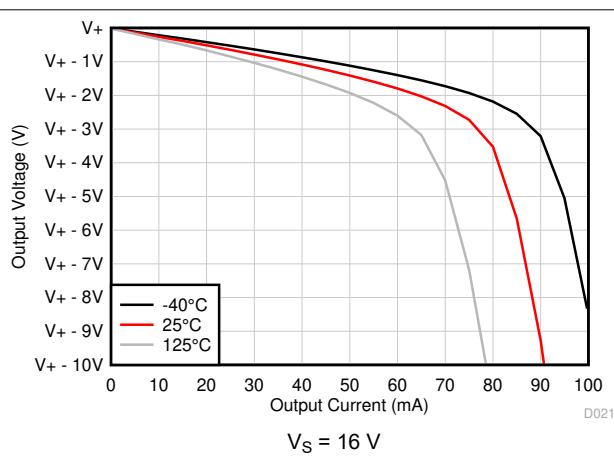


Figure 6-16. Output Voltage Swing vs Output Current (Sourcing)

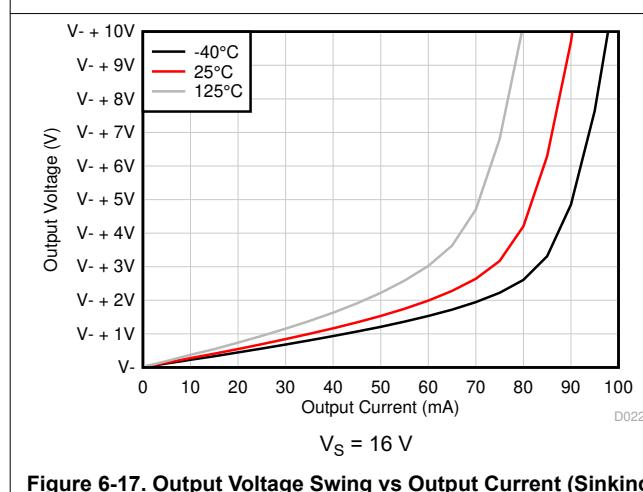


Figure 6-17. Output Voltage Swing vs Output Current (Sinking)

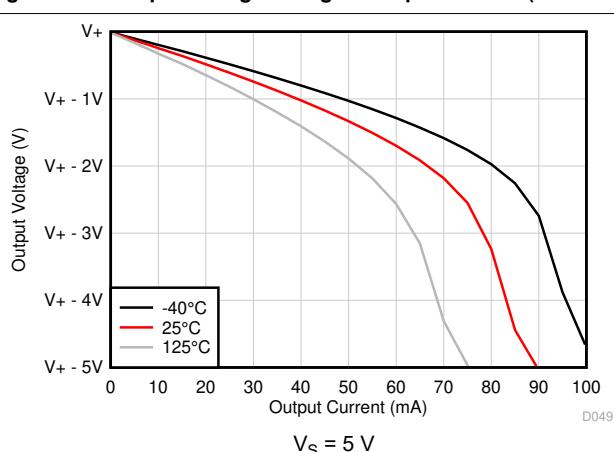


Figure 6-18. Output Voltage Swing vs Output Current (Sourcing)

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ (unless otherwise noted)

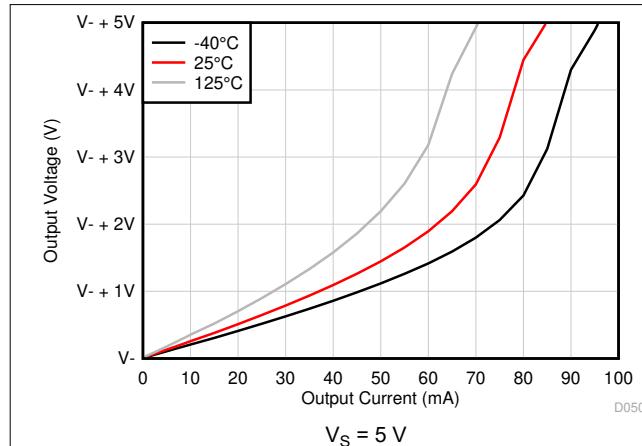


Figure 6-19. Output Voltage Swing vs Output Current (Sinking)

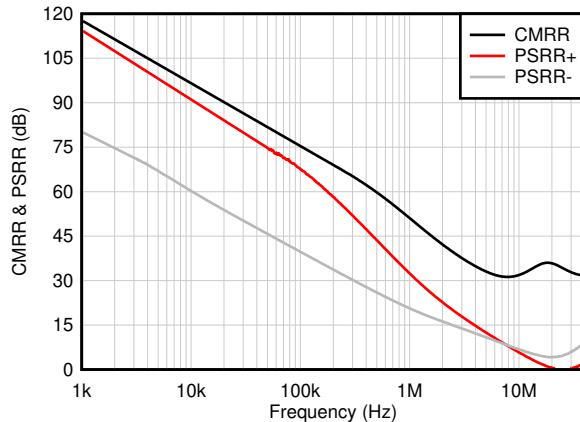


Figure 6-20. CMRR and PSRR vs Frequency

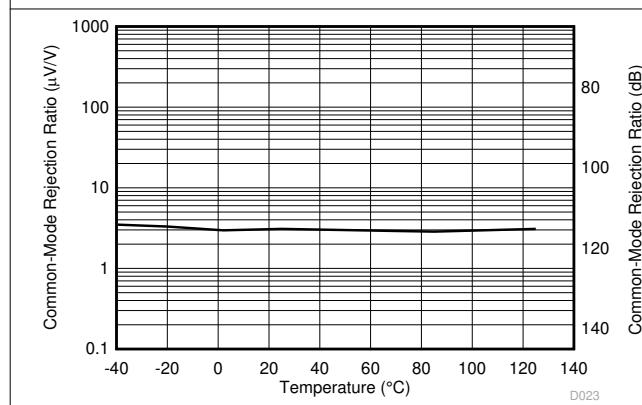


Figure 6-21. CMRR vs Temperature

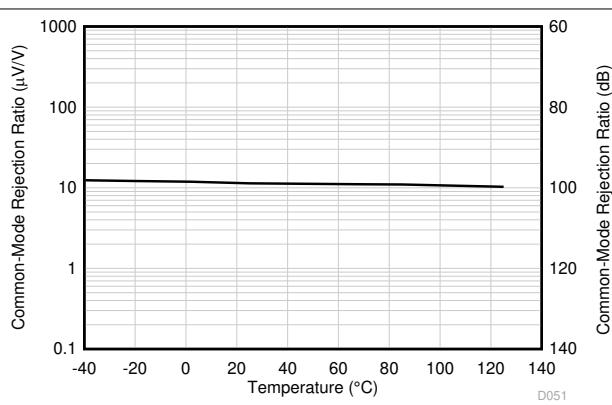


Figure 6-22. CMRR vs Temperature

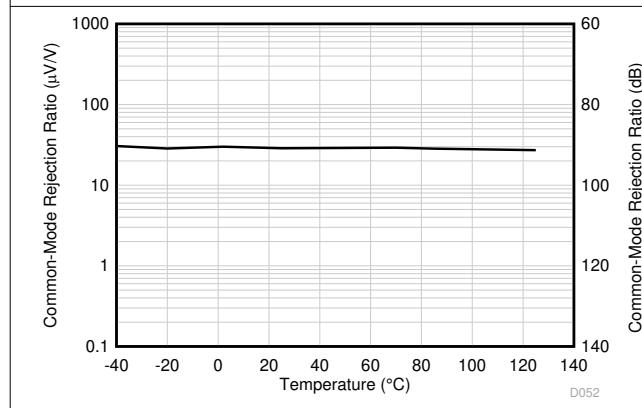


Figure 6-23. CMRR vs Temperature

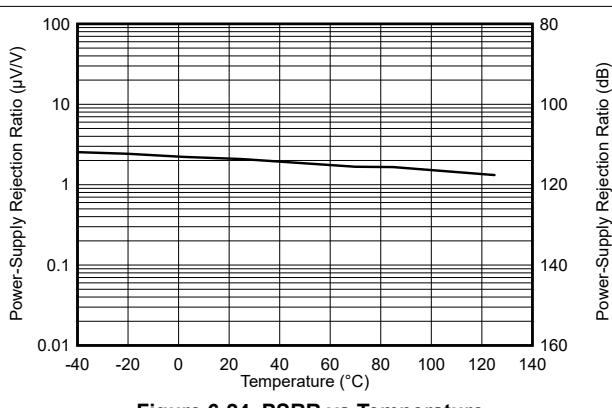


Figure 6-24. PSRR vs Temperature

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ (unless otherwise noted)

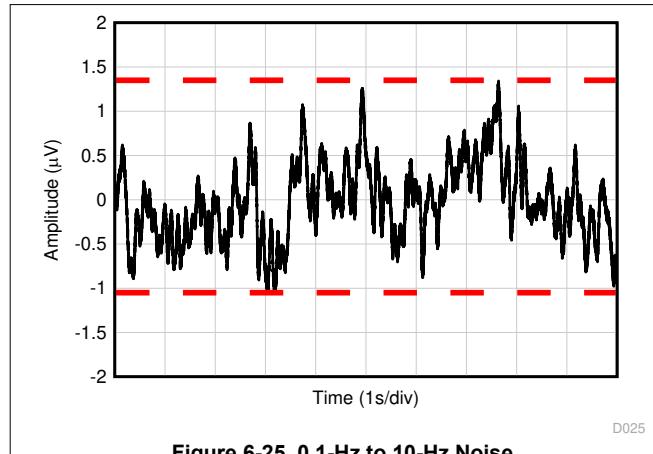


Figure 6-25. 0.1-Hz to 10-Hz Noise

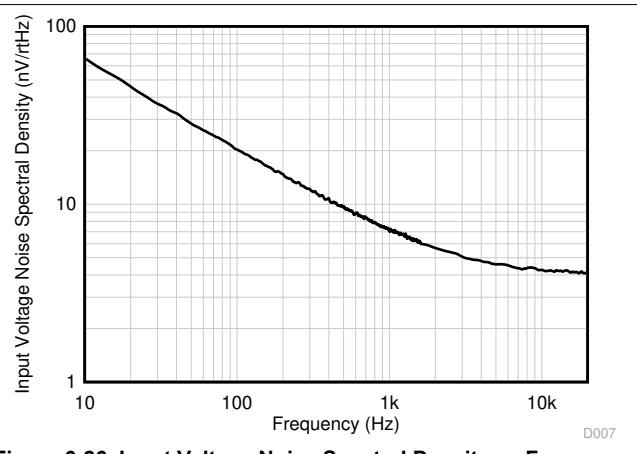


Figure 6-26. Input Voltage Noise Spectral Density vs Frequency

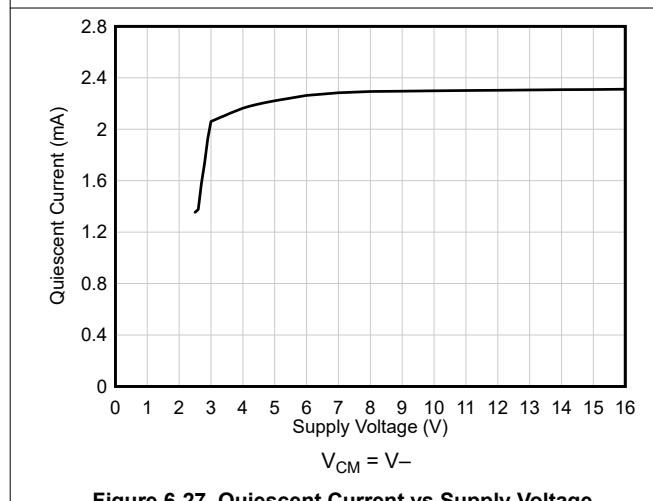


Figure 6-27. Quiescent Current vs Supply Voltage

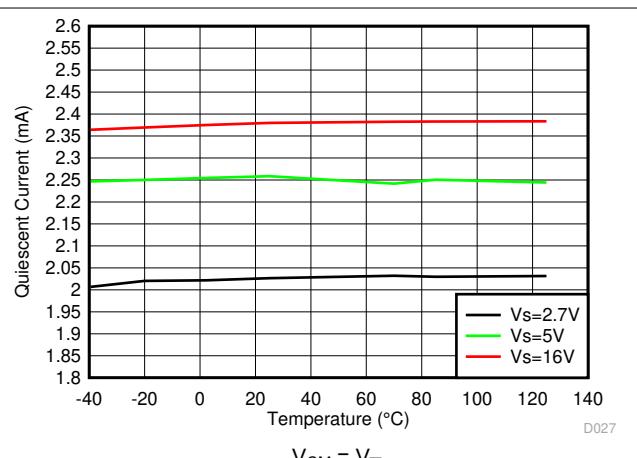


Figure 6-28. Quiescent Current vs Temperature

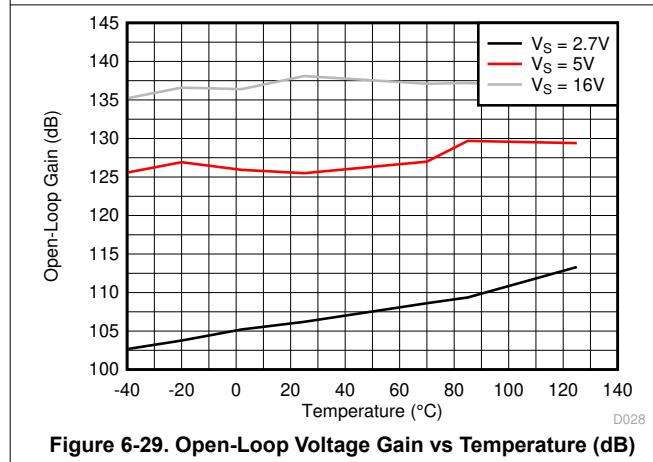


Figure 6-29. Open-Loop Voltage Gain vs Temperature (dB)

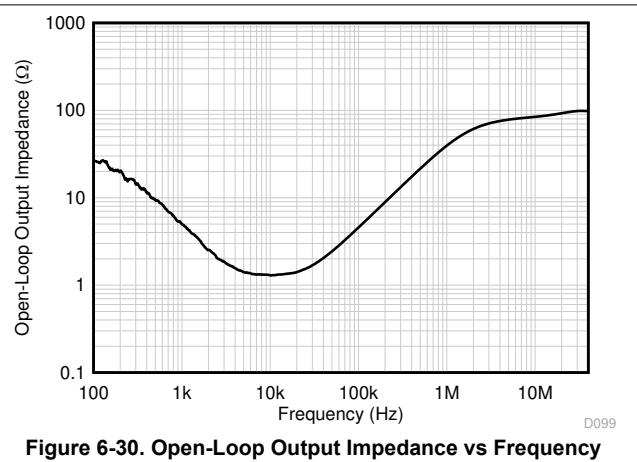


Figure 6-30. Open-Loop Output Impedance vs Frequency

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ (unless otherwise noted)

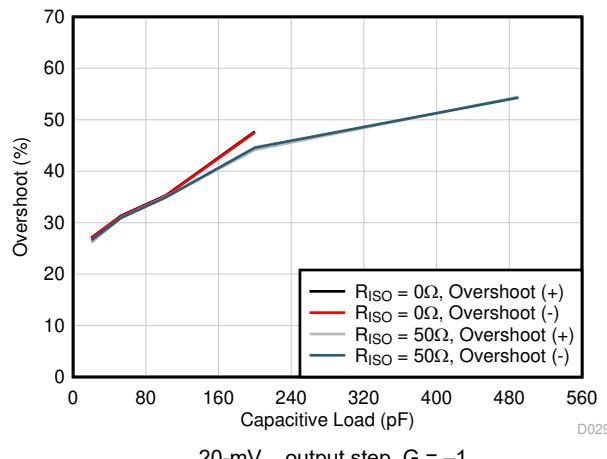


Figure 6-31. Small-Signal Overshoot vs Capacitive Load

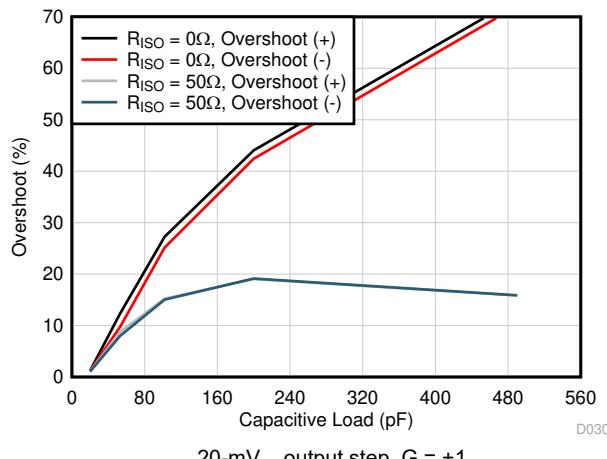


Figure 6-32. Small-Signal Overshoot vs Capacitive Load

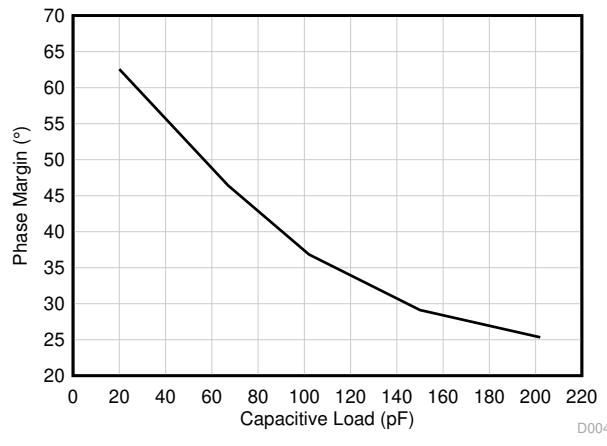


Figure 6-33. Phase Margin vs Capacitive Load

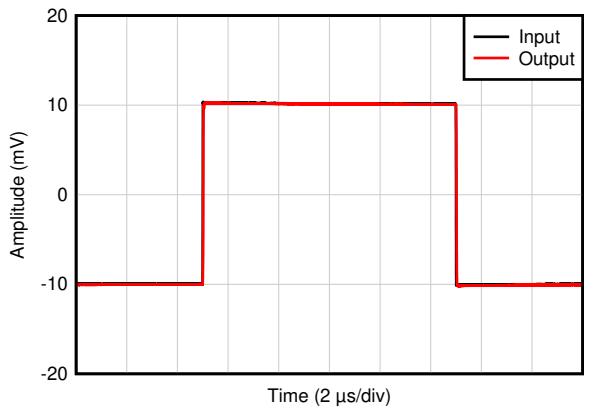


Figure 6-34. Small-Signal Step Response

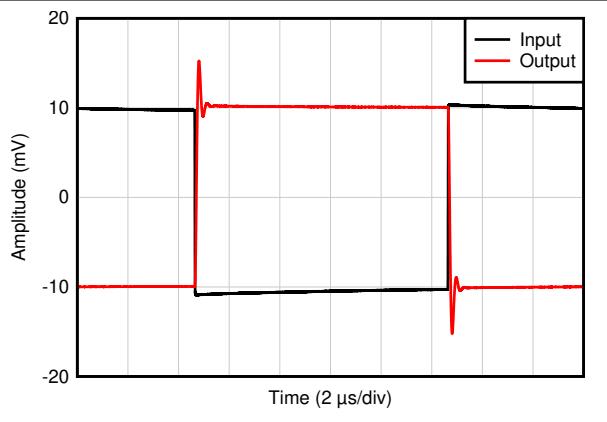


Figure 6-35. Small-Signal Step Response

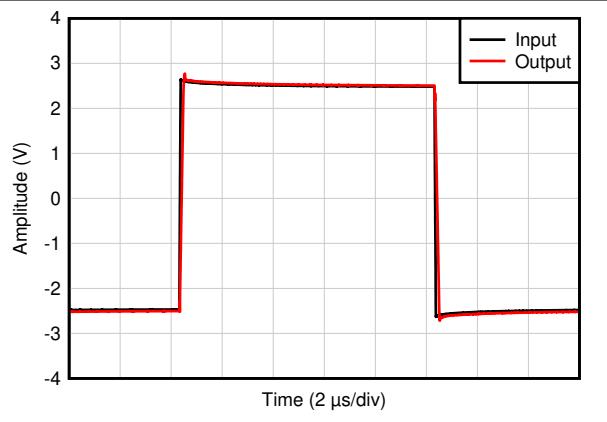
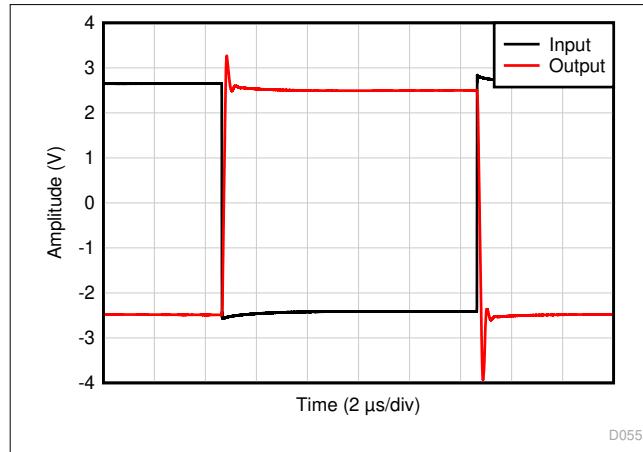


Figure 6-36. Large-Signal Step Response

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ (unless otherwise noted)



$C_L = 20\text{ pF}$, $G = -1$, 5-V_{pp} step response

Figure 6-37. Large-Signal Step Response

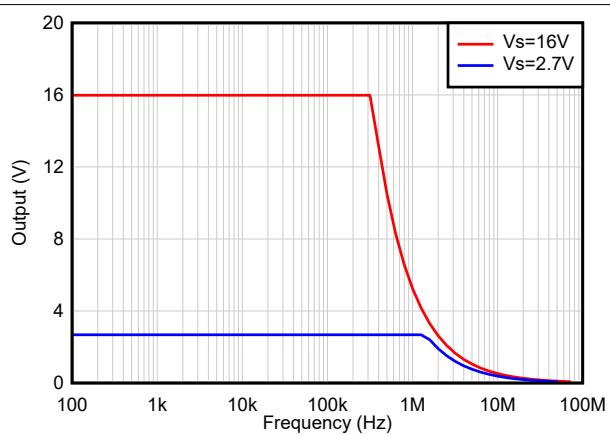


Figure 6-38. Maximum Output Voltage vs Frequency

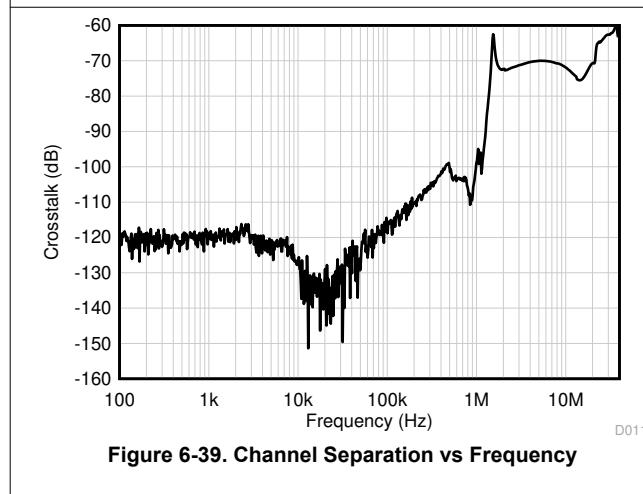


Figure 6-39. Channel Separation vs Frequency

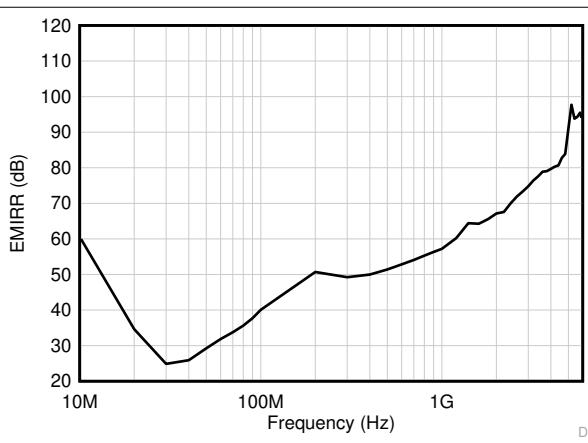


Figure 6-40. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

7 Detailed Description

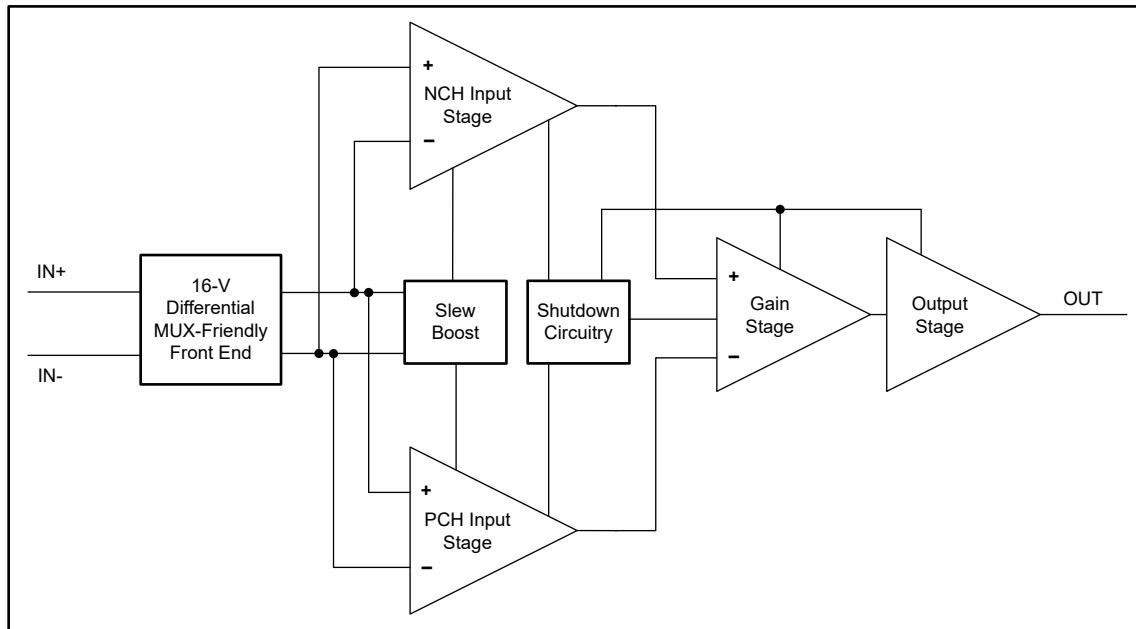
7.1 Overview

The TLV916x family (TLV9161, TLV9162, and TLV9164) is a family of 16-V, general-purpose, operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset ($\pm 210 \mu\text{V}$, typ), low offset drift ($\pm 0.25 \mu\text{V}/^\circ\text{C}$, typ), and 11-MHz bandwidth.

Features such as differential and common-mode input voltage range to the supply rail, high short-circuit current ($\pm 73 \text{ mA}$), high slew rate (33 V/ μs), and shutdown make the TLV916x a flexible, robust, and high-performance operational amplifier for 16-V industrial applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Protection Circuitry

The TLV916x uses a special input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. Figure 7-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 7-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

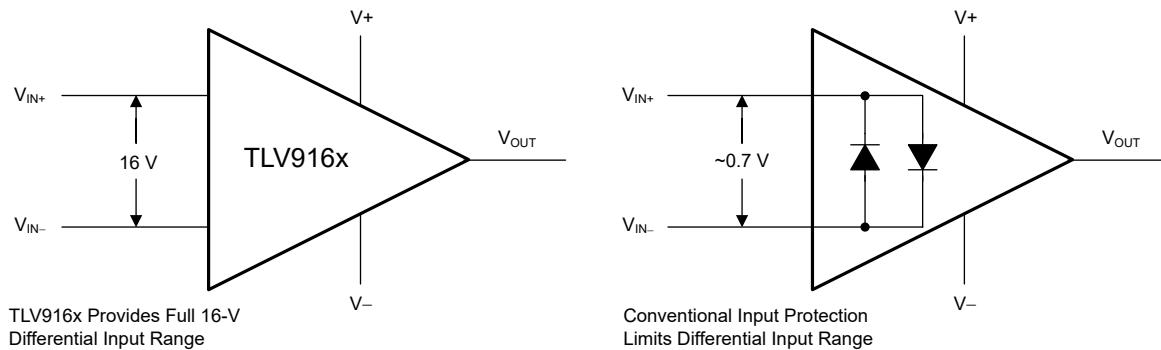


Figure 7-1. TLV916x Input Protection Does Not Limit Differential Input Capability

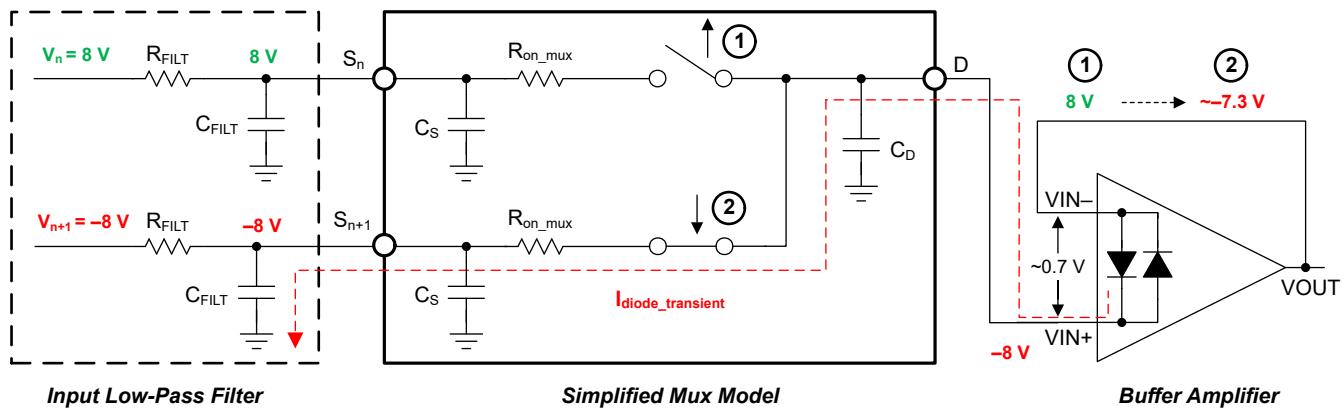


Figure 7-2. Back-to-Back Diodes Create Settling Issues

The TLV916x family of operational amplifiers provides a true high-impedance differential input capability using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The TLV916x tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 16 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; see the TI TechNote [MUX-Friendly Precision Operational Amplifiers](#) for more information.

7.3.2 EMI Rejection

The TLV916x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV916x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 7-3 shows the results of this testing on the TLV916x. Table 7-1 shows the EMIRR IN+ values for the TLV916x at particular frequencies commonly encountered in real-world applications. The [EMI Rejection Ratio of Operational](#)

Amplifiers application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

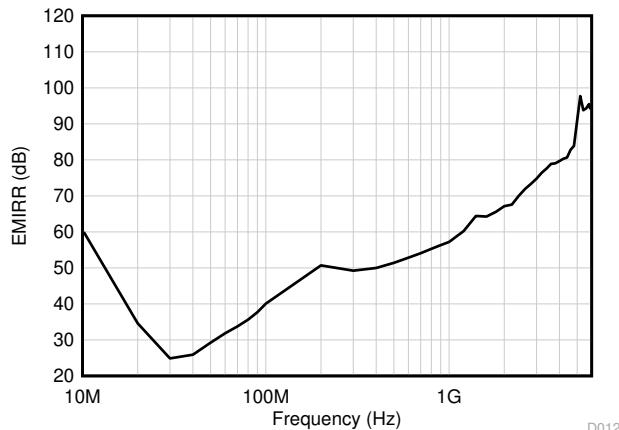


Figure 7-3. EMIRR Testing

Table 7-1. TLV9161 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	50.0 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	56.3 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	65.6 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	70.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	78.9 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	91.0 dB

7.3.3 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the TLV916x is 150°C. Exceeding this temperature causes damage to the device. The TLV916x has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. [Figure 7-4](#) shows an application example for the TLV9162 that has significant self heating because of its power dissipation (0.627 W). In this example, both channels have a quiescent power dissipation while one of the channels has a significant load. Thermal calculations indicate that for an ambient temperature of 60°C, the device junction temperature reaches 175°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. [Figure 7-4](#) shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 5 V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L . If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected. Please note that thermal performance can vary greatly depending on the package selected and the PCB layout design. This example uses the thermal performance of the TSSOP (8) package.

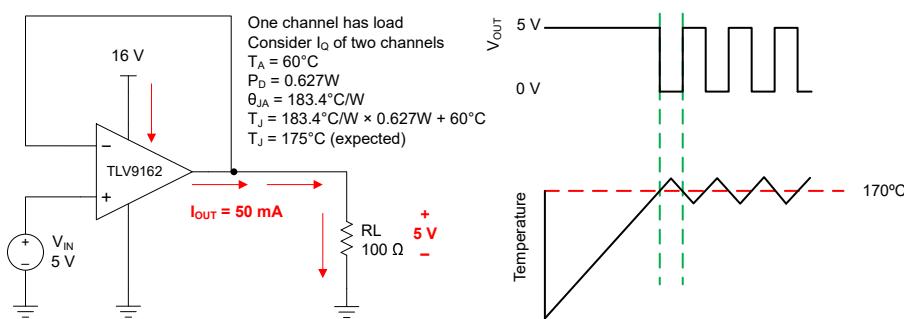


Figure 7-4. Thermal Protection

7.3.4 Capacitive Load and Stability

The TLV916x features an output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive larger capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see [Figure 7-5](#) and [Figure 7-6](#). The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

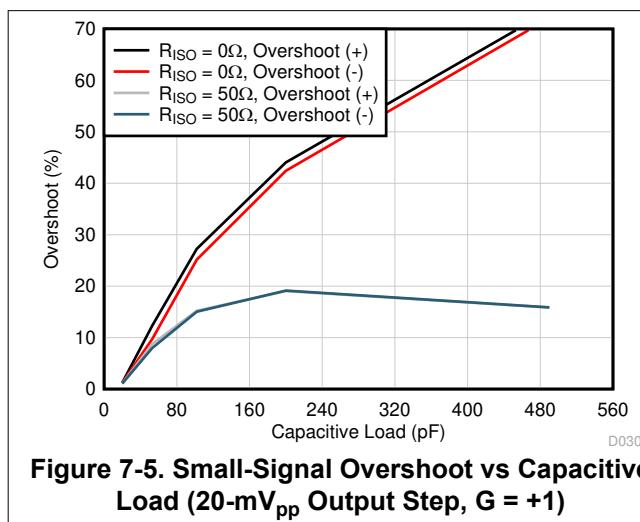


Figure 7-5. Small-Signal Overshoot vs Capacitive Load (20-mV_{pp} Output Step, G = +1)

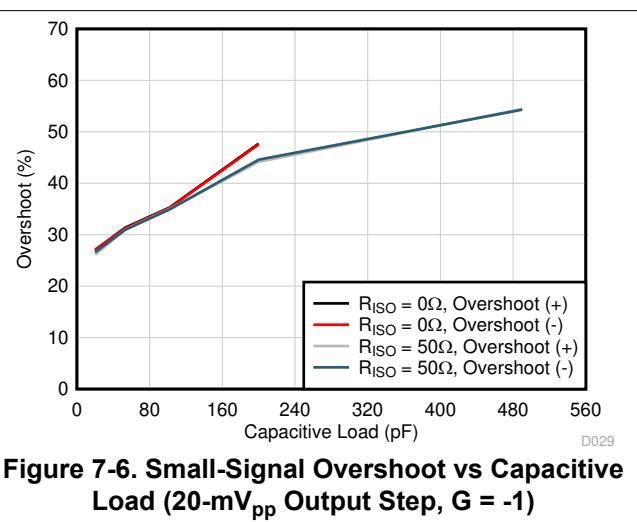


Figure 7-6. Small-Signal Overshoot vs Capacitive Load (20-mV_{pp} Output Step, G = -1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO} , in series with the output, as shown in [Figure 7-7](#). This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L , and is generally negligible at low output levels. A high capacitive load drive makes the TLV916x well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in [Figure 7-7](#) uses an isolation resistor, R_{ISO} , to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

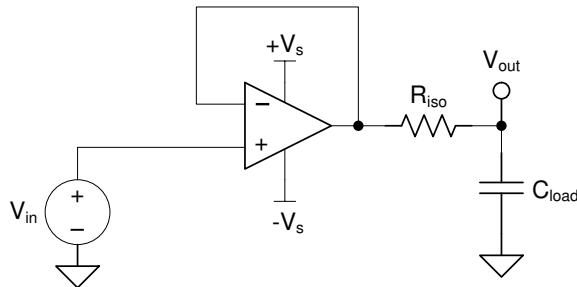


Figure 7-7. Extending Capacitive Load Drive With the TLV9161

7.3.5 Common-Mode Voltage Range

The TLV916x is a 16-V, rail-to-rail input operational amplifier with an input common-mode range that extends to both supply rails. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in [Figure 7-8](#). The N-channel pair is active for input voltages close to the positive rail, typically from $(V_+) - 1\text{ V}$ to the positive supply. The P-channel pair is active for inputs from the negative supply to approximately $(V_+) - 2\text{ V}$. There is a small transition region, typically $(V_+) - 2\text{ V}$ to $(V_+) - 1\text{ V}$ in which both input pairs are on. This transition region can vary modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

[Figure 6-5](#) shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see [Op Amps With Complementary-Pair Input Stages](#) application note.

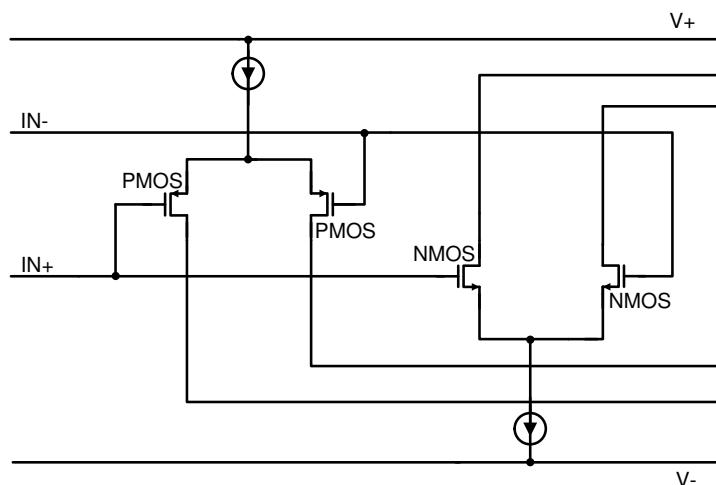


Figure 7-8. Rail-to-Rail Input Stage

7.3.6 Phase Reversal Protection

The TLV916x family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLV916x is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. For more information on phase reversal, see [Op Amps With Complementary-Pair Input Stages](#) application note.

7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 7-9 shows an illustration of the ESD circuits contained in the TLV916x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

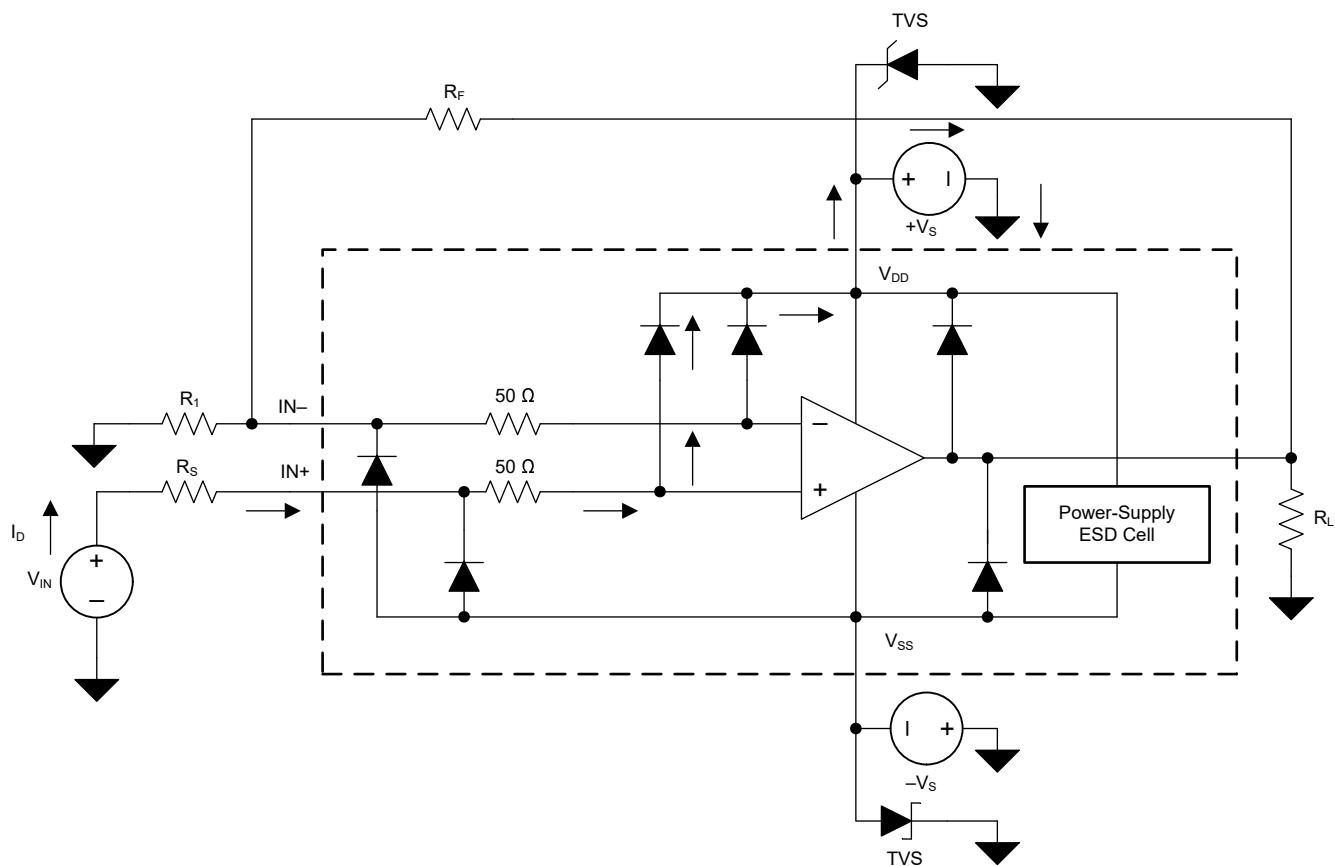


Figure 7-9. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example; 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

7.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV916x is approximately 120 ns.

7.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* ("bell curve"), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the [Electrical Characteristics](#) table.

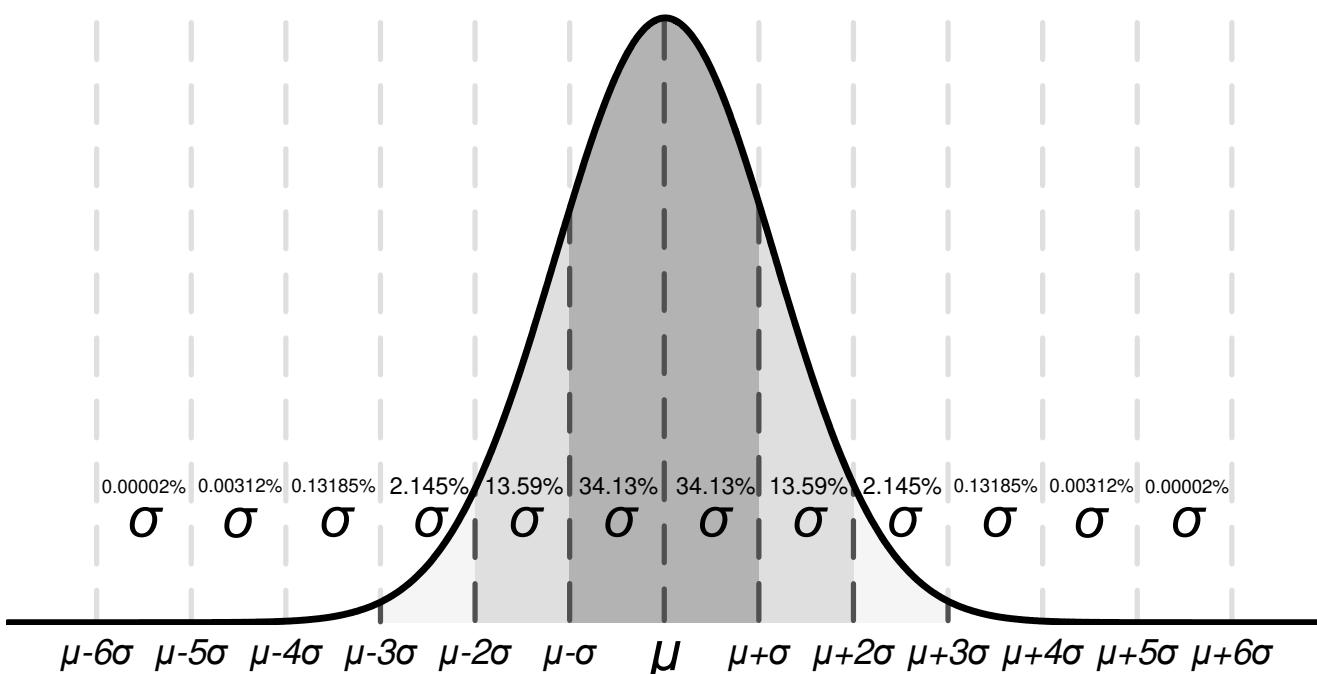


Figure 7-10. Ideal Gaussian Distribution

Figure 7-10 shows an example distribution, where μ , or *mu*, is the mean of the distribution, and where σ , or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the [Electrical Characteristics](#) table are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation ($\mu + \sigma$) in order to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for TLV916x, the typical input voltage offset is 210 μ V, so 68.2% of all TLV916x devices are expected to have an offset from

–210 μ V to 210 μ V. At 4 σ ($\pm 840 \mu$ V), 99.9937% of the distribution has an offset voltage less than $\pm 840 \mu$ V, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the TLV916x family has a maximum offset voltage of 1 mV at 25°C, and even though this corresponds to about 5- σ (≈ 1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 1 mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6- σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the TLV916x family does not have a maximum or minimum for offset voltage drift, but based on the typical value of 0.25 μ V/°C in the [Electrical Characteristics](#) table, it can be calculated that the 6- σ value for offset voltage drift is about 1.5 μ V/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

7.3.10 Packages With an Exposed Thermal Pad

The TLV916x family is available in the WSON-8 (DSG) package which features an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other than V– is not allowed, and performance of the device is not assured when doing so.

7.3.11 Shutdown

The TLV916xS devices feature one or more shutdown pins (SHDN) that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes about 36 μ A. The SHDN pins are active high, meaning that shutdown mode is enabled when the input to the SHDN pin is a valid logic high. The amplifier is enabled when the input to the SHDN pin is a valid logic low.

The SHDN pins are referenced to the negative supply rail of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the SHDN pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1.1 V and V+. The shutdown pin circuitry includes a pull-down resistor, which will inherently pull the voltage of the pin to the negative supply rail if not driven. Thus, to enable the amplifier, the SHDN pins should either be left floating or driven to a valid logic low. To disable the amplifier, the SHDN pins must be driven to a valid logic high. The maximum voltage allowed at the SHDN pins is V+. Exceeding V+ will damage the device.

The SHDN pins are high-impedance CMOS inputs. Channels of single and dual op amp packages are independently controlled, and channels of quad op amp packages are controlled in pairs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The typical enable time out of shutdown is 5 μ s; disable time is 3 μ s. When disabled, the output assumes a high-impedance state. This architecture allows the TLV916xS family to operate as a gated amplifier, multiplexer, or programmable-gain amplifier. Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-k Ω load to V– is required. If using the TLV916xS without a load, the resulting turnoff time significantly increases.

7.4 Device Functional Modes

The TLV916x has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (± 1.35 V). The maximum power supply voltage for the TLV916x is 16 V (± 8 V).

The TLV916xS devices feature a shutdown pin, which can be used to place the op amp into a low-power mode. See [Shutdown](#) section for more information.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TLV916x family offers excellent DC precision and AC performance. These devices operate up to 16-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 11-MHz bandwidth and high output drive. These features make the TLV916x a robust, high-performance operational amplifier for 16-V industrial applications.

8.2 Typical Applications

8.2.1 Low-Side Current Measurement

Figure 8-1 shows the TLV9161 configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 8-1 including theory, calculations, simulations, and measured data, see TI Precision Design [TIPD129, 0-A to 1-A Single-Supply Low-Side Current-Sensing Solution](#).

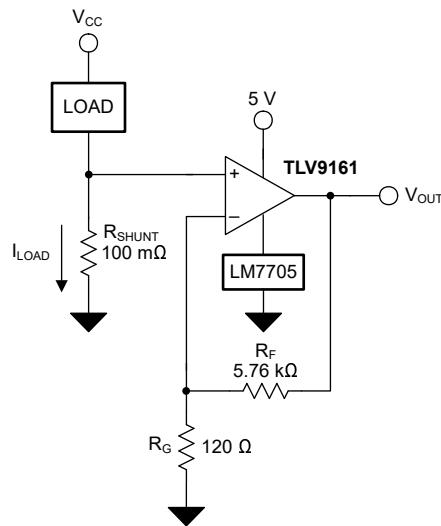


Figure 8-1. TLV9161 in a Low-Side, Current-Sensing Application

8.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

8.2.1.2 Detailed Design Procedure

The transfer function of the circuit in [Figure 8-1](#) is given in [Equation 1](#).

$$V_{\text{OUT}} = I_{\text{LOAD}} \times R_{\text{SHUNT}} \times \text{Gain} \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using [Equation 2](#).

$$R_{\text{SHUNT}} = \frac{V_{\text{SHUNT_MAX}}}{I_{\text{LOAD_MAX}}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

Using [Equation 2](#), R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV9161 to produce an output voltage of 0 V to 4.9 V. The gain needed by the TLV9161 to produce the necessary output voltage is calculated using [Equation 3](#).

$$\text{Gain} = \frac{(V_{\text{OUT_MAX}} - V_{\text{OUT_MIN}})}{(V_{\text{IN_MAX}} - V_{\text{IN_MIN}})} \quad (3)$$

Using [Equation 3](#), the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G . [Equation 4](#) is used to size the resistors, R_F and R_G , to set the gain of the TLV9161 to 49 V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing R_F as 5.76 kΩ, R_G is calculated to be 120 Ω. R_F and R_G were chosen as 5.76 kΩ and 120 Ω because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. However, excessively large resistors will generate thermal noise that exceeds the intrinsic noise of the op amp [Figure 8-2](#) shows the measured transfer function of the circuit shown in [Figure 8-1](#).

8.2.1.3 Application Curve

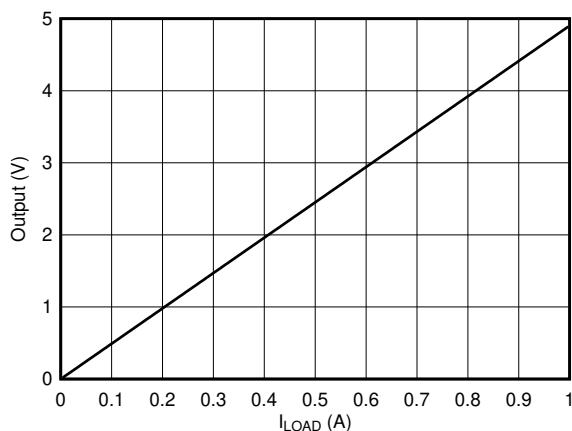


Figure 8-2. Low-Side, Current-Sense, Transfer Function

8.2.2 Buffered Multiplexer

The TLV916xS shutdown devices can be configured to create a buffered multiplexer. Outputs can be connected together on a common bus and the shutdown pins can be used to select the desired channel to pass through. Since the amplifier circuitry has been designed such that disable transitions occur faster than enable transitions, the amplifier naturally exhibits a "break before make" switch topology. Amplifier outputs enter a high impedance state when placed in shutdown, so there is no risk of bus contention when connecting multiple channel outputs together. Additionally, because outputs are isolated from inputs, there is no concern about the impedance at the input of each channel interacting undesirably with the impedance at the output, like an amplifier gain stage or ADC driver circuit. Also, because this topology uses amplifiers instead of MOSFET switches, other common issues with multiplexers such as charge injection or signal error due to R_{ON} effects are eliminated.

Figure 8-3 shows an example topology for a basic 2:1 multiplexer. When SEL is low, channel 1 is selected and active; when SEL is high, channel 2 is selected and active. For more information on how to use the TLV916xS shutdown function, see the shutdown section in [Section 7.3.11](#)

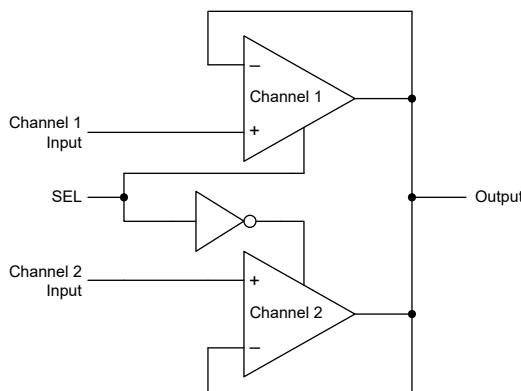


Figure 8-3. Precision Reference Buffer

9 Power Supply Recommendations

The TLV916x is specified for operation from 2.7 V to 16 V (± 1.35 V to ± 8 V); many specifications apply from -40°C to 125°C or with specific supply voltage and test conditions.

CAUTION

Supply voltages larger than 20 V can permanently damage the device; see the [Absolute Maximum Ratings](#) section.

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout](#) section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 10-2](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

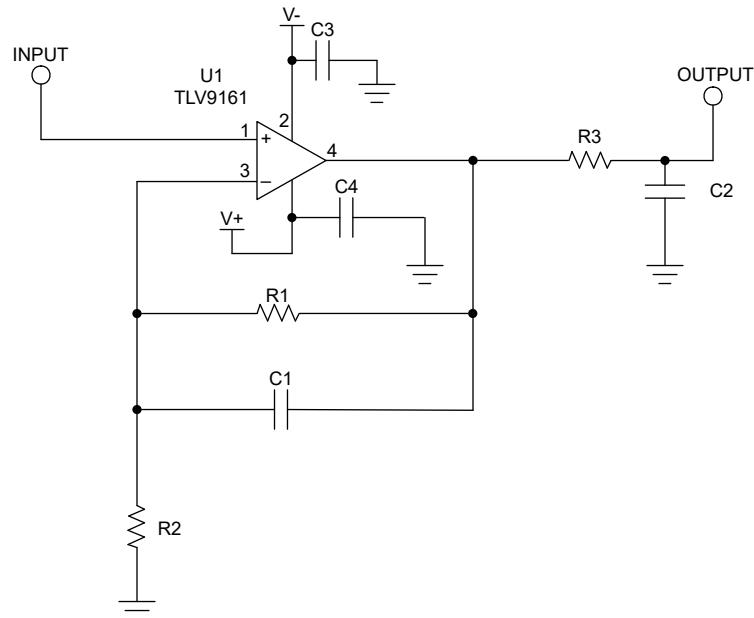


Figure 10-1. Schematic for Noninverting Configuration Layout Example

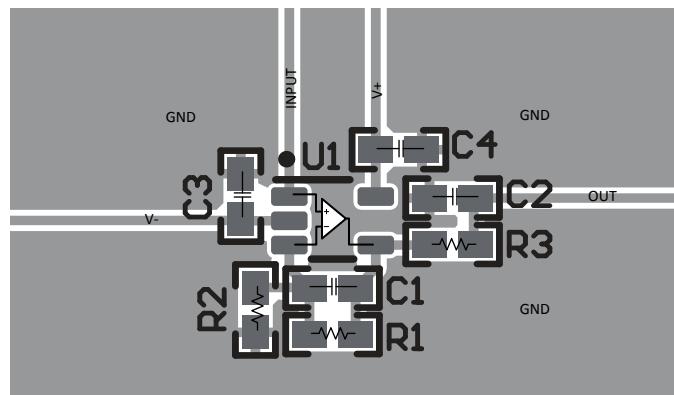


Figure 10-2. Operational Amplifier Board Layout for Noninverting Configuration - SC70 (DCK) Package

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

11.2 Documentation Support

11.2.1 Related Documentation

Texas Instruments, [Analog Engineer's Circuit Cookbook: Amplifiers](#)

Texas Instruments, [AN31 amplifier circuit collection](#) application note

Texas Instruments, [MUX-Friendly, Precision Operational Amplifiers](#) application brief

Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers](#) application note

Texas Instruments, [Op Amps With Complementary-Pair Input Stages](#) application note

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9161IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T61DB	Samples
TLV9161IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1JT	Samples
TLV9161SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T91SD	Samples
TLV9162IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2ICF	Samples
TLV9162IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2JVT	Samples
TLV9162IDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9162D	Samples
TLV9162IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HZH	Samples
TLV9162IPWR	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9162P	Samples
TLV9164IDR	ACTIVE	SOIC	D	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9164D	Samples
TLV9164IPWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9164PW	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

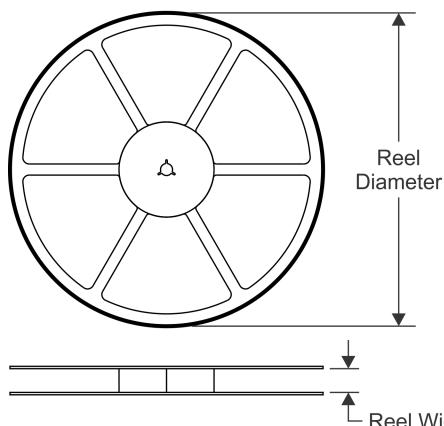
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

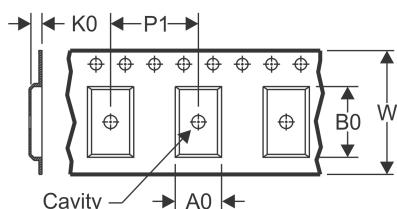
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

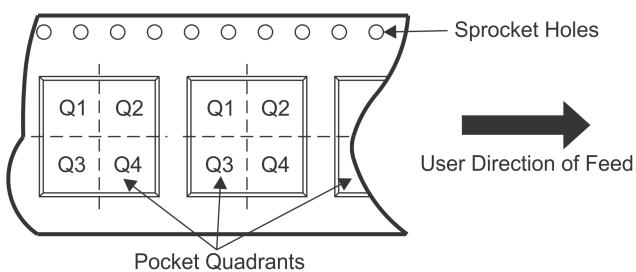


TAPE DIMENSIONS



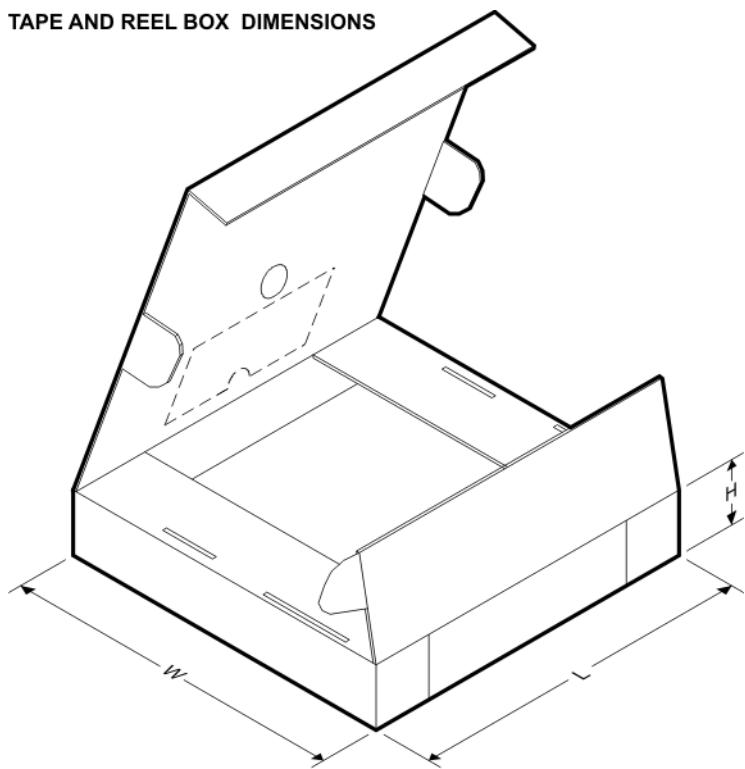
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9161IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9161IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9161SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9162IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9162IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9162IPWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9164IDR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9164IPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

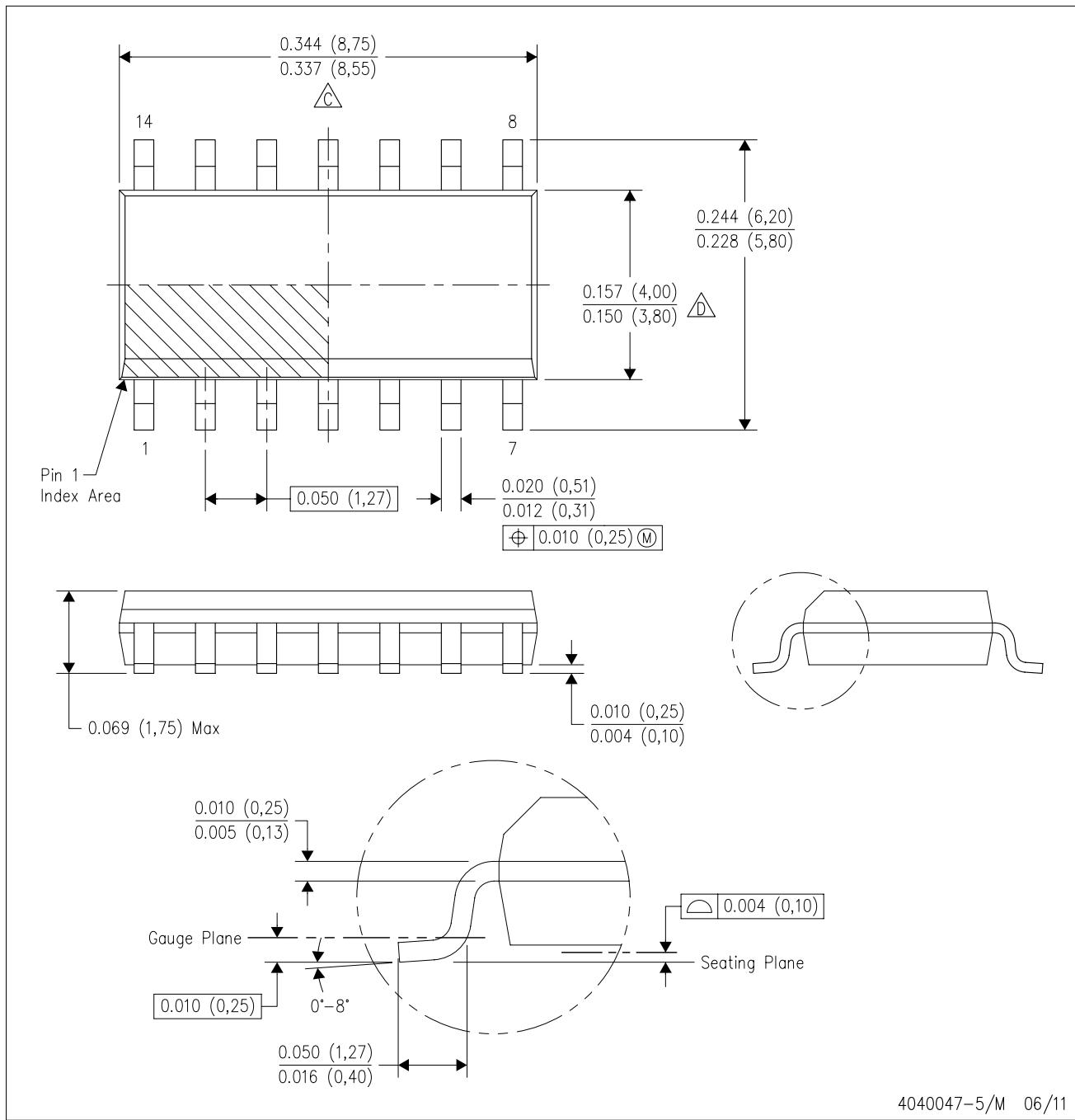
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9161IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9161IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV9161SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9162IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9162IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9162IPWR	TSSOP	PW	8	3000	853.0	449.0	35.0
TLV9164IDR	SOIC	D	14	3000	853.0	449.0	35.0
TLV9164IPWR	TSSOP	PW	14	3000	853.0	449.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

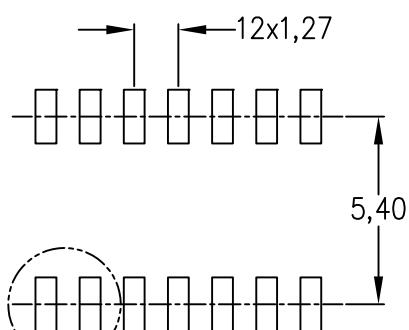
E. Reference JEDEC MS-012 variation AB.

LAND PATTERN DATA

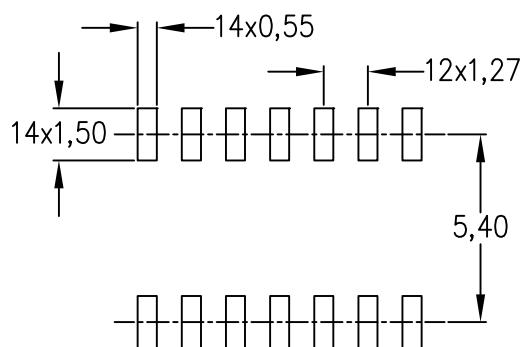
D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

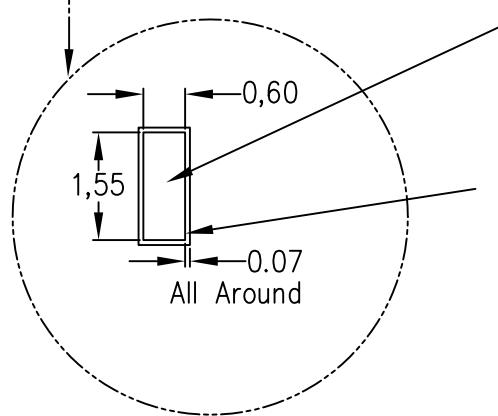
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Example
Non Soldermask Defined Pad



Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

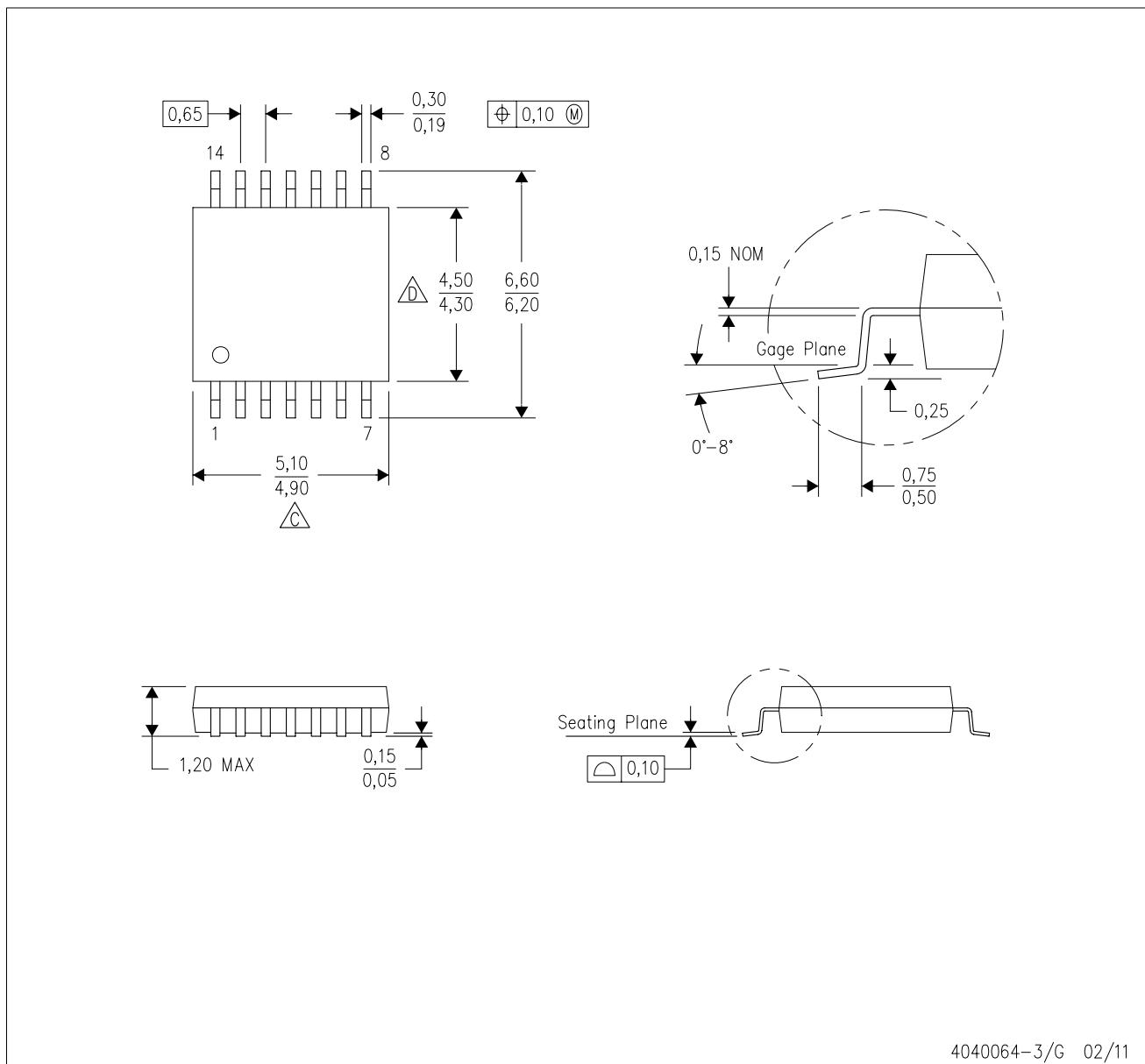
4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

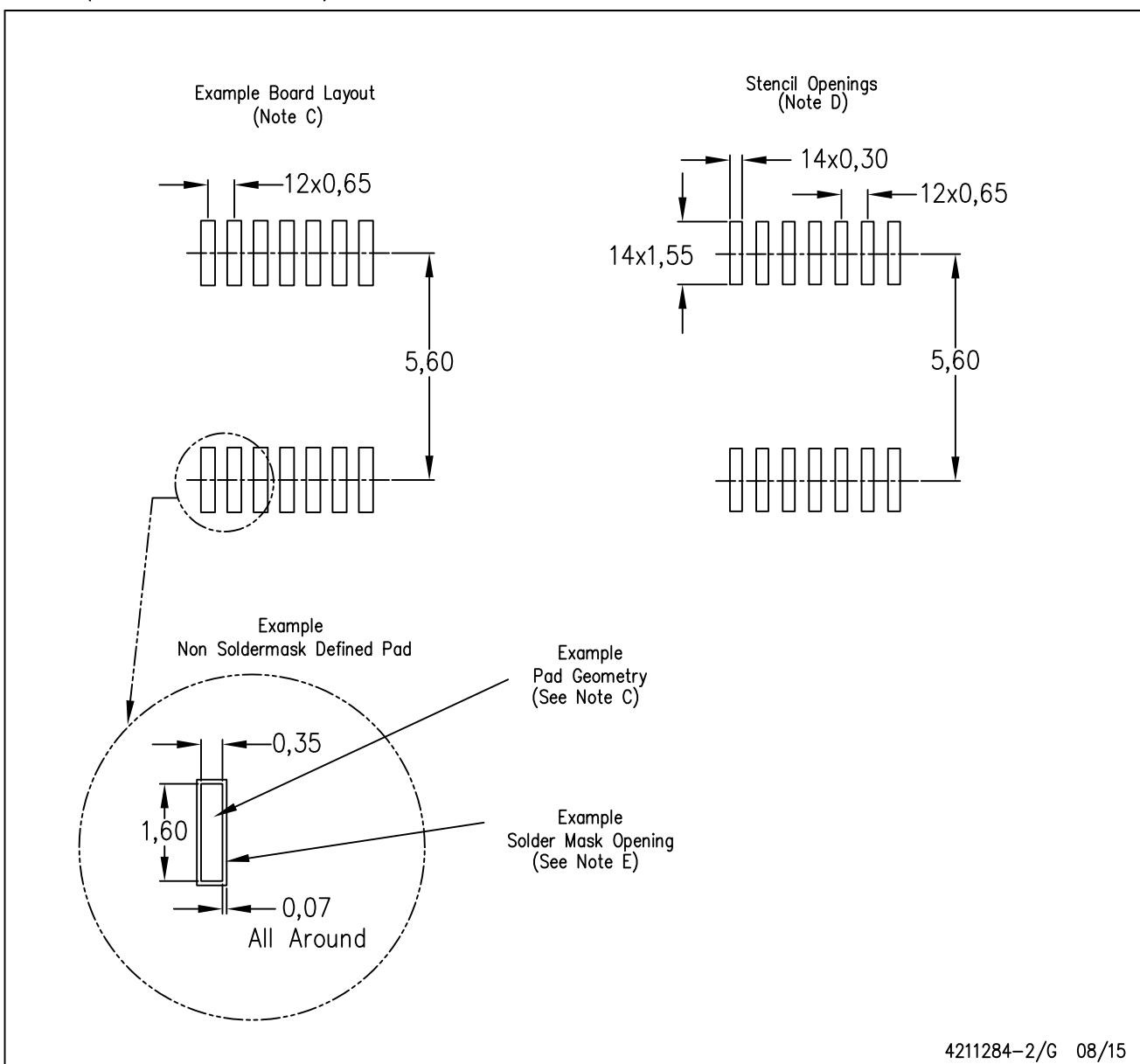
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

LAND PATTERN DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

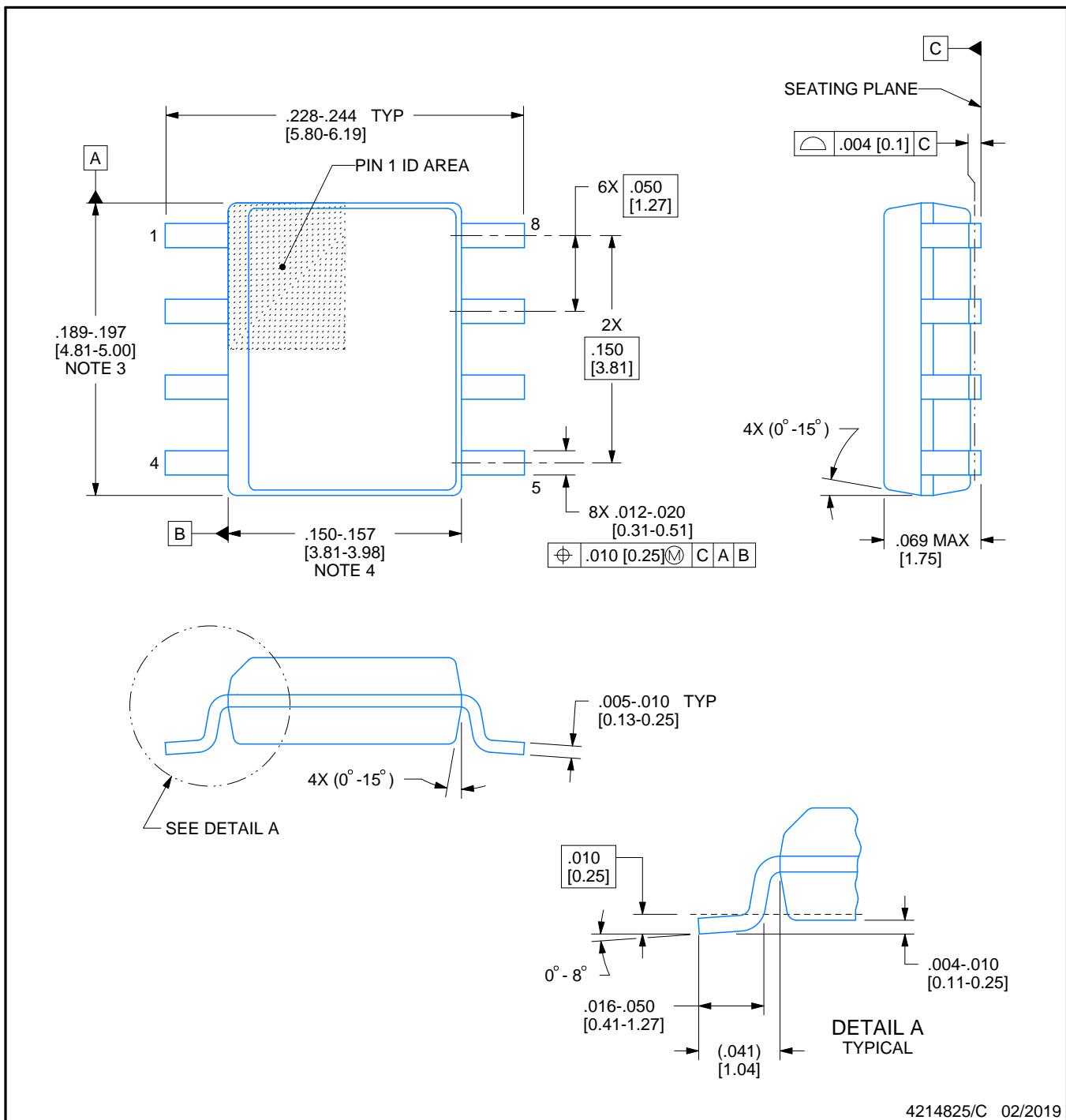
D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

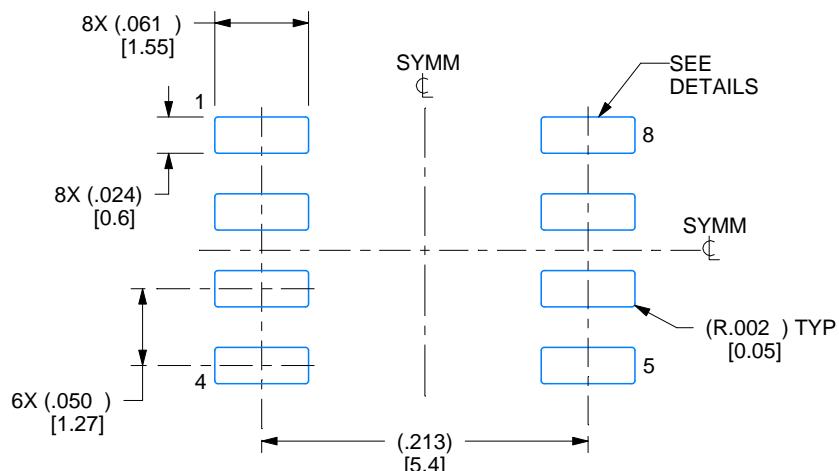
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

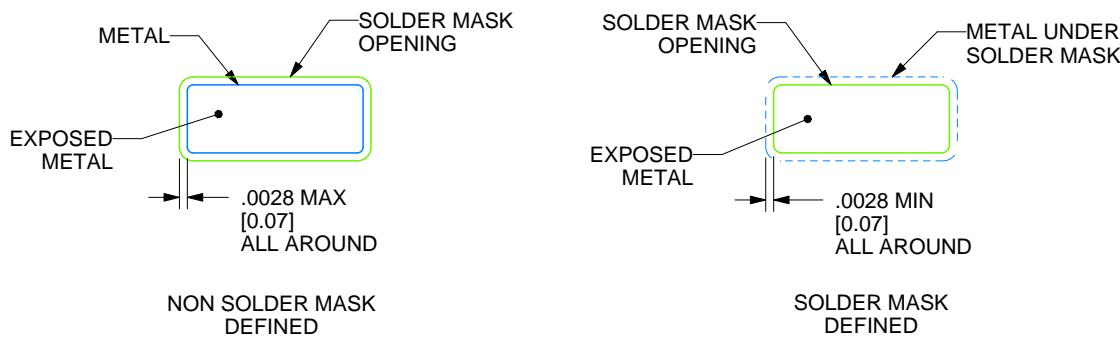
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

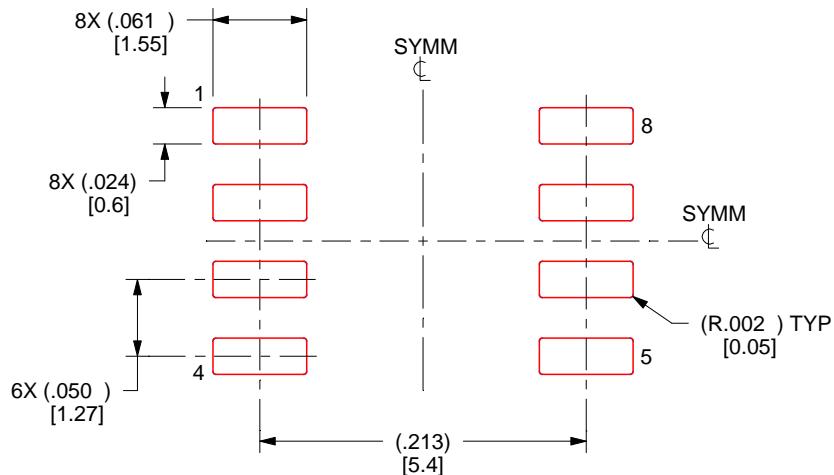
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

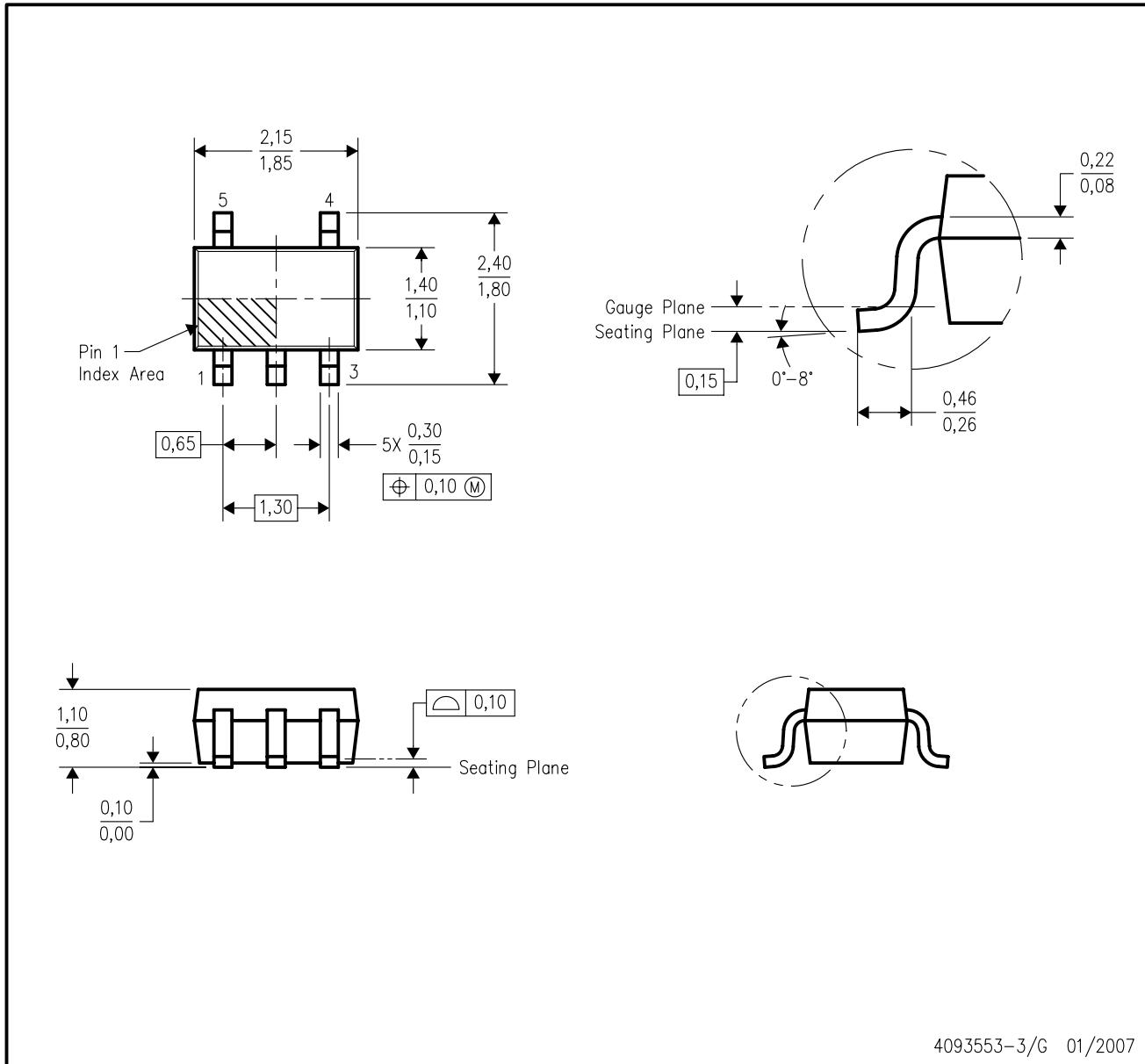
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

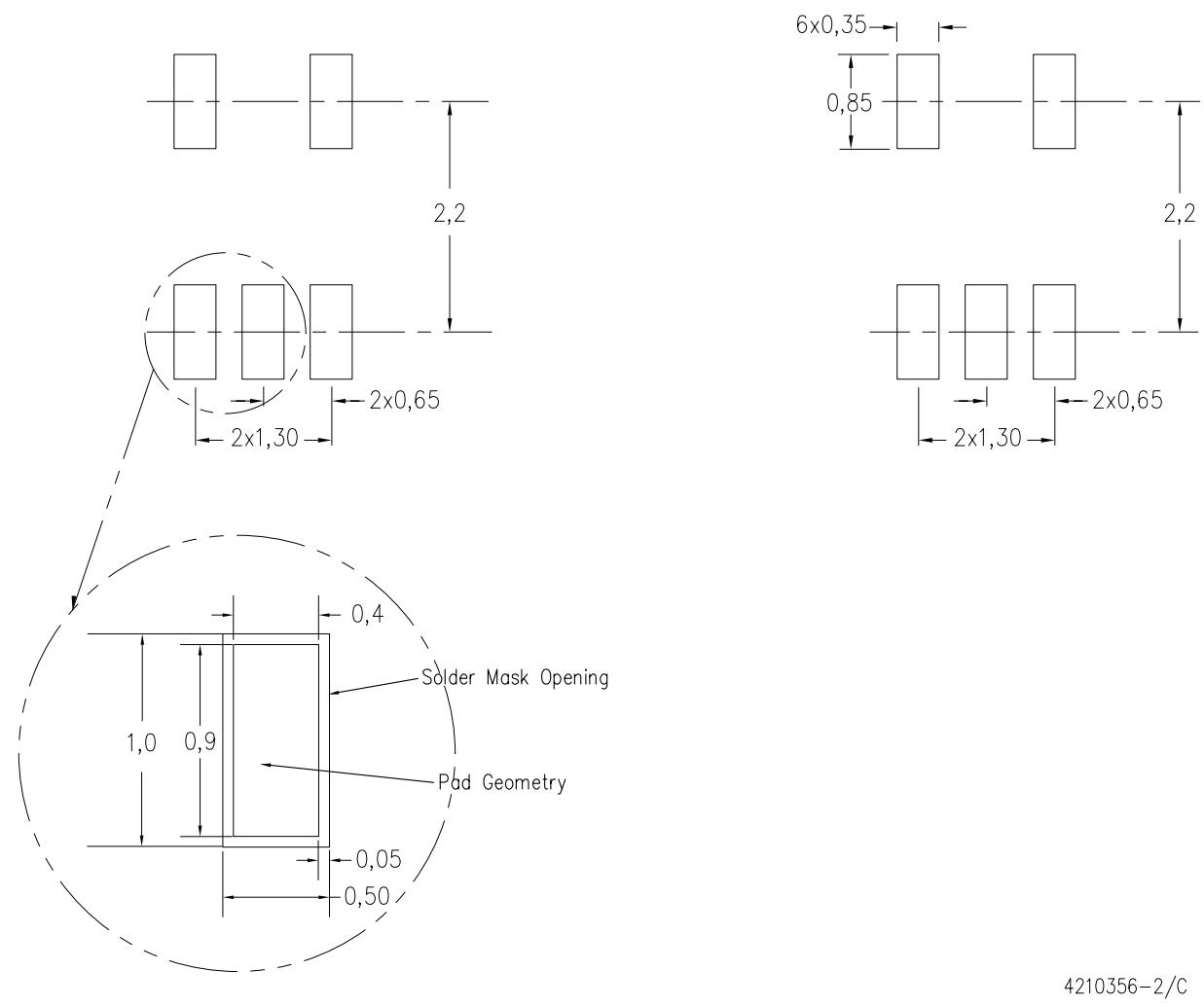
LAND PATTERN DATA

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



4210356-2/C 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

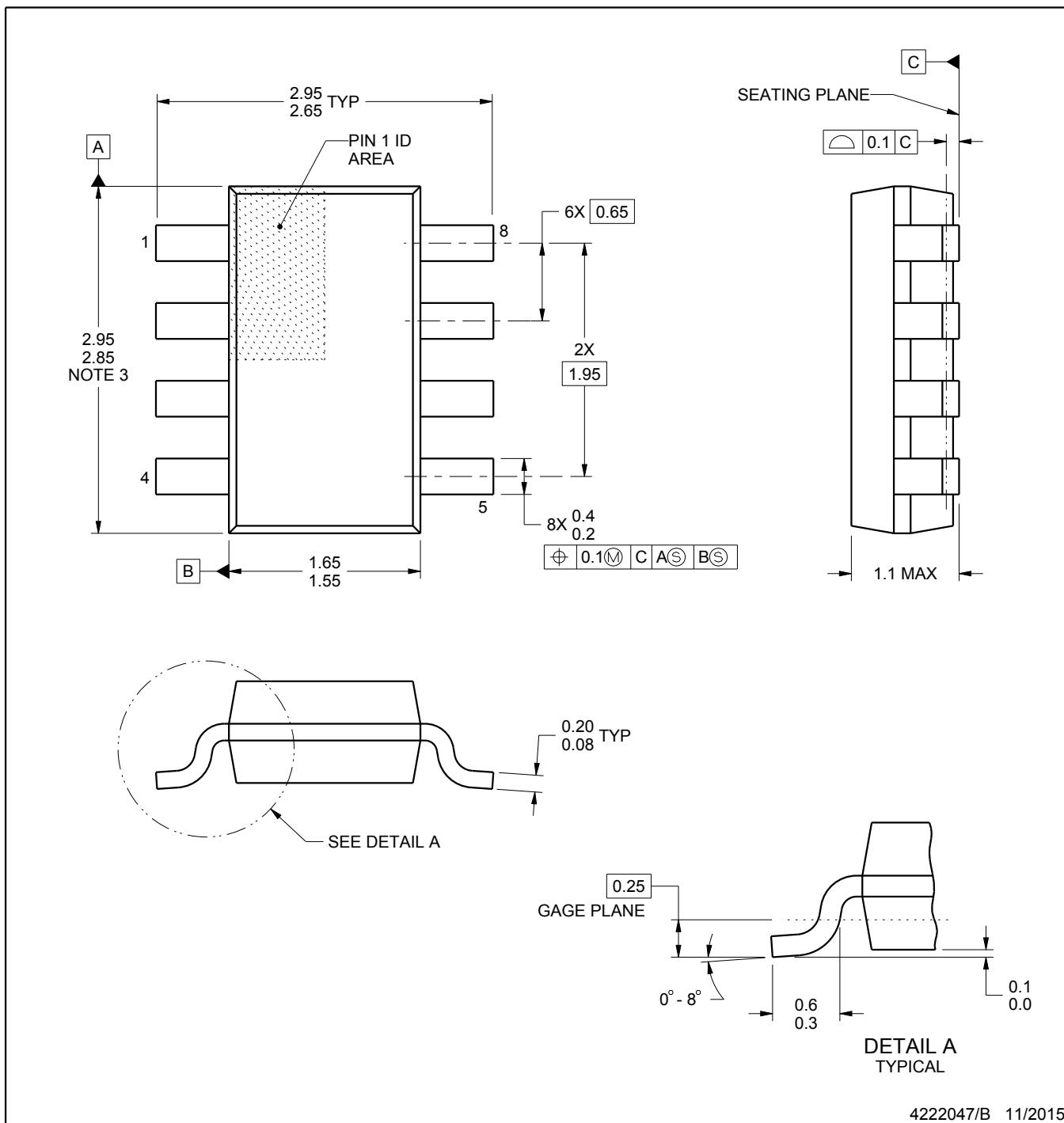
PACKAGE OUTLINE

DDF0008A



SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

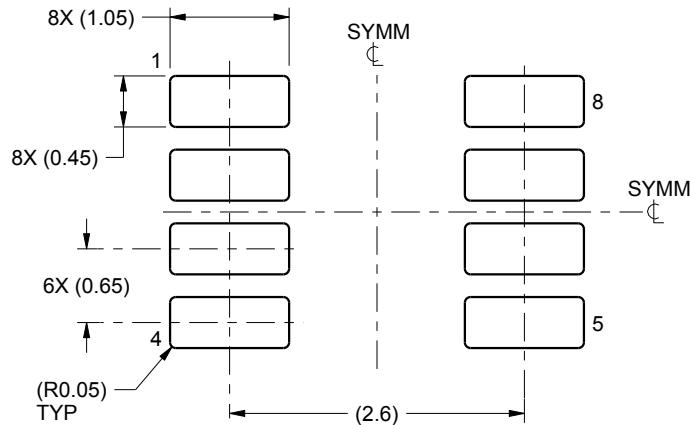
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

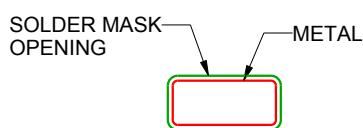
DDF0008A

SOT-23 - 1.1 mm max height

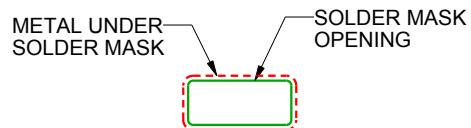
PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

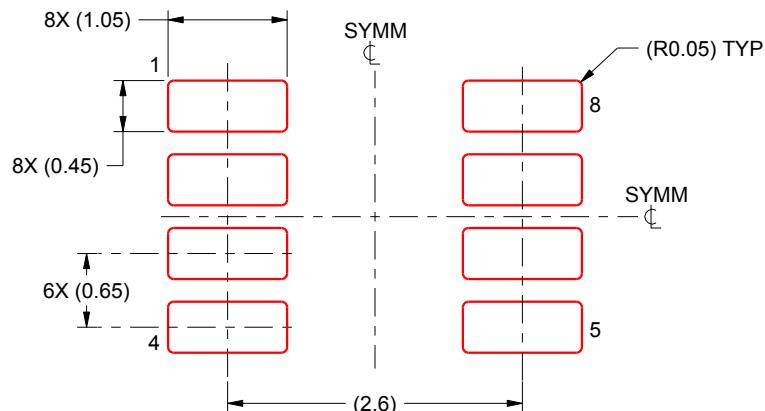
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

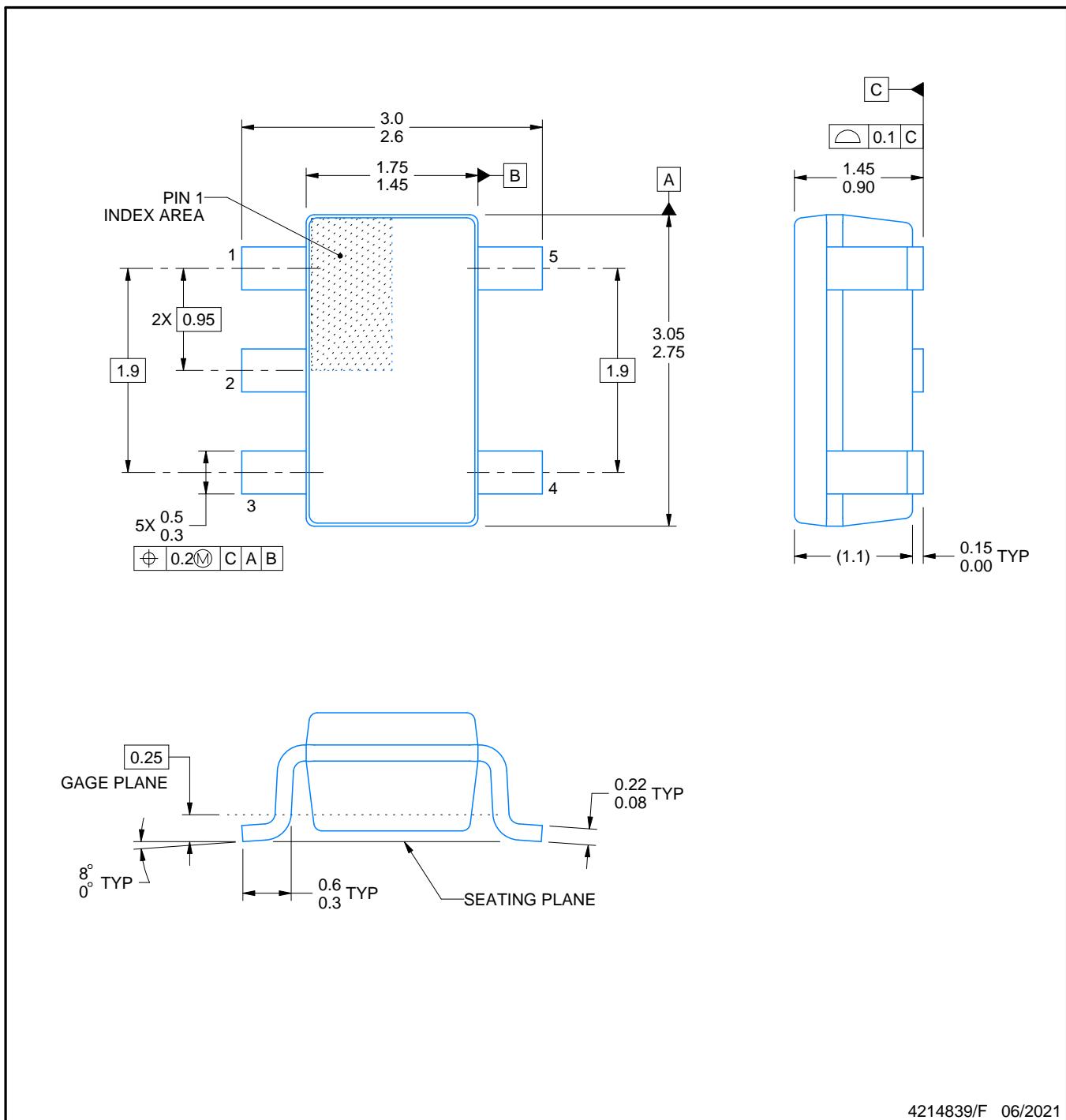
PACKAGE OUTLINE

DBV0005A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

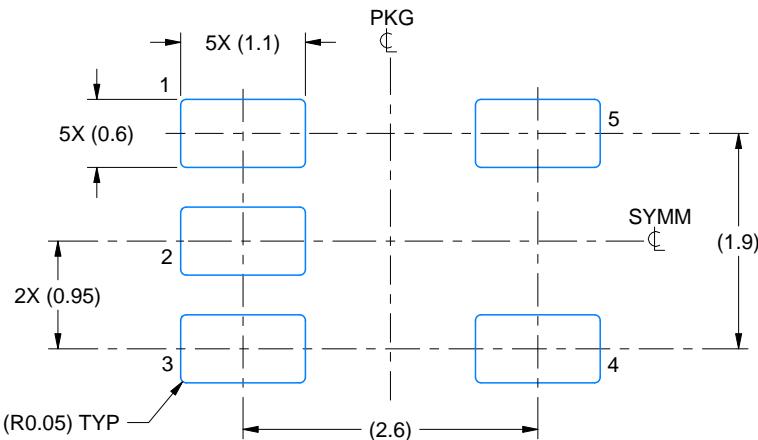
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

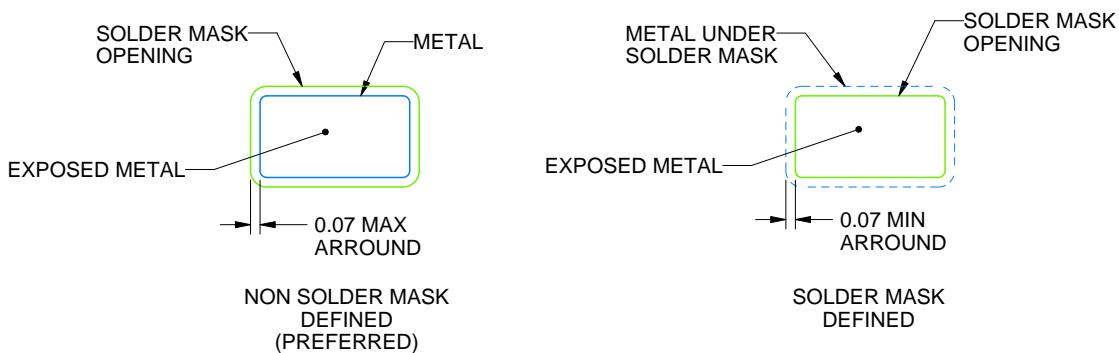
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

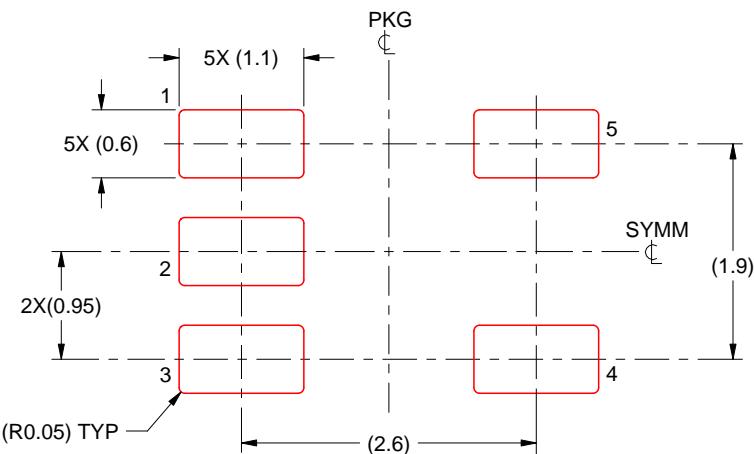
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

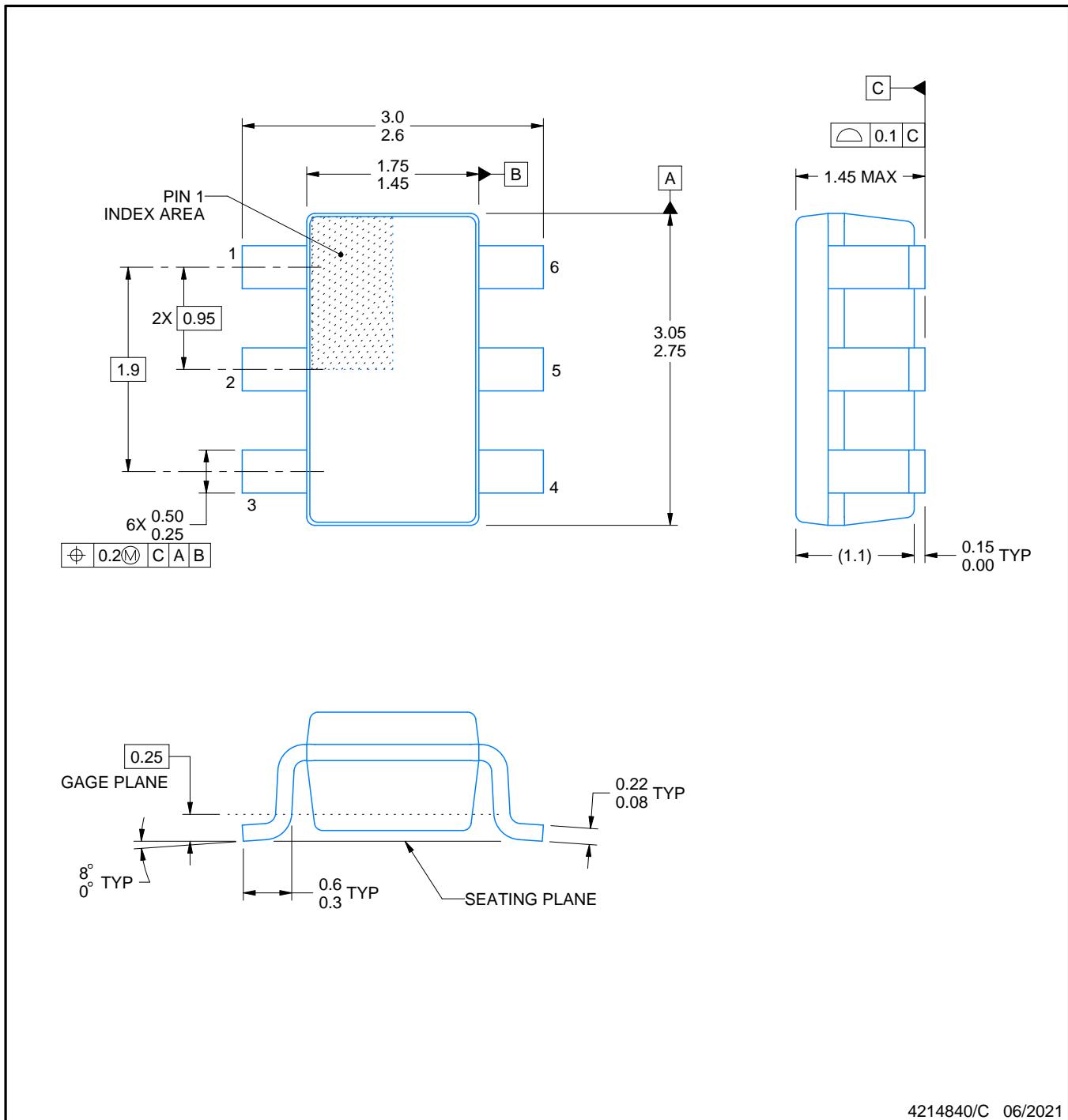
PACKAGE OUTLINE

DBV0006A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

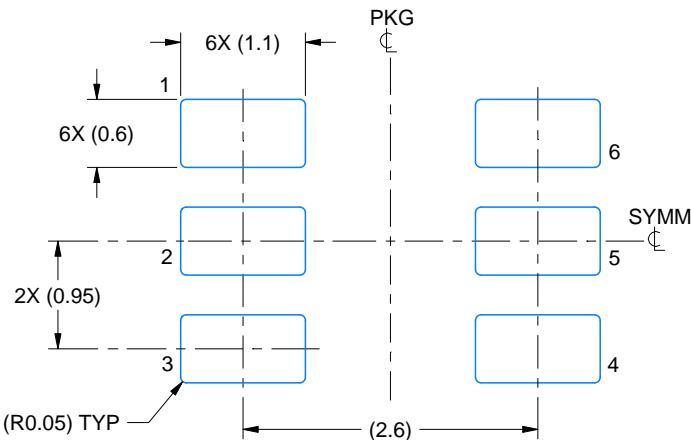
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
 5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

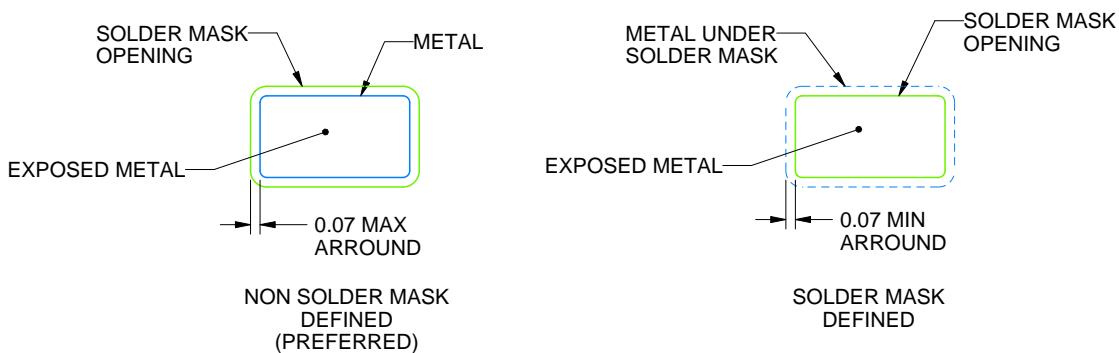
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

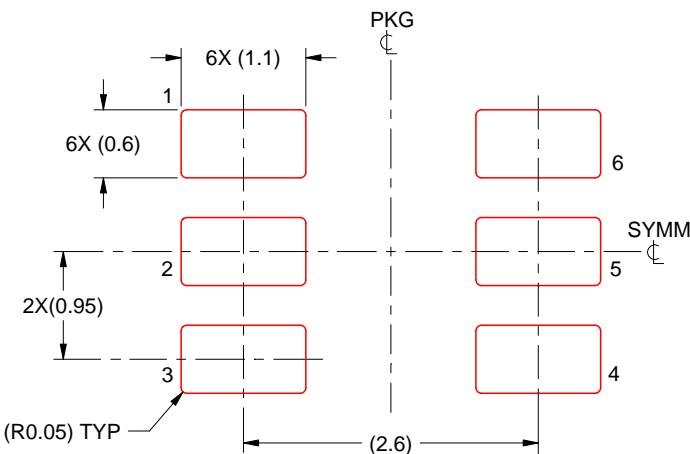
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

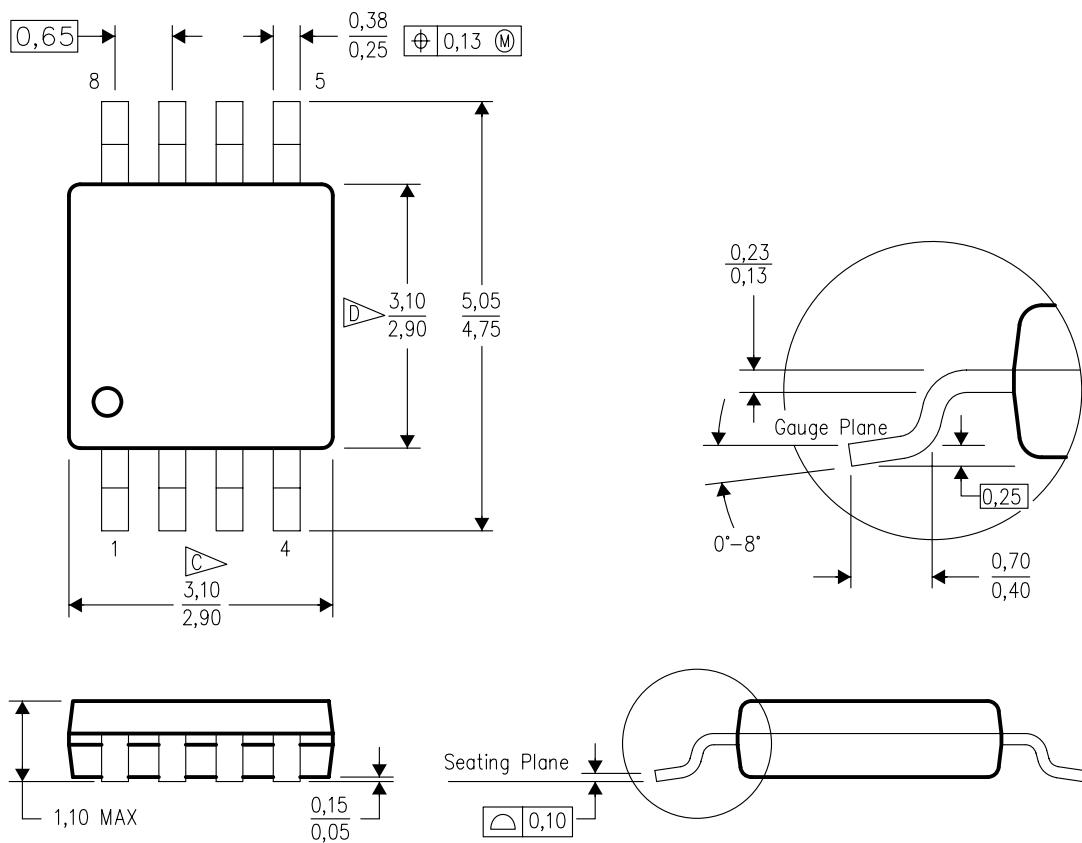
4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

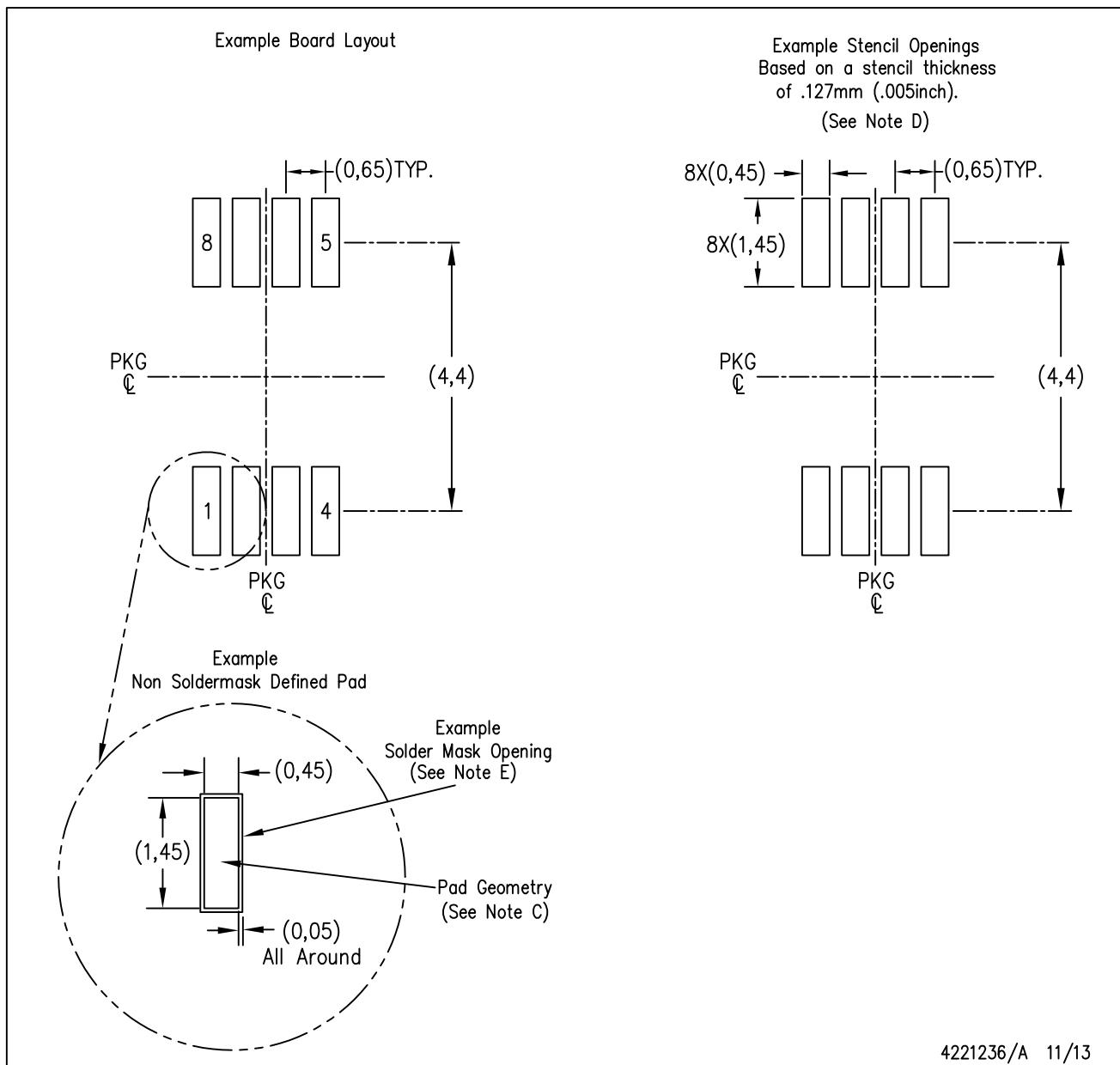
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

E. Falls within JEDEC MO-187 variation AA, except interlead flash.

LAND PATTERN DATA

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

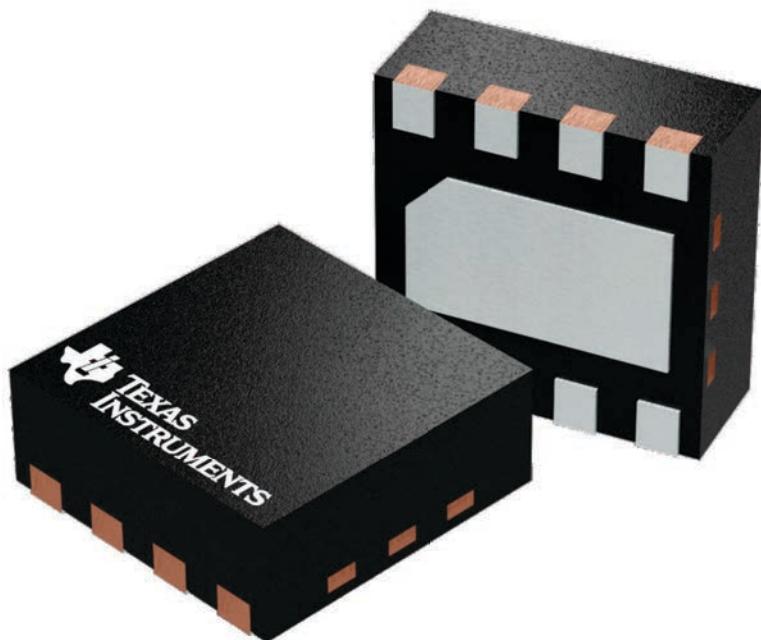
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

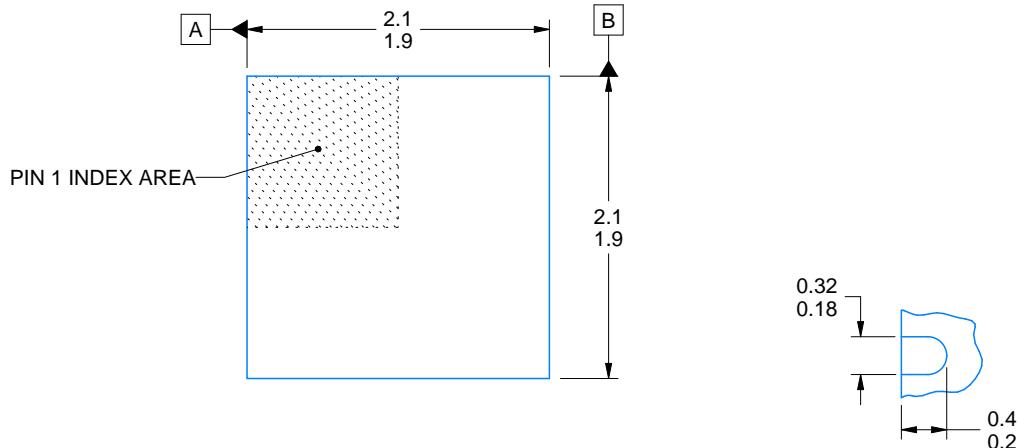
PACKAGE OUTLINE

DSG0008A

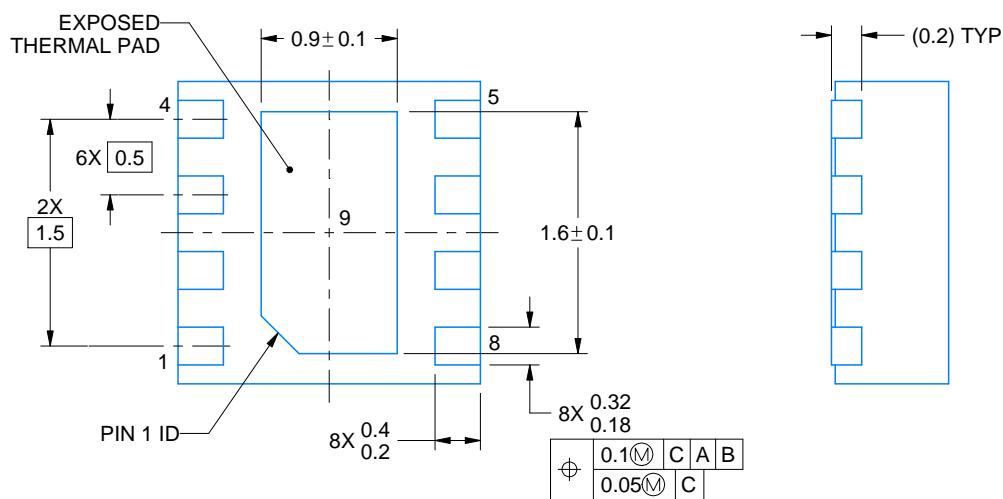
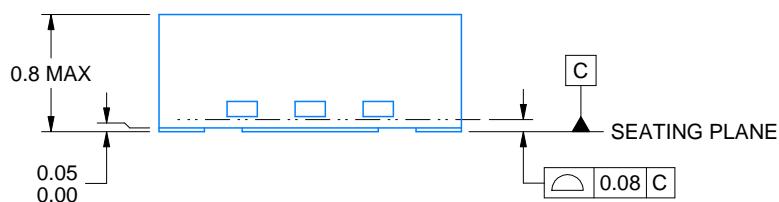


WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



ALTERNATIVE TERMINAL SHAPE
TYPICAL



4218900/D 04/2020

NOTES:

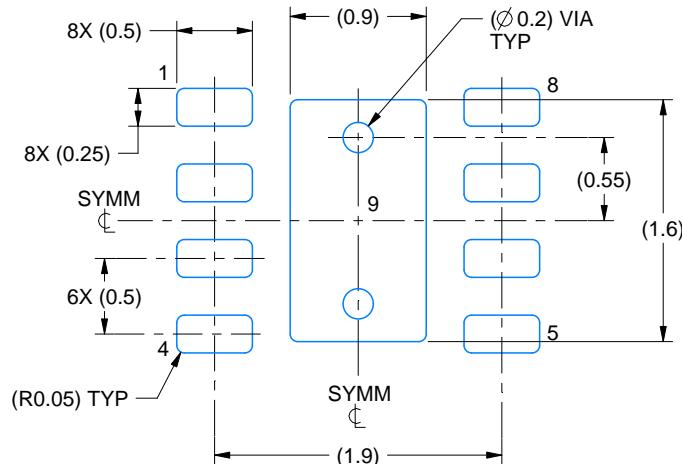
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

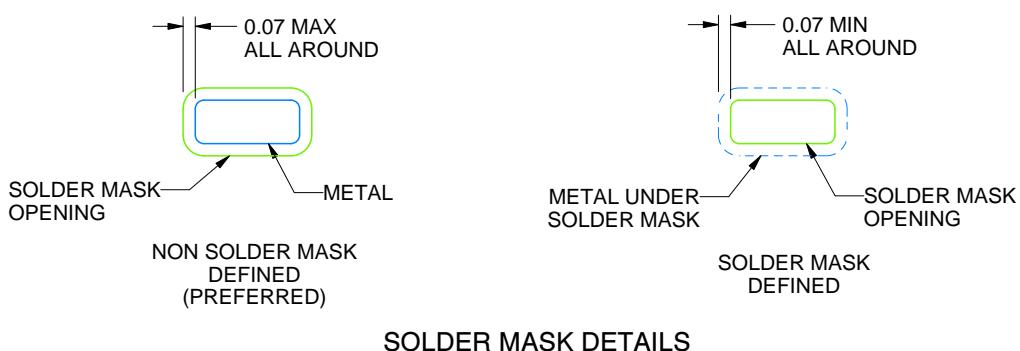
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

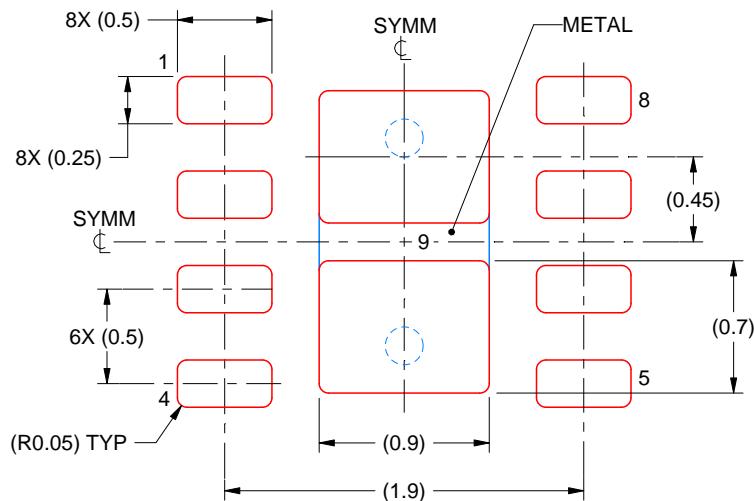
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/D 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

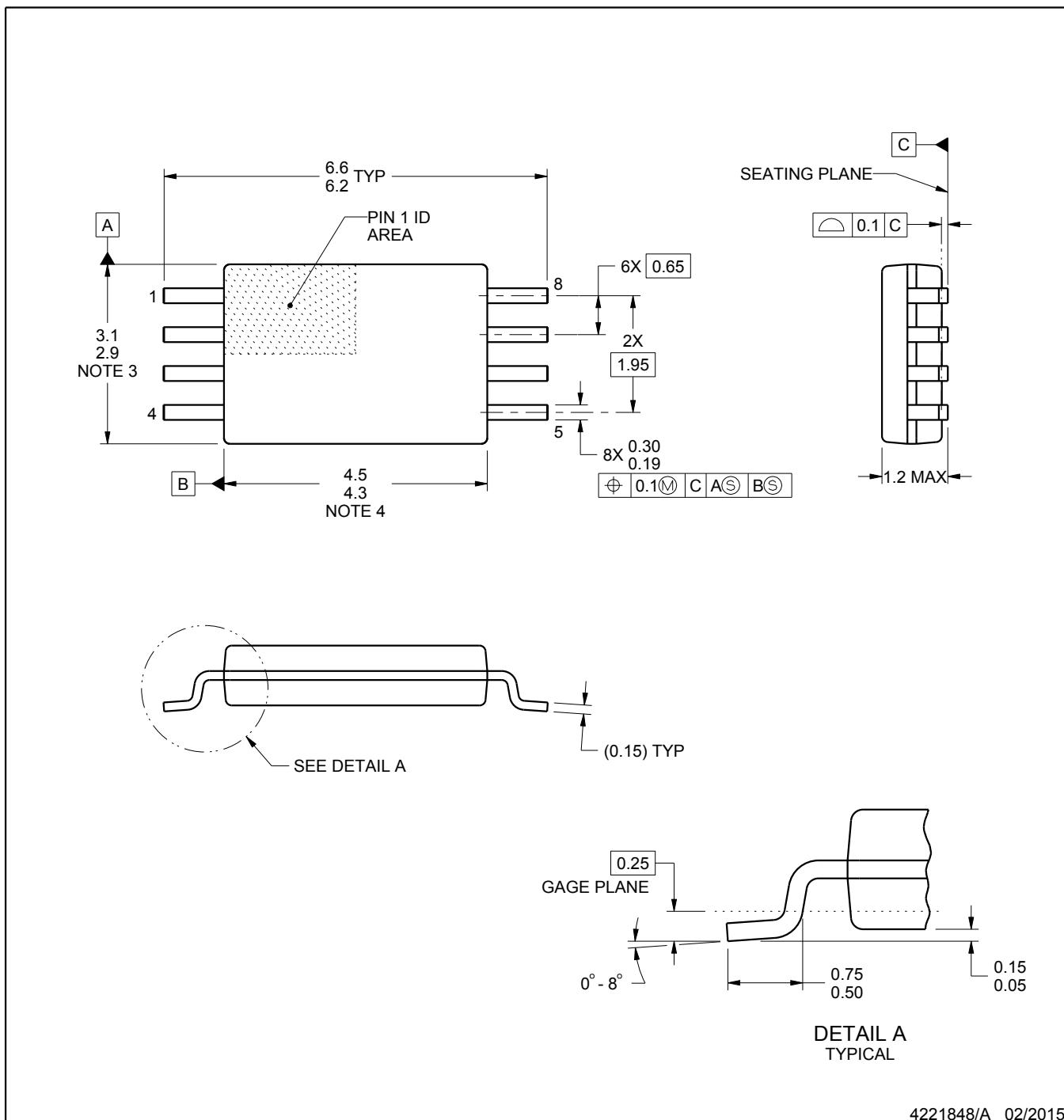
PACKAGE OUTLINE

PW0008A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

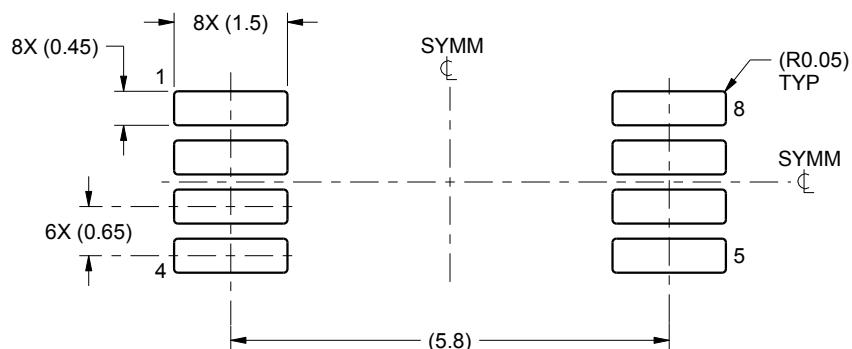
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

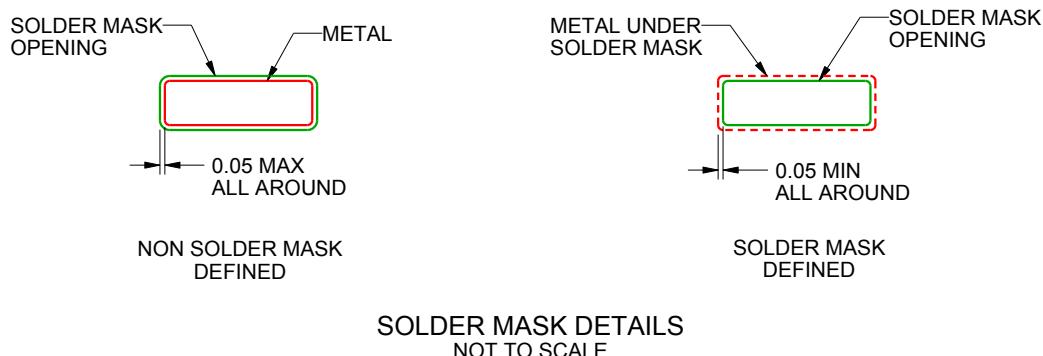
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



4221848/A 02/2015

NOTES: (continued)

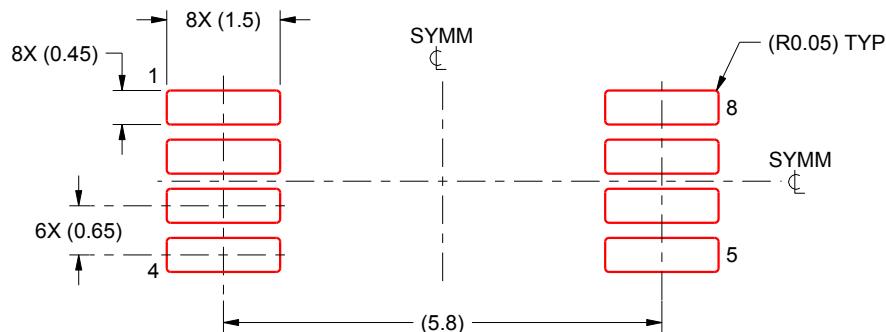
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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