



## 8-DIGIT FLUORESCENT DISPLAY DRIVER FOR MICROCOMPUTOR

### DESCRIPTION

The M54844P, a semiconductor integrated circuit fabricated with using IIL technology, is designed for driving an 8-digit, 8-segment fluorescent display.

### FEATURES

- Can be used in either an 8-digit or 7-digit plus a decimal point.
- 4-bit data input
- Mode-input controllable display mode
- Internal clock generator
- Wide operating voltage ( $V_{CC}=5\sim 12V$ )

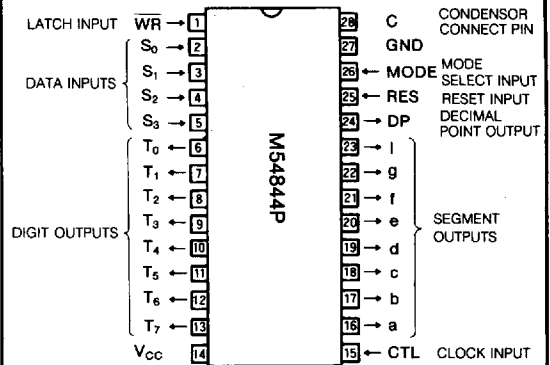
### APPLICATION

Micro computer display  
Digital equipment for industrial and consumer use

### FUNCTION

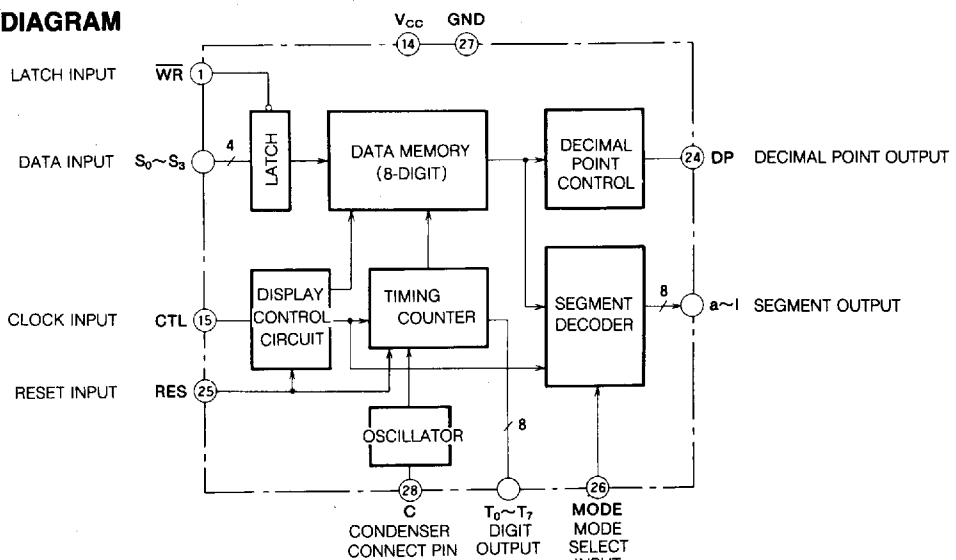
The M54844p, a decoder/driver for fluorescent displays, has a 4-bit  $\times$  8-digit memory. Employing the dynamic lighting method, it can light an 8-segment, 8-digit device. Two indication modes can be selected, by the setting of the MODE input.

### PIN CONFIGURATIONS (TOP VIEW)



Outline 28P4

### BLOCK DIAGRAM



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DESCRIPTION OF OPERATION

1. Output after reset and during reset.  
Outputs during reset (RES=high-state) is shown in the following chart.

Output pin		Output level
Digit output	T <sub>0</sub>	H
	T <sub>1</sub> ~T <sub>7</sub>	L
Segment output	a~I	L
	DP	L

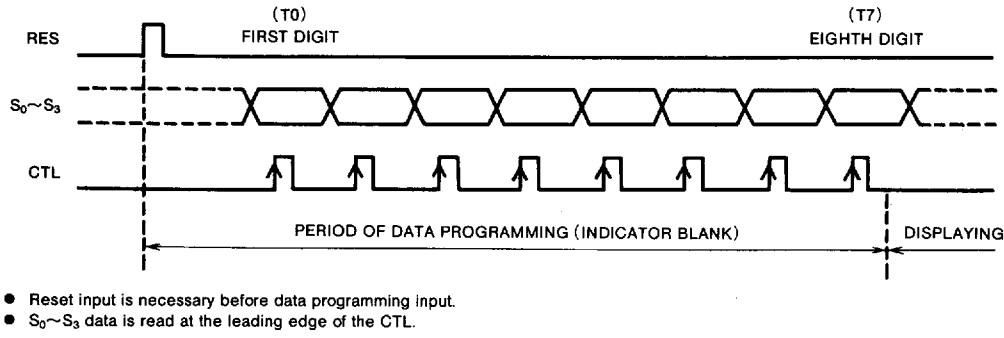
After reset, the outputs T<sub>0</sub>~T<sub>7</sub> are scanned beginning with T<sub>0</sub>. Outputs S<sub>a</sub>~S<sub>i</sub> and DP remain in low-state until CTL has been input for 8 cycles.

2. Decimal point setting  
The location of the decimal point depends on the contents of the data memory corresponding to T<sub>0</sub>. When the decimal point is to be displayed, digit T<sub>0</sub> cannot be used.  
The display position of the decimal point is as follows.

Content of digit T <sub>0</sub>	Display position of decimal point
0 or 8	T <sub>1</sub>
1 or 9	T <sub>2</sub>
2 or A	T <sub>3</sub>
3 or B	T <sub>4</sub>
4 or C	T <sub>5</sub>
5 or D	T <sub>6</sub>
6 or E	T <sub>7</sub>
7 or F	T <sub>0</sub>

3. Operation timing

(1) Data programming



(2) Output timing

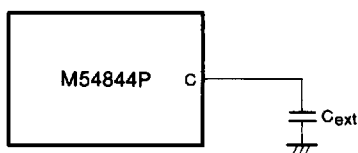
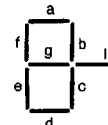


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## DISPLAY CHARACTERS

Hexadecimal code Mode	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
I	0	1	2	3	4	5	6	7	8	9	-	E	C	-	0	
II					4						a	b	c	d	e	+

Mode I is displayed when MODE input is low-state.  
Mode II is displayed when MODE input is high-state.



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}$	Supply voltage		$-0.3 \sim +15$	V
$V_i$	Input voltage		$-0.3 \sim V_{CC}$	V
$V_{CC}-V_O$	Voltage between the power supply and output pin	Output off-state	$-0.3 \sim +35$	V
$T_{opr}$	Operating temperature		$-30 \sim +85$	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature		$-55 \sim +125$	$^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS ( $T_a = -30 \sim +85^{\circ}\text{C}$ , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{CC}$	Supply voltage	4.5	10	12	V
$V_{CC}-V_O$	Voltage between the power supply and output pin			33	V

ELECTRICAL CHARACTERISTICS ( $T_a = -30 \sim +85^{\circ}\text{C}$ ,  $V_{CC} = 10\text{V}$ , unless otherwise noted)

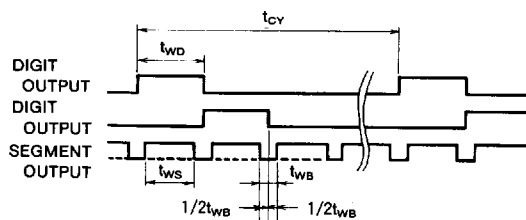
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{IH}$	High-level input voltage		2		$V_{CC}$	V
$V_{IL}$	Low-level input voltage		0		0.7	V
$I_{IH}$	High-level input current	$V_{IH} = 10\text{V}$			20	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{IL} = 0.5\text{V}$			-200	$\mu\text{A}$
$V_{OH}$	High-level output voltage	$I_{OH} = -10\text{mA}$	8			V
$I_{OLK}$	Output leak current	$V_O = -20\text{V}$			-30	$\mu\text{A}$
$I_{CC}$	Supply current	Display off-state		12	18	mA
$t_{ws}$	Segment output width	$C_{ext} = 1000\text{pF}$	130	260	520	$\mu\text{s}$
$t_{wb}$	Segment blank width	$C_{ext} = 1000\text{pF}$	20	40	80	$\mu\text{s}$
$t_{wD}$	Digit output width	$C_{ext} = 1000\text{pF}$	150	300	600	$\mu\text{s}$
$t_{CY}$	Digit period	$C_{ext} = 1000\text{pF}$	1.2	2.4	4.8	ms

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**TIMING REQUIREMENTS** ( $T_a = -30 \sim +85^\circ\text{C}$ ,  $V_{cc} = 4.5 \sim 12\text{V}$ , unless otherwise noted)

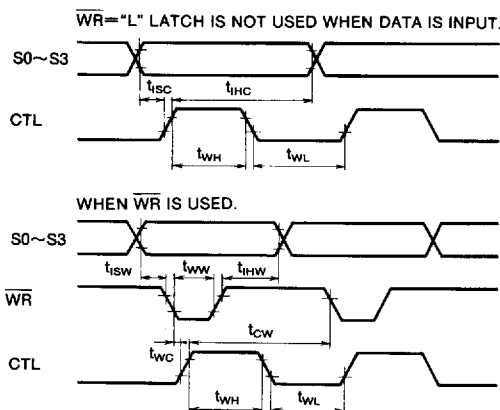
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{ISC}$	Input setup time in relation to CLK		5			$\mu\text{s}$
$t_{IHC}$	Input hold time in relation to CLK		10			$\mu\text{s}$
$t_{WH}$	High-level CTL width		5			$\mu\text{s}$
$t_{WL}$	Low-level CTL width		10			$\mu\text{s}$
$t_{ISW}$	Input setup time in relation to WR		0			$\mu\text{s}$
$t_{IHW}$	Input hold time in relation to WR		5			$\mu\text{s}$
$t_{WW}$	WR width		5			$\mu\text{s}$
$t_{WC}$	WR $\rightarrow$ CTL		5			$\mu\text{s}$
$t_{CW}$	CTL $\rightarrow$ WR		15			$\mu\text{s}$

**OUTPUT TIMING DIAGRAM**



DIGIT OUTPUT WIDTH  $t_{wd} = 15t_{osc}$   
SEGMENT OUTPUT WIDTH  $t_{ws} = 13t_{osc}$   
SEGMENT BLANK WIDTH  $t_{wb} = 2t_{osc}$   
( $t_{osc}$  is oscillation period of the oscillator circuit.)

**INPUT TIMING DIAGRAM**



WR="L" LATCH IS NOT USED WHEN DATA IS INPUT.

WHEN WR IS USED.