DATA SHEET

NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD7001

8-BIT CMOS SERIAL I/O ANALOG-TO-DIGITAL CONVERTER

The μPD7001 is a high performance, low power 8-bit CMOS A/D converter which consists of a 4-channel analog multiplexer and a digital interface circuit for serial data I/O. It uses successive approximation as a conversion technique.
An A/D conversion system can be easily designed with the μPD7001 including all circuits for A/D conversion. The μPD7001 can be directly connected to 8-bit or 4-bit microprocessors.

FEATURES

- Single chip A/D converter
- Resolution: 8-bit
- 4-channel analog multiplexer
- Auto-zeroscale and auto-fullscale corrections without any external components
- Serial data transmission
- High input impedance: 1 000 MΩ
- Single +5 V power supply
- Low power operation
- Available in 16-pin plastic DIP
- Conversion speed: 140 μs TYP.
- Linearity: 0.8 %

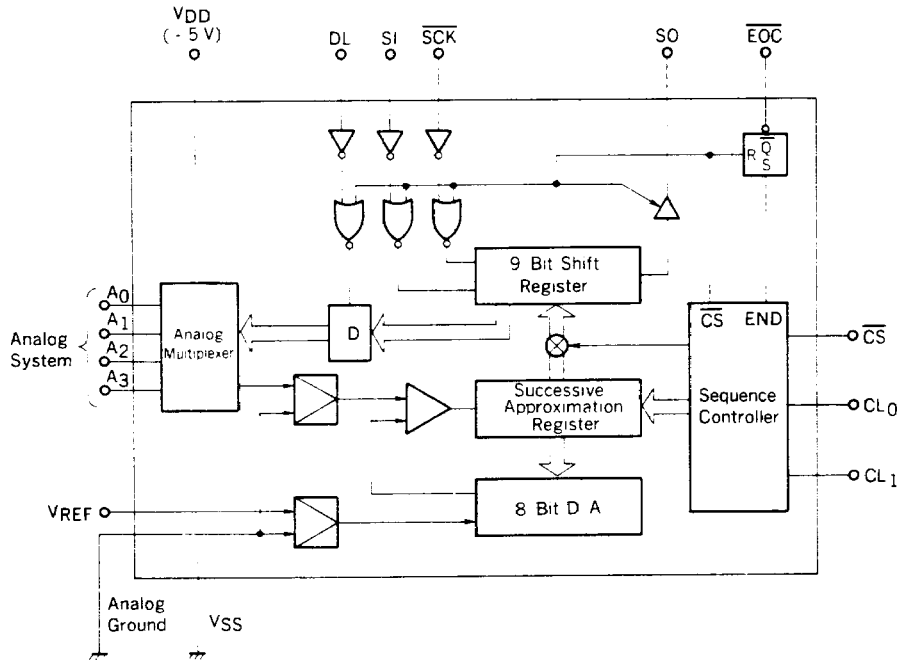
ORDERING INFORMATION

Ordering Code	Package
μPD7001C	16-pin plastic DIP (300 mil)

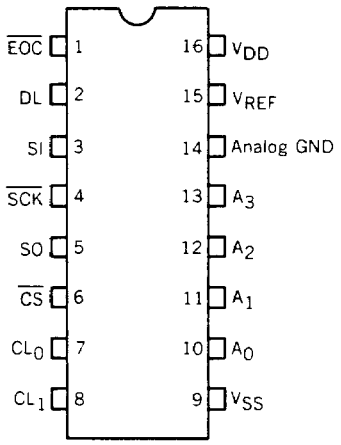
NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

© NEC Corporation 1988

BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



PIN IDENTIFICATION

PIN NO.	PIN NAME	SYMBOL	FUNCTION
1	End of Conversion	$\overline{EOC}$	High impedance when $\overline{CS}$ = Low. Open drain output.
2	Data Latch	DL	MPX addresses are latched at the falling edge of DL input.
3	Serial Input	SI	Pin to accept MPX address data. Data read at the rising edge of $\overline{SCK}$ input.
4	Serial Clock	$\overline{SCK}$	$\overline{SCK}$ controls the shift operation of I/O interface 8-bit shift register. Input.
5	Serial Output	SO	Conversion data in shift register are output at the falling edge of $\overline{SCK}$. High impedance when $\overline{CS}$ = High. Open drain output.
6	Chip Select	$\overline{CS}$	$\overline{CS}$ = High: A/D conversion mode $\overline{CS}$ = Low: Interface mode. Input
7	Clock	CL_0	Pin for clock oscillation.
8	Clock	CL_1	Pin for clock oscillation.
9	Digital Ground	V_{SS}	Ground terminal. Tie to GND with analog GND externally.
10 – 13	Analog Inputs	A_0 to A_3	Analog input terminals.
14	Analog GND	GND	Ground terminal for analog inputs and references.
15	Reference Input	V_{REF}	Pin to set full scale voltage. V_{REF} to +2.5 V.
16	Power Supply	V_{DD}	V_{DD} (+5 V)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Power Dissipation	P_T	200	mW
Analog Input Voltage	V_{IA}	−0.3 to V_{DD} +0.3	V
Reference Voltage	V_{REF}	−0.3 to V_{DD} +0.3	V
Digital Input Voltage	V_{ID}	−0.3 to +12	V
Maximum Pull-up Voltage	V_{DD2}	+12	V
Operating Temperature	T_{opt}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +125	°C

DC CHARACTERISTICS

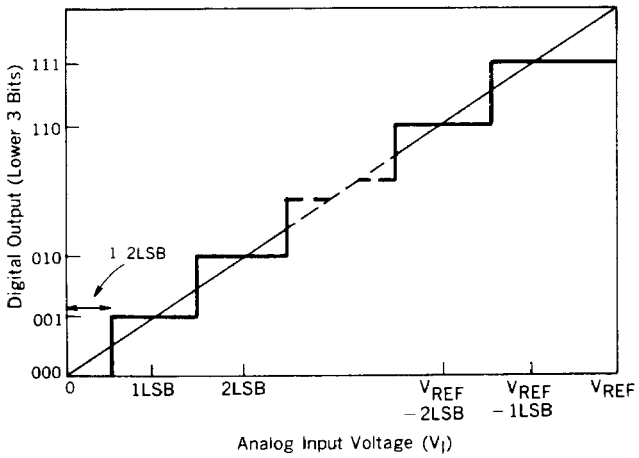
(T_a = +25 °C ± 2 °C; f_{CK} = 400 kHz, V_{DD} = ±5 V, ±0.25 V, V_{REF} = 2.500 V, Note 1)

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
Resolution				8	Bit	
Nonlinearity	NL			0.8	%FSR	
Full-Scale Error			1	2	LSB	
Full-Scale Error Temperature Coefficient			30		ppm/°C	
Zero Error				2	LSB	
Zero Error Temperature Coefficient			30		ppm/°C	
Total Unadjusted Error 1	TUE1			2	LSB	Note 4
Total Unadjusted Error 2	TUE2			2	LSB	Note 5
Analog Input Voltage	V_{IA}	0		V_{REF}	V	Note 1
Analog Input Resistance	R_I		1000		MΩ	V_I = 0 to V_{DD}
Conversion Time	T_{CONV}		140		μs	Note 2
Clock Frequency Range	f_{CK}	0.01	0.4	0.5	MHz	
Clock Frequency Distribution	Δf_{CK}		±5	±20	%	R = 27 kΩ, C = 47 pF, f_{CK} ≈ 400 kHz
Serial Clock Frequency	f_{SCK}		0.5		MHz	Note 3
High Level Voltage	V_{IH}	3.6			V	
Low Level Voltage	V_{IL}			1.4	V	
Digital Input Leakage Current	I_{ID}		1.0	10	μA	V_I = V_{SS} to +10 V
Low Level Output Voltage	V_{OL}			0.4	V	I_{DL} = 1.7 mA
Output Leakage Current	I_{LEAK}		1.0	10	μA	V_O = +10 V
Power Dissipation	P_d		5	15	mW	

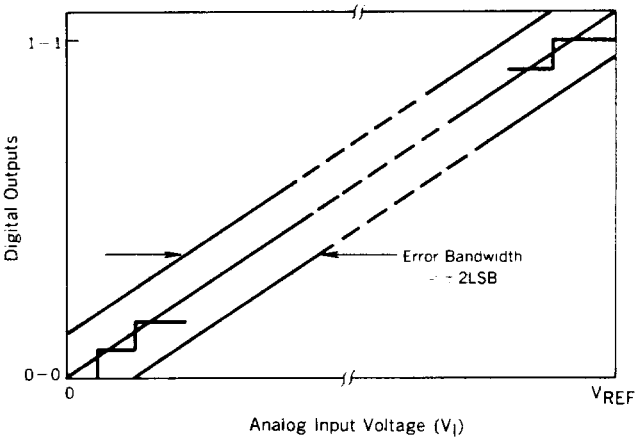
Notes: 1. All digital outputs are put at a high level when $V_I > V_{REF}$.
2. A/D conversion is started with $\overline{CS}$ going high; at the final step of the first A/D conversion, $\overline{EOC}$ is low. The conversion time is: $t_{CONV} = 56/f_{CK}$
3. For $f_{SCK} < 500$ kHz, the load capacitor (stray capacitance included) and the pull-up resistor, which are connected to serial output, are required to be not more than 30 pF and 3 kΩ respectively.
4. V_{DD} = 5.00 V, V_{REF} = 2.5 ±0.25 V
5. V_{DD} = 4.5 to 5.5 V, V_{REF} = 2.500 V

OPERATING CHARACTERISTICS

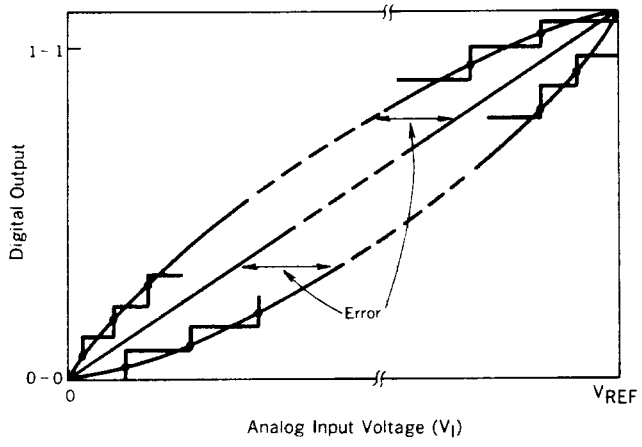
IDEAL INPUT/OUTPUT TRANSFER CHARACTERISTICS



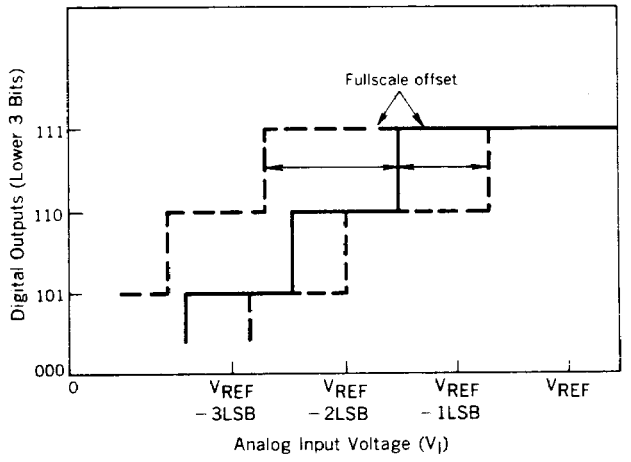
TOTAL UNADJUSTED ERROR



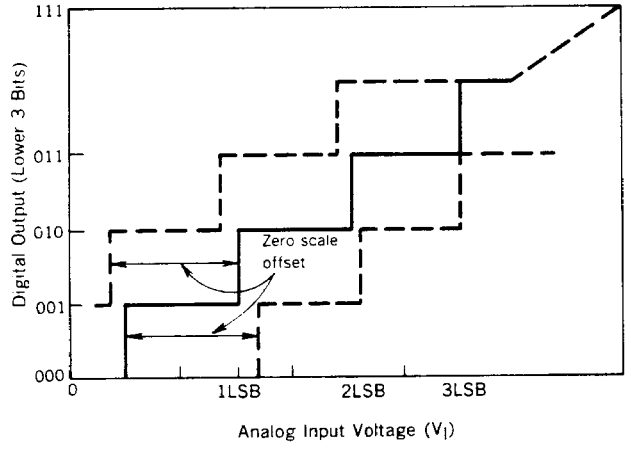
LINEARITY ERROR



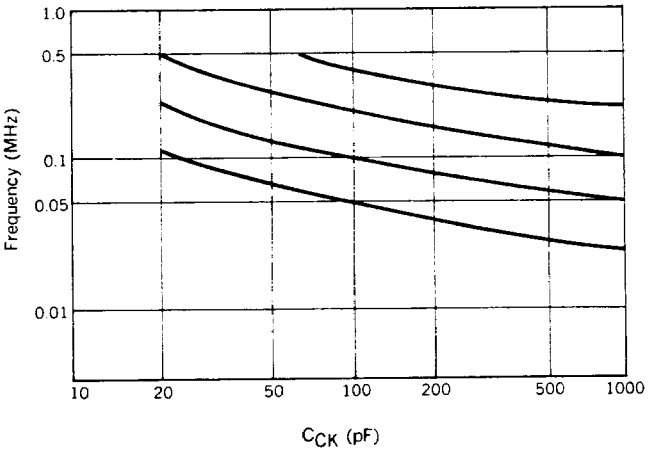
FULL SCALE ERROR



ZERO SCALE ERROR

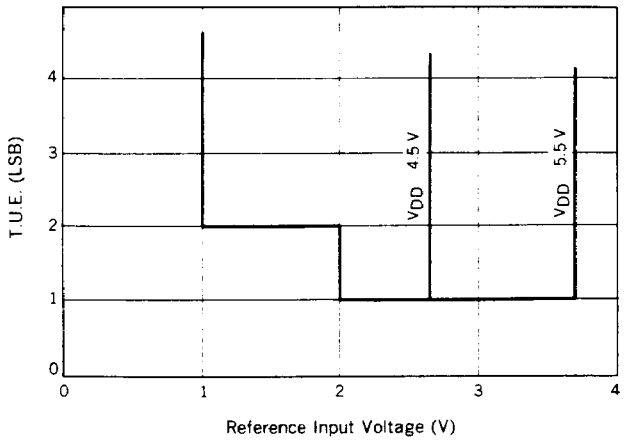


CLOCK FREQUENCY RANGE

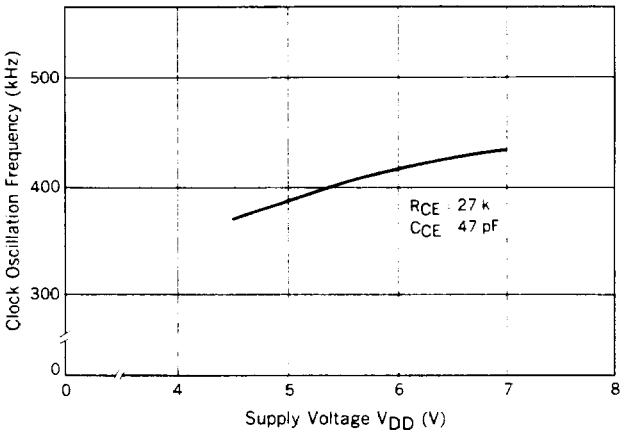


OPERATING CHARACTERISTICS (T_a = 25 °C)

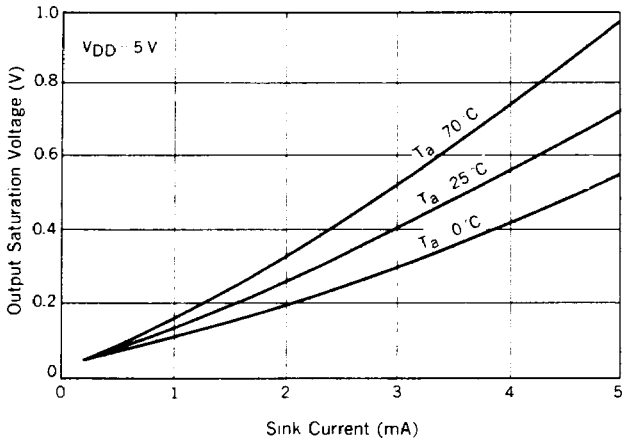
T.U.E. vs. V_{REF}



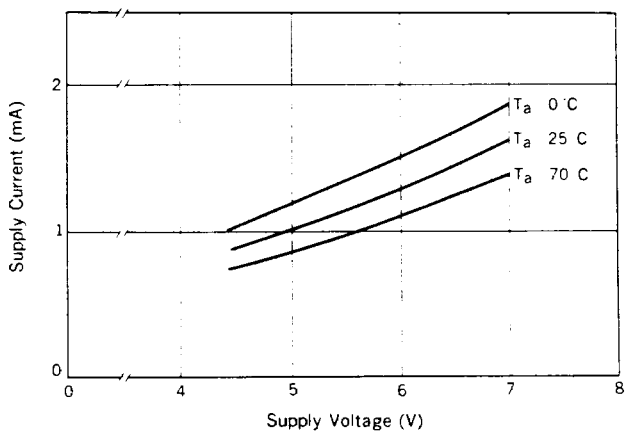
CLOCK OSCILLATION FREQUENCY vs. CURRENT CHARACTERISTICS



OUTPUT SINK CURRENT vs. SATURATION VOLTAGE CHARACTERISTICS



SUPPLY VOLTAGE vs. CURRENT CHARACTERISTICS



AC CHARACTERISTICS

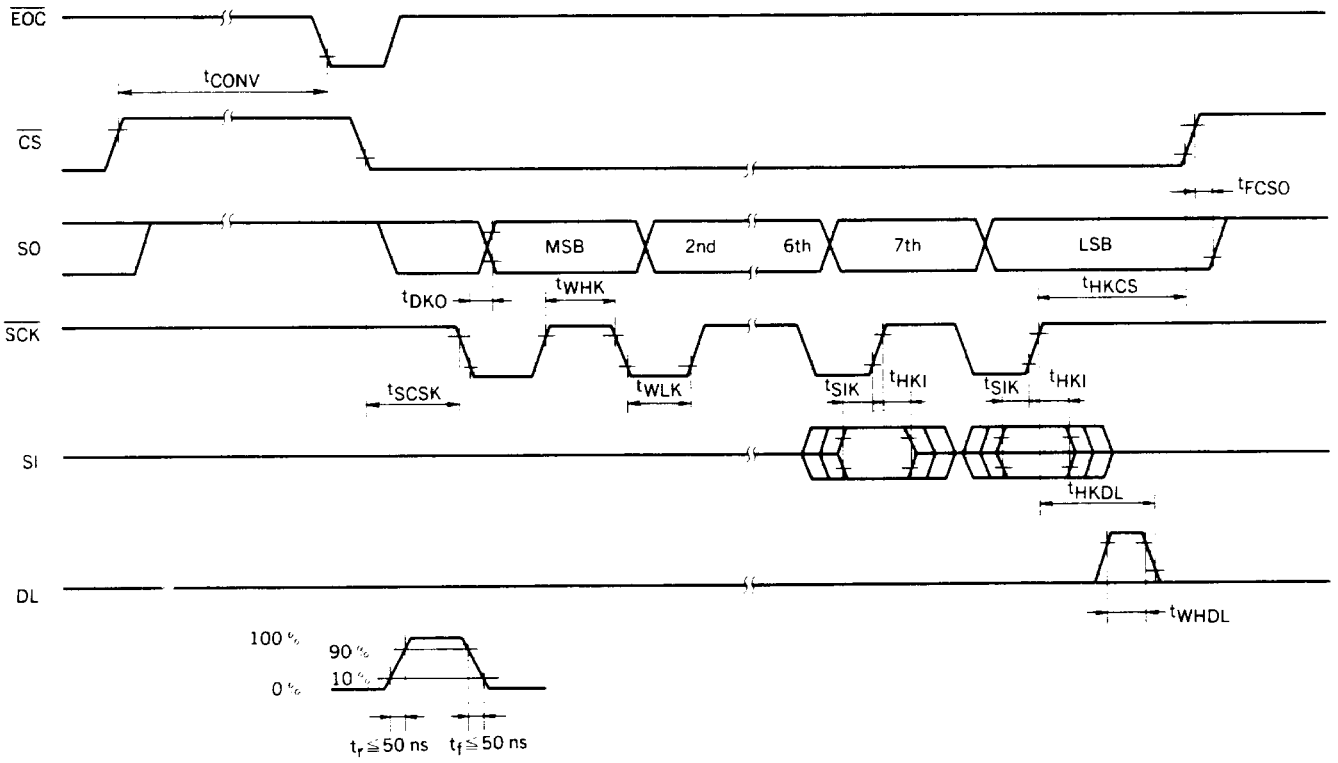
(T_a = +25 °C ± 2 °C; f_{CK} = 400 kHz, V_{DD} = ±5 V, Note 1)

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
$\overline{EOC}$ Hold Time	t_{HECS}	0			μs	$\overline{EOC}$ to $\overline{CS}$
CS Setup Time	t_{SCSK}	12.5			μs	$\overline{CS}$ to $\overline{SCK}$ Note 1
Address Data Setup Time	t_{SIK}	150			ns	
Address Data Hold Time	t_{HKI}	100			ns	
High Level Serial Clock Pulse Width	t_{WHK}	400			ns	
Low Level Serial Clock Pulse Width	t_{WLK}	400			ns	
Data Latch Hold Time	t_{HKDL}	200			ns	$\overline{SCK}$ to DL
Data Latch Pulse Width	t_{WHDL}	200			ns	
Serial Data Delay Time	t_{DKO}			500	ns	$\overline{SCK}$ to SO, R_L = 3 kΩ (Note 2), C_L = 30 pF
Delay Time to Floating SO	t_{FCSO}			250	ns	$\overline{CS}$ to High Impedance SO
$\overline{CS}$ Hold Time	t_{HKCS}	200			ns	

Notes: 1. When $\overline{CS}$ is high, the μPD7001 performs A/D conversion and does not accept any external digital signal. It remains at the previous state continuously. When $\overline{CS}$ is low, the data is exchanged with the external digital circuits. However, 5 internal clock pulses are needed before digital data is output. The rating corresponds to the 5 clock signal pulses: $t_{SCSK}(min) = 5/f_{CK}$

2. The serial data delay time depends on load capacitance and pull-up resistance: $t_{DKO}\uparrow = 2.3 \times R_L \times C_L + 100$ ns.

TIMING CHART



OPERATIONS OF INTERNAL CIRCUIT BLOCKS

Sequence Controller

When $\overline{CS}$ is high, the sequence controller controls the internal A/D conversion sequence of the μPD7001. One A/D conversion takes 56 internal clock pulses to complete. As the final step, the conversion data is transferred to the shift register, and $\overline{EOC}$ goes low. After this A/D conversion sequence is completed, the sequence controller is initialized to execute the next conversion. Thus, conversion data in the shift register is refreshed every 56 clock pulses.

Shift Register

A 9-bit shift register is incorporated in the μPD7001 for serial data exchange with peripheral devices. The serial input, output, and clock terminal of the shift register are strobed by the internal chip selects signal and are connected to SI, SO and $\overline{SCK}$ pins respectively. A low level of $\overline{CS}$ enables the interface with external peripheral devices. The shift register outputs data at the falling edge of $\overline{SCK}$ and accepts data at its rising edge. In addition, for analog multiplexer address setting, the two input bits of the shift register are connected to the address decoder, and the address data is latched at the falling edge of DL.

Analog Multiplexer

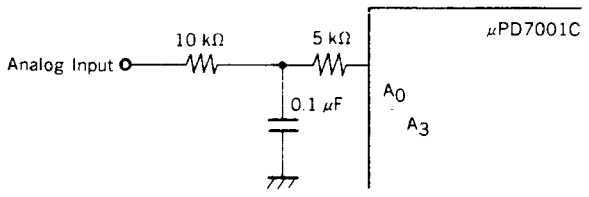
One analog input signal from A_0–A_3 is selected through the addressed multiplexer channel, and this input signal is transferred to the input of the A/D converter.

A/D Converter

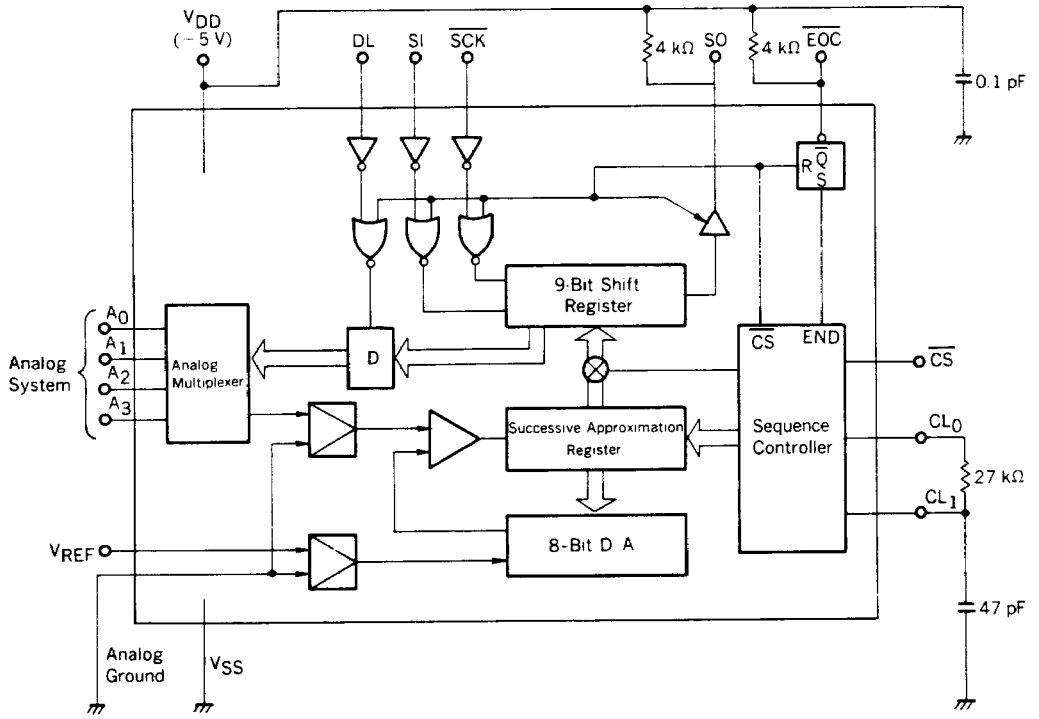
The A/D converter section contains the successive approximation register, the 8-bit D/A converter, comparator and buffer amplifier. Voltage at the V_{REF} pin is used as a reference for the A/D conversion.

A/D conversion is executed automatically by the internal sequence controller. Because the μPD7001 uses the successive approximation technique, change in analog input voltage during the conversion causes a conversion error. Therefore, a low pass filter, and sample and hold circuit should be connected at the input to stabilize the conversion.

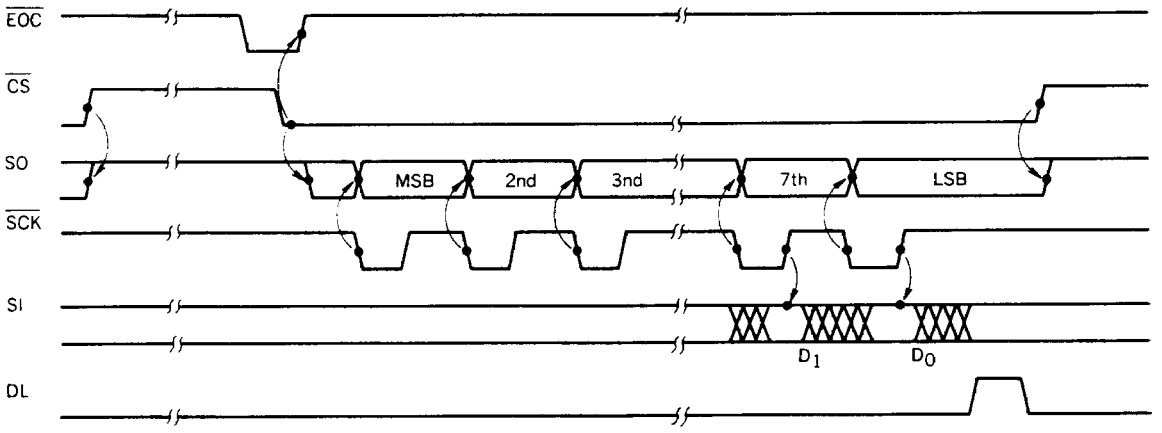
1. Data held in the internal sequence controller and address latch just after power-on is random. Therefore, an MPX address setting and a sequence controller resetting are required before a first conversion data reading.
2. When using long wires to connect external components and μPD7001 terminals, noise induction and some interference must be expected and taken into account.
3. The μPD7001 uses the successive approximation technique for A/D conversion; therefore, a sample and hold circuit is required when a fast varying analog input signal is applied. In addition, a C-R filter as shown below should be used, in order to minimize noise in a DC analog input signal.



EXAMPLE OF THE APPLICATION CIRCUIT



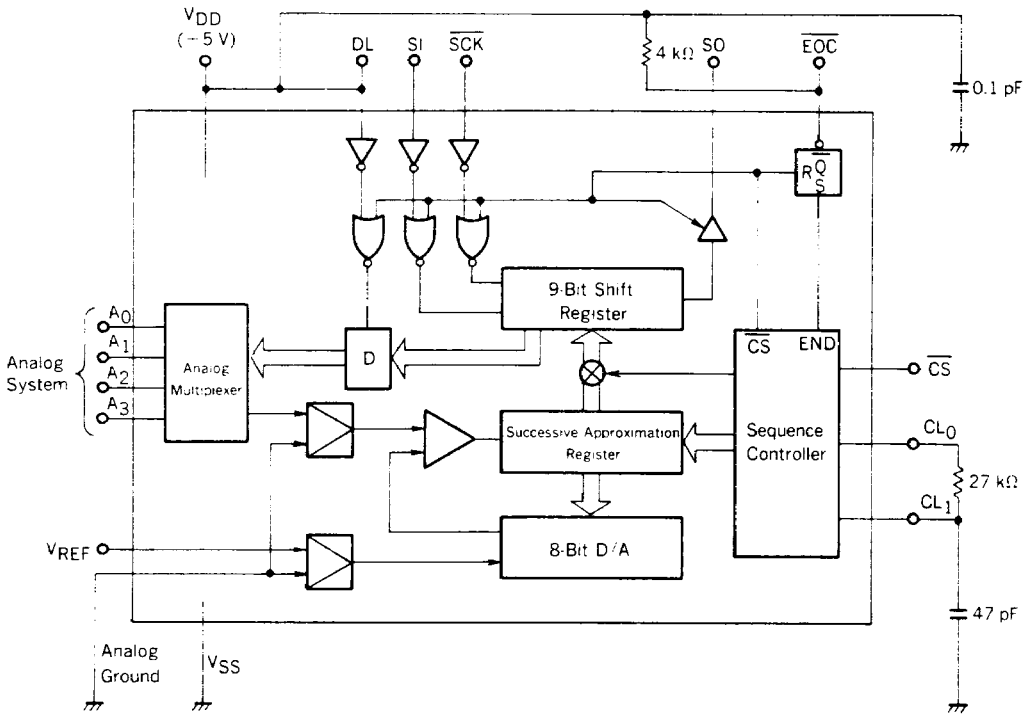
TIMING CHART



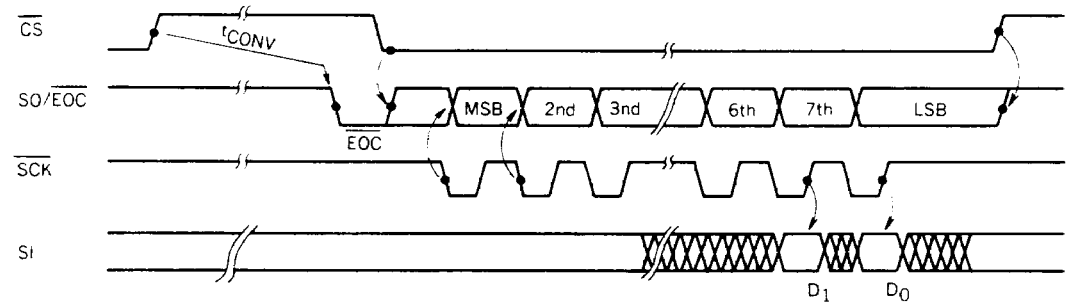
Multiplexer Channel Selection

Analog Input Address	D0	D1
A_0	Low	Low
A_1	High	Low
A_2	Low	High
A_3	High	High

APPLICATION EXAMPLE: REDUCING DIGITAL I/O TERMINALS



TIMING CHART

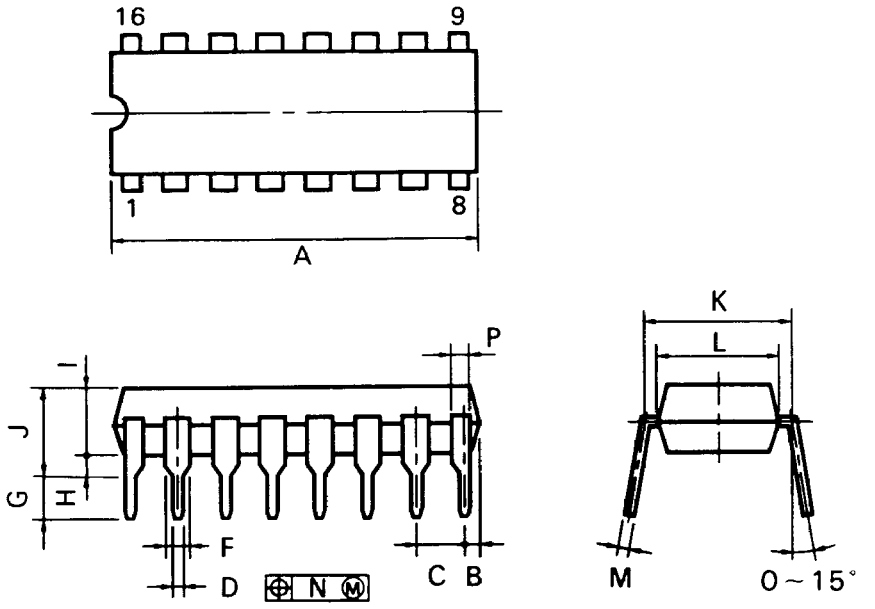


In this application, an MPX address write is required in every Date Read.

A wired OR connection is feasible, because $\overline{EOC}$ and SO are both open drain output and the signal output timing of $\overline{EOC}$ is different from that of SO.

The DL signal is strobed by $\overline{CS}$ in the chip. Therefore, by connecting DL to V_{DD}, MPX Address Data is latched at the rising edge of $\overline{CS}$.

16PIN PLASTIC DIP (300 mil)



P16C-100-300A,C

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.0 MIN.	0.039 MIN.

IC-2238
June 1988M
Printed in Japan

026270