MOS DIGITAL INTEGRATED CIRCUIT μ PD6300C

LATCH and DRIVER for FIP **CMOS LSI**

DESCRIPTION

The µPD6300C is a latch and driver CMOS IC for FIP (Fluorescent Indicator Panel). For multiplex wiring, the μ PD6300C is supplied with the serial interface circuit, 20 bit shift register, 20 bit data latch and 20 bit drivers. The serial data transfer from the data source to the $\mu PD6300C$ is accomplished with 3 or 4 signals.

FEATURES

• Serial Input 20 bit Sift Register Incorporated.

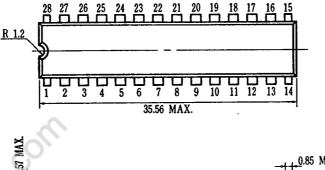
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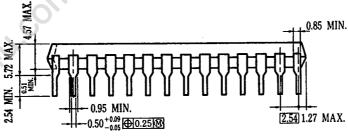
- 20 bit Output Data Latch Incorporated.
- 20 bit Output Drivers for FIP.
- Output Characteristics Vout = 40 V.

- Serial Interface Format: Compatible with NEC microcomputer.
- Brightness Control Enable: External Duty Control.
- Wide Operating Temperature Range Topt = -40 to +85 °C.
- 28 PIN Plastic Molded Slim DIP (Dual In line Package).

PACKAGE DIMENSIONS (Unit: mm)

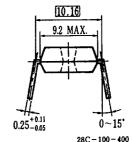
28PIN PLASTIC DIP(400mil)





NEC cannot assume a'. / responsibility for any circuits shown or represent that

they are free from patent infringement.



ABSOLUTE MAXIMUM RATINGS ($T_a = 25$ °C)

Supply Voltage at VDD terminal	VDD	-0.3 to +7.0 *1	V
Input Voltage	VIN	-0.3 to V _{DD} *1	V
Output Voltage (1~7, 15~27 Pins)	V _{O0} to V _{O19}	_35 *1, *2	V
Output Current (1~7, 15~27 Pins)	100 to 1019	– 5	mA
Operating Temperature Range	Topt	-40 to +85	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C

Notes: *1; These Voltage are referenced to the VSS.

*2; V_{DD} = 5 V

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature Range	T _{opt}	-40		+85	°C
Operating Supply Voltage	V _{DD}			5.5	V
Output Voltage (1~7, 15~27 Pins)	V _{O0 to} V _{O19}		-22	-35	. V
Output Current (1~7, 15~27 Pins)	100 to 1019		-2.0	-5.0	mA
Input Voltage High	VIH	0.7 V _{DD}		VDD	V
Input Voltage Low	VIL	VSS		0.3 V _{DD}	V
SCK Frequency	fSCK			500	kHz
SCK Cycle Time	tKCY	2.0			μs
SCK High Level Pulse Width	tКН	0.9			μs
SCK Low Level Pulse Width	tKL	0.9			μs
SI Setup Time to SCK1	^t SIK	0.4		<u> </u>	μs
SI Hold Time	[†] KSI	0.4			μs
CS↓-SCK↓ Valid Time	tCSL	0			μs
CS↓→SCK† Valid Time	tCSH	0.9		ļ	μs
SCK →LH↓ Valid Time	tSKL	0			μs
LH Low Level Pulse Width	tLL	1.8			μs
LH†-CS† Valid Time	tLHC	0.9			μs
LH Delay Time	tLHD			1.9	μs
	Operating Temperature Range Operating Supply Voltage Output Voltage (1~7, 15~27 Pins) Output Current (1~7, 15~27 Pins) Input Voltage High Input Voltage Low SCK Frequency SCK Cycle Time SCK High Level Pulse Width SCK Low Level Pulse Width SI Setup Time to SCK† SI Hold Time CS↓—SCK↓ Valid Time CS↓—SCK↓ Valid Time LH Low Level Pulse Width LH ↑—CS† Valid Time	Operating Temperature Range Operating Supply Voltage Output Voltage (1~7, 15~27 Pins) Output Current (1~7, 15~27 Pins) Input Voltage High Input Voltage High VIH Input Voltage Low SCK Frequency SCK Cycle Time tKCY SCK High Level Pulse Width SI Setup Time to SCK SI Hold Time CSI—SCK Valid Time tCSI SCK -LH Valid Time tSKL LH Low Level Pulse Width tLL LH1—CS† Valid Time tLHC	Operating Temperature Range Topt -40 Operating Supply Voltage VDD 4.5 Output Voltage (1~7, 15~27 Pins) V00 to V019 0 Output Current (1~7, 15~27 Pins) IO0 to IO19 0.7 VDD Input Voltage High VIH 0.7 VDD Input Voltage Low VIL VSS SCK Frequency fSCK 5CK SCK Cycle Time tKCY 2.0 SCK High Level Pulse Width tKH 0.9 SCK Low Level Pulse Width tKL 0.9 SI Setup Time to SCK† tSIK 0.4 SI Hold Time tCSL 0 CSI→SCK† Valid Time tCSL 0 SCK ¬LH‡ Valid Time tSKL 0 LH Low Level Pulse Width tLL 1.8 LH†→CS† Valid Time tLHC 0.9	Operating Temperature Range Topt -40 Operating Supply Voltage VDD 4.5 5.0 Output Voltage (1~7, 15~27 Pins) VO0 to VO19 -22 Output Current (1~7, 15~27 Pins) IO0 to IO19 -2.0 Input Voltage High VIH 0.7 VDD Input Voltage Low VIL VSS SCK Frequency fSCK -5CK SCK Cycle Time tKCY 2.0 SCK High Level Pulse Width tKH 0.9 SCK Low Level Pulse Width tKL 0.9 SI Setup Time to SCK† tSIK 0.4 SI Hold Time tCSI 0 CSI→SCK† Valid Time tCSH 0.9 SCK →LH‡ Valid Time tSKL 0 LH Low Level Pulse Width tLL 1.8 LH Low Level Pulse Width tLHC 0.9	Operating Temperature Range Topt -40 +85 Operating Supply Voltage VDD 4.5 5.0 5.5 Output Voltage (1~7, 15~27 Pins) VO0 toVO19 -22 -35 Output Current (1~7, 15~27 Pins) IO0 toIO19 -2.0 -5.0 Input Voltage High VIH 0.7 VDD VDD Input Voltage Low VIL VSS 0.3 VDD SCK Frequency fSCK 500 500 SCK Cycle Time tKCY 2.0

Notes: *3; These Voltage are referenced to the VDD.

^{*4;} See Fig. 1

^{*5;} See Fig. 2

^{*6;} See Fig. 3

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ELECTRICAL CHARACTERISTICS (Recommended Operating Conditions)

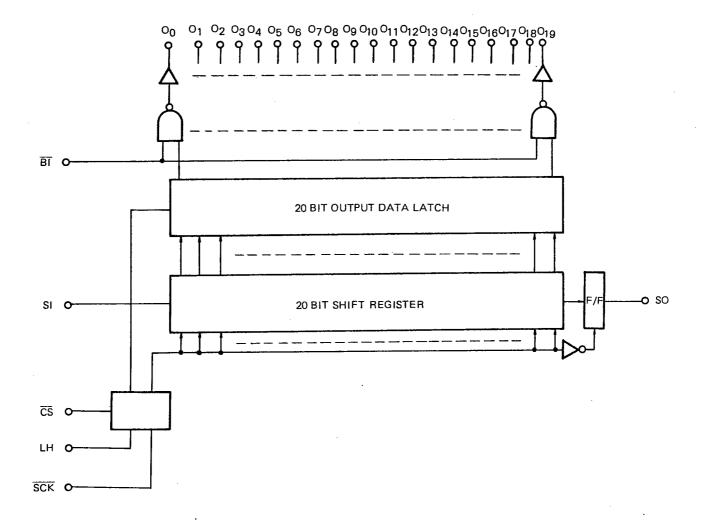
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Leakage Current	HL		-	±10	μΑ	VIN=VSS or VDD
SO Output Voltage High	VsoH	V _{DD} -1			V	ISOH=-1 mA
SO Output Voltage Low	VSOL			0.4	٧	ISOL=0.8 mA
Output Voltage High (1~7, 15~27 Pins)	Vo	V _{DD} -15				IO=-5 mA
					\ \	O0toO19 Output
Output Leakage Current (1~7,15~27 Pins)	lOLL1			1.0	μΑ	V ₀ =-10 V
	lOLL2			10.0	μΑ	V₀=-20 V
Supply Current at VDD Terminal	IDD					V _{DD} =5.5 V
				1	mA	All Input = [High]
						All Output = Open
SCKI →SO Valid Time	tKSO			0.5	μs	See Fig. 4
Input Capacitance	CIN			15	рF	f=1 MHz

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BLOCK DIAGRAM

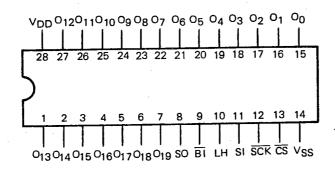


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PIN CONNECTION (Top View)



FUNCTION

00~019 :

Output, P ch MOS Open Drain

These 20 Outputs are the Outputs of 20 bit output data latch and can drive FIP directly.

ΒI

Blanking Input

When "L" level signal is supplied to the BI, O₀ to O₁₉ are disable.

"H": O0 to O19 are active.

LH

Latch and Hold Input

When "L" level signal is supplied to the LH,

The data of 20 bit shift register are normally transferred the 20 bit output data latch. At the time of the rising edge of LH; the data of 20 bit output data latch are hold.

"H"; The data of 20 bit output data latch are protected.

SI

Serial Data Input

SCK

Serial Clock Input

The SI data are read and stored in the 20 bit shift register at the rising edge of $\overline{\text{SCK}}$.

SO

Serial Data Output. CMOS push-pull

The SO is a signal of serial output data from 20 bit sift register.

CS

Chip Select Input

When the CS is "L" level, the LH and SCK are active.

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NEC ELECTRON DEVICE

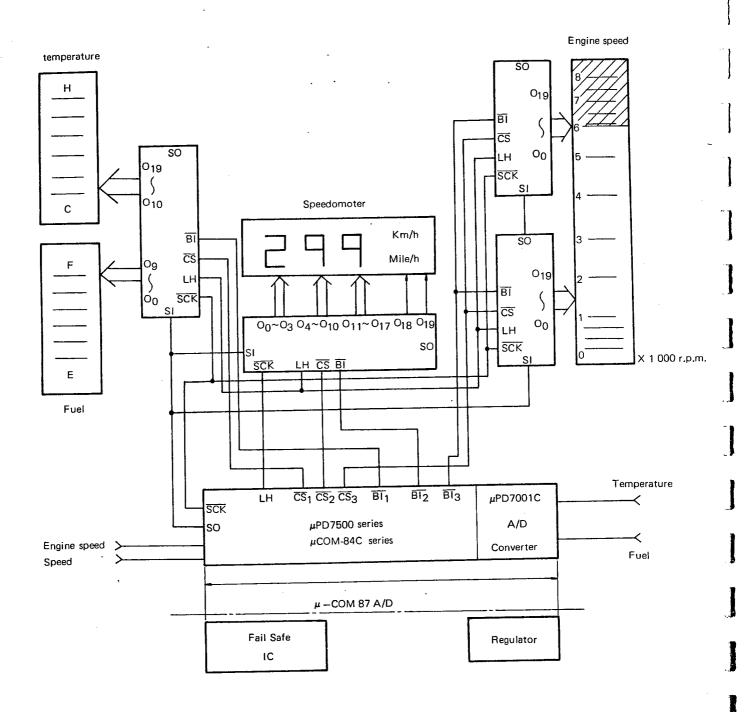
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APPLICATION CIRCUIT

AUTOMOTIVE DASHBOARD SYSTEM



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EXAMPLE OF SOFTWARE

Using of serial I/O of μ -COM75 series Subroutine of 24 bit data transfer

SI OUT :

ANP 6, 0BH

LHLI 05H

LOOP

LAM HL

TAMSIO

SIO

SKI 2

JCP \$-2

DLS

JCP LOOP

ANP 6, 7

ORP 6,8

ORP 6, 4

RT

RAM				
· (ADD)	3	2	1	0
00Н	03	02	01	00
01H	07	06	05	04
02H	011	010	O ₉	08
03H	015	014	013	012
04H	019	018	017	0 ₁₆
05H	023	022	021	O ₂₀

 $\mathsf{P}_{62} - \overline{\mathsf{CS}}$

P63 - LH

