

September 1983 Revised February 1999

MM74HC251 8-Channel 3-STATE Multiplexer

General Description

The MM74HC251 8-channel digital multiplexer with 3-STATE outputs utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power consumption of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The large output drive capability and 3-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is HIGH, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed

to the Y and W outputs. The 74HC logic family is speed, function, as well as pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $\rm V_{CC}$ and ground.

Features

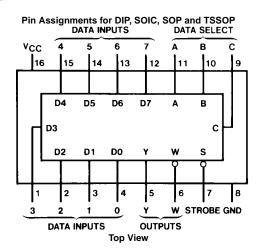
- Typical propagation delay Data select to Y: 26 ns
- Wide supply range: 2–6V
- Low power supply quiescent current: 80 µA maximum (74HC)
- 3-STATE outputs for interface to bus oriented systems

Ordering Code:

Order Number	Package Number	Package Description
MM74HC251M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74HC251SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC251MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC251N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

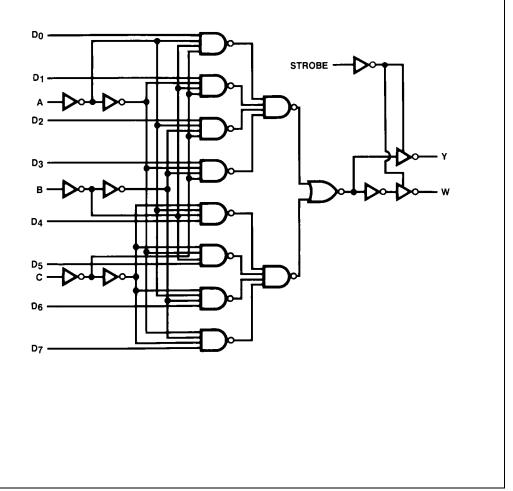


Truth Table

	Ir	Outputs				
	Select			v	w	
С	В	Α	S		••	
Х	Х	Х	Н	Z	Z	
L	L	L	L	D0	D0	
L	L	Н	L	D1	D1	
L	Н	L	L	D2	D2	
L	Н	Н	L	D3	D3	
Н	L	L	L	D4	D4	
Н	L	Н	L	D5	D5	
Н	Н	L	L	D6	D6	
Н	Н	Н	L	D7	D7	

$$\begin{split} H = & \text{HIGH Logic Level}, \, L = LOW \, \text{Logic Level} \\ X = & \text{Irrelevant}, \, Z = & \text{High Impedance (off)} \\ D0, \, D1. \quad . \quad D7 = & \text{The level of the respective D input} \end{split}$$

Logic Diagram



Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V _{CC})	-0.5 to $+7.0$ V
DC Input Voltage (V _{IN})	-1.5 to V_{CC} $+1.5V$
DC Output Voltage (V _{OUT})	-0.5 to V_{CC} $+0.5V$
Clamp Diode Current (I _{IK} , I _{OK})	±20 mA
DC Output Current, per pin (I _{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T _{STG})	-65°C to +150°C
Power Dissipation (P _D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T _L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units			
Supply Voltage (V _{CC})	2	6	V			
DC Input or Output Voltage						
(V _{IN} , V _{OUT})	0	V_{CC}	V			
Operating Temperature Range (T _A)	-40	+85	°C			
Input Rise or Fall Times						
$(t_r, t_f) V_{CC} = 2.0V$		1000	ns			
$V_{CC} = 4.5V$		500	ns			
$V_{CC} = 6.0V$		400	ns			
Note 1: Absolute Maximum Ratings are those values beyond which dam-						

age to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: –
12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	$T_A = -55$ to $125^{\circ}C$	Units
Syllibol	Farameter	Conditions	*cc	Тур		Guaranteed L		
V _{IH}	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V
	Input Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V _{IL}	Maximum LOW Level		2.0V		0.5	0.5	0.5	V
	Input Voltage		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level	$V_{IN} = V_{IH}$ or V_{IL}						
	Output Voltage	$ I_{OUT} \le 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level	$V_{IN} = V_{IH}$ or V_{IL}						
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μΑ
	Current							
l _{OZ}	Maximum 3-STATE	Strobe = V _{CC}	6.0V		±0.5	±5	±10	μΑ
	Leakage Current	$V_{OUT} = V_{CC}$ or GND						
Icc	Maximum Quiescent	V _{IN} = V _{CC} or GND	6.0V		8.0	80	160	μА
	Supply Current	$I_{OUT} = 0 \mu A$						

Note 4: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

 $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

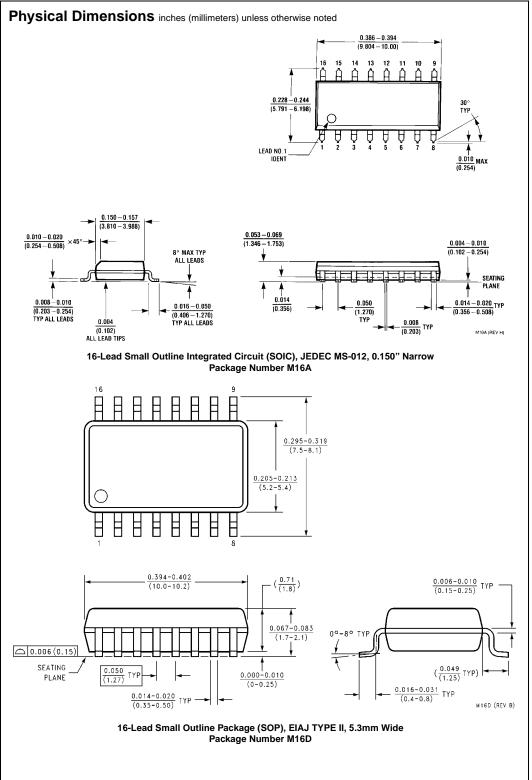
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
	Mariana Baranatia Balan		00		
t _{PHL} , t _{PLH}	Maximum Propagation Delay		26	35	ns
	A, B or C to Y				
t _{PHL} , t _{PLH}	Maximum Propagation		27	35	ns
	Delay, A, B or C to W				
t _{PHL} , t _{PLH}	Maximum Propagation		22	29	ns
	Delay, Any D to Y				
t _{PHL} , t _{PLH}	Maximum Propagation		24	32	ns
	Delay, Any D to W				
t _{PZH} , t _{PZL}	Maximum Output Enable	$R_L = 1 k\Omega$	19	27	ns
- <u></u>	Time, W Output	C _L = 50 pF			
t _{PZH} , t _{PZL}	Maximum Output Enable	$R_L = 1 k\Omega$	19	26	ns
	Time, Y Output	C _L = 50 pF			
t _{PHZ} , t _{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$	26	40	ns
	W Output	$C_L = 5 pF$			
t _{PHZ} , t _{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$	27	35	ns
	Y Output	$C_L = 5 pF$			

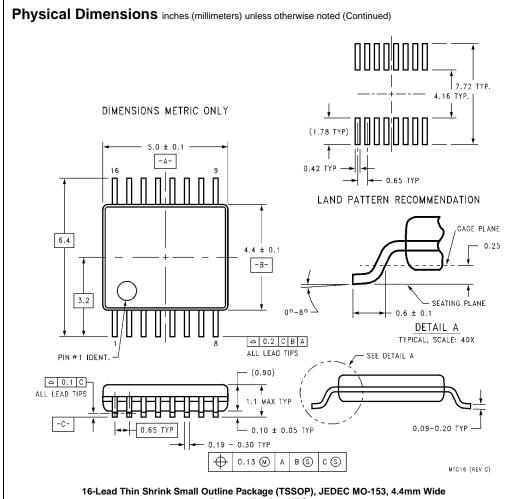
AC Electrical Characteristics

 $C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns} \text{ (unless otherwise specified)}$

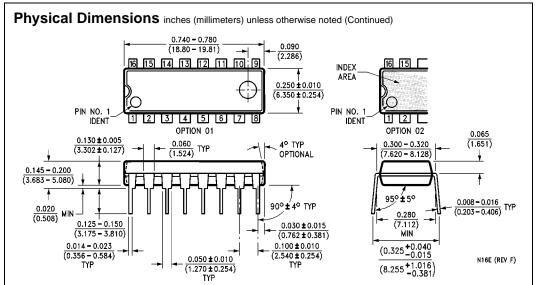
Symbol	Parameter	Conditions	v _{cc}	T _A = 25°C		$T_A = -40 \text{ to } 85^{\circ}\text{C}$	$T_A = -55$ to $125^{\circ}C$	Units
Cyllibol				Тур		Guaranteed L	anteed Limits	
t _{PHL} , t _{PLH}	Maximum Propagation Delay		2.0V	90	205	256	300	ns
	A, B or C to Y		4.5V	31	41	51	60	ns
			6.0V	26	35	44	51	ns
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	95	205	256	300	ns
	Delay, A, B or C to W		4.5V	32	41	51	60	ns
			6.0V	27	35	44	51	ns
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	70	195	244	283	ns
	Delay, any D to Y		4.5V	27	39	49	57	ns
			6.0V	23	33	41	48	ns
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	75	185	231	268	ns
	Delay, any D to W		4.5V	29	37	46	54	ns
			6.0V	25	32	40	46	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1 k\Omega$	2.0V	45	150	188	218	ns
	W Output		4.5V	21	30	38	44	ns
			6.0V	18	26	33	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1 k\Omega$	2.0V	45	145	181	210	ns
	Y Output		4.5V	21	29	36	42	ns
			6.0V	18	25	31	36	ns
t_{PHZ},t_{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$	2.0V	60	220	275	319	ns
	W Output		4.5V	29	44	55	64	ns
			6.0V	25	37	46	54	ns
t _{PHZ} , t _{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$	2.0V	60	195	244	283	ns
	Y Output		4.5V	30	39	49	57	ns
			6.0V	26	33	41	48	ns
t_{THL} , t_{TLH}	Maximum Output Rise		2.0V	30	75	95	110	ns
	and Fall Time		4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C _{PD}	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} f + I_{CC} \ V_{CC}$.





16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16A

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