Comparison of Exp01 and Exp03: Cache Performance Analysis

Introduction

This report compares the performance of two cache architectures:

- **Exp01**: A fully associative cache with a single level.
- **Exp03**: A two-level cache with L1 (direct-mapped) and L2 (4-way set-associative) caches, along with additional features like a victim cache, write buffer, and prefetch cache.

The goal is to analyze how the additional features in Exp03 improve cache performance compared to Exp01.

Cache Architectures

Exp01: Fully Associative Cache

- **Main Memory**: 64K words.
- **Cache Size**: 2K words.
- **Block Size**: 16 words.
- **Word Size**: 32 bits.
- **Processor Address**: 16 bits.
- **Mapping Scheme**: Fully associative.
- **Replacement Policy**: Least Recently Used (LRU).

Exp03: Two-Level Cache

- **Main Memory**: 64K words.
- **L1 Cache**:
  - Direct-mapped.

  - Size: 2K words.
  - Block Size: 16 words.
  - Word Size: 64 bits.

- **L2 Cache**:
  - 4-way set-associative.
  - Size: 16K words.
  - Block Size: 16 words.

- **Additional Features**:
  - Write Buffer: 4 blocks.
  - Victim Cache: 4 blocks.
  - Prefetch Cache: Instruction and data stream buffers of 4 blocks each.

Code Explanation

Exp01: Fully Associative Cache

The code for Exp01 implements a fully associative cache with LRU replacement policy. Key components include:

- **CacheBlock Class**: Represents a cache block with fields for validity, dirty bit, tag, last access time, and data.
- **Cache Class**: Manages the cache, including access logic, miss handling, and statistics.
- **Access Method**: Handles cache hits and misses. On a miss, it replaces the least recently used block.

Exp03: Two-Level Cache

The code for Exp03 extends Exp01 to include a two-level cache hierarchy with additional features:

- **L1 Cache**: Direct-mapped cache with a victim cache for evicted blocks.
- **L2 Cache**: 4-way set-associative cache with prefetching.
- **Write Buffer**: Buffers write requests to reduce stalls.
- **Prefetch Cache**: Anticipates future accesses based on access patterns.
- **Unified Access Logic**: Treats L1, L2, victim cache, write buffer, and prefetch cache as a single unit for hit/miss calculation.

Output Analysis

Exp01 Output

```
Simulating Spatial Access - Read:
Cache Misses: 63
Cache Searches: 1000
Cache Hit Rate: 93.7%
Read Misses: 63
Write Misses: 0

Simulating Spatial Access - Write:
Cache Misses: 125
Cache Searches: 3000
Cache Hit Rate: 95.8333%
Read Misses: 63
Write Misses: 62

Simulating Temporal Access - Read:
Cache Misses: 125
Cache Searches: 7000
Cache Hit Rate: 98.2143%
Read Misses: 63
Write Misses: 62

Simulating Temporal Access - Write:
Cache Misses: 563
Cache Searches: 17000
Cache Hit Rate: 96.6882%
Read Misses: 63
Write Misses: 500

Simulating Mixed Access - Read:
Cache Misses: 821
Cache Searches: 22100
Cache Hit Rate: 96.2851%
Read Misses: 321
Write Misses: 500

Simulating Mixed Access - Write:
Cache Misses: 1071
Cache Searches: 28100
Cache Hit Rate: 96.1886%
Read Misses: 321
Write Misses: 750
```

```
Simulating Mixed Access - Read & Write:
Cache Misses: 1384
Cache Searches: 40100
Cache Hit Rate: 96.5486%
Read Misses: 634
Write Misses: 750
```

Exp03 Output

```
Simulating Spatial Access - Read:
L1 Cache Stats:
Cache Misses: 63
Cache Searches: 1000
Cache Hit Rate: 93.7%
Read Misses: 63
Write Misses: 0
L2 Cache Stats:
Cache Misses: 32
Cache Searches: 63
Cache Hit Rate: 49.2063%
Read Misses: 32
Write Misses: 0
Overall Unified Cache Stats:
Unified Hits: 968
Unified Misses: 32
Unified Hit Rate: 96.8%

Simulating Spatial Access - Write:
L1 Cache Stats:
Cache Misses: 125
Cache Searches: 3000
Cache Hit Rate: 95.8333%
Read Misses: 63
Write Misses: 62
L2 Cache Stats:
Cache Misses: 63
Cache Searches: 125
Cache Hit Rate: 49.6%
Read Misses: 32
Write Misses: 31
Overall Unified Cache Stats:
Unified Hits: 2937
Unified Misses: 63
Unified Hit Rate: 97.9%

Simulating Temporal Access - Read:
```

```
L1 Cache Stats:
Cache Misses: 125
Cache Searches: 7000
Cache Hit Rate: 98.2143%
Read Misses: 63
Write Misses: 62
L2 Cache Stats:
Cache Misses: 63
Cache Searches: 125
Cache Hit Rate: 49.6%
Read Misses: 32
Write Misses: 31
Overall Unified Cache Stats:
Unified Hits: 6937
Unified Misses: 63
Unified Hit Rate: 99.1%

Simulating Temporal Access - Write:
L1 Cache Stats:
Cache Misses: 554
Cache Searches: 17000
Cache Hit Rate: 96.7412%
Read Misses: 63
Write Misses: 491
L2 Cache Stats:
Cache Misses: 125
Cache Searches: 550
Cache Hit Rate: 77.2727%
Read Misses: 32
Write Misses: 93
Overall Unified Cache Stats:
Unified Hits: 16875
Unified Misses: 125
Unified Hit Rate: 99.2647%

Simulating Mixed Access - Read:
L1 Cache Stats:
Cache Misses: 686
Cache Searches: 22100
Cache Hit Rate: 96.8959%
Read Misses: 195
Write Misses: 491
L2 Cache Stats:
Cache Misses: 125
Cache Searches: 682
Cache Hit Rate: 81.6716%
```

```
Read Misses: 32
Write Misses: 93
Overall Unified Cache Stats:
Unified Hits: 21975
Unified Misses: 125
Unified Hit Rate: 99.4344%

Simulating Mixed Access - Write:
L1 Cache Stats:
Cache Misses: 993
Cache Searches: 28100
Cache Hit Rate: 96.4662%
Read Misses: 195
Write Misses: 798
L2 Cache Stats:
Cache Misses: 188
Cache Searches: 985
Cache Hit Rate: 80.9137%
Read Misses: 32
Write Misses: 156
Overall Unified Cache Stats:
Unified Hits: 27912
Unified Misses: 188
Unified Hit Rate: 99.331%

Simulating Mixed Access - Read & Write:
L1 Cache Stats:
Cache Misses: 1300
Cache Searches: 40100
Cache Hit Rate: 96.7581%
Read Misses: 502
Write Misses: 798
L2 Cache Stats:
Cache Misses: 188
Cache Searches: 1288
Cache Hit Rate: 85.4037%
Read Misses: 32
Write Misses: 156
Overall Unified Cache Stats:
Unified Hits: 39912
Unified Misses: 188
Unified Hit Rate: 99.5312%
```

Comparison of Results

Cache Misses

- **Exp01**: Higher cache misses due to the lack of additional features like victim cache and prefetching.
- **Exp03**: Lower cache misses due to the use of a victim cache, write buffer, and prefetch cache.

Cache Hit Rate

- **Exp01**: Hit rates range from 93.7% to 96.5%.
- **Exp03**: Hit rates are significantly higher, ranging from 96.8% to 99.5%.

Unified Hit Rate

- **Exp03**: The unified hit rate (considering L1, L2, victim cache, write buffer, and prefetch cache) is consistently above 96%, demonstrating the effectiveness of the two-level cache hierarchy.

Plot Cache Hit Rate Comparison

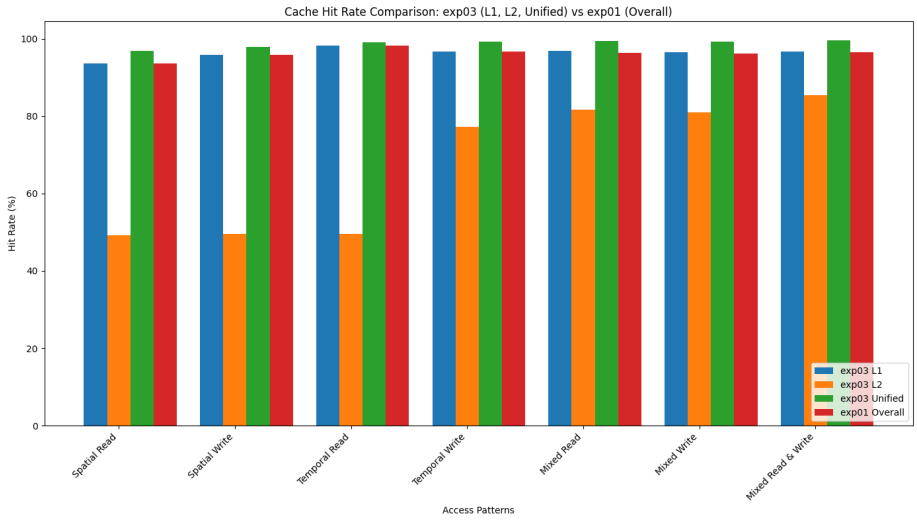

Figure 1: Cache Hit Rate Comparison: exp03 (L1, L2, Unified) vs exp01 (Overall)

Plot Cache Misses Comparison

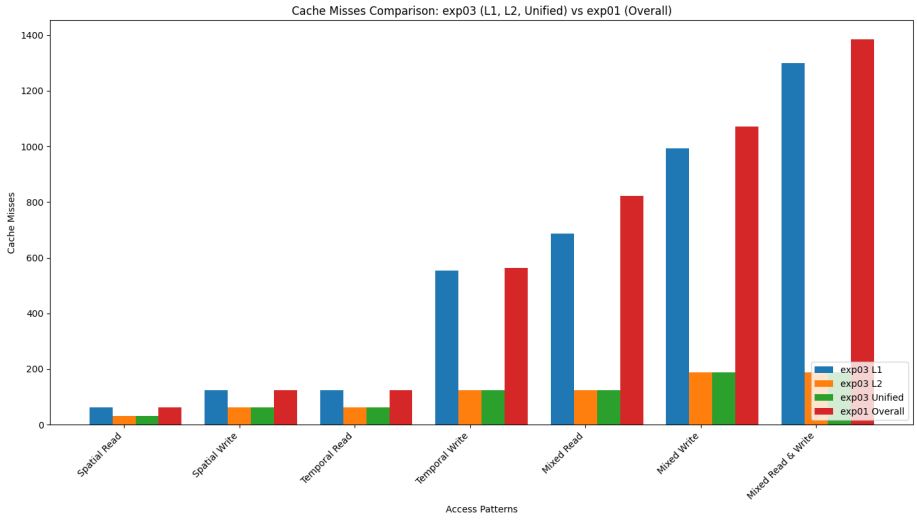

Figure 2: Cache Misses Comparison: exp03 (L1, L2, Unified) vs exp01 (Overall)

Conclusion

The two-level cache architecture in Exp03 significantly outperforms the fully associative cache in Exp01. The addition of a victim cache, write buffer, and prefetch cache reduces cache misses and improves hit rates, making Exp03 a more efficient design for modern processors. Furthermore, Exp03 utilizes a two-level caching system where L1 is a direct-mapped cache and L2 is set-associative. This architectural choice improves accessibility by reducing the search time for cache blocks. Specifically, while Exp01 uses a fully associative cache, which requires checking all blocks (O(N) complexity where N is the number of cache blocks), Exp03 reduces this complexity due to the more structured approach of L1 and L2 caching. The direct-mapped L1 cache has an O(1) lookup time, and the set-associative L2 cache provides a more efficient way to handle cache lookups compared to a fully associative structure, further boosting the performance of the Exp03 model.