PORTLAND STATE UNIVERSITY
CS201: COMPUTER SYSTEMS PROGRAMMING (SECTION 5)
SPRING 2020

HOMEWORK 5
DUE: JUNE 3rd, 2020 by 6:00 pm (Scan or Type and Submit ON D2L)

Instructions:

Show all your work. You must work in this assignment individually.

1) Assembly Programming
   a) **Write the following C function in Assembly**. You must follow the System V 64-bit calling convention and use AT&T Syntax notation. Note: You cannot change the algorithm in any way so your assembly function must still be recursive. (20 points)

```
long fibonacci(long n)
{
      if ( n == 0) return 0;
      else if ( n == 1) return 1;
            else return (fibonacci(n-1) + fibonacci(n-2));
}
```

   b) The Windows x86-64 calling convention passes function parameters in the registers RCX, RDX, R8 and R9 and returns values on register RAX. Caller saved registers are: RAX, RCX, RDX, R8, R9, R10 and R11, while callee-saved registers are RBX, RBP, RDI, RSI, RSP, R12, R13, R14, and R15. **Rewrite the assembly function from Part A using the Windows x86-64 calling convention** instead of the System V 64- bit calling convention. (16 points)

2) Pipelining
   a) A 5-Stage pipeline is composed of the following stages Instruction Fetch (IF), Decode (DE), Execute (EX), Memory Access (ME) and Register Write-back (WB). Assume the pipeline does not have a branch prediction unit, does not have superscalar support and does not support out of order execution. Assume that all memory accesses are in the L1 cache and therefore they do not introduce any stalls (as we assumed in Lecture)**. Show a pipeline diagram that shows the execution of each stage for the assembly code below**. Also **specify why each pipeline Stall is introduced**. (16 points)

```
addq %rax, (%rbx)
subq %rcx, %rax
movq $0, %rdx
movq $1, %rdx
xorq %rsi, (%rbx)
movq %rsi, %r10
```

```
movq %r10, %r11
```

3) Performance
   a) A famous hardware company is deciding to improve the performance of their multi-cycle processors but they can only do one of the possible options and they are not sure what the best decision is. Their current processor has the following instruction timings: Arithmetic 5 cycles, Branches 8 cycles, Load/Stores 6 cycles.
   The first option is to double the speed of the Arithmetic Logic Unit, thus reducing the instruction timing of their Arithmetic instructions to 3 cycles.
   The second option is to improve the branch unit that will reduce the instruction timing of branches to 4 cycles.
   It is believed that the typical instruction mix for this architecture is 40% arithmetic instructions, 30% branches and 30% load and stores. Use Amdahl's law to **compute the performance improvement of each option and decide which one is the best for the improved processor.** (16 points)

   b) A new smartphone just out on the market has a L1 cache with an access time of 1 cycle, an L2 cache with an access time of 5 cycles and DRAM with access time of 30 cycles. The latest benchmarks indicate that for most applications the L1 hit rate is 80% and L2 hit rate is 95%. **Compute the Average Memory Access Time for the memory hierarchy in this device**. (16 points)

   c) The new TurtleMax Hard Drive has an average seek time of 7 ms, it has an average rotational speed of 6000 RPM and 250 sectors/track. **Compute how much time it would take to read one sector.** (16 points)