

The Cycle-Accurate Game Boy Docs

Version 0.1

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1. Introduction

Since nobody seems to care about documenting the Game Boy good enough to make a cycle-accurate emulator (the only “documentation” there is right now is the source code of the emulator [Gambatte](#), and it requires a lot of time to understand how it works), I've decided to document it myself. The reason is that I'm making my own GB emulator and I just can't find any of the information I want, so I decided to document the GB while I code my own open-source emulator ([GiiBiiAdvance](#)) and check if my assumptions are correct. I've started with the timer, but I plan to document the complete Game Boy and Game Boy Color.

I'm using information from the [Pan Docs](#) (a LOT from here, in fact), the source code of [Gambatte](#) and some other documents by other authors (all of them in the credits of this file), but the most important source of knowledge about the Game Boy is the Game Boy itself! That's why I've created lots of test ROMs to verify specific behaviours of the original hardware. I have an original GB, a GB Pocket, two different GB Color, a GB Advance and a GBA SP. While most of the test give the same results in every hardware, there are some things that are different, so I've tried to document them as detailed as I can.

Here are some abbreviations and nomenclature I'll use in this document:

- DMG/GB: Original Game Boy (Dot Matrix Game)
- MGB/GBP: Game Boy Pocket / Game Boy Light
- SGB/SGB2: Super Game Boy / Super Game Boy 2
- CGB/GBC: Game Boy Color
- AGB/GBA: Game Boy Advance
- AGS/GBA SP: Game Boy Advance SP
- Clock: Oscillator clock frequency is 4194304 Hz (8388608 Hz in double speed mode)
- Cycle: CPU cycle frequency is 1048576 Hz (2097152 Hz in double speed mode)

Whenever I write sample code I'll use [RGBDS](#) syntax, and I'll use the definitions of the file “Gameboy Hardware definitions” (hardware.inc).

2. Memory

General memory map

Addresses	Name	Description
0000h – 3FFFh	ROM0	Non-switchable ROM Bank.
4000h – 7FFFh	ROMX	Switchable ROM bank.
8000h – 9FFFh	VRAM	Video RAM, switchable (0-1) in GBC mode.
A000h – BFFFh	SRAM	External RAM in cartridge, often battery buffered.
C000h – CFFFh	WRAM0	Work RAM.
D000h – DFFFh	WRAMX	Work RAM, switchable (1-7) in GBC mode
E000h – FDFh	ECHO WRAM	Mirror to C000h – DDFFh
FE00h – FE9Fh	OAM	(Object Attribute Table) Sprite information table.
FEA0h – FEFh	HOAM	Unusable memory.
FF00h – FF7Fh	I/O Registers	I/O registers are mapped here.
FF80h – FFEh	HRAM	Internal CPU RAM
FFFFh	IE Register	IRQ enable flags.

Jump Vectors in ROM0

Some addresses in ROM0 are jump vectors:

0000h, 0008h, 0010h, 0018h, 0020h, 0028h, 0030h, 0038h – For RST instruction of CPU.
0040h, 0048h, 0050h, 0058h, 0060h – Interrupt Vectors (VBL, LCD, Timer, Serial, Joypad)

Unused vectors may be used for whatever purpose the program wants. RST are special instructions like CALL, but they are 1 byte long instructions (CALL are 3 bytes long) and need 2 cycles less.

Cartridge Header in ROM0

The data from 100h to 14Fh of the ROM bank 0 is the ROM header. Contains some information about the program and the cartridge used. Some games don't fill correctly this area, though. For more information, read the chapter about it.

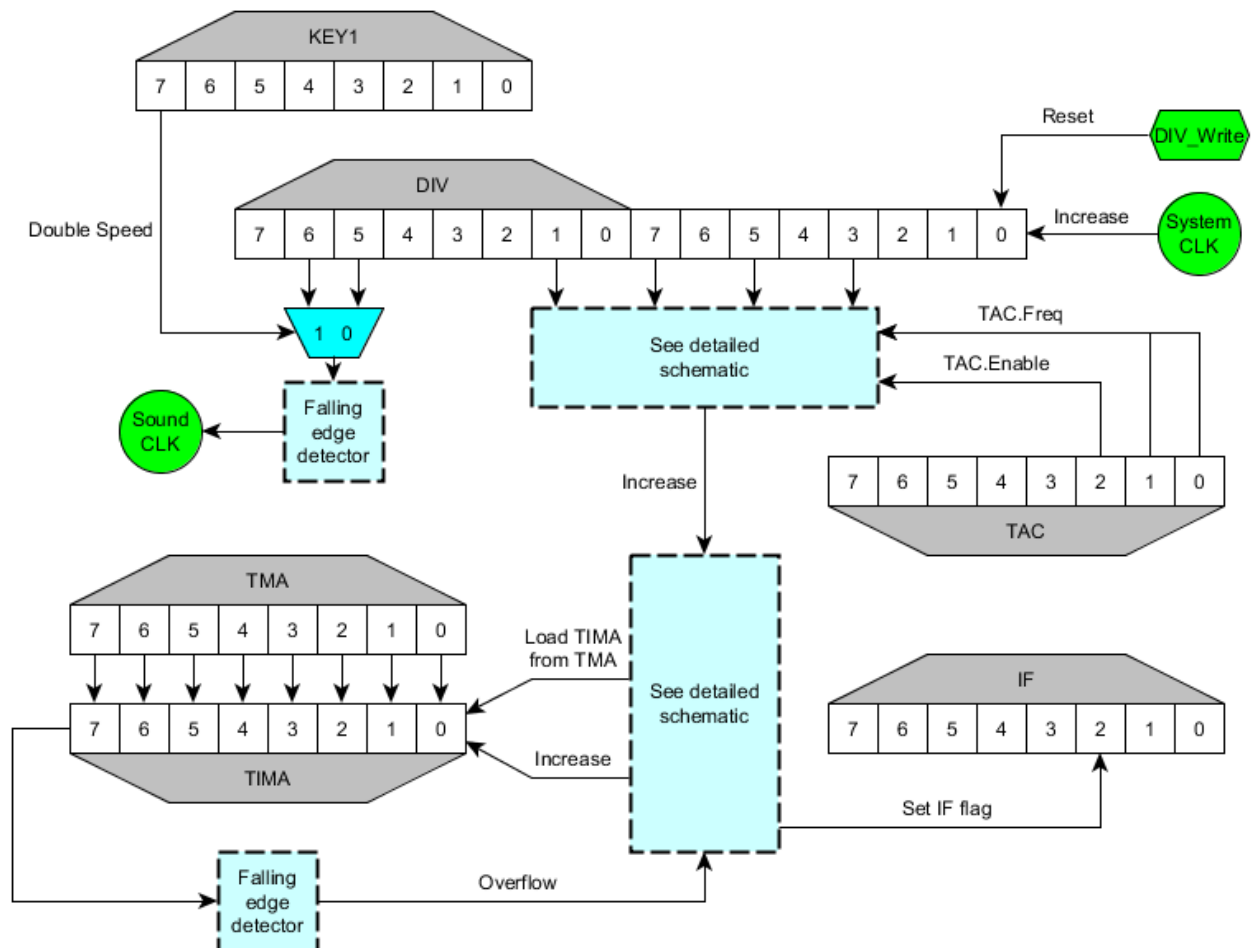
External Memory and Hardware

Areas from 0000h – 7FFFh and A000h – BFFFh are mapped to the cartridge. The first area is usually used for ROM, and the second one is used for RAM and external registers (if any). Writes to ROM area are interpreted by the Memory Bank Controller (MBC) chip.

3. Interrupts

4. Timer

The Game Boy timer subsystem is formed by the three timer registers (TIMA, TMA and TAC), and the DIV register. This is a simplified schematic:



FF04h - DIV - Divider Register (R/W*)

- It works by using an internal system 16 bit counter. The counter increases each clock (4 clocks per nop) and the value of DIV is the 8 MSB of the counter: Increases every 256 oscillator clocks.
- The value of DIV is the actual bits of the system internal counter, not a mirror, not a register that increases with the system internal counter: The actual bits of the counter mapped to memory.
- DIV overflows at 64 Hz in normal speed mode, 128 Hz in double speed mode.
- It can be written, but its value is reset to 0 no matter what the value written is. In fact, the whole system internal counter is set to 0. DIV is just its the 8 MSB of that counter, so DIV is set to 0 too.
- Serial clock is not derived from this counter, it is not affected by DIV register.

Interaction with APU

- The APU uses the DIV to update sweep (channel 1), fade in/out and time out, the same way the timer uses it to update itself.
- In normal speed mode the APU updates when bit 5 of DIV goes from 1 to 0 (256 Hz). In double speed mode, bit 6.
- Writing to DIV every instruction, for example, will make the APU produce the same frequency with the same volume even if sweep and fade out are enabled.
- Writing to DIV doesn't affect the frequency itself. The waveform generation is driven by another timer.

FF05h - TIMA - Timer Counter (R/W)

- This register is the timer counter, it increases at a certain frequency until it overflows. In that moment, the value in register TMA is loaded into TIMA and an interrupt is requested if the corresponding IE flag is set and IME is set to 1. The IRQ vector is address 0050h.

FF06h - TIMA - Timer Modulo (R/W)

The data in this register is loaded into TIMA when it overflows.

FF07h - TAC - Timer Control (R/W)

This register enables/disables the timer and sets its frequency.

Bit 2 - Timer Enable (0=Disable, 1=Enable)
Bits 1-0 - Main Frequency Divider

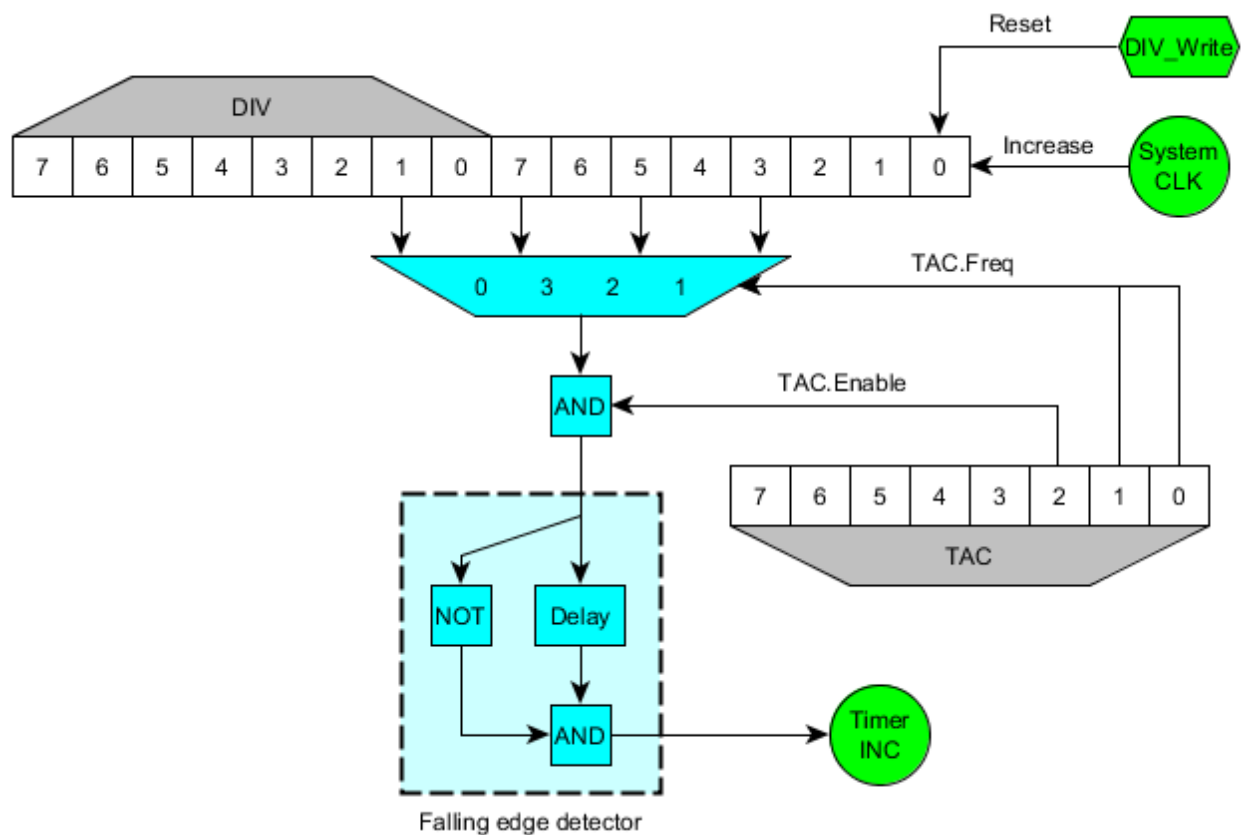
00:	4096 Hz (Increase every 1024 clocks)
01:	262144 Hz (" " 16 clocks)
10:	65536 Hz (" " 64 clocks)
11:	16386 Hz (" " 256 clocks)

Timer obscure behaviour

The signal used to increase the TIMA register is generated in a weird way. It selects the actual value of one bit of the system internal counter, and performs an and operation with the enable bit in TAC. This means that writing to the DIV register affects the timer too (writing to timer registers doesn't affect the DIV register).

- For example, if DIV register is written every 12 clocks, even in the fastest timer configuration, it will never increase. If the timer is configured to increase every 64 clocks but the program writes to it every 20 clocks, it will never increase (but it would if it was configured to increase every 16 clocks).

The next picture is a schematic of the relationship between the DIV register and the timer in a DMG or MGB for a better understanding of its behaviour:



As you can see, TAC register only selects the bit of the system internal counter that will be used to increase the timer counter. Then, it performs a logical AND operation with the enable bit in TAC and that signal goes to a falling edge detector.

For example, if timer is configured to increase every 64 clocks, TAC will select bit 5 of the system internal counter. As soon as it overflows from bit 5 and goes back to 0, the falling edge detector will trigger a pulse to increase TIMA register.

This circuit has three problems:

- When writing to DIV register the TIMA register can be increased if the counter has reached half the clocks it needs to increase, since the selected bit by the multiplexer will go from 1 to 0 (which is a falling edge, that will be detected by the falling edge detector).
- When disabling the timer, if the corresponding bit in the system counter is set to 1, the falling edge detector will see a change from 1 to 0, so TIMA will increase. This means that whenever half the clocks of the count are reached, TIMA will increase when disabling the timer.
- When changing TAC register value, if the old selected bit by the multiplexer was 0, the new one is 1, and the new enable bit of TAC is set to 1, it will increase TIMA.

This behaviour is a lot glitchier in newer models. DMG and MGB behave the same way (SGB and SGB2 haven't been tested), but GBC, AGB and AGS (GBA SP) are completely different. In fact, different revisions of the GBC have a different behaviour. The DMG behaviour when writing to TAC is this:

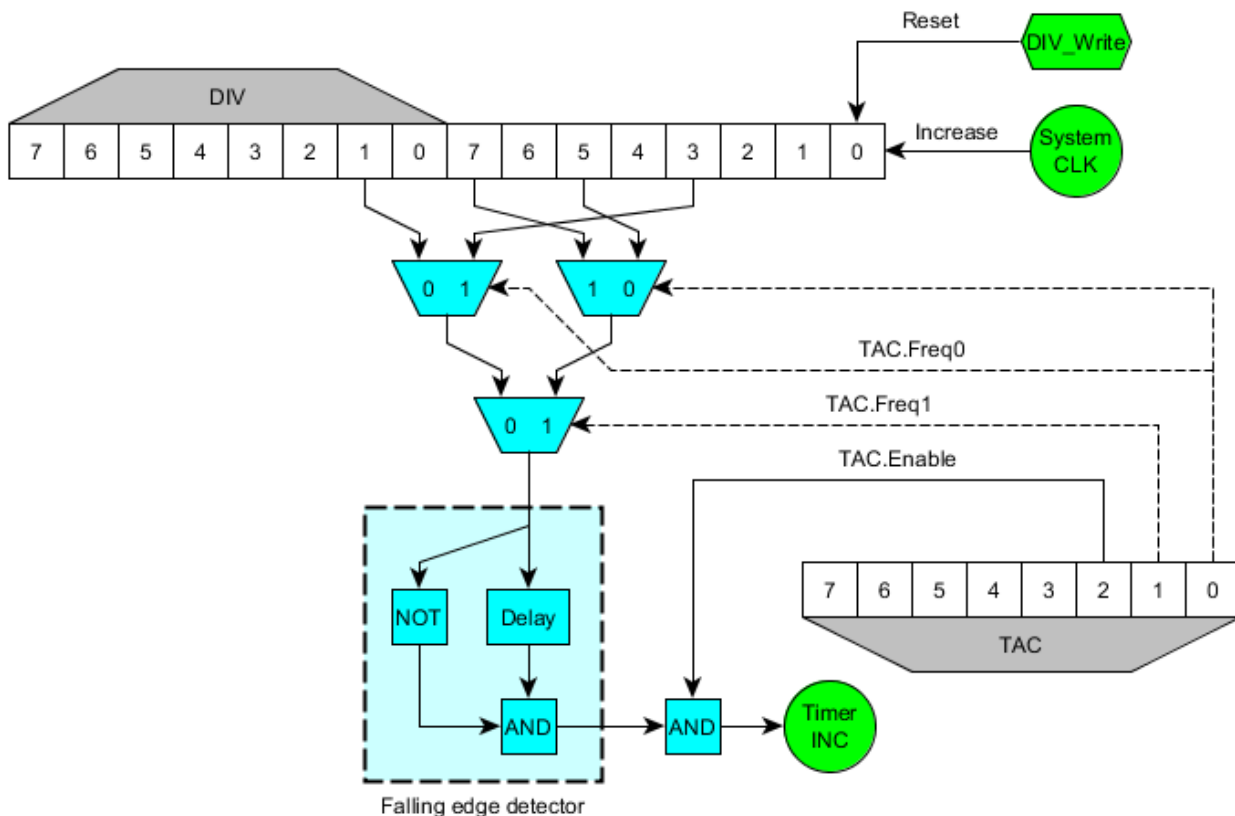

```

IF old_enable == 0 THEN
    glitch = 0 (*)
ELSE
    IF new_enable == 0 THEN
        glitch = (( (sys_clocks & (old_clocks/2)) != 0)
    ELSE
        glitch = (( (sys_clocks & (old_clocks/2)) != 0) && ( (sys_clocks & (new_clocks/2)) == 0)
    END IF
END IF

```

For example, if the old TAC value was 6, old_clocks is 64 and old_enabled is 1. If the written TAC value is 0, new_clocks is 1024 and new_enabled is 0.

The sentence marked with a (*) has a different behaviour in GBC (AGB and AGS seem to have strange behaviour even in the other statements). When enabling the timer and maintaining the same frequency it doesn't glitch. When disabling the timer it doesn't glitch either. When another change of value happens (so timer is enabled after the write), the behaviour depends on a race condition, so it cannot be predicted for every device. One possible explanation is that the AND gate corresponding to the enable bit is placed after the edge detector (?):



A safe way to set up the timer is:

```

ld a,TACF_16KHZ      ; Or the frequency needed.
ld [rTAC],a          ; Disable timer and load new frequency.
ld [rDIV],a           ; Reset system counter.
ld a,__TMA_VALUE__   ; __TMA_VALUE__ is any byte value.
ld [rTMA],a           ; Load modulo value in both
ld [rTIMA],a          ; TMA and TIMA registers.
ld a,TACF_16KHZ|TACF_START
ld [rDIV],a           ; Synchronize system counter.
ld [rTAC],a           ; Enable timer.

```

If the timer IRQ is going to be used:

```
ld  b,~IEF_TIMER
ld  a,[rIE]
and a,b
ld  [rIE],a          ; Clear IE timer flag.

ld  a,TACF_16KHZ
ld  [rTAC],a         ; Disable timer and load new frequency.
ld  [rDIV],a         ; Reset system counter.
ld  a,__TMA_VALUE__  ; __TMA_VALUE__ is any byte value.
ld  [rTMA],a         ; Load modulo value in both
ld  [rTIMA],a        ; TMA and TIMA registers.

ld  a,[rIF]
and a,b
ld  [rIF],a          ; Clear IF timer flag.
ld  b,IEF_TIMER
ld  a,[rIE]
or  a,b
ld  [rIE],a          ; Set IE timer flag.

ld  a,TACF_16KHZ|TACF_START
ld  [rDIV],a         ; Synchronize system counter.
ld  [rTAC],a         ; Enable timer.
```

Timer Overflow Behaviour

When TIMA overflows, the value from TMA is loaded and IF timer flag is set to 1, but this doesn't happen immediately. Timer IRQ is delayed 1 cycle (4 clocks) from the TIMA overflow. The TMA reload to TIMA is also delayed. For one cycle, after overflowing TIMA, the value in TIMA is 00h, not TMA.

For example (SYS is the system internal counter divided by 4 for easier understanding, each increment of the graph is 1 cycle, not 1 clock):

Timer overflows:

				[A]	[B]		
SYS	FD	FE	FF	00	01	02	03
TIMA	FF	FF	FF	00	23	23	23
TMA	23	23	23	23	23	23	23
IF	E0	E0	E0	E0	E4	E4	E4

Timer doesn't overflow:

				[C]			
SYS	FD	FE	FF	00	01	02	03
TIMA	45	45	45	46	46	46	46
TMA	23	23	23	23	23	23	23
IF	E0	E0	E0	E0	E0	E0	E0

- During the strange cycle [A] you can prevent the IF flag from being set and prevent the TIMA from being reloaded from TMA by writing a value to TIMA. That new value will be the one that stays in the TIMA register after the instruction. Writing to DIV, TAC or other registers won't prevent the IF flag from being set or TIMA from being reloaded.

- If you write to TIMA during the cycle that TMA is being loaded to it [B], the write will be ignored and TMA value will be written to TIMA instead.

- If TMA is written the same cycle it is loaded to TIMA [B], TIMA is also loaded with that value.

5. Serial

6. Video controller

7. Audio processing unit

8. The Game Boy Cartridge

9. Credits