Aaryan Dhawan

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Education/Affiliation

Virginia Tech, BS in Computer Engineering, Chip-Scale Integration — August 2020 - May 2024
Virginia Tech, M.Eng in Computer Engineering, VLSI and Design Automation — August 2024 - May 2026
Virginia Tech, Member of the BRICCS Research Group — Joined March 2025

- GPA: 3.7/4.0
- **Coursework:** Computer Architecture, VLSI circuit design, Digital/RTL design, Semiconductor manufacturing

Projects

Reservoir Computing Learning Engine RTL Design, June 2025 - Present

- Identified areas for optimization in State-of-the-Art RTL design for hardware learning engines
- Implemented resources reduction techniques to improve overall power consumption and increased system throughput
- Researching further extensions and applications of the learning engine design

Hardware Friendly Learning Rule for Spiking Neural Network, March 2025 - Present

- Researching highly performative neural network learning rules, optimized for binary classification
- Applying learning rules in a hardware efficient manner for local learning in a novel design for a Spiking neural network dealing with uni-variate data sets

Izhikevich Spiking Neural Network for FPGAs, Spring 2025

- Used a hardware-efficient Izhikevich Neuron model to create a Spiking Neural Network for Character Recognition for low-latency inference
- Created two versions of the network, one for high performance and the other for low resource utilization

GaN HEMT Package Design and Analysis, Spring 2025

- Created a package design for a Gallium Nitride High Electron Mobility Transistor in Ansys Q3D
- Package design was able to achieve low power loss and high current, reaching 65A drain current under a 48V drain/source load

McLaurin Series Solver Projects , Spring 2024

- Designed RTL models to solve the McLaurin Series using Intel Floating Point IP cores
- 3 solutions, each with a separate focus on performance, area, and bare metal programming

VLSI Circuit Design Projects , Fall 2023

- Series of VLSI circuit design project using Cadence Virtuoso, revolving designing and testing integrated circuit schematics and layouts
- Ranging from basic logic gates to 16-bit Fast Adders and 12-bit Braun Multiplier layouts, optimizing for low area, low power, and high performance

ReRAM Research Capstone Project, Fall 2023 - Spring 2024

- Led a senior level research group in understanding the thermodynamics and design of an experimental Resistive RAM chip. Assisted in model design in Ansys Workbench
- Develop Python based GUI to perform thermal analysis based on customer data to validate experiments and visualize data

Skills

C/C++ , Verilog/SystemVerilog, Python, MIPS/RISC-V Assembly, Xilinx Vivado ML, Intel Quartus Prime, Cadence Virtuoso