

# 1. Description

## 1.1. Project

Project Name	rtb-software
Board Name	NUCLEO-L4R5ZI
Generated with:	STM32CubeMX 6.1.2
Date	04/08/2021

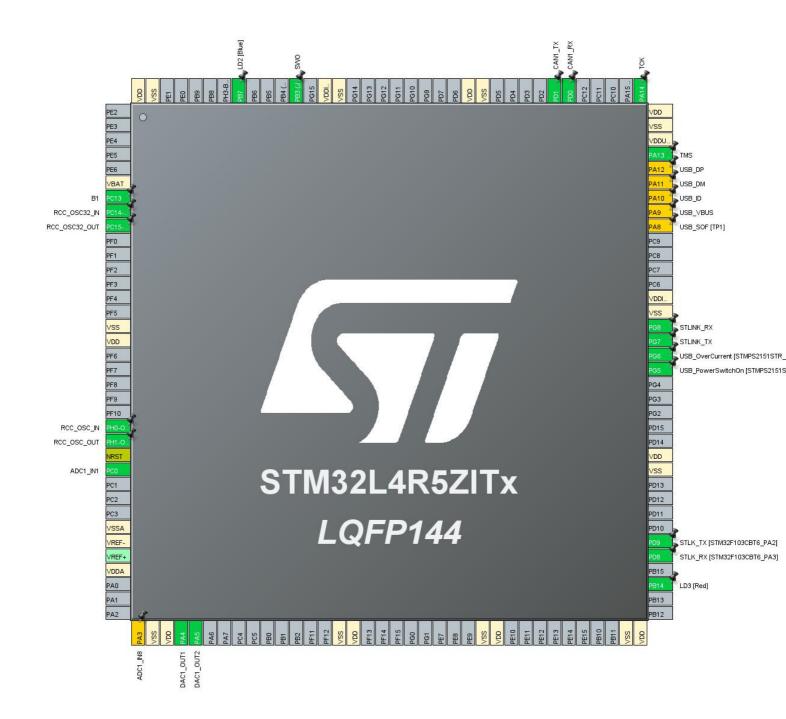
## 1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4R5/S5
MCU name	STM32L4R5ZITx
MCU Package	LQFP144
MCU Pin number	144

## 1.3. Core(s) information

Core(s)	Arm Cortex-M4

## 2. Pinout Configuration



# 3. Pins Configuration

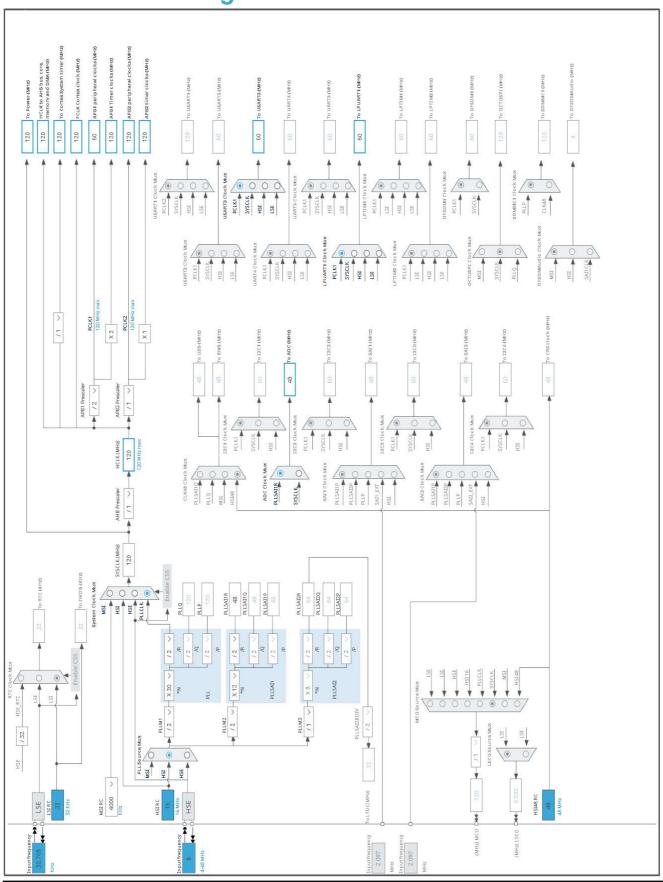
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	B1
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	ADC1_IN1	
30	VSSA	Power		
31	VREF-	Power		
33	VDDA	Power		
37	PA3 *	I/O	ADC1_IN8	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC1_OUT1	
41	PA5	I/O	DAC1_OUT2	
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VSS	Power		
72	VDD	Power		
75	PB14 **	I/O	GPIO_Output	LD3 [Red]
77	PD8	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
83	VSS	Power		
84	VDD	Power		
90	PG5 **	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
91	PG6 **	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
92	PG7	I/O	LPUART1_TX	STLINK_TX

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
93	PG8	I/O	LPUART1_RX	STLINK_RX
94	VSS	Power		
95	VDDIO2	Power		
100	PA8 *	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9 *	I/O	USB_OTG_FS_VBUS	USB_VBUS
102	PA10 *	I/O	USB_OTG_FS_ID	USB_ID
103	PA11 *	I/O	USB_OTG_FS_DM	USB_DM
104	PA12 *	I/O	USB_OTG_FS_DP	USB_DP
105	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	TMS
106	VDDUSB	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	TCK
114	PD0	I/O	CAN1_RX	
115	PD1	I/O	CAN1_TX	
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDDIO2	Power		
133	PB3 (JTDO/TRACESWO)	I/O	SYS_JTDO-SWO	SWO
137	PB7 **	I/O	GPIO_Output	LD2 [Blue]
143	VSS	Power		
144	VDD	Power		

<sup>\*\*</sup> The pin is affected with an I/O function

<sup>\*</sup> The pin is affected with a peripheral function but no peripheral mode is activated

## 4. Clock Tree Configuration



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# 5. Software Project

## 5.1. Project Settings

Name	Value
Project Name	rtb-software
Project Folder	/home/kongr45gpen/repos/rtb-software
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_L4 V1.16.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

## 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

## 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_DAC1_Init	DAC1
5	MX_LPUART1_UART_Init	LPUART1
6	MX_USART3_UART_Init	USART3
7	MX_TIM17_Init	TIM17
8	MX_ADC1_Init	ADC1
9	MX_TIM16_Init	TIM16
10	MX_CAN1_Init	CAN1

rtb-software Project
Configuration Report

# 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4R5/S5
MCU	STM32L4R5ZITx
Datasheet	DS12023_Rev0

### 6.2. Parameter Selection

Temperature	25
Vdd	3.0

## 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

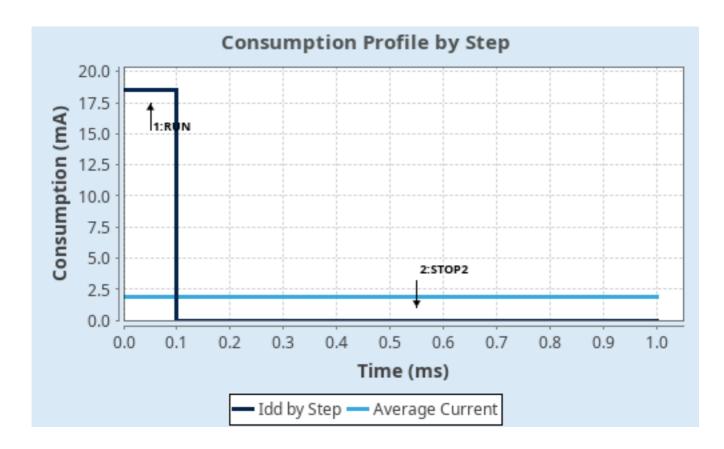
## 6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH-SingleBank	n/a
CPU Frequency	120 MHz	0 Hz
Clock Configuration	HSE BYP PLL ART	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	18.5 mA	2.55 µA
Duration	0.1 ms	0.9 ms
DMIPS	150.0	0.0
Ta Max	103.22	105
Category	In DS Table	In DS Table

### 6.5. Results

Sequence Time	1 ms	Average Current	1.85 mA
Battery Life	2 months, 15	Average DMIPS	150.0 DMIPS
	days, 11 hours	_	

## 6.6. Chart



## 7. Peripherals and Middlewares Configuration

#### 7.1. ADC1

### IN1: IN1 Single-ended

#### 7.1.1. Parameter Settings:

ADC\_Settings:

Clock Prescaler Asynchronous clock mode divided by 16 \*

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled
DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled

ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable
Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

Channel 1

Sampling Time 640.5 Cycles \*

Offset Number No offset

ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

**Analog Watchdog 1:** 

Enable Analog WatchDog1 Mode false

**Analog Watchdog 2:** 

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:** 

Enable Analog WatchDog3 Mode false

7.2. CAN1

mode: Activated

#### 7.2.1. Parameter Settings:

#### **Bit Timings Parameters:**

Prescaler (for Time Quantum) 64 \*

Time Quantum 

187500 \*

Time Quanta in Bit Segment 1 2 Times \* Time Quanta in Bit Segment 2 2 Times \* Time for one Bit 5333.33 \* **Baud Rate** 

ReSynchronization Jump Width 1 Time

**Basic Parameters:** 

Disable Time Triggered Communication Mode Disable Automatic Bus-Off Management Disable Automatic Wake-Up Mode Automatic Retransmission Enable \* Disable Receive Fifo Locked Mode Transmit Fifo Priority Disable

**Advanced Parameters:** 

Operating Mode Loopback \*

#### 7.3. DAC1

**OUT1 mode: Connected to external pin only** OUT2 mode: Connected to external pin only

#### 7.3.1. Parameter Settings:

#### **DAC Out1 Settings:**

Output Buffer Enable None Trigger

DAC High Frequency Mode Disable **User Trimming** Factory trimming Sample And Hold Sampleandhold Disable

**DAC Out2 Settings:** 

**Output Buffer** Enable None Trigger

**DAC High Frequency** Mode Disable **User Trimming** Factory trimming Sample And Hold Sampleandhold Disable

#### **7.4. LPUART1**

### Mode: Asynchronous

#### 7.4.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 1000000 \*

Word Length 8 Bits (including Parity) \*

Parity None Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Single Sample Disable
Prescaler 1

Fifo Mode Enable \*

Txfifo Threshold half full configuration \*
Rxfifo Threshold half full configuration \*

#### **Advanced Features:**

Auto Baudrate Mode Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Disable **Data Inversion** TX and RX pins Swapping Disable Enable Overrun Enable DMA on RX Error MSB First Disable

#### 7.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

#### 7.5.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Disabled
Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 64
MSI Calibration Value 0

MSI Auto Calibration Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

**Power Parameters:** 

Power Regulator Voltage Scale 1 boost

#### 7.6. SYS

**Debug: Trace Asynchronous Sw** 

Timebase Source: SysTick

#### 7.7. TIM16

mode: Activated

#### 7.7.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

Repetition Counter (RCR - 8 bits value)

auto-reload preload

1200 \*

50 \*

100 \*

#### 7.8. TIM17

mode: Activated

### 7.8.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

Repetition Counter (RCR - 8 bits value)

1200 \*

No Division

100 \*

auto-reload preload Disable

#### 7.9. **USART3**

### **Mode: Asynchronous**

#### 7.9.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

#### **Advanced Parameters:**

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration Rxfifo Threshold 1 eighth full configuration

#### **Advanced Features:**

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Disable **Data Inversion** Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

#### \* User modified value

# 8. System Configuration

## 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN1	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	Pull-up *	Very High	
	PD1	CAN1_TX	Alternate Function Push Pull	Pull-up *	Very High	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
LPUART1	PG7	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	STLINK_TX
	PG8	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	STLINK_RX
RCC	PC14- OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T (PC15)	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0- OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13 (JTMS/SWDI O)	SYS_JTMS- SWDIO	n/a	n/a	n/a	TMS
	PA14 (JTCK/SWC LK)	SYS_JTCK- SWCLK	n/a	n/a	n/a	TCK
	PB3 (JTDO/TRA CESWO)	SYS_JTDO- SWO	n/a	n/a	n/a	SWO
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	STLK_RX [STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	STLK_TX [STM32F103CBT6_PA2]
Single	PA3	ADC1_IN8	Analog mode for ADC	No pull-up and no pull-down	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
Mapped			conversion			
Signals	PA8	USB_OTG_FS_ SOF	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USB_SOF [TP1]
	PA9	USB_OTG_FS_ VBUS	Input mode	No pull-up and no pull-down	n/a	USB_VBUS
	PA10	USB_OTG_FS_I D	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USB_ID
	PA11	USB_OTG_FS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USB_DM
	PA12	USB_OTG_FS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USB_DP
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	B1
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PG5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PG6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]

### 8.2. DMA configuration

DMA request	Stream	Direction	Priority
LPUART1_TX	DMA1_Channel1	Memory To Peripheral	Low
LPUART1_RX	DMA1_Channel2	Peripheral To Memory	Medium *

### LPUART1\_TX: DMA1\_Channel1 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable \*

Peripheral Data Width: Byte
Memory Data Width: Byte

#### LPUART1\_RX: DMA1\_Channel2 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable \*

Peripheral Data Width: Byte Memory Data Width: Byte

## 8.3. NVIC configuration

## 8.3.1. NVIC

Interrupt Toble	Enable	Droopmetica Driority	CubDriority
Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	6	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
ADC1 global interrupt	true	8	0
CAN1 TX interrupt	true	0	0
CAN1 RX0 interrupt	true	0	0
CAN1 RX1 interrupt	true	0	0
CAN1 SCE interrupt	true	0	0
TIM1 update interrupt and TIM16 global interrupt	true	8	0
TIM1 trigger and commutation interrupts and TIM17 global interrupt	true	10	0
EXTI line[15:10] interrupts	true	1	0
LPUART1 global interrupt	true	1	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38		unused	
Flash global interrupt	unused		
RCC global interrupt	unused		
USART3 global interrupt	unused		
TIM6 global interrupt, DAC channel1 and channel2 underrun error interrupts	unused		
FPU global interrupt		unused	

## 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false

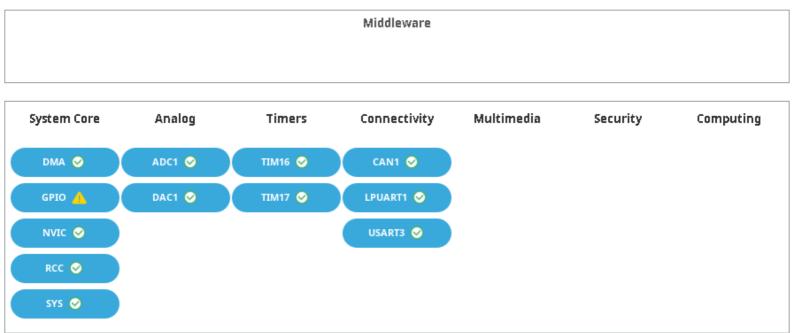
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel2 global interrupt	false	true	true
ADC1 global interrupt	false	true	true
CAN1 TX interrupt	false	true	true
CAN1 RX0 interrupt	false	true	true
CAN1 RX1 interrupt	false	true	true
CAN1 SCE interrupt	false	true	true
TIM1 update interrupt and TIM16 global interrupt	false	true	true
TIM1 trigger and commutation interrupts and TIM17 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
LPUART1 global interrupt	false	true	true

<sup>\*</sup> User modified value

# 9. System Views

9.1. Category view

9.1.1. Current



## 10. Docs & Resources

Type Link

Datasheet http://www.st.com/resource/en/datasheet/DM00366448.pdf

Reference http://www.st.com/resource/en/reference\_manual/DM00310109.pdf

manual

Programming http://www.st.com/resource/en/programming\_manual/DM00046982.pdf

manual

Errata sheet http://www.st.com/resource/en/errata\_sheet/DM00371862.pdf

Application note http://www.st.com/resource/en/application\_note/CD00160362.pdf

Application note http://www.st.com/resource/en/application\_note/CD00167594.pdf

Application note http://www.st.com/resource/en/application\_note/CD00211314.pdf

Application note http://www.st.com/resource/en/application\_note/CD00259245.pdf

Application note http://www.st.com/resource/en/application\_note/CD00264321.pdf

Application note http://www.st.com/resource/en/application\_note/CD00264342.pdf

Application note http://www.st.com/resource/en/application\_note/CD00264379.pdf

Application note http://www.st.com/resource/en/application\_note/DM00042534.pdf

Application note http://www.st.com/resource/en/application\_note/DM00072315.pdf

Application note http://www.st.com/resource/en/application\_note/DM00073742.pdf

Application note http://www.st.com/resource/en/application\_note/DM00073853.pdf

Application note http://www.st.com/resource/en/application\_note/DM00080497.pdf

Application note http://www.st.com/resource/en/application\_note/DM00081379.pdf

Application note http://www.st.com/resource/en/application\_note/DM00085385.pdf

Application note http://www.st.com/resource/en/application\_note/DM00087593.pdf

Application note http://www.st.com/resource/en/application\_note/DM00129215.pdf

Application note http://www.st.com/resource/en/application\_note/DM00151811.pdf

Application note http://www.st.com/resource/en/application\_note/DM00160482.pdf

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Application note http://www.st.com/resource/en/application\_note/DM00150423.pdf

Application note http://www.st.com/resource/en/application\_note/DM00209748.pdf

Application note http://www.st.com/resource/en/application\_note/DM00125306.pdf http://www.st.com/resource/en/application\_note/DM00141025.pdf Application note Application note http://www.st.com/resource/en/application\_note/DM00144612.pdf Application note http://www.st.com/resource/en/application\_note/DM00148033.pdf Application note http://www.st.com/resource/en/application\_note/DM00209768.pdf http://www.st.com/resource/en/application\_note/DM00216518.pdf Application note http://www.st.com/resource/en/application\_note/DM00220769.pdf Application note Application note http://www.st.com/resource/en/application\_note/DM00227538.pdf Application note http://www.st.com/resource/en/application note/DM00257177.pdf Application note http://www.st.com/resource/en/application note/DM00269143.pdf Application note http://www.st.com/resource/en/application\_note/DM00272912.pdf Application note http://www.st.com/resource/en/application\_note/DM00226326.pdf Application note http://www.st.com/resource/en/application\_note/DM00236305.pdf Application note http://www.st.com/resource/en/application\_note/DM00260952.pdf Application note http://www.st.com/resource/en/application\_note/DM00263732.pdf Application note http://www.st.com/resource/en/application\_note/DM00269146.pdf http://www.st.com/resource/en/application\_note/DM00296349.pdf Application note Application note http://www.st.com/resource/en/application\_note/DM00327191.pdf Application note http://www.st.com/resource/en/application\_note/DM00338361.pdf http://www.st.com/resource/en/application\_note/DM00287603.pdf Application note Application note http://www.st.com/resource/en/application\_note/DM00350156.pdf http://www.st.com/resource/en/application\_note/DM00355687.pdf Application note Application note http://www.st.com/resource/en/application\_note/DM00311483.pdf Application note http://www.st.com/resource/en/application\_note/DM00354244.pdf Application note http://www.st.com/resource/en/application\_note/DM00367673.pdf Application note http://www.st.com/resource/en/application\_note/DM00315319.pdf Application note http://www.st.com/resource/en/application\_note/DM00407776.pdf http://www.st.com/resource/en/application\_note/DM00407777.pdf Application note http://www.st.com/resource/en/application\_note/DM00371863.pdf Application note http://www.st.com/resource/en/application\_note/DM00380469.pdf Application note Application note http://www.st.com/resource/en/application\_note/DM00354333.pdf

Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00445657.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209772.pdf
Application note	http://www.st.com/resource/en/application_note/DM00476869.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660597.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf