Department of Electrical Engineering

Power Electronics Group

MACHINE DRIVES AND POWER ELECTRONICS DIVISON

Indian Institute of Technology Kharagpur

Development of a Soft-Switching Inverter Topology for Electric Vehicles

Submitted in fulfilment

Of the Requirements for the Project

In the department of Electrical Engineering under the

Power Electronics Group, IIT Kharagpur

By

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Under the supervision of

Dr. Gautam Poddar

Department of Electrical Engineering

Indian Institute of Technology

Kharagpur July 2022

DECLARATION

I certify that

(a) The work contained in this report has been done by me under the guidance of my supervisor.

(b) The work has not been submitted to any other Institute for any degree or diploma.

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Date: 15th July, 2022 Nilabha Das

Place: Kharagpur PAEE61R18

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

KHARAGPUR - 721302, INDIA

CERTIFICATE

This is to certify that the project report entitled "**Development of a Soft-Switching Inverter Topology for Electric Vehicles**" submitted by **Nilabha Das** to Indian Institute of Technology, Kharagpur is a record of bona fide work carried out by him under my supervision and guidance.

Date: 15th July, 2022
Place: Kharagpur

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Abstract

In this Project Quasi Resonance DC Link Inverter, Modified Quasi Resonance DC Link Inverter, Quasi Z source Inverter and Quasi Z source Inverter with Soft Switching was designed and implemented. Quasi Resonance DC Link Inverter consists of Quasi Resonance circuit in order to provide reduced voltage gradient (dv/dt) across inverter to decrease High Frequency Parasitic effects like EMI Noise and to provide Zero voltage switching (ZVS) to all switches of inverter, such that switching losses can be reduced and inverter switching frequency can be increased to reduced harmonics in the AC output of inverter and size of passive components is reduced. Quasi Z source inverter provides voltage boosting to input of inverter without adding additional switch at input of the inverter, when input battery voltage is low and high speed operation is required for Electric vehicle operation. Quasi Z source with soft switching provides both qualities of these two circuits in one circuit, voltage boosting as well as reduced voltage gradient across inverter by soft switching for all the switches of Inverter.

Modified Space Vector Pulse Width Modulation technique was used in order to improve DC Bus utilization. All the topologies were simulated and analyzed in MATLAB.

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I am grateful to my parents, who lent their unconditional love and emotional support to me and implanted in me the confidence to fight against all odds and helped to overcome the problems.

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List of symbols

V_{DC}	DC Link Voltage
S_{DC}	DC Link Series Switch
S_{r1}	Resonance circuit switch
D_r	Resonance circuit Diode
I_O	Inverter input current before switching
I_{OX}	Inverter input current after switching
C_r	Resonance Capacitor
C	Total Capacitance across inverter legs
C_O	Equivalent output capacitances of IGBTs
L_r &L_C	Resonance circuit Inductance
I_{tp1}&I_{tp2}	Resonance circuit trip currents
PWM	Pulse width modulation
SVPWM	Space vector Pulse width modulation
QRDCLI	Quasi Resonance DC link Inverter
ZVS	Zero Voltage Switching
ZCS	Zero current switching
V_{Cr_peak}	Maximum Voltage across resonance capacitor
V_C	Maximum Voltage across inverter legs
QZSI	Quasi Z Source Inverter
L_1&L_2	Quasi Z source Inverter Inductors
C_1&C_2	Quasi Z Source Inverter Capacitors
D	Shoot Through Duty Ratio
V_{in}	Input DC Battery Voltage

M	Modulation Index
ST	Shoot Through
NST	Non Shoot Through
PID	Proportional Plus Integral Plus Derivative
K_P	Proportional Controller Cofficient
K_I	Integral Controller Cofficient
S_1&S_2	QZS with soft switching auxiliary circuit switches

Chapter 1

Introduction

1.1 Introduction

The global push for greenhouse gas emission reduction and higher fuel costs have made the development of electric vehicles (EVs) more urgent than ever. In an EV, traction drive system is one of the key subsystem. High switching frequency in pulse width modulation (PWM) converters reduces the weight and size of passive components and thus reduces the cost as well as weight of power converters. In hard switching inverters switching frequency is limited by losses in the semiconductor devices during switching. Switching with large dv/dt reduces the switching losses. On the other side bigger voltage gradients (dv/dt) combined with long feeders lead to high-frequency (HF) parasitic effects, like EMI interference to components, overvoltage at motor terminals, capacitive currents in the insulation, etc.[3].Also a major problem with EV Drives are reduction of Input Battery voltage level, as the time passes, after certain run and usage ,EV battery voltage level gets reduced. For High speed Operation, more voltage is needed at input of motor. If Battery voltage is low or goes below a certain level then it is not able to supply sufficient amount of power to motor and motor has to run at lower speed, thus a reliable boosting topology is required.

The common solution for mitigating HF parasitic effects is the use of EMI filters. But In order to improve the power density, EMI filter size is of concern. Reduction of voltage gradient can also be provided with the help of quasi resonant converters. Resonant converters consist of combination of active and passive switches and passive components (inductors and capacitors).The main operating principle of these converters is to bring a low voltage across and/or low current through semiconductor devices during a switching status change through resonance.

Thus voltage gradient is reduced across inverter results in reduction of EMI interference as well as switching losses are also reduced due to ZVS turn on and turn off. Main problem with DC-link resonant inverters is over voltage stress across semiconductor devices, for that Modified quasi resonance DC Link inverter is developed, that limits voltage across switching devices to not go more than Input DC voltage. Thus all these arrangements provide suitable EV operation.

The Quasi Z source Inverter (QZSI) with its wide range voltage boosting ability is suitable for the application, where a three phase AC motor is supplied by a lower battery voltage .It does not use any additional switch at the input of inverter. Voltage boosting can also be provided by boost converter at the input of inverter but it uses additional switch, thus overall cost of system increases. QZSI provides unique features that can not be obtained by traditional Voltage source(VSI) and Current source inverter(CSI).The VSI is a buck(step down) inverter ,it means ac output voltage is limited below and can not exceed dc input voltage. The upper and lower devices of VSI cannot be turned on simultaneously either by purpose or by EMI noise ,otherwise a shoot through would occur and destroy the devices. Thus Dead time is provided between two switches of same phase leg,that creates distortion in waveform. The CSI is a boost(step up) inverter ,it means ac output voltage has to be greater than dc input voltage. In CSI at least one of upper leg switches and one lower leg switches has to be turned on, otherwise an open circuit across large input source inductor will destroy switches of CSI,this also creates distortion in the waveform.The QZSI overcomes above problems of VSI and CSI .It can work as both buck and boost inverter. When battery input voltage level is more than a certain level,it works as buck inverter and if Input battery voltage level is lesser, it provides boost operation by shoot through of all the switches of inverter. Thus it reduces total cost and further improves efficiency of traction drive system and provides a reliable operation.

At the last QZSI with soft switching is proposed. QZSI provides voltage boosting by shoot through operation, which is hard switching, so this topology is proposed to provide soft switching to reduce voltage gradient as well as voltage boosting for higher speed operation.

1.2 Motivation

Resonant converters are already successfully implemented in DC-DC converters, Improving efficiency, reducing losses. Similarly resonance in inverters is used to achieve control of rate of rise of voltage across load[1] and soft switching of all inverter switches. The Quasi Z source Inverter provides both buck boost ability of inverter by shoot through

of switches of inverter and resonance operation without using additional switch. Proposed

Quasi Z source Inverter with soft switching provides both qualities of QRDCLI and QZSI. In this project in part A an inverter topology having quasi resonant circuit in DC-Link and in part B an inverter topology having quasi Z source circuit in DC Link and in part C proposed inverter topology quasi Z source with soft switching is implemented.

1.3 Objectives

Development of Inverter topologies suitable for an EV application, such that it will have following objectives.

- To reduce High voltage gradient(dv/dt)across inverter, such that High Frequency parasitic effects like EMI interference to components, overvoltage at terminal of motor, capacitive current of insulation etc. are reduced as well as switching losses of inverter switches is reduced due to ZVS turn on and turn off.
- To limit voltage stress across all the switches of inverter as well as across switches of auxiliary circuit.
- To improve Input DC Bus utilization by using Modified Space vector Pulse width modulation.
- To provide Voltage boosting at the input of inverter, when Input battery voltage is less or when higher speed operation is required for an EV by Quasi Z source Inverter (QZSI) without adding additional switch at the input of inverter.
- To provide both soft switching, reduced high voltage gradient and voltage boosting for inverter operation by proposed QZSI with soft switching.
- To provide reliable operation for electric vehicle motor operation by isolating DC input from inverter switches during shoot through or by connecting a medium between them during shoot through.

1.4 Organization

Chapter 1 deals with introduction to thesis, and literature survey on existing topologies. Chapter 2 with explanation of operation of selected Quasi resonant DC-link inverter (QRDCLI) topology, modified QRDCLI topology with voltage clamping circuit. Chapter3 with design of QRDCLI. Chapter 4 deals simulation results of QRDCLI. Chapter 5 with Space vector pulse width modulation (SVPWM) and its implementation. Chapter 6 with explanation of operation of selected Quasi Z source inverter (QZSI) topology, design of QZSI and simulation results of QZSI. Chapter 7 with Feedforward-feedback control for DC side of QZSI. Chapter 8 with Proposed QZSI with soft switching and then Conclusions and future scope followed by references.

Chapter 2

Quasi Resonance DC-Link Inverter

2.1 Introduction

Selected topology [1] of quasi resonant DC-link inverter was shown in Fig 1. This topology consists of a quasi-resonant circuit with three additional active switches and inductor and capacitor.

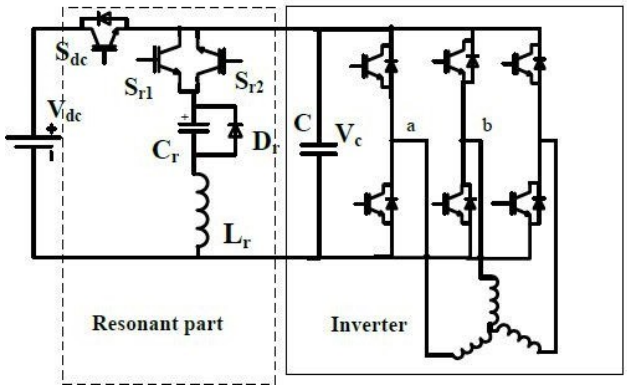


Fig. 1 Basic QRDCL inverter Circuit

Circuit shown in Fig 1 consists of eight modes of operation. Each mode was explained below with equivalent circuit in each mode. Simplified equivalent topology of Fig 1 is shown in Fig 2(When inverter is feeding a motor during one switching interval load can be assumed as constant current source). S_{INV} represents the inverter legs. On is equivalent to all switches of inverter legs are on. Off represents normal operation of inverter.

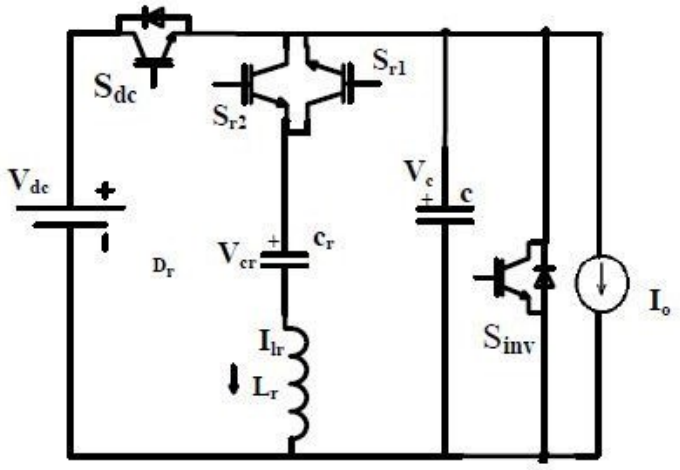


Fig.2 Equivalent circuit of basic QRDCL inverter

2.2 Present Circuit and Operation

Mode 0(M0)

In this mode Inverter is in steady state. Switch S_{DC} is on and inverter is connected to the source. In each leg respective switches are turned on according to the voltage vector required. The equivalent circuit is shown in Fig 3.

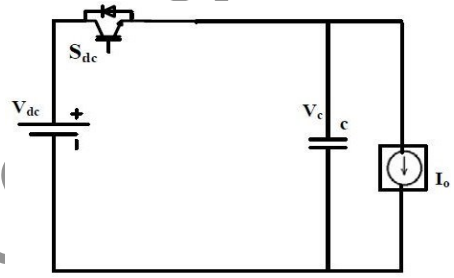


Fig. 3 equivalent circuit of Mode 0

Mode I(Ml)

Whenever any change in applied vector of inverter accordingly inverter leg switches has to change. In order to achieve reduced dv/dt across inverter and Zero voltage switching of inverter switches, voltage across legs has to reduce to zero by resonance [1]. After switching, voltage across inverter legs has to restore to DC-bus voltage by resonance. During charging and discharging of inverter leg capacitors(C), resonant circuit has to support the load current based on direction of load. In this mode energy required to operate resonance is stored in resonant capacitor(C_r) and inductor (L_r).The equivalent circuit is shown in Fig 4.

At $t=t_o$, switch S_{r1} will be turned on under Zero current switching. Current through inductor and voltage across capacitor C_r start increasing. Energy required for resonance

and load was stored in L_r (voltage rise across C_r is less). When current reaches to trip current I_{tp1}, mode I will be end. Voltage and current wave forms are shown in Fig 12.

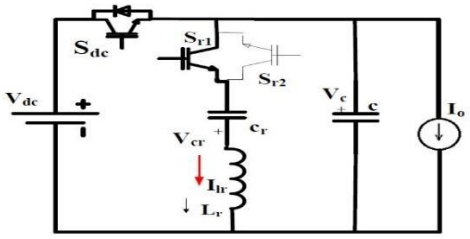


Fig. 4 equivalent circuit of Mode 1

Mode II(M2)

At $t=t_1$ mode II will start.At $t=t_1$ switch S_{DC} is turned off. Since current through L_r has to follow same direction as at $t=t_1$,inductor current starts discharging capacitor C,voltage across inverter legs becomes zero by resonance with decreased dv/dt slope at the end of mode II. This mode is analysed for dv/dt measurement.

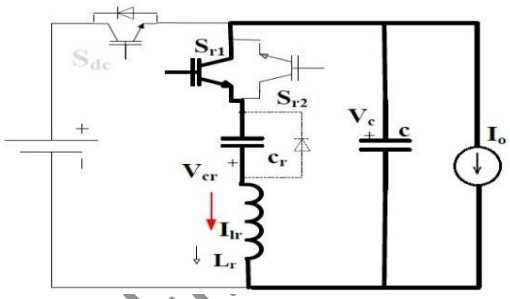


Fig. 5 equivalent circuit of Mode II

Mode III(M3)

After discharging capacitor C at $t=t_2$, (i.e. voltage across inverter legs reached to zero) inductor (L_r) current continue to flow through anti parallel diodes across inverter leg IGBTs. All inverter switches can be turned on under ZVS at this instance (i.e. S_{INV} can be turned on under Zero voltage condition). When inductor current reaches to zero ,voltage across capacitor C reaches to peak voltage ($V_{cr\ peak}$), storing the total energy. The equivalent circuit of inverter in this mode is shown in Fig 6.

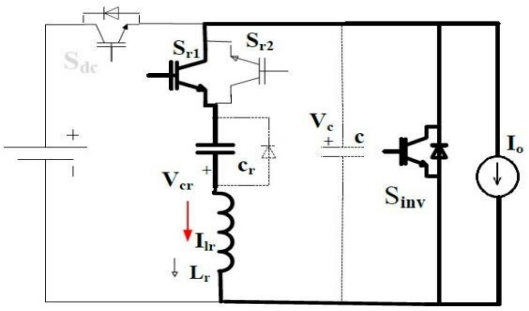


Fig. 6 equivalent circuit of Mode III

Mode IV(M4)

This mode starts at $t=t_3$.In this mode, voltage across resonant capacitor remains at $V_{cr}(t3)$.switch S_{r1},S_{r2},S_{DC} will remain off. Current i_L remains at zero until S_{r2} turned on. S_{INV} Continuous to be on (i.e. all inverter switches are turned on).This is equivalent to null vector. This duration can be controllable. The equivalent circuit in this mode is shownin Fig 7.

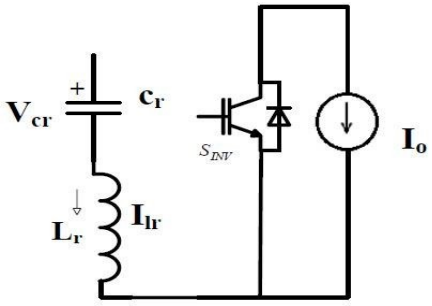


Fig. 7 equivalent circuit of Mode IV

Mode V(M5)

This mode starts at $t=t_4$. To apply new switching sequence, and to recharge the voltage across V_{c2} to DC-bus voltage by resonance with reduced dv/dt ,S_{r2} will be turned on. Capacitor C_r starts discharging. Current through inductor L_r, start increasing as shown in Fig 12. When current through inductor reaches to trip current I_{tp2},this mode will end. The equivalent circuit in his mode is shown in Fig 8.

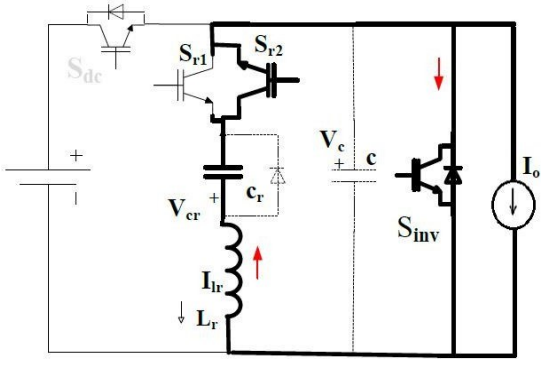


Fig. 8 equivalent circuit of ModeV

Mode VI(M6)

This mode start when inductor current reaches trip current $I_{tp2.}$ according to active vector respective inverter switches will be turned off under ZVS, remaining switches will be kept on (i.e. S_{INV} will be turned off in equivalent circuit). As a result of resonance between C, C_r, , L_r . Capacitor C starts charging with reduced dv/dt, and C_r, continuous to discharge. The equivalent circuit of inverter in this mode is shown in Fig 9.when voltage across C_r, reached to zero diode D_r become forward biased and starts conducting thus avoiding C_r to charge in reverse direction.

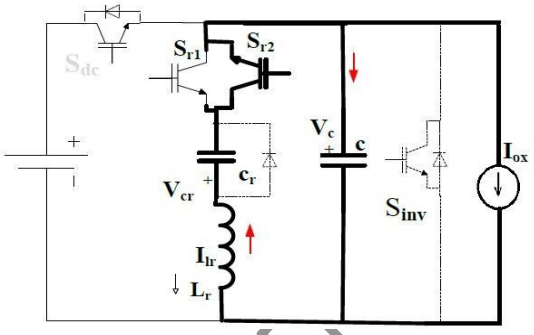


Fig. 9 equivalent circuit of Mode VI

Mode VII(M7)

This mode starts at $t=t_6$ when capacitor C_r completely discharges to zero, and diode D_r start conducting. Capacitor C will continuous to charge towards DC-bus voltage with reduced dv/dt . This mode ends when voltage across capacitor C is equal to DC-bus voltage, the switch $S_{D\ C}$ can be turned on under zero voltage condition. Inductor L_r supplies both current to charge C and load current in this mode. The equivalent circuit of inverter in this mode is shown in Fig 10.

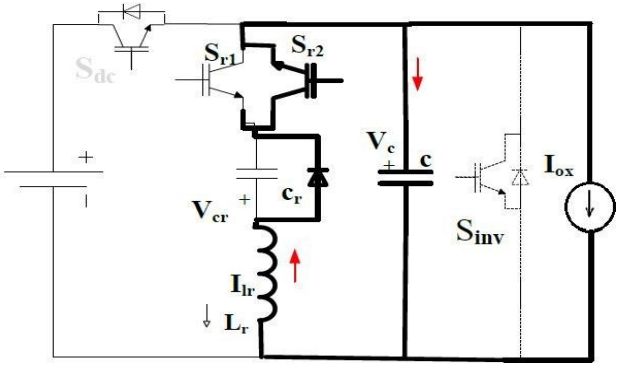


Fig. 10 equivalent circuit of Mode VII

Mode VIII(M8)

This mode starts at $t=t_7$, Since capacitor C charged to full DC bus voltage the current through inductor L_r, starts decreasing towards zero. Some part of inductor current delivered to load remaining sent back to DC-source by turning the anti-parallel diode of switch S_{DC}. This mode ends at $t=t_8$ when inductor L_r current reaches to zero thus entering in to mode 0. The equivalent circuit of inverter in this mode is shown in Fig 11.

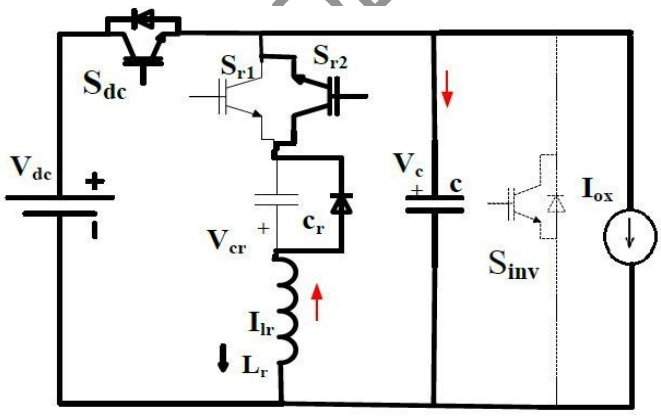


Fig. 11 equivalent circuit of Mode VIII

2.3 Typical Voltage and Current Waveform

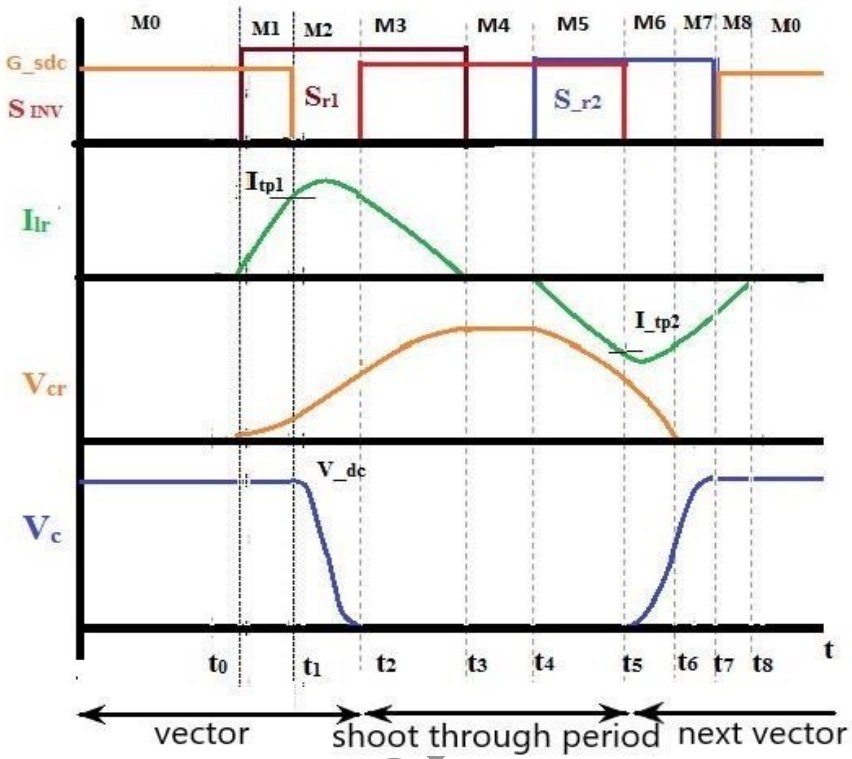


Fig 12 Typical voltage and current waveforms for QRDCL inverter

2.4 Proposed Modification

During turn off of S_{r1} and S_{r2}, switches has to recover through resonant inductor (L_r). As a result L_r and output capacitance of switches undergo resonance (as C_r is large compared with output capacitance of switches voltage variation across C_r significantly less) .This resonance causes voltage across S_{r1} and S_{r2} to rise up to twice the DC-bus voltage (for S_{r1}) or twice the peak voltage across C_r (for S_{r2}) respectively. In order to avoid over voltage stress across switches S_{r1} and S_{r2} topology in Fig 1 modified as shown in Fig 13. Coupled inductor L_c and diode D_c are used to clamp the voltage across S_{r1} to dc-bus voltage, and position of diode D_r is changed to clamp voltage across S_{r2} to peak voltage across C_r . The basic modes of operation of circuit in Fig 13 remain same as topology in Fig 1. Operation of circuit in topology Fig 13 is explained bellow.

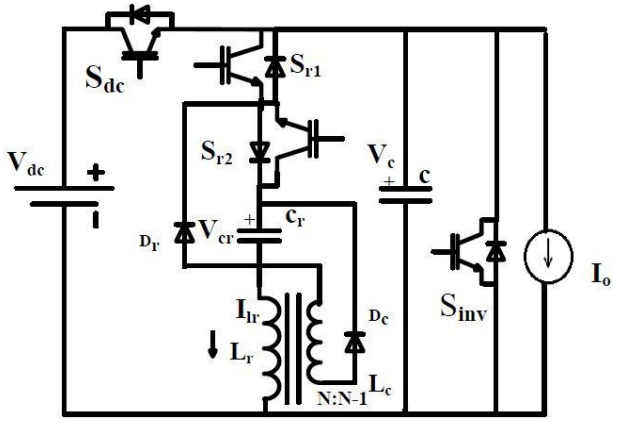


Fig. 13 Modified equivalent circuit of QRDCL Inverter

Mode 0,1,2 are same as in Basic Topology.In mode 3 ,V_{cr} >0,D_c remains off. At end of mode 3,at t =t_3 ,diode across S_{r2} will be off first (gate pulse to S_{r1} is still high).S_{r2} has to recover through resonant inductor L_r , during recovery ,switch of S_{r2} and inductor L_r under goes resonance. Voltage across S_{r2} has to reach peak voltage across V_{cr} . Due to resonance between S_{r2}, L_r ,voltage across S_{r2} reaches to twice the peak voltage across resonant capacitor C_r . This resonance occurs in basic topology. But in Modified Topology, whenever voltage across S_{r2} reach more than peak voltage across capacitor C_r,voltage across inductor L_r become positive. Cathode of diode D_r at zero potential (since Vc=0) positive voltage across L_r forward bias diode D_r , keeping voltage across resonant inductor zero when voltage across S_{r2} reached to zero.Thus avoiding over voltage across S_{r2}. Equivalent circuit of modified topology at end of mode III is shown in Fig 14.

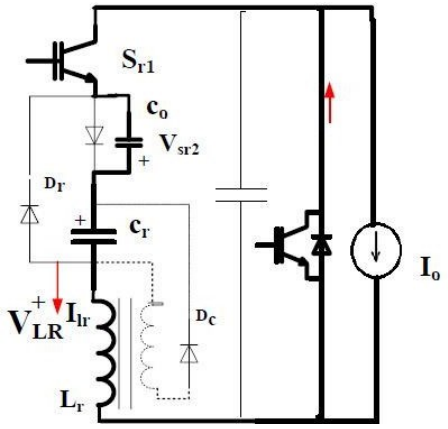


Fig. 14 equivalent circuit of Modified QRDCL inverter at end of Mode III

In mode IV, V,VI,VII diode D_c remains off. At end of mode VIII i.e. at $t=t_8$ current through inductor L_r become zero. When L_r current become zero anti parallel diode across switch S_{r1} has to block the DC-bus voltage since is still on. For the Basic Topology, during recovery of anti-parallel diode across S_{r1}, output capacitance of switch S_{r1} and resonant inductor L_r start resonating. As a result of this resonance ,the voltage across switch rises to twice the DC-link voltage, but for modified topology, when voltage across switch cross beyond DC-bus voltage, voltage across inductor L_r will become negative. Negative voltage across inductor L_r results in forward bias of diode D_c(voltage across V_{cr} is zero at $t=t_8$). Energy stored in inductor L_r due to recovery of switch S_{r1} will be fed to capacitor C_r . Capacitor C_r is large compared to output capacitance of switch, voltage rise across capacitor C_r is 3-4 percent of peak voltage across C_r. Thus clamping switch voltage to DC-bus voltage.

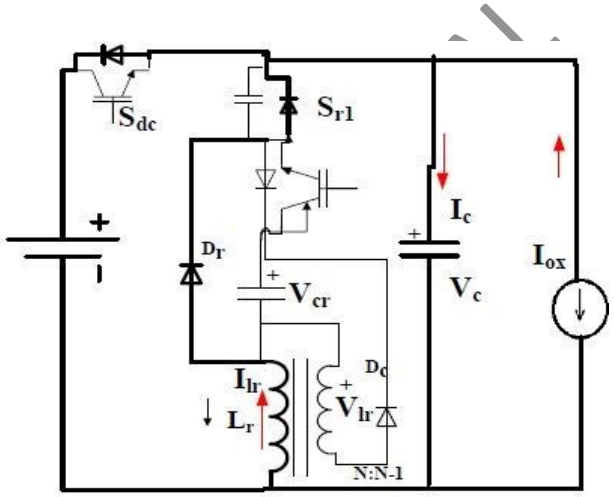


Fig. 15 equivalent circuit of modified QRDCL inverter at the end of mode VIII

Chapter 3

Resonance circuit elements and Trip current calculation

3.1 Design Considerations

The resonant circuit is designed to commutate peak load current of 7A in positive and negative direction. DC Link voltage is 400V. The specifications to design the quasi resonant dc link inverter circuit parameters are as follows:

1. The inverter input voltage must be pulled down to zero by resonance with reduced dv/dt and for zero voltage switching (ZVS) of inverter switches and again boosted to the DC source voltage.
2. The trip currents should be as small as possible in order to reduce the circuit power loss.
3. It is important to minimize the peak values of the resonant voltage and the resonant current in order to reduce the stress on circuit devices.
4. The resonant transition interval must be designed to be much shorter than inverter's switching cycle time.
5. At the end of mode 7 current through Inductor L_r must be greater than or equal to inverter input current, otherwise DC link capacitor discharges to meet load demand until S_{DC} is turned on again.
6. I_{tp1} decides the total energy required to discharge capacitor C voltage to zero in mode II and restore the voltage V_c to DC-bus voltage.

7. Trip current I_{tp2} ensures that Voltage across C_r drops to zero before recharging of C to DC bus voltage.

Specification1 is important for soft switching. It is not possible to satisfy all other design objectives simultaneously. The simulations are done for different values of the resonant elements. The proper values of resonant components can be obtained from the simulations.

3.2 Calculation of Trip currents

Calculative method to derive expression for I_{tp1} and I_{tp2} is presented in [1]. The resonant cycle is heavily influenced by the initial load current I_o and by I_{ox} at the next switching state. In mode M1, The energy required to operate complete resonance is stored in inductor L_r. In mode 2, Inductor has to discharge capacitor C to zero voltage, and has to support the load based on direction of current and in mode 3, the remaining energy in inductor is supplied to C_r, The energy required for operation of resonant circuit in Mode M6,M7 ,M8 has to stored in C_r .The Deriving Equation for I_{tp1} is as follows

$$I_i = \sqrt{\left(\frac{V_{dc}}{Z_5} + I_o + I_{ox}\right)^2 - \left(\frac{V_{dc}}{Z_5}\right)^2} - I_o \quad (1)$$

$$I_{tp1} = \sqrt{\left(\frac{V_{dc}}{Z_o}\right)^2 - \left(\frac{V_{dc}}{Z_o} - \frac{I_i^2 Z_o}{2V_{dc}}\right)^2} \quad (2)$$

The value of I_{tp2} must satisfy two needs [1]. First the current i_{L1} must be large enough to ensure that the oscillation is completed and V_c reaches the supply value V_{dc}. Second, the capacitor voltage V_{cr} must be zero at the end of a resonant cycle. For ease of calculation and reduction of modes we can assume that V_c reaches to V_{dc} same that when V_{cr} reaches to zero.

$$\frac{1}{2}C_r V_{cr(t5)}^2 + \frac{1}{2}L_r I_{tp2}^2 = \frac{1}{2}L_r I_{peak}^2 \quad (3)$$

$$-i_r = -\sqrt{\left(I_{tp2} + aI_{ox}\right)^2 + \left(\frac{V_{cr(t3)}}{Z_2}\right)^2 - \left(\frac{V_{dc}}{Z_2}\right)^2} - aI_{ox} \quad (4)$$

Trip currents I_{tp1} and I_{tp2} can be solved by solving above equations.

3.3 Resonance Inductor (L_r)

The resonant inductor is connected in series with S_{r1} and S_{r2} . In order to operate these two switches under zero current switching, the current rise in inductor during rise time of device should not be more than 10% of minimum peak current through switch. The minimum peak current is almost near to first trip current (I_{tp1}), I_{tp1} is considered for calculation of inductor L_r, I_{tp1} is found out to be 14A. The rise time of switch S_{r1} is 20ns from data sheets. The voltage across inductor, when S_{r1} on will be V_{dc} for short period. Then voltage equation across inductor will be

$$V_{dc} = -\frac{L_r di}{dt} \quad (di = 1.4A\,,\, dt = 20ns\,,\, V_{dc} = 400V) \qquad (5)$$

$$L_r = 7.81uH$$

3.4 Resonance Capacitor(C_r)

In mode 4, the resonant capacitor holds the total energy required for resonant operation. And from mode 6,7 the energy in capacitor must be support the load during M6,M7 ,charge the capacitor C to V_{dc} ,and at end of mode inductor L_r current must be more than or equal to load current .Peak voltage across capacitor must be less than V_{dc} ,by selecting value of peak voltage across capacitor ,and from that Cr is calculated. The calculated value is used to calculate circuit time intervals, and peak current in inductor. Several number of iterations are performed for different values of $V_{crpeak.}$ The values for which the entire switching can be done in less than 2us seconds is chosen .The corresponding value of C_r = 40nF.

3.5 Selection of Capacitor C

In order to select capacitor C, the operation of inverter in mode 6-7 is considered. At starting of mode 6 new switching state is applied i.e. turning off S_{INV}. The inductor L_r ,Cr, C will operate in resonance and charge capacitor C. The voltage rise across S_{INV} during fall time of switch S_{INV} should be less than 10% of full voltage across switch (10% of Vdc). From device data sheet fall time of device is 20ns. Maximum charging current is I_{tp2} to be three times the load current. From capacitor current equation

$$I_c = C\frac{dv}{dt} \qquad (6)$$

Solving above equation C = 4nF.

3.6 Simulation Specifications for QRDCLI

Output Power	2.1KW
Output Line to Line Voltage	245V
Maximum Load current	7A
Input DC voltage	400V
Resonance Capacitor (Cr)	40nF
Resonance Indcutor (Lr)	7.81uH
DC Link Capacitor(C)	4nF

Table 1. Simulation Specification for QRDCLI

Chapter 4

Simulation Results for QRDCL Inverter

Equivalent circuits of basic and modified topology were simulated in PSPICE 17.2 and exact circuit in MATLAB 2017b.Following are the results from PSPICE 17.2.

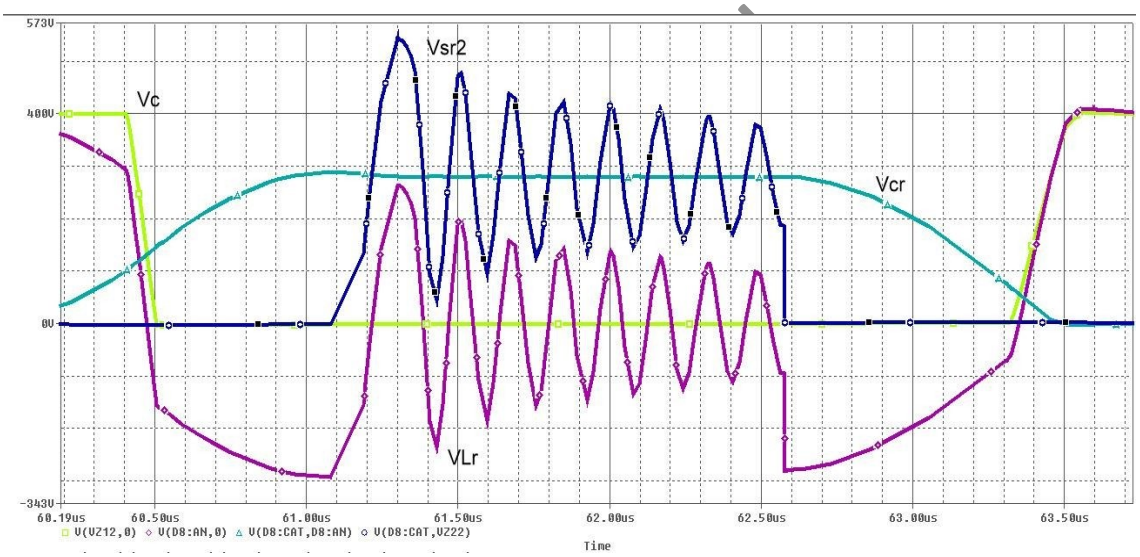


Fig. 16 Voltage across Sr2 ,C,Cr,Lr in basic topology

Fig.16 Shows oscillations of Vsr2 after mode 3 in basic topology,this is because of resonance between output capacitor of Vsr2 and Inductor Lr.Vsr2 goes above Vdc voltage.

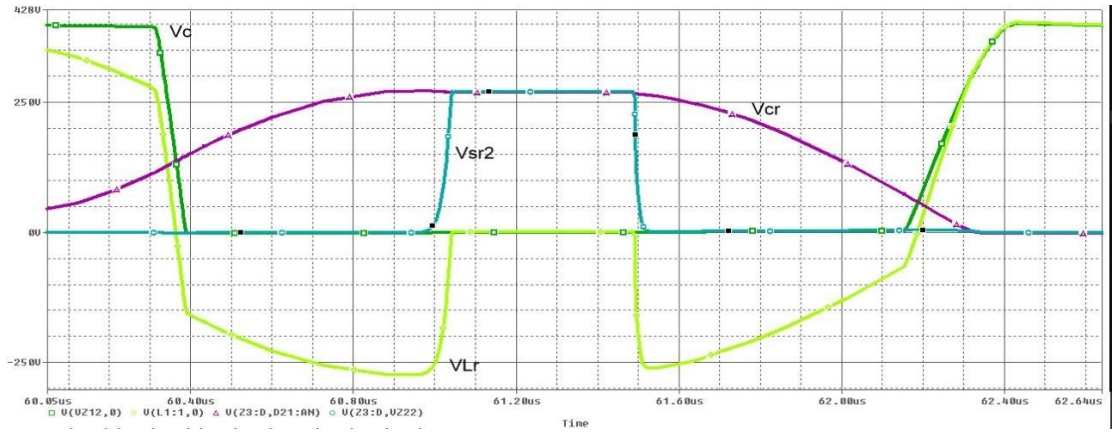


Fig.17 Voltage across Sr2,C,Cr,Lr in modified topology

Fig.17 shows Vsr2 is clamped to Vdc(400V) by clamp circuit in modified topology.

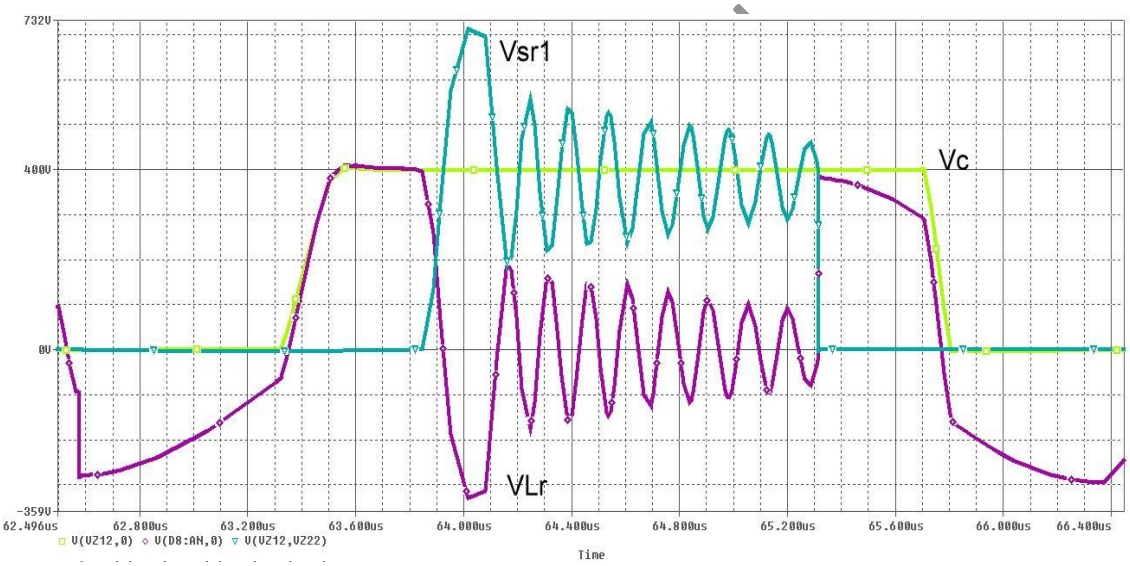


Fig.18 Voltage across Sr1, C ,Lr in basic topology

Fig.18 shows oscillation of Vsr1 at end of mode 8 in basic topology.this is because of resonance between output capacitor of Sr1 and inductor Lr.Vsr1 goes above Vdc voltage.

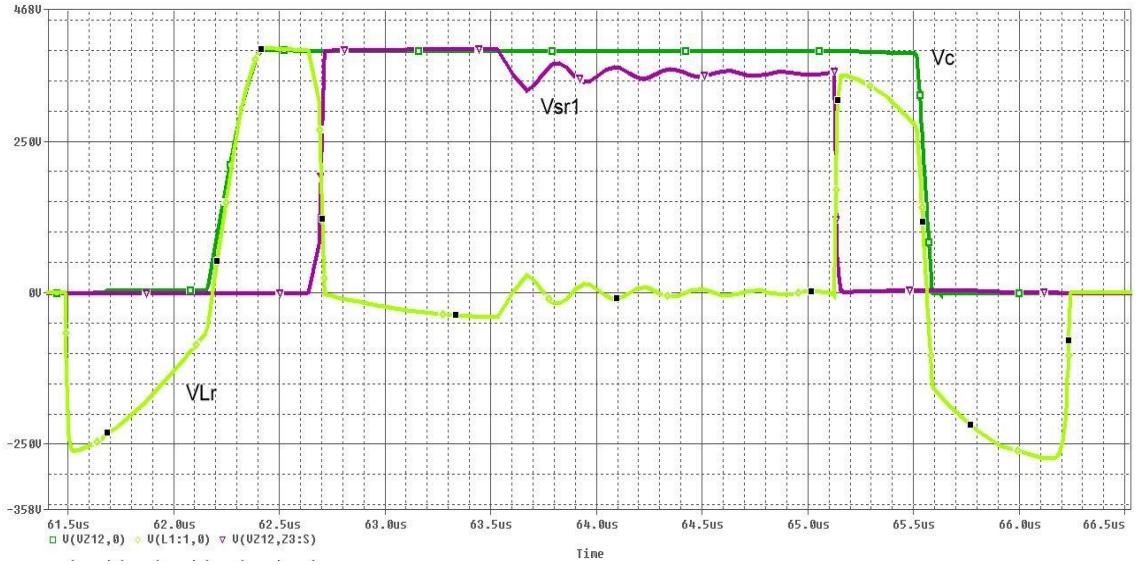


Fig.19 Voltage across Sr1, C ,Lr in modified topology

Fig.19 shows voltage Vsr1 is clamped to Vdc voltage by clamp circuit in modified topology. With L_r=7.81uH, C_r=40nF, C=4nF. voltage gradients are 2857V/us during discharge of Capacitor C and 1600V/us during recharge of Capacitor C. With L_r=30uH, C_r=0.47uF, C=0.14uF, maximum voltage gradients are 600V/us.Simulations were performed for first set of inductors and capacitors.Since voltage change across input is not steep now, THD of load current will also reduce.From Fig.19.1 THD of load current with VSI is 10.16%,but with QRDCLI ,THD is 7.28%.

Sampling time	= 1e-08 s		
Samples per cycle	= 2e+06		
DC component	= 0.06192		
Fundamental	= 6.733 peak (4.761 rms)		
THD	= 7.28%		
0 Hz	(DC):	0.92%	90.0°
50 Hz	(Fnd):	100.00%	-34.8°
100 Hz	(h2):	1.81%	78.7°
150 Hz	(h3):	1.77%	73.4°
200 Hz	(h4):	1.72%	68.2°
250 Hz	(h5):	1.45%	85.7°
300 Hz	(h6):	1.58%	59.2°
350 Hz	(h7):	1.74%	66.4°
400 Hz	(h8):	1.44%	51.4°
450 Hz	(h9):	1.37%	48.1°

Sampling time	= 1e-08 s		
Samples per cycle	= 2e+06		
DC component	= 0.09099		
Fundamental	= 6.887 peak (4.87 rms)		
THD	= 10.16%		
0 Hz	(DC):	1.32%	90.0°
50 Hz	(Fnd):	100.00%	233.5°
100 Hz	(h2):	2.59%	78.7°
150 Hz	(h3):	2.53%	73.3°
200 Hz	(h4):	2.45%	68.2°
250 Hz	(h5):	2.36%	63.4°
300 Hz	(h6):	2.27%	59.0°
350 Hz	(h7):	2.17%	55.0°
400 Hz	(h8):	2.06%	51.3°
450 Hz	(h9):	1.97%	48.0°

Fig.19.1 Load current THD comparison between VSI and QRDCLI

Chapter 5

Space Vector PWM

For all the topologies in this project, for PWM, we are using space vector PWM (SVPWM).In SVPWM reference is a resultant space vector, which rotates in space according to frequency of modulating three phase waves and by position of this space vector in different six sector, we can find out time duration of corresponding active vector and null vector for that sector.

In Quasi Resonance DC Link Inverter, whenever there is change (transition) in switching status from one active vector to next active vector or active vector to null vector, resonance circuit has to be operated for reduced dv/dt across inverter and for ZVS of all the switches of the inverter.

5.1 Triangle comparison based SVPWM

Triangle comparison based SVPWM is different than computational SVPWM. In computational SVPWM , mathematical formulas are used for calculation of time duration of two active vectors(T_A,T_B)and null vectors(T_o,T_7).In MATLAB implementing computation SVPWM become a bit complicated because two sampling time needs to be used ,one of calculating T_{AB07} at starting of switching time period(100us) and other for turning on and off switching devices(1ns).So one modification is made in form of Triangular comparison based SVPWM.

In Triangle comparison based SVPWM, one common voltage V_{CM} is added to all three reference voltages ,such that switching sequence of active vector and null vector in same as that of computational SVPWM and time duration of vector T_{AB07} is also

approximately same.

5.2 Calculation of common Voltage (V_{CM})

Suppose that V_a V_b V_c are the three reference voltages. One common voltage V_{CM} is added such that switching sequence of vectors and time durations of vectors T_{AB07} remains. Suppose V_a^*,V_b^*,V_c^* are the reference voltage after addition of common voltage. Then

$$V_a^* = V_a + V_{CM} \quad (7)$$

$$V_b^* = V_b + V_{CM} \quad (8)$$

$$V_c^* = V_c + V_{CM} \quad (9)$$

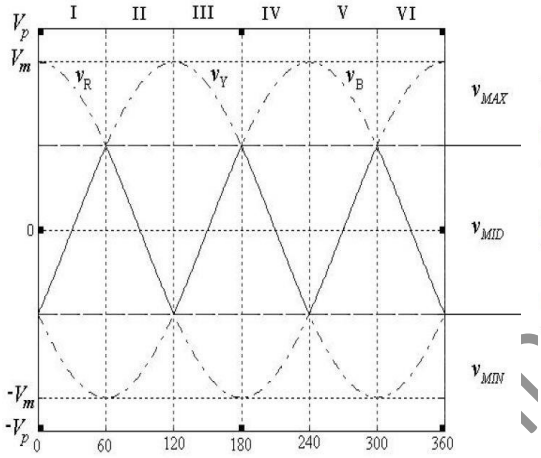


Fig 20. V_{MAX},V_{MIN}, V_{MID} in six sectors

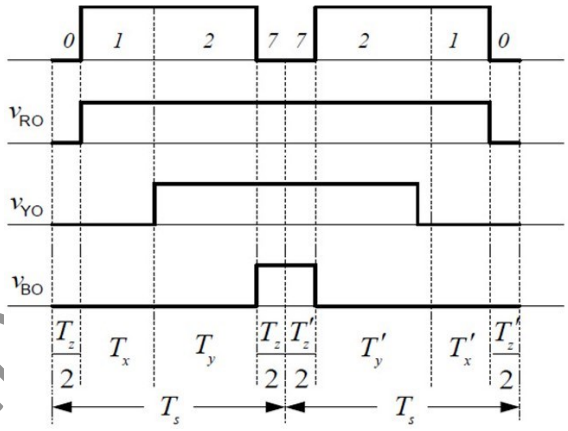


Fig. 21 active, null vector time in SVPWM sector1

Now in any of switching period these V_a^*,V_b^*,V_c^* ,depending on their magnitude and polarity ,will be V_{MAX}^*,V_{MID}^*,V_{MID}^*.Null vector period at starting of SVPWM is same as half of null vector at mid duration. Thus

$$V_p - V_{MAX}^* = V_{MIN}^* - V_n \text{ where } V_p = 1 \; and \; V_n = -1$$

$$V_{MAX}^* + V_{MIN}^* = 0$$

$$V_{CM} = -\frac{V_{MAX} + V_{MIN}}{2} = 0.5V_{MID} \quad (10)$$

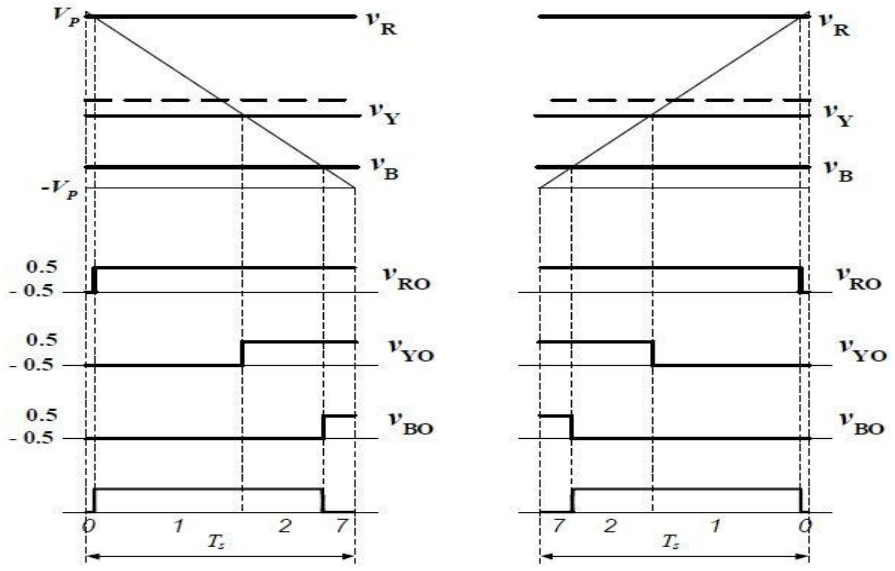


Fig.22 triangular comparison based SVPWM

These V_{CM} is to be added in each reference voltage V_{abc} to get V_{abc}^*. V_{abc}^* is compared with Triangular carrier wave (Frequency 10KHz) to get switching gate pulses for all switches of Inverter. Using SVPWM we can get 15% more modulation index, thus DC bus utilization increases. Fig.22 shows Triangular comparison based SVPWM. Fig.23 shows shoot through duration in one switching period.

Fig.23 shoot through duration (red) in one switching period for QRDCLI

Chapter 6

Quasi Z Source Inverter

6.1 Introduction

If battery voltage decreases after a certain run and higher speed operation is required for an EV, motor won't be getting enough voltage from DC side for its High speed operation. Battery life also decreases due to aging. Thus we need boosting of voltage to supply sufficient ac output voltage without decreasing reliability and efficiency of drive system. Although VSI with boost converter increases overall efficiency of drive system by regulating DC Link voltage, but it brings additional cost due to added additional switch at the input. Therefore one topology Z source inverter (ZSI) was invented [2] and its modification Quasi Z source inverter(QZSI) is used here[4].The QZSI does not use additional switch at the input, thus reduce cost , also it increases efficiency and provides reliable operation for drive system.

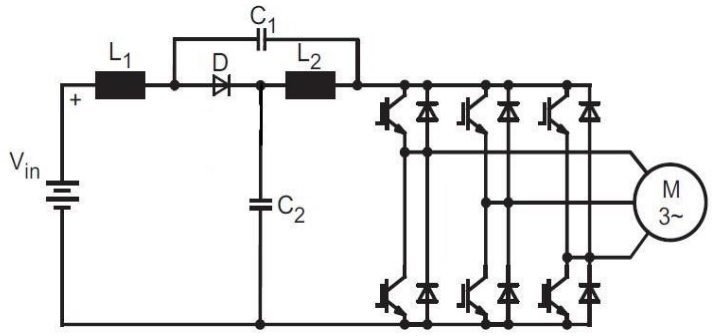


Fig.24 Quasi Z source Inverter

There are basically two switching state possible, while operating QZSI. Shoot Through state and Non Shoot Through state .Non shoot through state consists of Active state and Zero state. Shoot through state is used for boosting of voltage. The operation of both states are discussed below.

6.2 Modes of Operation

6.2.1 Shoot through State

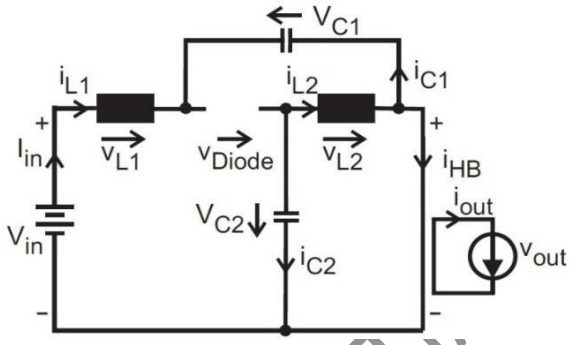


Fig.25 QZSI in shoot through duration

In shoot through state, all the switches of inverter are turned on. capacitor C1,C2 gives energy to Inductor L1,L2 by resonance. The minimum duration of null vector(T_{o_min}) is calculated in any of the switching period by deriving relation between shoot through duty ratio and modulation index for required AC output voltage and Shoot through state is applied for that minimum duration of null vector (000 or 111),thus diode of QZSI gets reversed biased and capacitors C1 and C2 gives their energy to inductor ,thus energy of inductor increases, which it gives to capacitor in next state.

6.2.2 Non Shoot through State

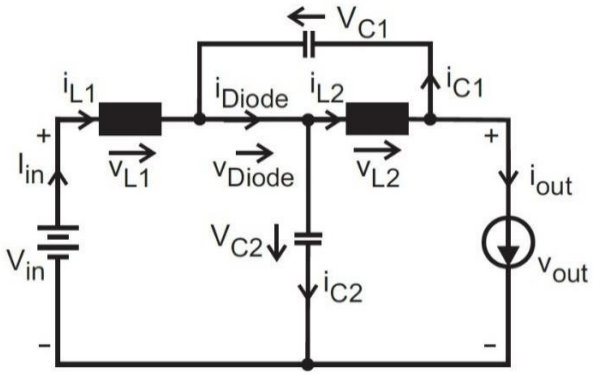


Fig.26 QZSI in Non shoot through duration

In non shoot through state, inductor transfers their energy to capacitor ,thus boosted voltage (Vc1 + Vc2) appears across input of inverter and effective input voltage of inverter increases thus boosting of voltage happens.

6.3 Switching average for inductor current and capacitor voltage

All the switching average value of Current (i_{L1},i_{L2}) and Voltage (V_{C1},V_{C2}) is calculated below using volt second balance across inductor and current second balance through capacitor. t_A is non shoot through duration, t_{ST} is shoot through duration.

$$V_{L1} = \frac{(V_{in}-v_{c2})t_A Ts+(V_{in}+v_{c1})t_{ST}Ts}{Ts} = 0 \quad (11)$$

$$V_{L2} = \frac{(-v_{c1})t_A Ts + (v_{c2})t_{ST}Ts}{Ts} = 0 \quad (12)$$

$$I_{c1} = \frac{(i_{L2}-i_o)t_A Ts+(-i_{L1})t_{ST}Ts}{Ts} = 0 \quad (13)$$

$$I_{c2} = \frac{(i_{L1}-i_o)t_A Ts+(-i_{L2})t_{ST}Ts}{Ts} = 0 \quad (14)$$

Hence

$$V_{c1} = \frac{V_{in}.D}{1-2D} \quad (15)$$

$$V_{c2} = \frac{V_{in}(1-D)}{1-2D} \quad (16)$$

$$I_{L1} = I_{L2} = \frac{i_o(1-D)}{1-2D} \quad (17)$$

Where V_{C1} is average voltage across C1, V_{C2} is average voltage across C2 and I_{L1},I_{L2} average current through L1 and L2, D is shoot through duty ratio.

6.4 QZSI Design for EV operation

For Design of QZSI, we took Load as 10KW ,230 V_{LL} rms .Using SVPWM DC link minimum Voltage($V_{DC\ min}$) = $\frac{230}{0.612\times1.15} = 326.8$ volt. It means that if battery voltage > $V_{DC\ min}$, normal VSI operation will be there and no need of voltage boosting operation .If Battery Voltage < $V_{DC\ min}$,and High speed operation is required, we need to do Boost operation .This Boost duration we are applying in every switching period and it equals to time duration of minimum null vector duration in any switching period, which is shown in Fig.27.

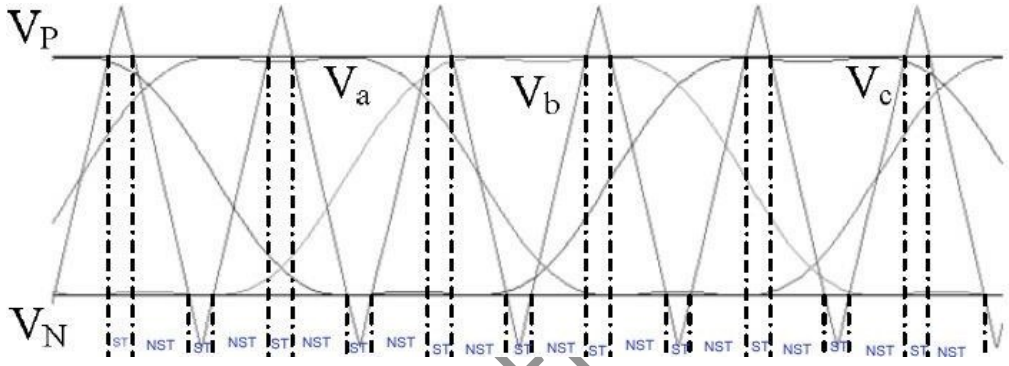


Fig.27 Shoot through duration in switching periods

6.4.1 Duty Ratio and Modulation Index Relation

From Fig.27 relation between Modulation index(M) and Shoot through duty ratio(d) is

$$d = 1 - \frac{\sqrt{3}}{2}M \quad \text{or} \quad M = \frac{1-d}{\sqrt{3}/2} \tag{18}$$

During Non shoot through Period voltage appearing across input of inverter is

$$V_{dc} = V_{C1} + V_{C2} = \frac{Vin}{1-2d} \tag{19}$$

Thus from relation V_{LL}_rms = 0.612× M × Vdc ,we get desired shoot through duty(d) and then Modulation Index(M).Suppose $V_{Battery}$ has came to 230 Volt ,which is very less than 326.8 V .in this case from above formula put V_{in} =230 V .We get d = 0.2282 and M = 0.8911.From eq.19 duty ratio limit is 0.5,but we generally don't go upto that because then capacitor won't have enough energy to charge inductor and output voltage of QZS decreases.

6.4.2 Selection of Inductor

Inductor is selected based on current ripple consideration, If we consider loss of inverter and motor = 90% ,then $I_{L\ avg} = \frac{10KW/0.9}{230\ V}$ = 48.3A,Considering a Shoot through duration of inductor, From $V_L = L\frac{di}{dt}$.

$$L \geq V_L \frac{dt}{di} \tag{20}$$

Considering Inductors during Shoot through period and current ripple as 5% of average value, dt as half of shoot through time and V_L as 328.6 V. we get

$$L1, L2 \geq 1540.6uH$$

6.4.3 Selection of Capacitor

Capacitor is selected based on Voltage ripple consideration, suppose for both capacitor , Voltage ripple across them is 5%, From shoot through duration

$$I_c = C\frac{dV}{dt} \tag{21}$$

$$C \geq I_c \frac{dt}{dV}$$

Considering Capacitor C1,during Shoot through period and voltage ripple as 5% of average value, dt as half of duty cycle time, I_c as average inductor current.we get

$$C1 \geq 114.2uF$$

Thus we take $C_1 = C_2 = 114.2uF$

6.4.4 Simulation specifications

Output Power	10KW
Output Line voltage	230 V
Input Battery Voltage	230 V
Quasi Resonance Inductor L1,L2	1540.6uH
Quasi Resonance Capacitor C1,C2	114.2uF
Shoot through duration every T_{sw}	22.82us
Modulation Index	0.8911

Table 2. Simulation Specifications for QZSI

6.5 Simulation Results for QZSI

Open Loop Control for QZSI was simulated in MATLAB 2017b.Simulation results are as follows. Here S.T. represent Shoot through Duration, N.S.T. represent Non Shoot through duration. DC side waveforms are for one switching period (100us).

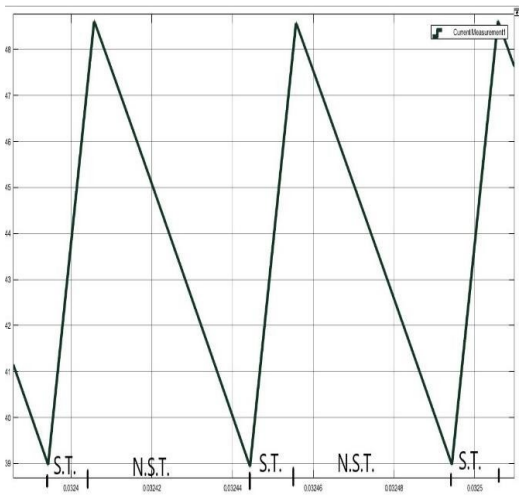


Fig.28 current through inductor 2

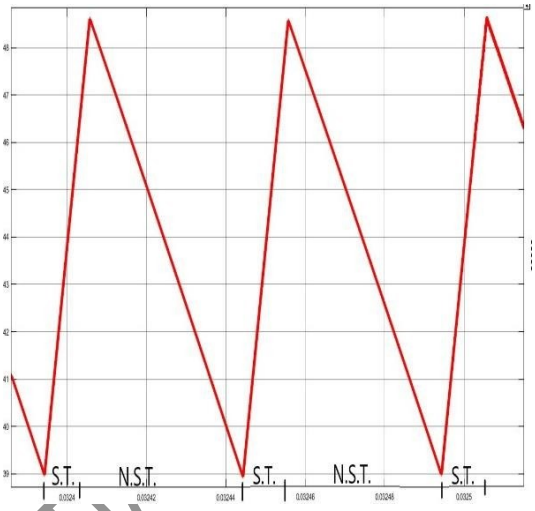


Fig.29 current through inductor 1

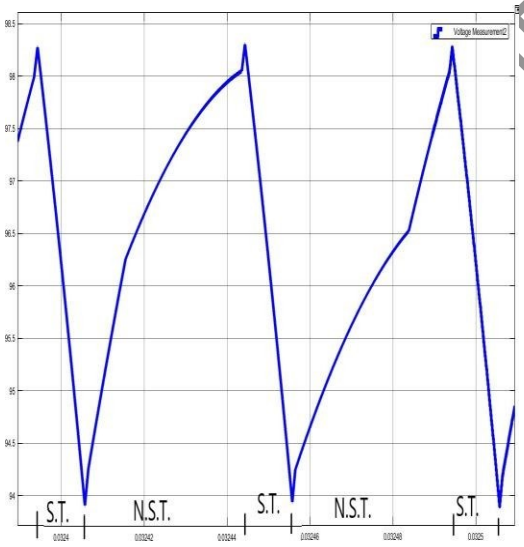


Fig.30 Voltage across capacitor 1

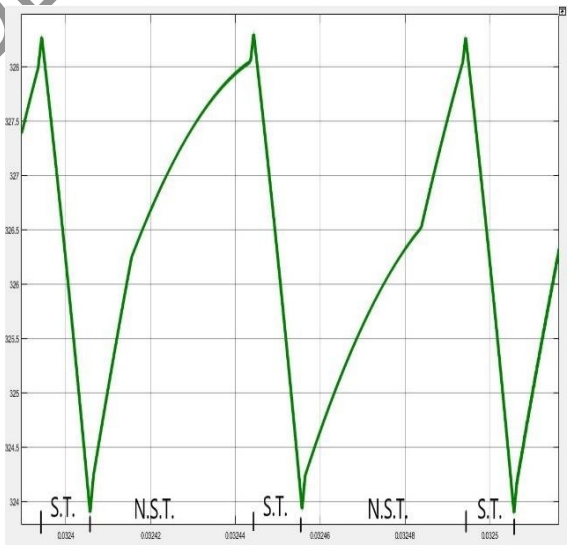


Fig.31 Voltage across capacitor 2

Fig. 28 and 29 shows current through inductor 1 and 2 ,since voltage across both indcutor are same in all states, thus average value and waveform will also be same.From

waveform in Shoot through state(ST) inductor current increases,because capacitor gives energy to inductor in S.T. state.Average value of both inductors are 44A.

Fig.30 and 31 shows voltage across capacitor 1 and capacitor 2.by switching averaging, we came to know both capacitor voltages differ by V_{input}(230V),which is also shown in waveform. In S.T. state capacitor voltage decreases,because it gives energy to inductor.V_{C1} = 96V,V_{C2} =326.8V

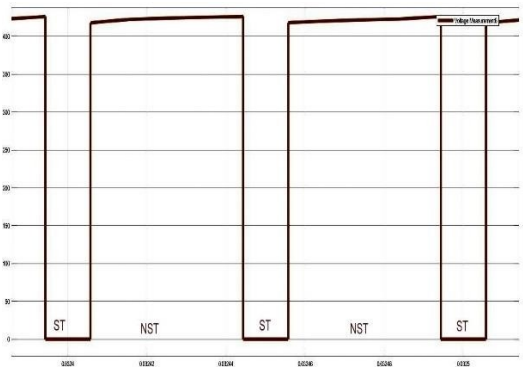


Fig.32 Voltage across inverter input

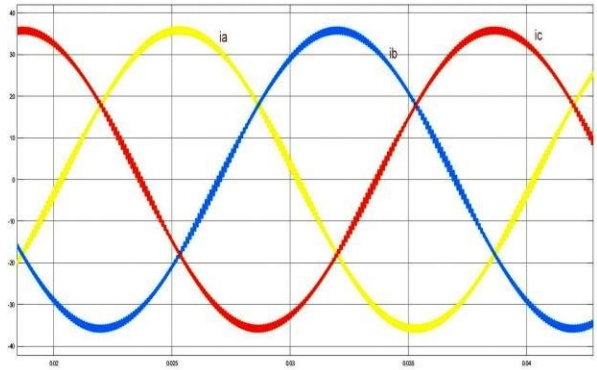
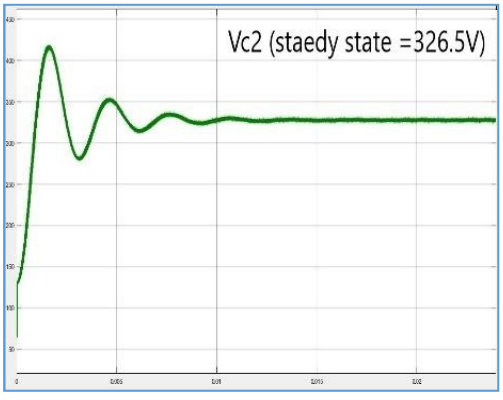


Fig.33 Output three phase current

Fig.32 shows voltage across input of inverter. In S.T. state it is zero because all the switches of inverter are turned on, in N.S.T. state it is sum of Vc1 and Vc2, which is 423V,thus effective voltage across input increases and we get boosted voltage at input of inverter and desired ac output voltage 230V_{LL} . Figure 33 shows three phase ac load current.Fig. 33.1 shows open loop Vc2 and iL1 response. By analyzing transient state,we need closed loop control.



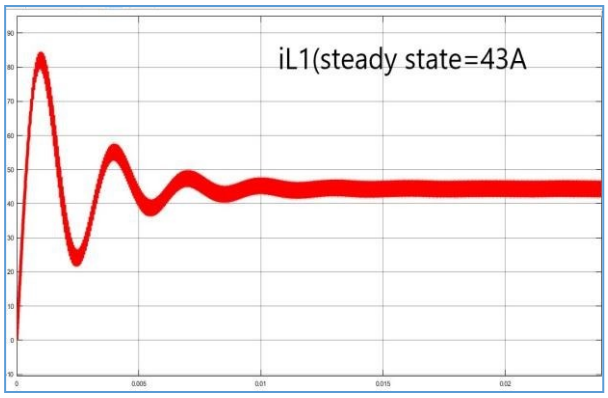


Fig.33.1 Vc2 and iL1 Open loop response

Chapter 7

Feedforward-Feedback control for DC Side QZSI

7.1 Introduction

Feedforward uses the measurement of an input disturbance to the plant as additional information for enhancing single-loop PID control performance. This measurement provides an "early warning" that the controlled variable will be upset some time in the future. With this warning the feedforward controller has the opportunity to adjust the manipulated variable (duty ratio here) before the controlled variable (voltage or current here) deviates from its set point [6].Note that the feedforward controller does not use an output of the process. This is the first example of a controller that does not use feedback control; hence the new name feedforward. Feedforward is usually combined with feedback so that important features of feedback are retained in the overall strategy.

Comparison of feedforward and feedback principles

	Feedforward	Feedback
advantages	Compensates for a disturbance before the process output is affected	Provides zero steady state offset
	Does not affect the stability of the control system	Effective for all disturbance

Disadvantages	Cannot eliminate steady state offset	Does not take control action until the process output variable has deviated from its set point
	Requires a sensor and model for each disturbance	Affects the stability of the closed loop control system

Table 3. Advantages and Disadvantages of Feedback and Feedforward control

The feedforward controller ensures perfect control, if the models used are perfect or the measured disturbance is the only disturbance experienced by the process. Neither of conditions 1 or 2 is generally satisfied. Therefore feedforward control is always combined with feedback control.

Equation for Inductors and Capacitors during shoot through State

$$L_1 \frac{di_{L1}}{dt} = V_{in} + V_{C1} \quad (22)$$

$$L_2 \frac{di_{L2}}{dt} = V_{C2} \quad (23)$$

$$C_1 \frac{dv_{c1}}{dt} = -i_{L1} \quad (24)$$

$$C_2 \frac{dv_{c2}}{dt} = -i_{L2} \quad (25)$$

Equation for Inductors and Capacitors during non-shoot through State

$$L_1 \frac{di_{L1}}{dt} = V_{in} - V_{C2} \quad (26)$$

$$L_2 \frac{di_{L2}}{dt} = -V_{c1} \quad (27)$$

$$C_1 \frac{dv_{c1}}{dt} = i_{L2} - i_o \quad (28)$$

$$C_2 \frac{dv_{c2}}{dt} = i_{L1} - i_o \quad (29)$$

Multiplying Shoot through equations with d and non-shoot through equations with (1-d) and add

$$L_1 \frac{di_{L1}}{dt} = V_{in} + (V_{c1} + V_{c2})d - V_{C2} \quad (30)$$

$$C_2 \frac{dv_{c2}}{dt} = -i_{L2}d + (i_{L1} - i_o)(1-d) \quad (31)$$

$$\frac{L_1}{(V_{C1} + V_{c2})} \frac{di_{L1}}{dt} + \frac{V_{c2} - V_{in}}{(V_{C1} + V_{c2})} = d \quad (32)$$

$$\frac{C_2}{(1-2d)} \frac{dv_{c2}}{dt} + \frac{i_o(1-d)}{(1-2d)} = i_{L1} \quad (33)$$

From above equations(32,33) first terms are output of controller and second terms are feedforward terms. Inner current loop controls i_{L1} and outer voltage loop controls v_{c2}. Bandwidth of outer loop should be less than 1/10 of inner loop. For first equation, i_{L1} and d are taken variables, others are constant. For second equation, V_{c2} and i_{L1} are taken as variable, others as constant.

7.2 Controller Design

First we need to design inner current loop. For feedforward control, equations are linearized and we get first order transfer function, thus controller design becomes easy. By state space analysis ,transfer functions we get of order 4,but controller design for them is complex[8]. Neglecting the feedforward term, Open loop transfer function $\frac{iL1(s)}{d(s)}$ becomes

$$\frac{i_{L1}(s)}{d(s)} = \frac{(V_{C1} + V_{C2})}{L_1 s} = \frac{K}{s} \text{ where } K = \frac{(V_{C1} + V_{C2})}{L_1} \quad (34)$$

Based on the design consideration discussed in last section, $(V_{C1} + V_{C2}) = 423.6V$ and L_1=1540.6uH. First we will see, whether only proportional controller is sufficient or not. With Proportional controller coefficient (K_P),Open loop transfer function becomes

$$\frac{i_{L1}(s)}{d(s)} = \frac{K_P(V_{C1} + V_{C2})}{L_1 s} = \frac{K}{s} \text{ where } K = \frac{K_P(V_{C1} + V_{C2})}{L_1} \quad (35)$$

Thus Closed loop transfer function

$$\frac{i^*_{L1}(s)}{i_{L1}} = \frac{K}{s + K} \quad (36)$$

Thus bandwidth for current loop

$$\omega_i = K = \frac{K_P(V_{C1}+V_{C2})}{L_1} \tag{37}$$

If ω_i=6000 rad/s (less than 1/10 of switching frequency) , K_P=0.021843

From Fig.34, it is clear that only K_P is sufficient for inner loop controller design, thus we don't need to add K_I, since i_{L1} steady state error is very less.

Now we will see outer loop controller design. Outer loop bandwidth will be less than 1/10 of inner loop, thus it will see inner loop as constant equal to unity. From eq.38 outer loop OLTF is

$$\frac{v_{C2}(s)}{i_{L1}(s)} = \frac{1-2d}{C_2 s} \tag{38}$$

First we will see, whether only proportional controller is sufficient or not. with Proportional controller coefficient (K_P) ,Open loop transfer function becomes

$$\frac{v_{C2}(s)}{i_{L1}(s)} = \frac{K_P(1-2d)}{C_2 s} = \frac{K}{s} \text{ where } K = \frac{K_P(1-2d)}{C_2} \tag{39}$$

Thus Closed loop transfer function

$$\frac{v^*_{C2}(s)}{v_{C2}(s)} = \frac{K}{s+K} \tag{40}$$

Bandwidth for outer loop $\omega_v = K = \frac{\omega_i}{10} = 600$ rad/s. here d=0.2281 and C_2=114.6uF gives K_P =0.1264.From Fig.35 ,it is clear, that only proportional controller is not sufficient ,because steady state error is very high(10% here). Thus we will use proportional plus integral (PI) controller ($K_P + \frac{K_I}{s}$). with PI controller coefficient (K_P and K_I) ,Open loop transfer function becomes

$$\frac{v_{C2}(s)}{i_{L1}(s)} = \frac{(K_P + \frac{K_I}{s})(1-2d)}{C_2 s} = \frac{(K_P + \frac{K_I}{s})}{C'_2 s} \text{ where } C'_2 = \frac{C_2}{1-2d} \tag{41}$$

Closed loop transfer function becomes

$$\frac{v^*_{C2}(s)}{v_{C2}(s)} = \frac{K_P s + K_I}{s^2 + \frac{K_P}{C'_2} s + \frac{K_I}{C'_2}} \frac{1}{C'_2} \tag{42}$$

For second order system, with critical damping response, damping ratio (ε) =1 gives fastest response without overshoot.

$$\text{Bandwidth } (\omega_v) = \frac{1}{\text{Time constant}} = \sqrt{\frac{K_I}{C'_2}} \text{ and } 2\varepsilon\omega_n = \frac{K_P}{C'_2} \tag{43}$$

After putting different values of bandwidth (ω_v), at $\omega_v = 463$ rad/s ,K_P =0.144 and K_I =45.2422 gives best steady state and transient response. Fig 36

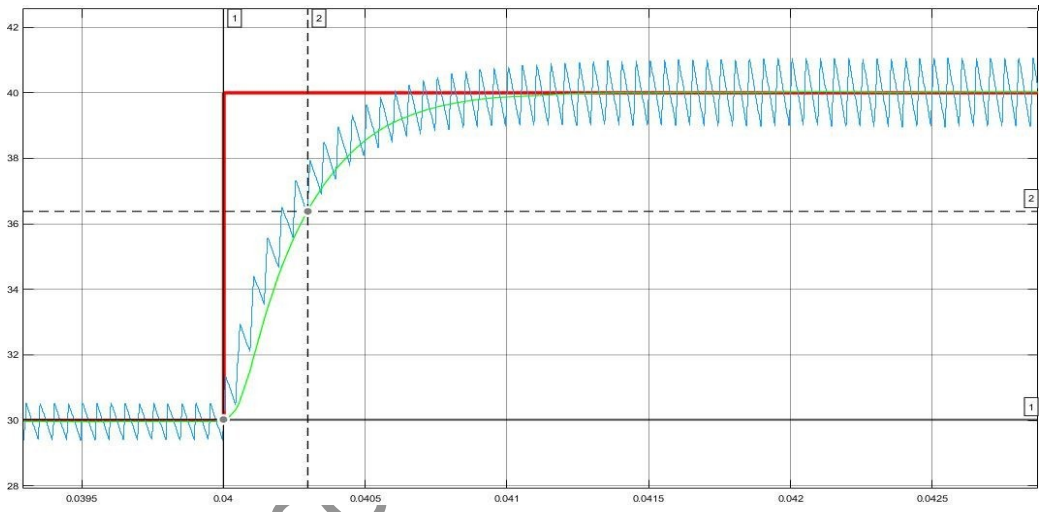


Fig.34 inner current loop step response

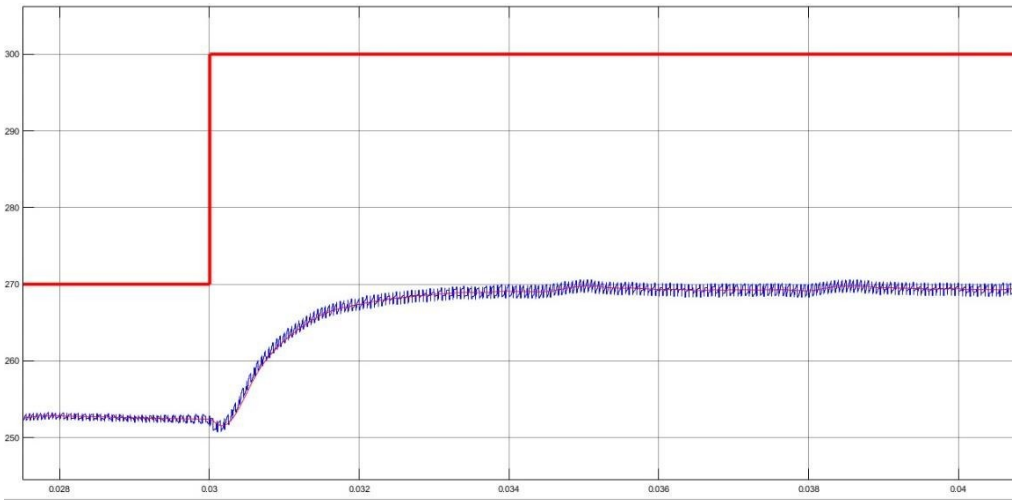


Fig.35 outer voltage loop response with only P controller

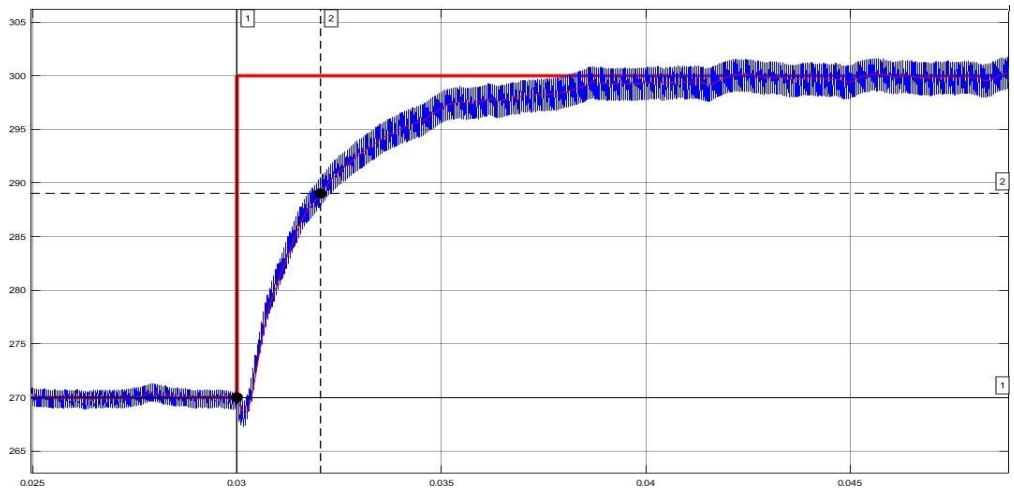
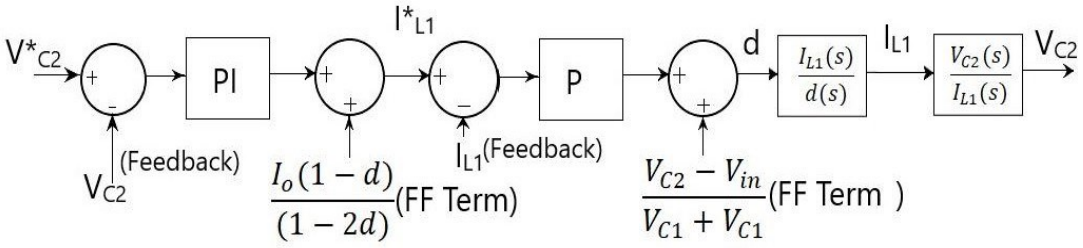


Fig.36 Outer voltage loop response with PI controller

Fig.37 shows current i_{L1} response , reference is step input ,changing from 30A to 40A at 0.04s,time constant is 297us.Fig.34 shows voltage V_{C2} response with only P controller, reference is step input changing from 270V to 300V at 0.03s.steady state error is 10%,thus we need PI controller. Fig.35 shows voltage V_{C2} response with PI controller, thus steady state error is very less. Fig.36 shows block diagram of feedforward-feedback control.



$$\frac{V_{C2}(s)}{I_{L1}(s)} = \frac{1-2d}{C_2 s}$$

$$\frac{I_{L1}(s)}{d(s)} = \frac{V_{C1}+V_{C2}}{L_1 s}$$

Fig. 37 Feedforward Feedback control for QZSI

Chapter 8

Proposed Quasi Z source inverter with Soft Switching

8.1 Introduction

So far we have discussed Quasi Resonance DC Link Inverter for reduced dv/dt across inverter to decrease high frequency parasitic effects and for soft switching of Inverter switches and Quasi Z source inverter for voltage boosting, when input battery voltage is low and high speed operation is required. However, if we want above mentioned qualities to both topologies in one topology, the cascaded connection will increase total number of components, resulting a severe compromise to its size, cost, weight and complexity .In Quasi Z source inverter, the shoot through current is two times the inductor current, which contributes high voltage gradient (dv/dt) across inverter, EMI noises and switching losses operating in the hard switching condition.

Proposed Quasi Z source inverter with soft switching is shown in Fig.36. Quasi resonance part, which is also auxiliary circuit is connected between Inverter and Quasi Z source for providing reduced dv/dt and soft switching of all switches of inverter [5].Circuit shown in Fig.38 consists of five modes of operation. Each mode is explained below with equivalent circuit.

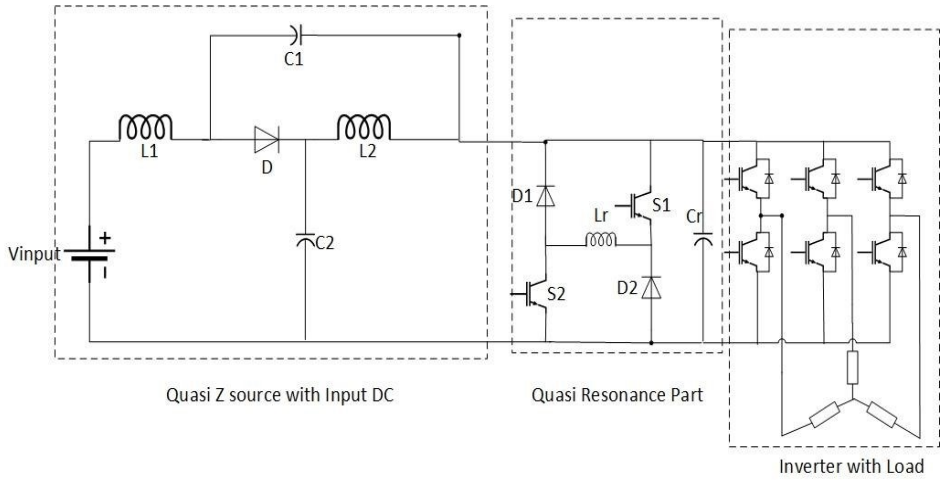


Fig.38 Proposed QZSI with soft switching

Simplified equivalent of topology in Fig.36 in one switching period is shown in Fig.37 (when inverter is feeding a load during one switching interval, load can be assumed as constant current source).S presents the inverter leg. S on is equivalent to all switches of inverter legs are on. S off represents normal operation of inverter. Five modes of operation are explained below.

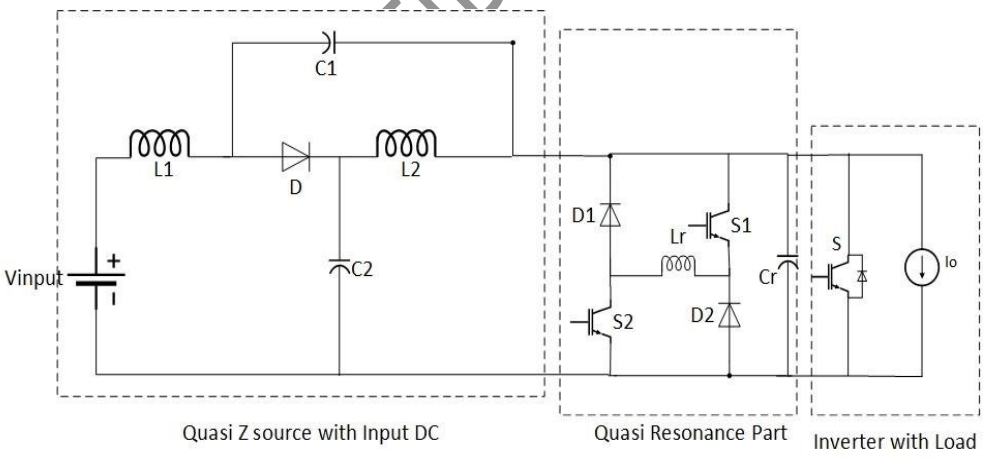


Fig.39 Equivalent circuit of QZSI with soft switching

8.2 Present Circuit and Operation

Quasi Z source operation will be same as discussed in last topology,here we will mainly discuss operation of quasi resonance part.

Mode 0(M0)

In this mode inverter is in steady state. Switch S_1, S_2, S are off and diode D is on. Boosted voltage of Quasi Z source is applied to inverter input, which is sum of voltage across C_1 and C_2.Diode D is on, because while going from shoot through to non shoot through, V_{Cr} gets charged, when $V_{Cr} > (V_{C1}+V_{C2})$,diode D becomes on.

$$i_D = i_{L1} + i_{L2} - I_o = 2i_L - I_o \quad (44)$$

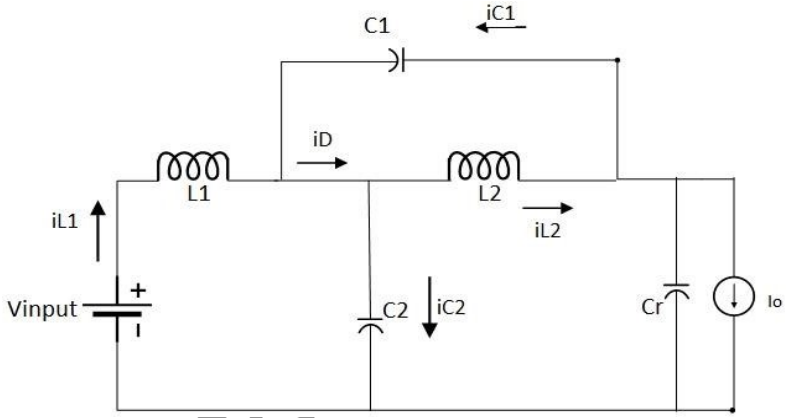


Fig.40 Equivalent circuit of Mode 0

Mode I(M1)

Whenever any change in applied vector of inverter accordingly inverter leg switches has to change. In order to achieve reduced voltage gradient as well as ZVS of inverter switches, voltage across legs has to reduce to zero by resonance. Since voltage across inverter input(V_{cr}) is clamped to $V_{C1}+V_{C2}$,first V_{cr} should be pulled down to zero by resonance, for that diode D should be turned off. Thus switches S_1 and S_2 from auxiliary circuit are tuned on under Zero current switching(ZCS) some time before active vector transition under Zero switching condition (ZVS) simultaneously with same gate pulse, such that current through diode is pulled down to zero and then V_{cr} can be reduced to zero by resonance.

$$i_D = i_{L1} + i_{L2} - I_o - i_{Lr} = 2i_L - I_o - i_{Lr} \quad (45)$$

When i_{Lr} is increased sufficiently such that, $(I_o + i_{Lr}) > 2i_L$,diode D turns off.

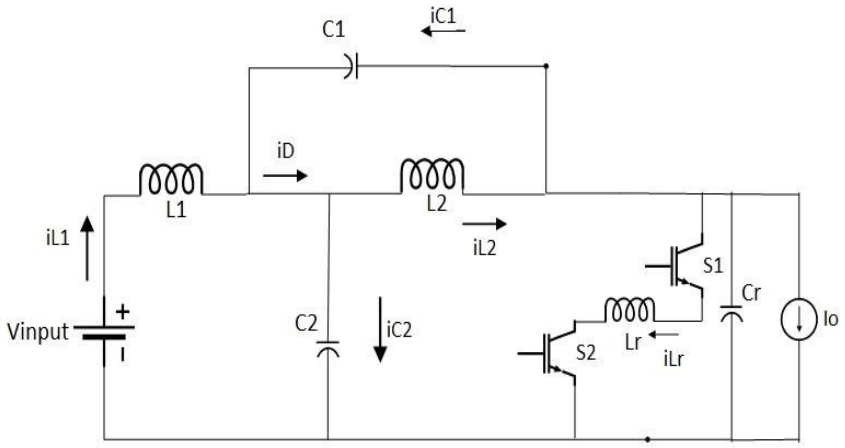


Fig.41 Equivalent circuit of Mode 1

Mode II(M2)

Now capacitor C_r is not clamped to $V_{C1}+V_{C2}$, and it starts giving its energy to inductor L_r .At the end of Mode II ,V_{cr} becomes zero by resonance with reduced dv/dt.

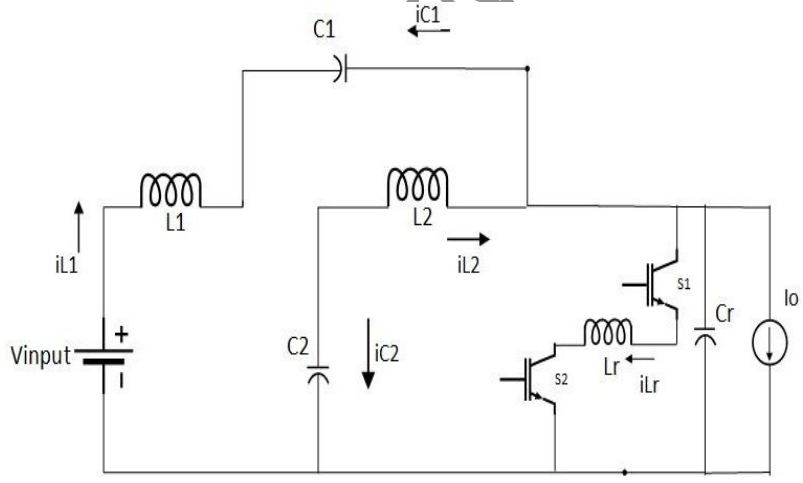


Fig.42 Equivalent circuit of Mode 2

Mode III(M3)

Since V_{cr} has become zero with reduced voltage gradient, antiparallel diode of inverter switches are turned on and in this situation ,all switches of inverter can be turned on under zero voltage switching condition(ZVS). This mode has adjustable time period

according to how much boost, QZS circuit required for voltage boost. In this mode Capacitors of QZS gives energy to inductors of QZS and i_{L1} and i_{L2} increases.

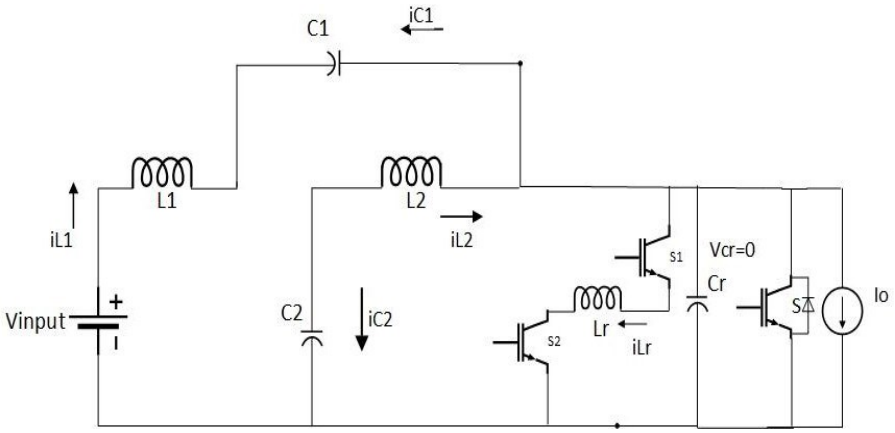


Fig.43 Equivalent circuit of Mode 3

Mode IV(M4)

To apply new switching state, and to recharge C_r again to $V_{C1}+V_{C2}$ by resonance with reduced dv/dt, according to active vector respective inverter switches will be turned off, remaining switches are kept on, switch S as well as S_1S_2 is turned off under ZVS in equivalent circuit. Now i_{Lr} starts flowing from D1 and D2 and C_r is charged to $V_{C1}+V_{C2}$,thus diode D is turned on.

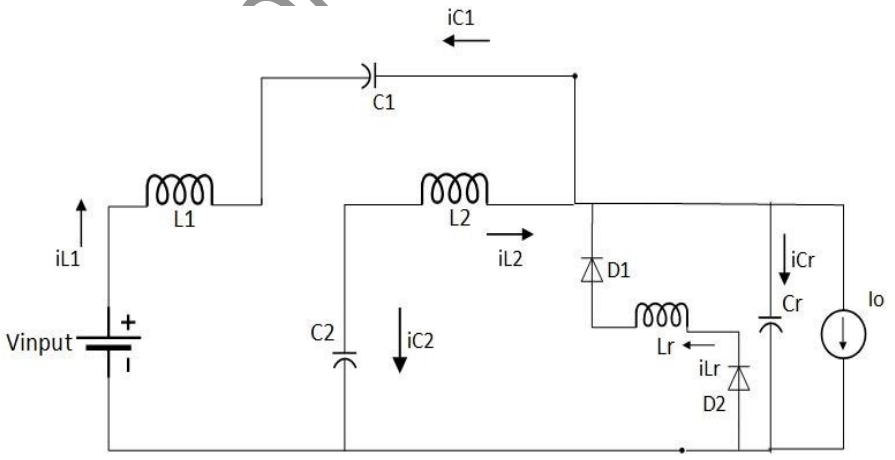


Fig.44 Equivalent circuit of Mode 4

Mode V(M5)

When $V_{Cr} > (V_{C1} + V_{C2})$,diode D gets forward biased,and boosted voltage applied to input of inverter. Diode D carried addition current flowing from L_r. Capacitor C_1 and

C_2 gets more energy, but since L_r value is very low, its energy will be low and it does not affect boost operation much and that can be taken care by closed loop by adjusting duty ratio of shoot through time period. This mode ends with i_{Lr} becomes zero.

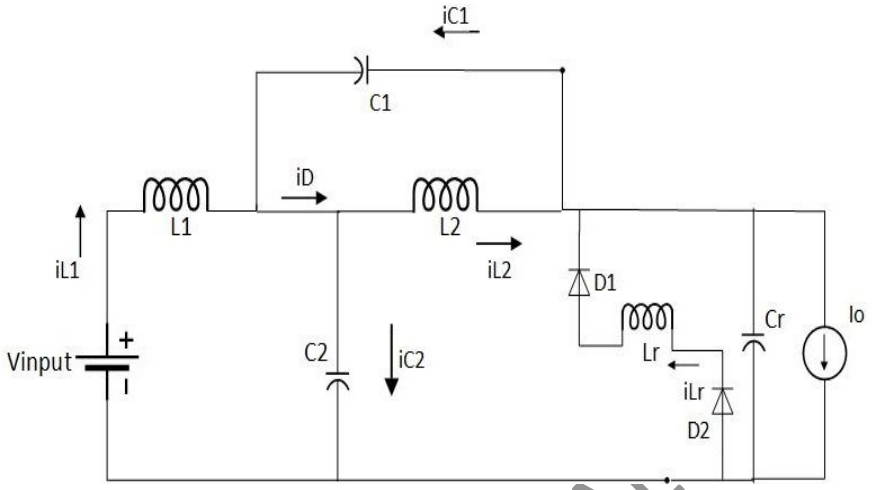


Fig.45 Equivalent circuit of Mode 5

8.3 Typical current and voltage waveform

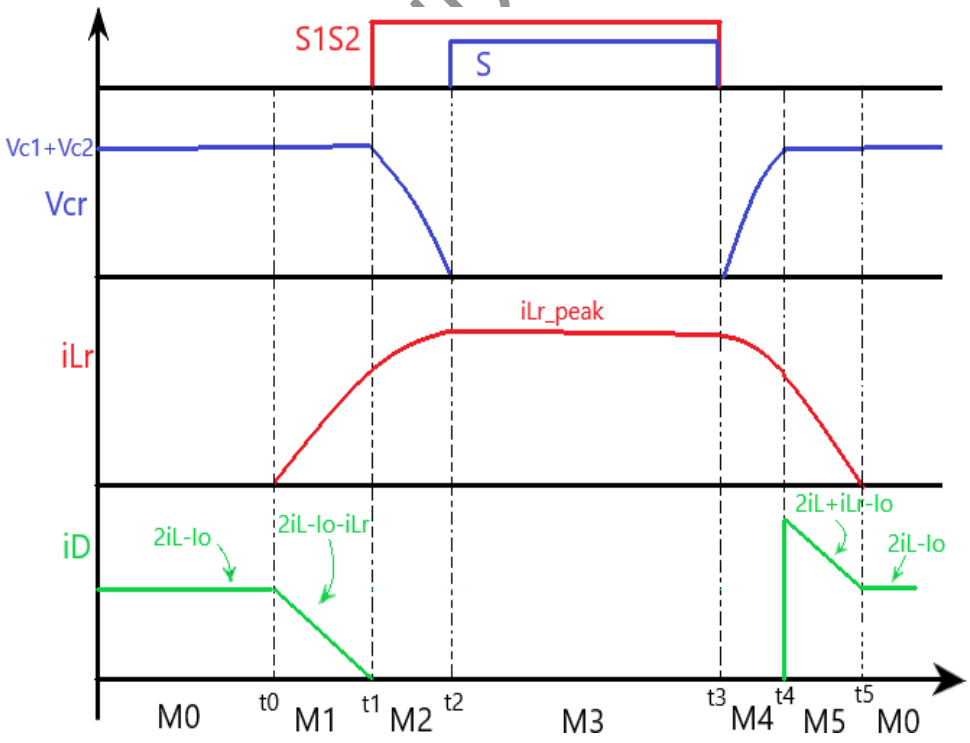


Fig. 46 Typical Voltage and current waveform

8.4 Simulation Parameters

Parameters	Value
Input DC Voltage	230V
Inductor L_1,L_2	1540uH
Capacitor C_1,C_2	114.6uF
Resonance Inductor L_r	4uH
Resonance Capacitor C_r	30nF
Load current Io	30A
Switching Frequency	10KHz
Shoot through duty ratio	0.2

Table 4. Simulation Specifications for Proposed QZSI with soft switching

8.5 Simulation waveforms for QZSI with soft switching

Equivalent circuit of Proposed QZSI with soft switching was simulated in MATLAB 2017b.switching time period was 100us.shoot through duty ratio was 0.2, thus 20us shoot through period.

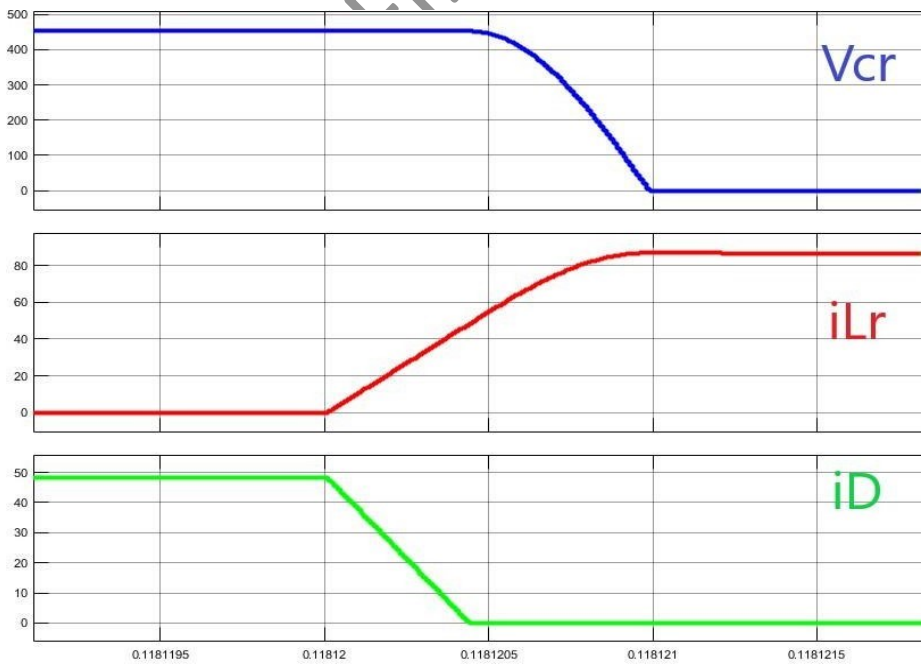


Fig.47 Waveforms during discharge of Cr voltage

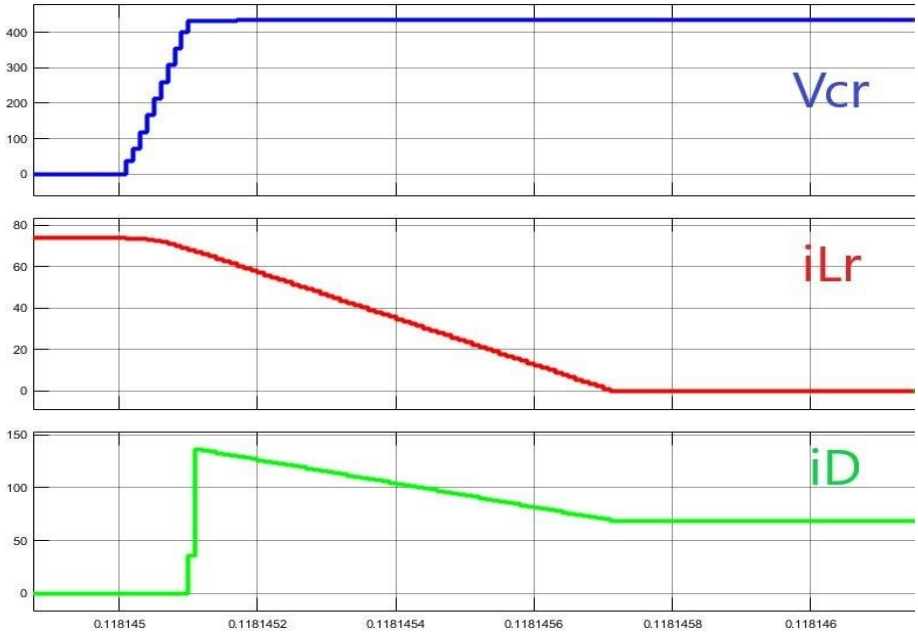


Fig.48 Waveforms during recharge of C_r voltage

Fig.47 shows discharge of capacitor C_r ,maximum current flowing through L_r is 86.8A .Fig.48 shows recharge of capacitor C_r .according to QZS operation $V_{C1}+V_{C2}$=390,but here it is 450V ,because of extra energy provide by L_r during mode 5,but that will be taken care by closed loop control. From the figures during discharge of C_r, voltage gradient across inverter is 900V/us and during recharge, it is around 3000V/us. By changing resonance elements, we can change voltage gradients as well as resonance time duration. THD of line current will decrease for Proposed QZSI with soft switching compared to QZSI.

Chapter 9

Conclusion and Future works

Conclusion

Quasi Resonance DC Link inverter was designed and simulated for reduced voltage gradient and lossless switching. A modified SVPWM technique is used to improve DC bus utilization. Problem with excess voltage stress across resonance switches was solved using modified topology and switch voltages were clamped to DC bus voltage using voltage clamping circuit.

Quasi Z source inverter was designed and simulated for voltage boosting for high speed operation of drive without using additional switch at the input. SVPWM technique was used for PWM and shoot through period was provided for minimum null vector duration in any of the switching time period of SVPWM. Thus desired AC output voltage was obtained. Quasi Z source inverter with soft switching was proposed, which provides desired voltage boosting as well as reduced voltage gradient to reduce EMI interferences and soft switching. The operations of all the topologies were verified in simulation software, ensures suitable, efficient and reliable for an EV application

Scope for future works

Open loop control is performed for QRDCL inverter and QZSI with soft switching and closed loop Feedforward-Feedback control is performed for DC Side QZS inverter in simulation platforms. Future extension of this project will be practical implementation of all the topologies for PMSM and induction motor drives.

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