Performance Analysis of NoC Structure based on Star-Mesh Topology

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Abstract— **The fabrication technology development of the semiconductor leads the evolutional design methodology to reconsider the efficiency, such as reusability and scalability. NoC (Network On Chip) is the remarkable alternative to support this trend that provides the interface between IPs. In this paper, the general performance analysis through considering the characteristic of the NoC was done with the proposed NoC topology. Besides, the performance at the topology which is the specification application, 4-channel H.264 decoder, was predicted in advance. We could build the environment facilitating the adjustment of the buffer size and mapping of IP with this scheme.**

Keywords-component; NoC, topology, IP, reusability, scalability, H.264

I. INTRODUCTION

The NoC (Network on a Chip) was proposed in order to solve the structural problem and the frequency limitation appeared with the development of the semiconductor processor technology [1][3]. While the character of the SoC (System on Chip) changes to the reuse of IP in which the design circumstance is pre-verified, the integrated composition on a chip becomes more complicated by the demand of the market about the simultaneous implementation of the various functional block and the high-end specification, such as HD resolution Codec IP, 3D accelerator IP and multi-processor core. In the situation requiring the mass IPs and the performance of a high-end specification on a chip, it will be confronted with the situation where it cannot endure with the structure of the bus-oriented interface. The bus-oriented structure will show a limitation in case that many independent master blocks and the data transmission through the parallel processing on a chip are necessary. It is the NoC to be proposed to replace the bus-oriented structure. The NoC has the prospect that it solves the problem with the bus-oriented structure, such as the complexity of the implementation and the limitation of the operating frequency.

But, even though NoC is regarded as the alternative of the bus-oriented interface environment, Up to date, the performance analysis and the concrete result about the specific application with the NoC fabric are nearly unprecedented. Nevertheless, to use the usual pattern, such as the random pattern and the uniformly generating pattern to approximate the traffic load of the specific application, was the generalized method for analyzing the performance [2]. This kind of the evaluation has the disadvantage of getting only the average value in case that reconfigurability and programmability of chip are simultaneously high like the GPP (General Purposed Processor). With this simulation method, the area cost is wasted or insufficient according to the applied application. And it is mainly suitable to the mesh type among the NoC topology. This paper describes the method for predicting the input buffer size of the switch with the proposed SMT (Star Mesh Topology)-NoC structure in the upper level. And we performed to build the environment measuring the effectiveness of the proposed SMT-NoC with the 4-channel H.264 decoder. We achieved these works in order to get the suitable model like the cycle accuracy hardware though CLM (Cycle Level Model) of SystemC.

This paper is organized as follows. Section 2 presents the structure and component of the previous NoC. In Section 3, we describe the proposed NoC topology and simulation scheme. Section 4 shows experimental results. Conclusion and future works are drawn in Section 5.

II. NETWORK ON CHIP

The NoC is developed on the object to enhance more transfer efficiency and more modular than the bus-oriented communication interface. The structure of NoC is classified into the calculation unit and transmit unit. Calculation unit is referred to as the specific IPs, usual processor and memory. Transmit unit is referred to as the functional blocks to implement the protocol of the NoC and to connect between the calculation unit. And the topology referring to the connection type between the switch affects the scalability and performance of application.

A. Data Transmission of The NoC

The NoC has the transfer mode that divide message into the standard unit referred to as the packet. In the bus-oriented structure, only one fair of IPs, such as master and slave in case of the AMBA (Advanced Microcontroller Bus Architecture) protocol, possess a transmission fabric at regular intervals. This transmission strategy has only a method about the increase in frequency to improve the operating performance. But the NoC has a feature that simultaneously transfers the data between multiple IPs. Because it sets up several paths to

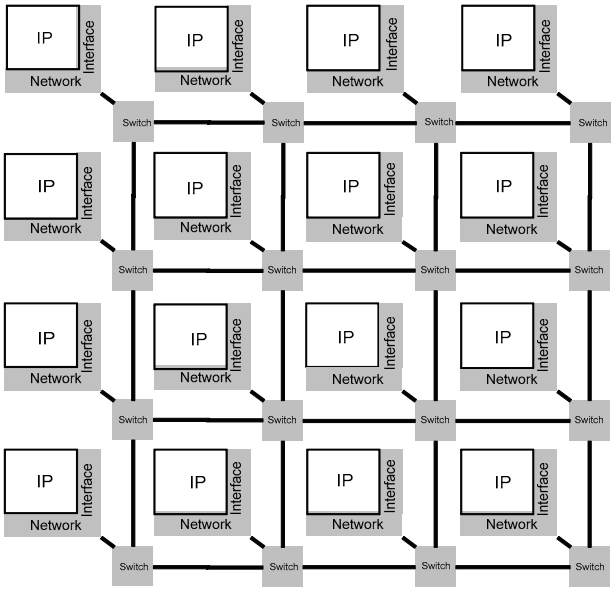

Figure 1. Regular NoC Structure

transfer the packet from the source point to the destination point by using the switching scheme referred to as the packet switching.

That is, the transfer message is generated by calculation units. The NI (Network Interface) converts the message to several packets. Again, a generated packet from the NI is disassembled by several flits and arrives at the destination location through the switch. The NoC usually applies the wormhole routing scheme that divides a packet into several flits in consideration of the area cost. After arriving at the destination location, the NI, connected to the target IP, assembles packets to send message for the target IP. In the process where packets are transmitted, switches appropriately perform the switching with a packet-by-packet in case packets require the transmission of the same path.

B. NoC Topology

The connection type between the switch to compromise the NoC is referred to as topology. Generally, the topology of the NoC is usually identical with that of the computer network. According to the connection type, it influences on the simplicity of the implementation and the efficiency of the transfer. The topology is usually classified into the regular type and the non-regular type by the shape of the switch connection. The regular type, such as mesh and xxx, usually has a good performance but does not have the scalability of the design and the convenience of design. On the other hand, the non-regular type, such as star and xxx, has the reverse characteristic of the regular type. Therefore, a designer has to select the suitable topology according to the performance of the application and scale of the whole design. But at the same time, when a performance and simplicity are pursued, there is a limit with the existing topology types.

III. STAR MESH TOPOLOGY NOC

The SMT-NoC proposed in this paper satisfies the structural simplicity and the performance efficiency at the same time. While the design simplicity of the mesh topology is maintained, it has the short latency of the star topology. In case that latency has to be short and the transmission frequency of data is high, it connects to the same star switch to prevent the performance degradation. The structure to be proposed is appropriate in case the number of master IPs exceed 8.

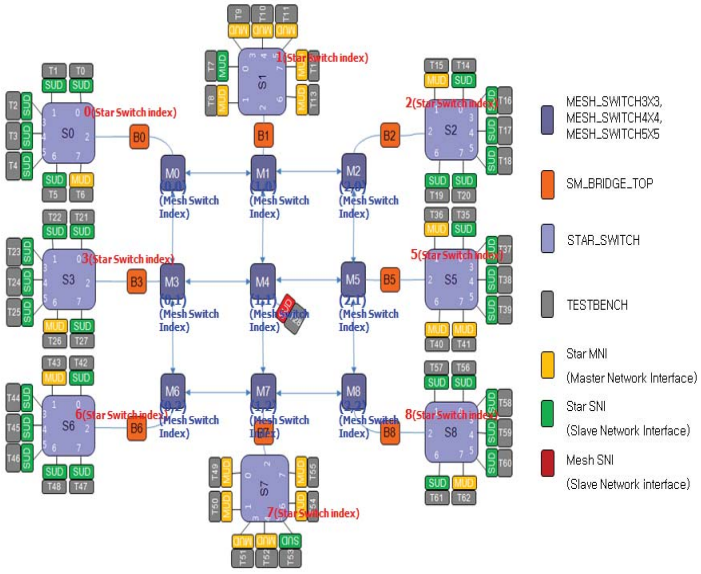

Figure 2. SMT-NoC Structure and Components

A. SMT-NoC Protocol

The SMT-NoC protocol is divided into 2 areas. Those are the protocol of the star switching stage and the protocol of the mesh switching stage. Typically, the star protocol is considered a short latency and a mesh protocol is considered a high scalability.

Table 1. Protocol layer of the SMT-NoC

Protocol Layer	Star Protocol	Mesh Protocol
Transport	-Master Network Interface -Slave Network Interface -Fixed size packet format	-Mesh Network Interface -Variable size mesh packet format
Network	-Source routing scheme -Round Robin arbitration -Route information modification	-XY routing scheme -Round Robin Arbitration -Source/Target Routing Index Comparison
Data link	-Wormhole routing scheme -Flit based flow control	-Wormhole routing scheme -Flit based flow control
Physical	-Source synchronous data transaction	-Source synchronous data transaction

Components of the SMT-NoC in figure 2 are required to implement the protocols in table 1. The NI is mainly responsible to the transport layer and some part of the network layer. And the switch is responsible to the data link layer and physical layer.

B. *SMT-NoC Components*

- *Traffic Generator*

The TG (Traffic Generator) has the function simulating the traffic pattern in internal modules comprising the H.264 decoder and generating the random pattern. Because it has the function for the transceiver of the traffic by the schedule script files. It can produce and consume traffic as H.264 internal modules and the random pattern generator. Particularly, the latency of the packet in the destination IP is calculated by using the departure time inserted into the packet data field from a source IP. The handshake protocol between the TG is added to simulate the controllable scheduling as the scheduling of the H.264 decoder between internal modules.

- *Network Interface*

The NI (Network Interface) carries out the role of converting the message into packets for the transmission of the NoC. Several functional fields in one packet are distinguished with the address, the data and control information fields. Each of fields in one packet is filled by the NI with the IP control. Two NIs are needed in the proposed SMT-NoC structure, because the format of packet between the star protocol and mesh protocol is different. According to the kind of message received from IPs, the NI has to have the role to make different transmission mode. The holding of IP by the network congestion has to be prevented in case of transmission data.

- *Switch*

The switch transmits packets by using the wormhole routing scheme. Since the wormhole routing scheme divides a packet into several flits, the flow control for the flit unit is necessary for a switch. So, all operations are progressed with the flit unit. The switch has buffers referred to as input buffer at the input stage. The input buffer has the role to buffer several flits inserted through the input port. It is necessary to effectually manage the input buffer size because of occupying as the important factor at the whole consumption of the NoC area. Buffered flits are controlled to decide the output port and to receive the grant signal by control block. If several flits require the same output-port, the control block should minimize the buffering time of flits by using the efficient grant algorithm. This paper applies the Round-Robin algorithm for the efficient grant algorithm and simple implementation. And it has the strategy to guarantee the QoS (Quality of Service) of the transfer latency according to the priority. For simulation depending on the buffer size, we applied the controllable size of the buffer by using the circular buffer model. The latency from the input stage to the output stage is 3 cycles.

IV. SIMULATION & PERFORMANCE ESTIMATION

We performed two simulations for the performance evaluation of the proposed SMT-NoC. Firstly, it is the general performance analysis using the random pattern. Secondly, by using the pattern increasing the parallel transfer with the JM reference source code of the H.264 decoder standard, we got the performance of the 4 channel H.264 decoder. Structure for this simulation is the same as figure 2. The TG connecting playing total 57 IP roles is possible.

A. *Random Pattern Insertion*

A simulation in this paper regarded the network load as the number of the packet inputted to the proposed SMT-NoC. With the Gaussian distribution, Network load 40 is a case that TG can produce a packet with 40 cycle interval. And, network load 2 is that all TGs generate a packet every 2 cycles. We set up the boundary of the network load from 40 to 2. After randomly selecting the destination IP of the input pattern, the whole latency was measured according to the buffer size 10 and the buffer size 30. Moreover, the latency according to the closeness between IPs connected to the same star switch was also measured. Closeness 70 is a case that 70 percent among packets produced by TG is sent for another TG connected to the same star switch. If the traffic volume of an application can be known in advance, the input buffer size of the suitable switch can be appropriately set through this simulation. Approximately, the remarkable difference of the performance by the buffer size seems to be appeared by the traffic load 9 in figure 3. Under the network load 10, the performance difference according to the buffer size could be negligible.

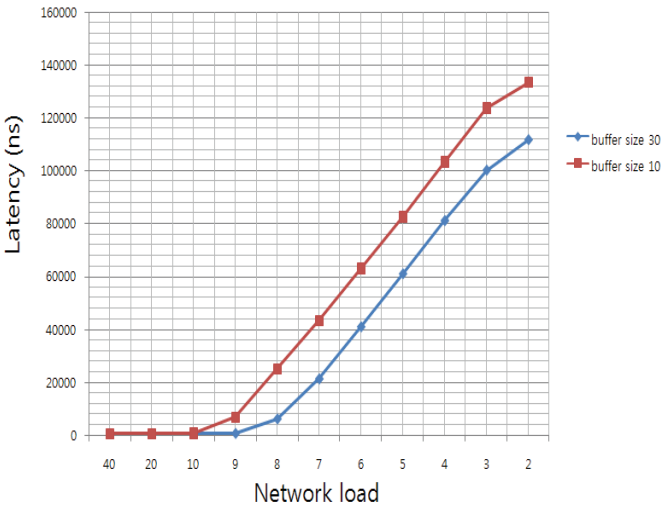

Figure 3. The average latency depending on two buffer size

Through results of figure 4, we confirmed that closeness has the strong resistivity against the network load. By this reason, if DMA and memory are located at the same star switch in the real application, its performance would upgrade.

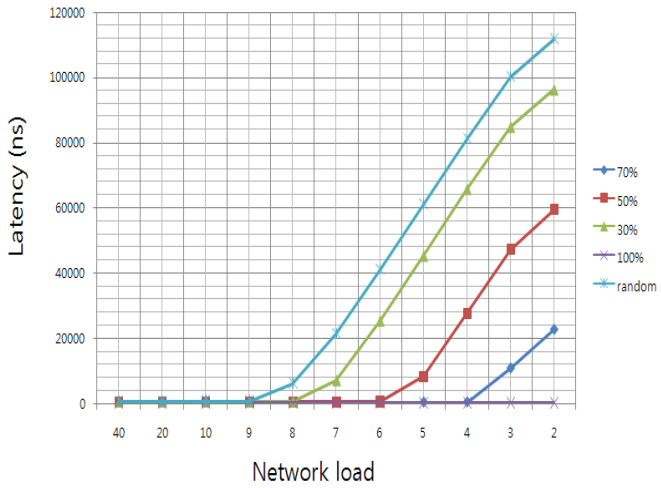

Figure 4. The average latency depending on the IP relation

B. 4-Channel H.264 Decoder

After modifying the JM reference standard source code into the scheduling of the increased parallelism, we described the TG schedule files to simulate the H.264 decoder internal module. We could get the ideal throughput to confirm the parallelism of the scheduling. Ideal throughput metric was got as value by supposing non network congestion and for evaluating the parallelism of the schedule. This throughput is 27.8Gbps. But this value is a non-achievable throughput. It is only the reference numerical value toward the maximum performance of NoC. The buffer size 10 for this simulation set up by the simulation result of the previous section. As considering the closeness between IPs, DMA and Memory were located at same star switch. Under these conditions, 4-channel H.264 decoder to be compromised as 48 internal modules got the performance of 14.1Gbps throughput. It is 50.7% of ideal throughput.

V. CONCLUSION

We achieved the performance evaluation about the random pattern and 4-channel H.264 Decoder with the SMT-NoC based on SystemC CLM to implement the structure of figure 2 and hardware-like as the cycle accuracy model. Through our work, we found the resistivity against the traffic load by using the closeness between IP. And we got the guide lines about the proper buffer size depending on the traffic load. Moreover, the performance of 4-channel H.264 decoder with the SMT-NoC could be predicted in advance.

ACKNOWLEDGMENT

This work was partly supported by the IT R&D program of IITA [2008-S-001-01, A Smart Eye based on Convergence SoC]

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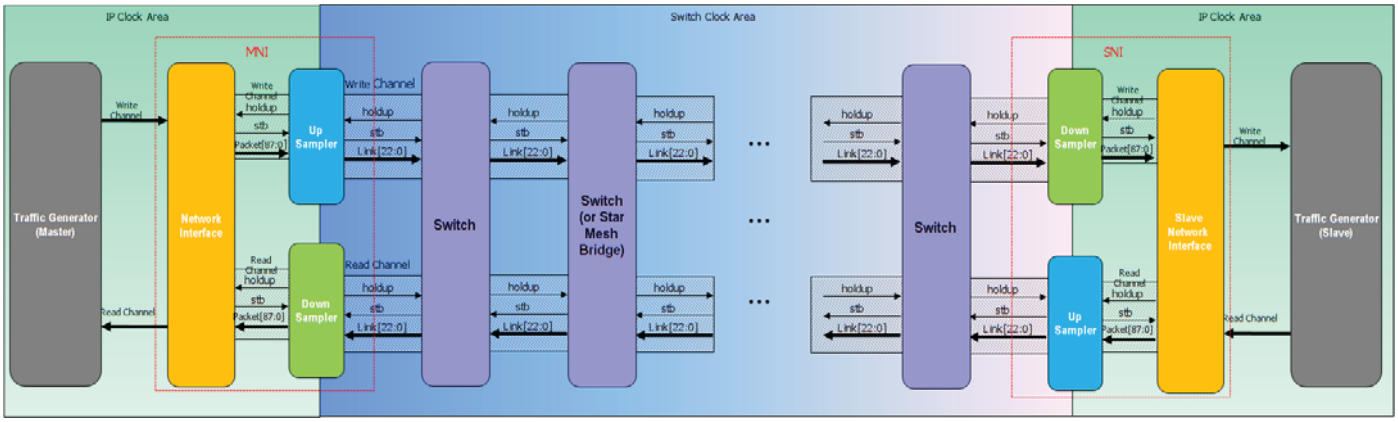

Figure 5. Interface of the SMT-NoC Components