Design Trade-offs in Energy Efficient NoC Architectures

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***Abstract*— This paper studies design trade-offs in energy efficient Networks-on-Chip by evaluating every network architecture that derives when we apply all possible variations of design-configuration parameters on a baseline 2D mesh. Network separation (P), concentration (C), express channels (X), flit widths (W), and virtual channels (V). Our comperative analysis selects the network architecture configuration that gives the best energy delay product (EDP) while allowing a maximum area margin of 15% over the most energy efficient configuration of the baseline.**

I. Introduction

Existing NoC schemes address the energy inefficiency at network architecture level and present important findings. However, they may appear to have conflicting results and limited design space (P, C, X) coverage. Psathakis et al. [1] address the later issue, and explore the architectural choices (P, C, X) by employing specific flit widths and virtual channel counts (W, V) to equalize the bisection bandwidth and input buffer storage. Although a fixed distribution of network resources implies a fairness among the evaluated NoCs, previous studies have also shown that W, V parameters may impose significant energy overheads when they are not properly optimized.

To this end, this work examines the design space through different perspective. It combines both the architectural variations (P, C, X) and configurations (W, V) on a baseline 2D mesh and selects the network architecture configuration that gives the best energy delay product (EDP) while allowing a maximum area margin of 15% over the most energy efficient configuration of the baseline.

We assume 64 processing elements (PEs) and use synthetic workloads that exhibit diverse communication behaviors with two corner cases of control to data packet ratios. We consider a homogeneous (HOM) and two forms of heterogeneous (HET1 and HET2) schemes[1] for network separation (P), concentration degree equal to 4 (C), 2-hop and 4-hop intervals for express physical channels (X), 4 flit widths (W), and 4 virtual channel counts (V).

II. Preliminaries

A typical system employs 3 message classes: request messages (read/write requests), intervention messages (forwarding/invalidation requests), and response messages (read/write replies). Thus, we can separate a single physical network (SPN) by: *(i)* two subnetworks where each carries all message classes (HOM), *(ii)* two subnetworks where each carries a subset of the message classes (HET1), and *(iii)* as many subnetworks as the total message classes (HET2).

Regarding the X parameter, we pick the EPN[2] scheme due to its scalability characteristics. In particular, the EPN maintains the maximum input/output router port growth constant (equal to 2) and independent of node count ($O(1)$). Moreover, bisection wires grow independently of node count ($O(1)$) and grow only by $\lfloor \frac{exp}{2} \rfloor + 1$ times, resulting in $O(exp)$ complexity.

We use the following convention in order to refer to any of the NoC architectures: We first place the C symbol if concentration applies, followed by the X2 or X4 symbol, if express physical channels apply, and finally HOM, HET1 or HET2, if separation applies, otherwise we place SPN.

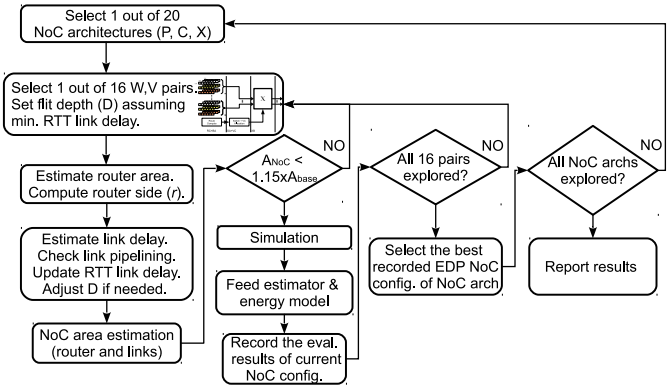

Fig. 1: Experimental methodology for 64 PEs.

III. Methodology

We consider tiled chip multiprocessors (CMP) with 64 tiles and map each tile on a single PE. We assume a $150mm^2$ die area, 45nm ITRS Low Standby Power device technology, an on-chip voltage of 1.1 V, and 2GHz clock frequency.

For router components, we assume a 3-stage input-buffered speculative router, equipped with credit based flow control, a 2-port register FIFO for buffer accesses, a DOR X-Y

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[1] Section II describes these schemes in detail.
[2] EPN [2] connects non-adjacent routers with express physical channels bypassing 3 routers using a 4-hop express interval (exp=4) on X or Y dimension. Our work also explores the exp=2 case.

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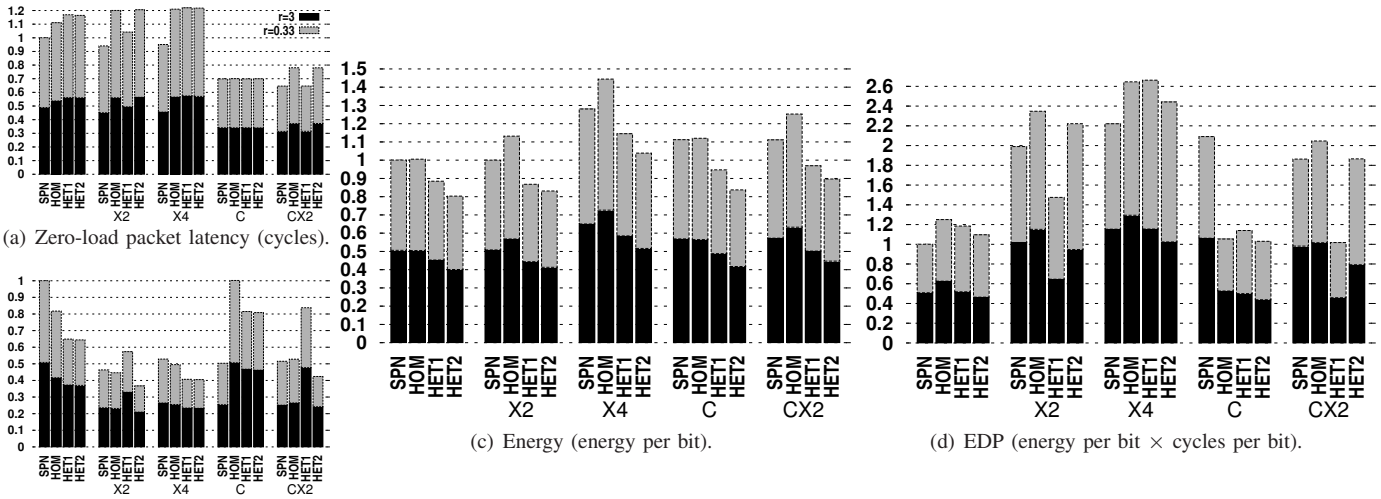

(a) Zero-load packet latency (cycles).

(b) Bandwidth (bits per cycle).

(c) Energy (energy per bit).

(d) EDP (energy per bit × cycles per bit).

Fig. 2: Performance and energy for 64 PEs.

algorithm for route computation, and a tree-based multiplexor for crossbar traversals.

Considering the links, we correlate the link length (l) with the side of die area (X), the express interval (exp), the number of PEs, the concentration degree (C), and the router side (r): $l = (X \times exp/\sqrt{PEs/C}) - r$. Whenever the l parameter exceeds a threshold, we insert a pipeline stage. We assume this threshold equal to $1.5mm$, because its delay[3] ($\sim 330ps$) meets the 2 GHz clock period ($500ps$).

We distinguish packet types as *control* (128 bits) and *data* (640 bits), and employ the $r_{c\backslash d}$ parameter to illustrate the ratio of control to data packet count. Control packets carry read/intervention requests and write replies. Data packets carry read replies and write requests. We set the $r_{c\backslash d}$ parameter according to traffic characterization results of previous efforts considering two corner cases: 3 data packets per control packet ($r_{c\backslash d}$=0.33) and 3 control packets per data packet ($r_{c\backslash d}$=3).

We use the cycle accurate simulator Booksim2 [4] and get the required statistics for performance and energy evaluation. We estimate the energy by feeding the Orion3 [5] and our NoC model with the Booksim2 statistics. We implement HET1, HET2, and EPN schemes in Booksim2 and extend Orion3 with our custom[4] link pipelining model. Regarding the fact that a NoC often operates under low loads, we derive the simulator statistics when the NoC operates at twice its zero-load latency, similar to previous efforts' methodology [6, 7].

Our synthetic workload mix consists of four traffic patterns: uniform, neighbor, bit complement, and transpose. We picked this traffic mix to ensure diverse communication behaviors and avoid biasing the workload in favor of one topology.

When our methodology procedure begins, we first set the baseline area reference point by evaluating all 16 configurations (W,V) and select the one with the best EDP. Detailed steps of our methodology are depicted in Fig. 1.

[3]45nm ITRS-LSTP with 30% wire delay overhead (CACTI [3])

[4]Derived empirically through post-PnR simulations of piped/non-piped wires for 65, 90, 130, and 180 nm, and then projecting for 45nm.

IV. Results

Our results (Fig. 2) indicate that for 64 PEs, the baseline provides the highest energy efficiency. Although the C-{HOM, HET2} and CX2-HET2 show comparable EDP, the baseline is still sufficient. Considering the energy savings, the HET2 separation scheme combined with either concentration or express physical links of an interval equal to 2, offers 16% energy savings and the exclusive use of HET2 scheme results in 20% energy savings. We also observe the load imbalance (as control to data packet ratio decreases) of heterogeneous architectures, worsen the energy efficiency by ∼30%. In terms of performance, concentration combined with express physical channels of an interval equal to 2, using either the HET1 scheme or not, improves 35% the latency whereas, the baseline is sufficient in order to maintain high bandwidth at low loads.

Acknowledgment

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