Mesh-Star Hybrid NoC Architecture with CDMA Switch

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***Abstract*—The Network-on-Chip (NoC) concept has been proposed to replace conventional bus-based system architectures to create scalable and flexible future SoC designs. A 2D-mesh topology is one of the most frequently mentioned topologies for an NoC design due to its natural layout mapping onto an SoC. However, the 2D-mesh topology NoC has a hot-spot problem at the center of the network and presents difficulties in multicasting. In this paper, we propose a novel multicastable CDMA switch and an efficient mesh-star hybrid topology. This approach leads to reduced traffic at the center of the network and better performance with multicasting. Our switch has been synthesized using a 0.13*μm* CMOS technology library.**

I. INTRODUCTION

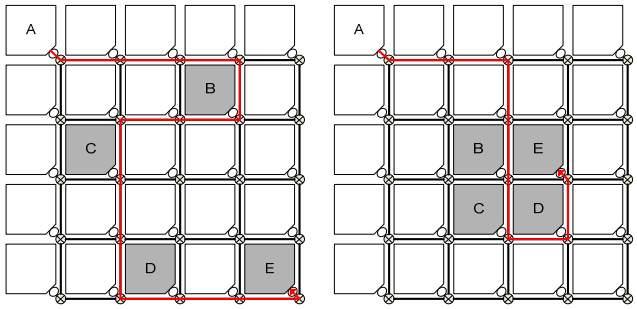
As ITRS reported, gate delay is decreasing as technology scales but global wire delay is increasing exponentially [1]. Network-on-Chip (NoC) concepts have emerged to resolve the limitations of conventional bus-based systems in terms of scalability and high throughput requirements. Recently, many researchers have proposed a variety of NoC structures [2, 3, 4]. In NoCs, processing elements (PEs) such as CPU, DSP, I/Os, ASICs and memories are interconnected by switches based on specific topologies and communicate by routing packets.

In spite of the disadvantages of buses, they do provide for multicasting in a natural way. Many applications require support for multicasting, such as sending a global command message to a group of processing elements or implementing a cache coherency protocol.

The 2D-mesh topology is one of the most frequently considered NoC topologies because of its direct mapping and layout onto a chip [5]. However, applying multicasting concepts to a 2D-mesh network poses challenges. Researchers have proposed multicasting methods for a 2D-mesh network but with the primary focus being the avoidance of deadlock [6]. Also, Code Division Multiple Access (CDMA)-based NoC techniques have been introduced but the conventional CDMA switch does not support multicasting and cannot be directly connected to a 2D mesh network [7].

In this paper, we propose a novel multicastable CDMA switch and an efficient mesh-star hybrid architecture for NoCs.

II. A CONVENTIONAL MULTICASTIG CONCEPT IN 2D MESH NETWORK



(a) without grouping (b) with grouping

Figure 1. Example of basic multicasting on a 2D-mesh NoC.

Fig. 1 (a) shows the basic concept of multicasting in a 5x5 2D-mesh network. Assume that PE A has a packet to be delivered to PEs B, C, D and E. Without the support of multicasting, PE A must unicast the same packet to each destination four times. This series unicasting of the same packet will increase both network traffic and the chances of contention. A basic multicasting method shown in Fig. 1 (a) is for PE A to first transmit a packet to PE B. Once the packet is received by PE B then PE B retransmits the packet to PE C. Continuing in this fashion, the packet is delivered to PE D and finally to PE E. Compared to series unicasting, this method will reduce network traffic. However, the packet still has a long distance to travel from the source PE to the final destination PE. Of course, an appropriate routing algorithm has to be applied to prevent deadlock and to increase the efficiency of the network. Another, problem is that the packet is not delivered to all destinations at the same time. If the packet is real-time data and requires time-sensitive processing then these different arrival times could pose a significant difficulty at the system level.

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Fig. 1 (b) illustrates that PEs B, C, D and E are placed closer together at the center of the network and PE A is multicasting a packet to the group of PEs. As can be seen from Fig. 1, we can reduce the total multicasting hop count by placing the multicasting destinations closer. Therefore, if frequent multicasting to a group is required then it is better to place the PEs in the group closer to each other. Also, in many applications, we may have several PEs which communicate with each other more frequently than with other PEs, such as a processor and cache memories. Therefore, if there is a higher probability of communication between some specific PEs, we can reduce network traffic by placing those PEs closer to each other. However, if we place the frequently communicating group at the center of the network then their frequent communication would increase the chances for contention because the traffic load at the center of an ordinary mesh network is much higher than average. If we place the group at the corner of the 2D-mesh network then we would reduce this problem. However, in that case the hop count to the farthest PE will increase.

III. IMPREMENTATION OF THE PROPOSED SWITCH

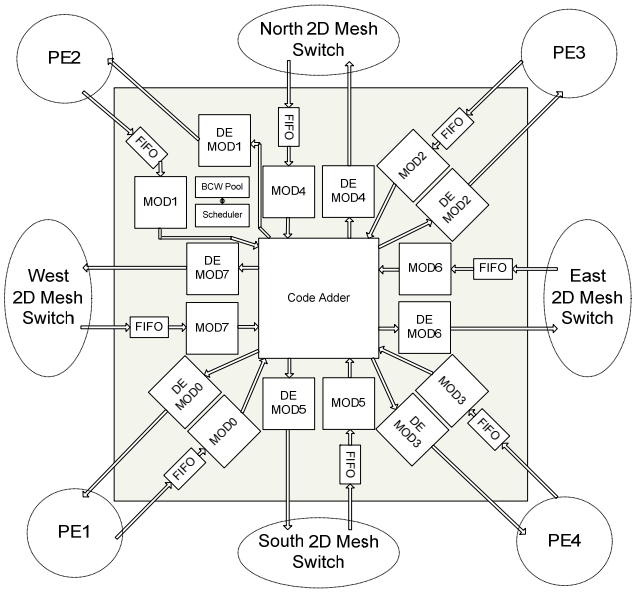

Figure 2. Block diagram of the proposed switch.

The proposed switch uses CDMA techniques rather then conventional MUX-based switches. Fig. 2 shows the block diagram of the proposed switch. Eight modulator and demodulator sets are connected through the code adder. Four modulators and demodulators are connected to each other through conventional 2D-mesh switches. The other four modulators and demodulators are connected to four PEs. A packet can be delivered to one PE or to multiple PEs which are connected to this switch. Any PEs which are directly linked by this switch can unicast or multicast a packet to each other. Binary Walsh codes are used for this switch.

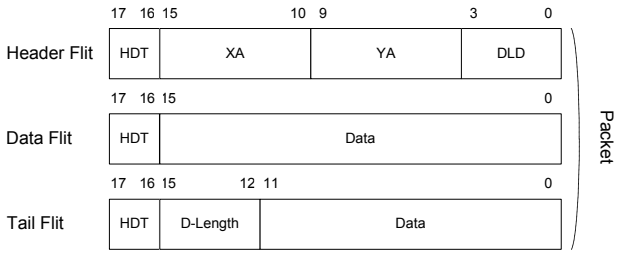

Figure 3. Flit based packet format for the network.

A. Packet format

In the network, we apply the wormhole concept and design the proposed switch with a 16-bit data field which is extendable, if needed. Wormhole routing splits a packet into smaller units which are called flits. Fig. 3 shows the flit formats. A two-bit Header-Data-Tail (HDT) field within each flit represents the type of the flit: "01" for header flit, "11" for data flit, "10" for tail flit, and "00" for idle. The XY routing algorithm is applied for the 2D-mesh part of the network, where XA and YA represent the X-Address and Y-Address, respectively. Each switch in the network has its own XA and YA. For example, the switch which is located at the top-left of a 5x5 2D-mesh has (1, 1) for its address, whereas (5, 5) is the address of the switch at the bottom right. For the conventional 2D-mesh switch which is connected in the network, a packet is delivered to the next switch based on the values of XA and YA. If XA and YA match those for the switch then the packet is sent to the PE which is connected to the switch. The DLD field represents the destination-local-demodulator address which is used in the proposed CDMA switch. If a packet is received by the switch and the XA and YA match those of the switch then the received packet is delivered to a PE or PEs based on the DLD field of the header flit. If the header flit of a packet is received then a codeword is assigned by the scheduler. The data flits all use the same assigned codeword; once the tail flit has been received then the scheduler will return that codeword to the codeword pool. The D-Length field in the tail flit is an optional field which points to the last effective data bit in the tail flit.

B. Scheduling

Once a modulator receives a header flit then it requests codeword assignment from the scheduler block. The codewords in Fig. 4 are stored in the codeword pool which has a FIFO-like structure. A codeword is assigned by the following process.

- Check the XA, YA and DLD fields of the received header.
- Check for contention.
- Read a codeword from the codeword pool.
- Set Input Codeword Assignment Table (ICWAT).
- Based on ICWAT, set Output Codeword Assignment Table (OCWAT).

$$Codeword = \begin{bmatrix} 00000000 \\ 01010101 \\ 00110011 \\ 01100110 \\ 00001111 \\ 01011010 \\ 00111100 \\ 01101001 \end{bmatrix}$$

Figure 4. Walsh codewords.

If XA and YA match those of the switch, the DLD field of the received header is stored to the Destination Local Demodulator Register (DLDR) in the ICWAT if no contention exists. Each bit of DLDR represents a destination demodulator. Therefore, if the DLDR for modulator 0 (DLDR0) is "00000010" then PE1 is transmitting a packet to PE2. Similarly, "00001110" would be placed in DLDR0 when PE1 is multicasting a packet to PE2, PE3 and PE4. If XA or YA of the received packet is not same as that of the switch it means that the packet needs to be sent to another switch. In such a case, the scheduler sets DLDR based on Table I.

TABLE I. DLDR MAPPING.

Address Comparison	DLDR value in ICWAT
S_XA > RH_XA	"100000000" (To West)
S_XA < RH_XA	"01000000" (To East)
S_YA > RH_YA	"00010000" (To North)
S_YA < RH_YA	"00100000" (To South)
S_XA = RH_XA S_YA = RH_YA	Based on DLD field of the received header flit

Note 1: S_XA, S_YA: XA, YA are those assigned to the switch.

Note 2: RH_XA, RH_YA: XA, YA are those of received header flit

Table II shows an example setting of the ICWAT and OCWAT. PE1 is multicasting data to PE3 and PE4 using codeword "01010101". A packet from the north port is multicast to PE1 and PE2. A packet from the west port is delivered to the south port. The valid (V) bit in OCWAT is set based on the DLDR of ICWAT. Demodulators are in the idle mode until this bit is set to '1'. The same codeword is assigned for the source modulator and destination demodulator. Therefore, the codeword that is assigned to modulator 4, which is connected to the north port, is the same as the codeword that is assigned to demodulators 0 and 1, which are connected to PE1 and PE2, respectively.

The DLDR and V-bit are cleared and the assigned codeword is returned to the codeword pool when the tale flit is received.

TABLE II. EXAMPLE SETTING OF ICWAT AND OCWAT.

MOD Num	ICWAT		OCWAT		*DMOD Num*
	DLDR	*Codeword*	*V*	*Codeword*	
0	00001100	01010101	1	00110011	0
1	00000000	00000000	1	00110011	1
2	00000000	00000000	1	01010101	2
3	00000000	00000000	1	01010101	3
4	00000011	00110011	0	-	4
5	00000000	00000000	1	01100110	5
6	00000000	00000000	0	-	6
7	00100000	01100110	0	-	7

C. Modulation and Demodulation

Once a header flit is received and the codeword is assigned then the modulator modulates each data bit of the packet based on the algorithm of Table III.

TABLE III. MODULATION ALGORITHM.

Input bit of a packet	Modulated data
0	Codeword itself
1	Inverted codeword

The modulated data from each modulator are sent to the code adder block where they are summed. The summed data are sent to all of the demodulators. The equations for the decision factor λ, which is calculated at each demodulator, are:

$$D[i] = \begin{cases} (2S[i] - L) \text{ if codeword[i] is 0} \\ (L - 2S[i]) \text{ if codeword[i] is 1} \end{cases} \quad (1)$$

$$\lambda = \sum_{i=0}^{L-1} \frac{D[i]}{L} \quad (2)$$

where L is the codeword length, $S[i]$ is the sum of the modulated values at codeword bit position i, $D[i]$ is the decision variable at codeword bit position i and λ is the decision factor.

If the V-bit is set to '1' then the demodulator is activated and calculates the λ value based on the assigned codeword in the OCWAT. Otherwise, the demodulator is in an idle mode so as to save power. The demodulator extracts the original data based on the λ value, as shown in Table IV.

TABLE IV. DEMODULATION ALGORITHM.

V-bit	λ Value	Demodulated data bit
1	+1	1
1	-1	0
0	-	No received data

IV. MESH- STAR HYBRID NOC

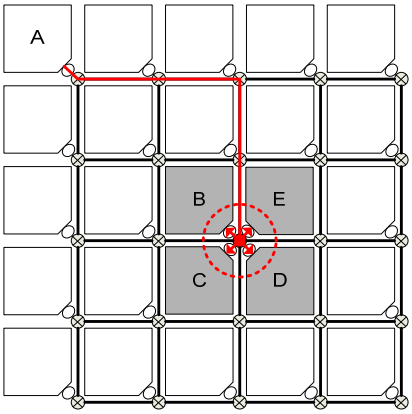

Figure 5. 5x5 2D mesh-star hybrid NoC.

Fig. 5 illustrates a multicasting example in the mesh-star hybrid NoC. We placed the CDMA switch inside of the dashed circle. Four PEs, B, C, D and E, are directly connected by the switch. Also, four conventional 2D-mesh switches are linked through the switch. One benefit of this architecture is that links are not utilized when PEs that are directly connected to the switch are communicating with each other, freeing them up for other traffic. This can lessen the hot spot problem at the center of the network. Another benefit is that it can reduce the multicasting hop count. Comparing Fig. 1 (b) and Fig. 5, we can see that the PEs in gray are at the same positions. However, the PEs in Fig. 5 have a reduced multicasting hop count, which increases network efficiency. Also, the multicasting data is delivered at the same time at the destinations, which is important in real-time or time-sensitive applications.

V. RESULTS

A. Comparison results.

TABLE V. COMPERISON BETWEEN 2D-MESH AND HYBRID NOC.

	2D Mesh	2D Mesh-Star Hybrid	% improved
Min hop in group	2	1	50 %
Max hop in group	3	1	67 %
Min hop to the most far PE from the group	7	5	29 %
Min total hop for multicasting from the most close PE which is located out of the group	5	2	60 %
Min total hop for multicasting from the most far PE which is located out of the group	8	5	38 %
Occupy link during the communication within group	Yes	No	-
Multicasting data arrive at the same time to the group	No	Yes	-

Table V compares Fig. 1 (b) with Fig. 5. As can be seen from the table, we can minimize the hop count and reduce network traffic by using the proposed switch. Here we use only one CDMA switch; however, if it is required, we can include several CDMA switches in an NoC. Also, we can increase or decrease the number of PEs which are directly connected to the switch based on the requirements of an application.

B. Synthesis results.

TABLE VI. SYNTHESIS RESULTS.

Slack met for	500 MHz Clock
Combinational area	261,392 μm^2
Non-combinational area	68,595 μm^2
Total cell area	329,987 μm^2
Total dynamic power	78.2 mW
Cell leakage power	78.3 µW

A UMC 0.13μm CMOS technology high-speed ASIC library was used for logic synthesis. The synthesis results for our proposed switch are presented in Table VI.

VI. CONCLUSIONS

In this paper, we have presented a novel multicastable CDMA-based switch and associated hybrid NoC based on the 2D-mesh and star topologies. The proposed switch connects 4 PEs and 4 links. The switch can unicast and multicast data between the PEs which are directly connected to it. Also, the switch can unicast and multicast packets from other conventional 2D-mesh switches into the group. This approach can mitigate the hot spot problem of the network and increase network efficiency. The switch has been designed and synthesized using a 0.13μm high-speed ASIC technology library.

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