A case study of application specific NoC design

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***Abstract*—Network-on-chip (NoC) is emerging as an effective architecture which address the shortcomings of traditional bus-based System-on-chip (SoC). NoC has been under investigation for several years and many different architecture and various protocols have been proposed. However, compared to the general -purpose NoC, the methodology to design application specific NoC provides greater practical insight. In this paper, we present the design process of application specific NoC. According to this design flow, we design a 4×4 2D mesh platform and give the result of the specific NoC mapped with a OFDM receiver application.**

Keywords-Network-on-chip; application specific NoC; 2D mesh; OFDM receiver

I. INTRODUCTION

With the rapid development of system integration and process technology of IC, the communication architecture among various modules has become the key problem to guarantee the whole system performance. The traditional bus architecture of SoC has several problems seriously restricting the average communication efficiency, such as the huge clock tree, the high power consumption and the limited scalability. NoC based on network connection can solve the bottleneck problems of SoC based on bus. NoC architecture can contain a large amount of IP cores, supporting various applications. And its low power consumption, small size and the flexible characteristics make NoC very feasible and applicable to be used in future mobile terminal [4] and 4G communication system [8].

As a technology for the high data-rate wireless communication, the OFDM is the outstanding technology. The frequency selective characteristic enables the robust communication in the multi-path fading wireless channel. It is considered as the main candidates for the high speed next generation wireless communication. These communication systems will bring a large number of processors, memories and accelerator cores to support evolving standards and new applications. Computation and communication complexity are skyrocketing. Therefore, the heterogeneous nature of on-chip cores, and the energy efficiency requirements typical of future wireless communications call for application specific NoC which can eliminate much of the overheads. However, application specific NoC must be supported by adequate design flow to reduce design time and effort.

In our work, we survey the main challenges in application specific NoC design, and analyze and examine the design flow of application specific NoC. This can guides the methodology to design the system on a NoC simulation platform. We select the target application as OFDM receiver, which is important in the future wireless communication system. Our platform embraces the communication architecture and the computing resources, which include 17 IP cores, such as MIMO decoding, channel estimation, RX buffer, and etc. Under the accurate task scheduling, these IP cores can complete the OFDM modulation effectively and efficiency. The communication architecture is a 2D mesh NoC including 17 nodes.

The rest of this work is as follows: in section 2, the general design flow of application specific NoC is introduced and analyzed. In section 3, the 2D mesh NoC is designed and synthesized. In section 4, the target system is mapped and the power evaluation is presented. Our conclusion will be drawn in section 5.

II. DESIGN FLOW OF APPLICATION SPECIFIC NOC

The design flow of application specific NoC describes how to obtain the final SoC from the particular application and design objective, which meets the customer requirements [1]. The complete design process consists of three steps, as Fig1, which are architecture design, RTL description and system implementation.

Architecture design is the design of the topology or structure of the network and setting of various design parameters (such as frequency of operation or link-width).The key problem of this first step is the selection of topology. Several early works favored the use of standard topologies under the assumption that the wires can be well structured in such topologies [2]. These approaches are adequate for the homogeneous or traffic predictable systems, such as the general multi-processor system on chip. However, in the heterogeneous systems, the IP cores have different sizes, unbalanced traffic distributions and unpredictable flows. Thus, standard topologies can poorly matches the specific application requirements. Therefore, the optimization model is needed to realize the customized topology or the structure for heterogeneous SoC. Moreover, we need to determine the parameter and communication protocols of NoC, including switching mechanism, routing algorithm, flow control mechanism [6] and so on.

The main task of intermediate design phase is to complete the RTL description of the communication architecture designed in the first step. SystemC, VHDL and Verilog can be used in the RTL description step, which can simulate in the

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behavior level and verify the connection structure, confirming the correctness in the first step design.

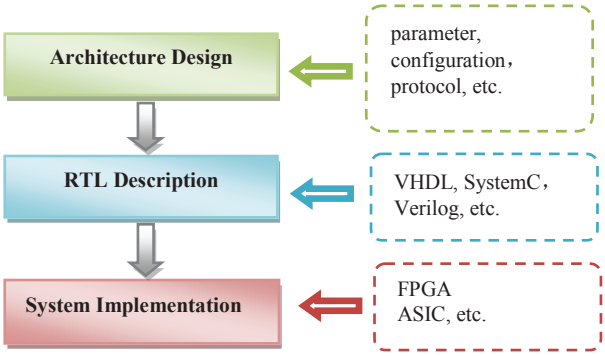

Figure.1 Design flow of application specific NoC

The last step is system implementation, which realize and convert the hardware description language documents into actual system on chip in FPGA or ASIC [3]. The functional verifications and tests in the system level are completed in the final step.

According to the characteristics in our target system, we have simplified the first design phase. The architecture in our work adopts 2D mesh topology, wormhole switching and XY routing algorithm. The detailed consideration will be discussed in the section 4.

In the following section, we will describe the NoC architecture design in our work, especially the router structure and the method to connect the IP cores.

III. 2D MESH PLATFORM

A. ROUTER

After determining the parameters and the communication protocols, we divide the NoC router as nine functional modules, shown as the Fig2: input buffer (Ibuffer) , input flow control (IFC), head decoder (HD), routing computation (RC), virtual channel arbitration (VA), switch arbitration (SA), control logic(CL), output flow control (OFC) and crossbar:

Ibuffer: Store the coming flit to prevent the packet loss when there is congestion;

IFC: Build a table conserving the present usage status of every virtual channel; inform the previous nodes the timing to send flits, in case the sending rate surpasses the processing rate.

TABLE I PARAMETERS OF THE 2D MESH PLATFORM

topology	switching	routing algorithm	flow control	radix	number of vc	depth of vc
2Dmesh	wormhole	XY	hand-shake	5	4/port	8flit/vc

HD: Detect the request type and transfer it to the CL module, decode the address information in head flits and send the routing request to the RC module.

RC: Complete the routing computation with the XY algorithm and send the result to the CL and VA.

VA: Allocate an available virtual channel to every request with round-robin scheme.

SA: Arbitrate the competition of different requests and allocate the switch to a certain request in every present clock.

CL: Build a table conserving path information-the output port and the next virtual channel, guarantee body flits and tail flits can be forwarded through their accurate paths.

OFC: Send the forwarding request to IFC module to get the usage status of virtual channels.

Crossbar: Set the switch with the configuration information from SA module and forward the present flit

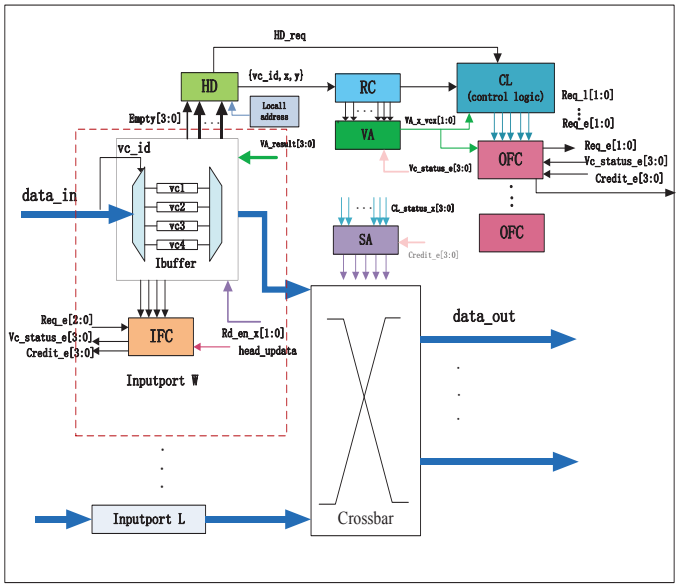

Figure.2 Diagram of the router

B. 4×4 2D mesh platform

With 16 instantiations of the above NoC router， we respectively connect the corresponding data wires and the control wires into a 4×4 mesh platform. The addressing scheme and the interconnection method is shown in Fig3. The red solid lines represent the input data and the output data between adjacent routers. The lines in other colors are the control wires, exchanging the interconnection signals. The black solid lines are the data wires between routers and their IP cores.

We use the ISE FPGA design kits to simulate and synthesize our NoC platform. The Simulation results assure the NoC connection architecture can correctly and efficiently forward the packets from their source to the destination. With the XST tools, we get the synthesis reports showing the resource consumption. The router spends 6087 registers and 8542 LUT units, which are 6% and 4% of a Xilinx V-5 FPGA chip. Its maximum frequency is 163MHz. The 2D mesh platform spends 75314 registers and106202 LUT units which

take up 61% and 88% chip resource of a Xilinx V-5 FPGA chip and the maximum frequency is 152.5MHz.

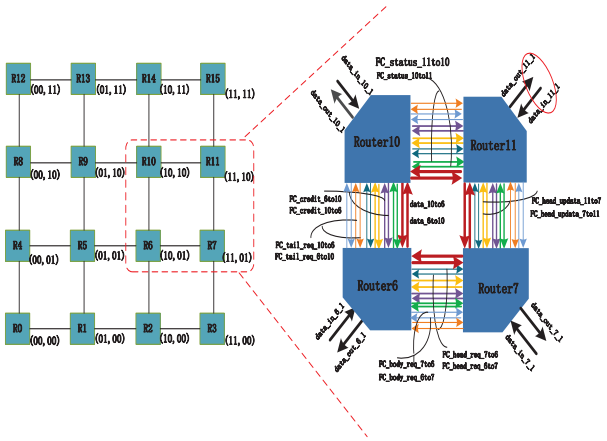

Figure.3 2D mesh platform

IV. OFDM RECEICER BASED ON 2D MESH ARCHITECTURE

The future wireless systems firstly require the high data transmission speed, as well as guarantying the quality of service. Thus, the demodulation technology should have a high cell rate and a long period. With such requirements and consideration, Orthogonal Frequency Division Multiplexing (OFDM) becomes an important technology in 4G communication system. OFDM technology is fit for high-speed transmission, which can achieve a high Spectrum efficiency, have the outstanding InterSymbol Interference (ISI) characteristic and can combat delay dispersion and multipath fading.

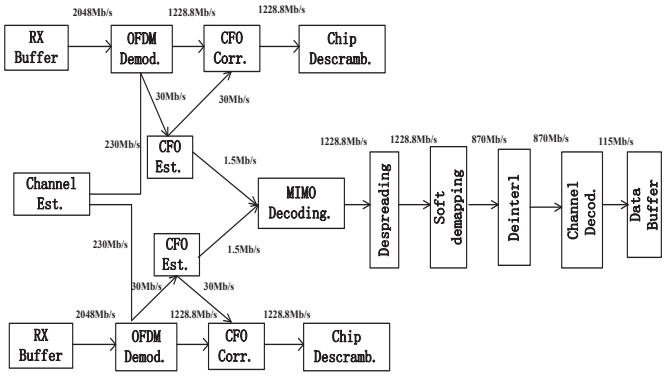

Figure.4 Core-graph for the OFDM receiver

In the 80s, with the developments of electronic technology and the very large scale integration (VLSI), OFDM technology enters a new period and finally be applied in the high speed modem. Further, in the 90s, OFDM is developed into a essential technology in the advanced wireless communication, which is being widely used in video, broadcast and civil communication system, such as ADSL, DAB with ETS standard, HDTV and WLAN.

The core graph of OFDM receiver is shown in Fig.4 [7]. Although it looks like the OFDM receiver is executed sequentially, when it is mapped in our NoC platform, the control and configuration signals, memory access signals and reconfigurable IP cores can be executed in parallel. Therefore, the latency will decrease and the overall throughput will increase by a large amount.

Our target system has some specific characteristics, which can simplify the first step of design flow of application specific NoC and decide the basic protocols in our architecture:

a. Most of the modules mainly communicate with few neighbors, and traffic is principally local except for control. In consequence, the network doesn't need a high order topology. A 2D mesh topology is sufficient and has been implemented for this study.

b. The IP cores are specialized and the traffic is rather predictable and data-independent, so a deterministic routing algorithm is appropriate.

c. Communications are often burst and short. So packet switching is preferable to circuit-switching since no connection time is needed, which is time-consuming. We use wormhole switching mechanism with low latency.

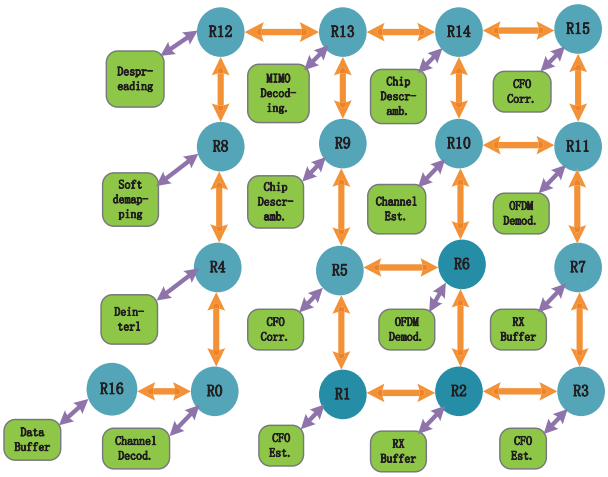

Figure.5 OFDM receiver base on the NoC architecture

In addition to the topology, the routing algorithm and the other basic communication protocols, the mapping algorithm can impact the system greatly. A poor mapping algorithm would generate hot spots in the center of network, which can deteriorate the whole performance and reliabilityof the NoC system, especially in the mesh topology network. Therefore, we aim at the traffic balance and use the artificial fish swarm algorithm [5]to map the OFDM receiver into a 2D mesh NoC. The mapping result is shown in Fig.5. According to the specific traffic characteristics between each pair of nodes, we trim off the unused wires and shut down the idle ports, which can further reduce the power consumption, chip area and other hardware resources. After the optimization process, we have the traffic distribution result, as shown in Fig.6. Our OFDM

receiver based on 2D mesh topology consumes 184.7011mJ with no hot spots.

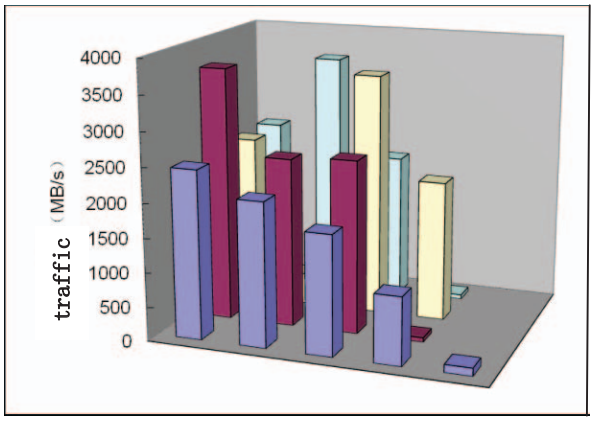

Figure. 6 Spatial traffic distribution

V. CONCLUSION

In this paper, we have presented the design flow of application specific NoC. According to this process, we design an OFDM receiver based on 2D mesh connection architecture.

First, we analyze the requirements and the communication characteristics to design the basic parameters and principle protocols, such as topology, routing algorithm, switch mechanism and the flow control mechanism. In our target system, we design a 2D mesh NoC with XY routing algorithm and wormhole mechanism.

Second, we choose the Verilog language to complete the intermediate design phase---RTL description of the communication architecture. In this paper, we present the router structure and the interconnection method to constitute an entire 2D mesh NoC platform. Further, we use the artificial fish swarm algorithm to map the OFSM receiver into the NoC platform. At last, we test and verify the application specific NoC target the OFDM receive and evaluate the power and resource consumption.

In the future, we will complete the system implementation using FPGA chips, verify the functional accuracy and test the system performance under actual traffic, taking the wire delay and power consumption into account.

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