

Performance Analysis of 16×16 , 32×32 , 64×64 2-D Mesh Topologies for Network on Chip

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Abstract—Network on Chip (NoC) is an up-coming worldview that adapts to the expanding many-sided quality and correspondence prerequisite of future System on Chip (SoC). Numerous topologies with various capacities have been proposed for NoCs, various topologies and parameters are chosen based on different NoC applications. In this paper, we have modeled the Mesh topology for 4×4 and 8×8 , 16×16 , 32×32 , 64×64 nodes for varying packets size (0.1 and 16000 kB), queue size (5–200), link bandwidth (10–200 Mbps), link propagation delay (10–200 ms), over CBR (5 and 10 Mbps) and FTP applications. The performance of throughput and propagation delay of packets from given source node to destination node is studied for low (0.512 kB) and high load (64 kB) applications. Point by point similar investigation of the reproduction brings about terms of latency and throughput are displayed. The outcomes can be utilized as a rule for NoC architects to settle on fitting decisions keeping in mind the end goal to accomplish ideal execution for respective applications of future wireless communications systems is to provide sensor data transmission high-data-rate, quality of service (QoS), low cost, speed of wireless access. Multiple-input multipleoutput (MIMO) wireless technology meet these demands spectral efficiency, and improved link reliability.

Index Terms—NoC (Network on Chip), SoC (System on Chip), Mesh Topology, Verification, MIMO.

I. INTRODUCTION

Tremendous developments in VLSI technology as per International Technology and Roadmap for Semi-conductors (ITRS), the Integrated Circuit (IC) productions organizations started producing single silicon chips with thousand billion integrated transistors each, utilizing nano-meter design [1]. This allows integration of thousands of homogenous and heterogeneous parts together to give full usefulness of an application on a single chip called System on Chip (SoC). When there are thousands of homogenous or heterogeneous Intellectual Property (IPs), the communication between various IP blocks become the focus of designing high performance and reliable SoC [2], [3]. With great deal of IPs, the bus and point-to-point technology; clearly it'll cause a high value, as well as interconnect delay, power consumption and traffic collision. Likewise conventional transport based interconnect structures can't scale adequately past a specific number of imparting assets, consequently, turning into a bottleneck toward the billion transistor chip [2]. To adapt to the wastefulness of

transports, VLSI analysts, concocted a novel packet based interconnect design for future SoCs—Network on Chip (NoC). The thinking is to relate various resources on a chip through a framework where correspondence happens using groups rather than interfacing the advantages by method for dedicated wires.

MIMO utilizes various radio wires at both the transmitter and receiver to enhance the correspondence execution in remote systems. MIMO innovation has pulled in consideration in WC, in light of the fact that it offers critical increments in information throughput and connection extend without extra data transmission or transmit control. It accomplishes this by higher unearthly productivity (more bits every second per hertz of data transfer capacity) and connection unwavering quality or differing qualities (lessened blurring). As a result of these properties, MIMO is flow subject of global remote research. In this paper concentrating on outline of remote systems utilizing network topology. That is execution usin Noc Platform. Here presented work topologies for MIMO application.

NoC has been proposed as a highly structured and scalable solution to address communication problems in SoC. On chip interconnection network provides advantages over dedicated wiring and buses, i.e. low-latency, low-power consumption and scalability. Each resource should be contacted to a switch in the network via a network interface (NI). More topologies have been discussed for this switch network includes 2D Mesh, Folded Torus, Ring, Butterfly Fat Tree, Octagon and irregular connection net-works. The most of place efficient ones on a 2D Mesh and binary tree [4]. There is favorable position in work topology [7] as it has its own particular manner of steering called source directing. This component in this topology gives a proficient encoding of way data with just few bits. Obviously every jump is adequately encoded with just two bits. As the bundle which is entering the switch is sustained with a pre-characterized choice about the goal port, outlining of switch is made fundamentally basic. Since the header is made with just couple of bits, the plan is basic and additionally the system not reliant with the size.

This paper organized to first section introduction of MIMO, NoC, Second section discuss the state of art NoC technology, and third section modeling of the proposed mesh topology, introduced different mesh topologies, discuss the results

analysis. At last fourth stage is the discussion and conclusion of proposed system.

II. LITERATURE SURVEY AND STATE OF THE ART IN NoC

Some related works for the parking space management system based on wireless sensor networks are reviewed in this.

A. Topology Methodologies

Many researchers are found proposing demonstration of NoC in simulating environment in analytical and simulation based model in 2 & 3-dimensions for various types of topologies like as mentioned above. Topologies such as mesh, torus, octagon, SPIN, BFT etc. were analyzed for performance i.e. delay parameters [25]. Source directing i.e. the source hub decides just its neighboring hubs that are included in message conveyance is utilized for work topology. For the situation of Octagon, embrace the various leveled address-based directing. BFT, CLICHE, and Folded Torus give bring down throughput than SPIN and Octagon. The 2D work and 2D torus interconnection systems has been assessed, where they actualized both with and without affirmation instrument and parcels has been sent utilizing uniform movement design. Comes about demonstrate that, the torus has a decent execution and quick when affirmation instrument is utilized and work perform better when without affirmation component is utilized [26], [28].

Facilitate, structures on these topologies are homogenous and heterogeneous in nature which depend on customization and parameterization abilities implanted in it, wherein the vast majority of the NoC bolster homogenous models which can be tweaked each time according to the application necessity and is more proficient in term of region, power, latency. NoC recreation and assessment stage permitting planners to reenact and assess the NoC execution with various system arrangement parameters. The proposed stage has been actualized in System to be effectively adjusted with a specific end goal to adjust distinctive reenactment procedures and spare the reproduction time. The switch task based plan strategy is utilized for situation of processing elements (PE) on first layers and their limited association with the switches is put on the second layer. Ikki Fujiwara et al [24], presented execution corruption by deactivated centers in 2-D Mesh NoCs [6], [23]. The impacts of deactivated centers on the execution of the system on-chips (NoCs) intensive cycle-exact system reproductions. It is cleared up that the area of the deactivated center emphatically influences the dormancy and the throughput. Organize on Chip (NoC) speaks to a promising arrangement as interconnect for MPSoC Systems. A great deal of research has been led on NoC plan, in any case, more work is required as far as down to earth configuration issues. They talked about the proposition to the future many center NoC structures utilized by star, various leveled star, and fat-tree arrange topologies and huge size switches. Their NoC arrangement utilizes the measurement arrange directing XYZ, wormhole exchanging, and input virtual channels lining. They have blended the RTL model of the switch design utilizing FPGA Xilinx XC3S1600E. They

have additionally tried the composed switch on account of topology 3D-work ($n \times n \times n$) and think about it against a ($n \times n$) 2D outline [27], [34], [44].

B. Routing Architectures and Related Research

Once the architecture is decided the routing architecture plays important role of implementing functionality of simple switching to intelligent routing. The switching techniques are classified based on network characteristics. There are two types of switching i.e. circuit switching which reserve path and packets switching which established path while traversing. The bundle exchanging is named wormhole, store and forward and virtual slice through exchanging. For circuit exchanging systems, switches are planned with no buffering while bundle switch arranges some buffering is required as the information is full bosomed. Wang zhang et al proposed engineering of 2 dimensional work topology, planned with Odd-Even (OE) directing calculation [14]. Routing can be centralized, source, distributed or multiphase which are usually implemented lookup table or finite state machines. The implementation can be altered from deterministic approach for adaptability depends on the runtime situations of networks. Assessment comes about demonstrate that source directing gives higher dormancy and throughput execution when contrasted with comparing disseminated routing [15], [21], introduced a novel low dormancy, high throughput and blame tolerant 3D-Network on-Chip, steering calculation named Look Ahead Fault Tolerant directing calculation (LAFT). They executed the proposed calculation on a genuine 3D-NoC engineering (3D-OASIS-NoC) which has demonstrated great execution, versatility and robustness, conclude that our proposed calculation effectively gives adaptation to internal failure and elite at a sensible, low equipment cost.

C. Flow Control and Link Management

Flow control determines how arrange assets like channel transfer speed, cushion limit and control state are assigned to bundle navigating over system. The cushioned stream control has a few variations like credit based stream, handshaking signal, recognize stream control, slow down/go stream control and T-mistake stream control. Umamaheswari S et al, proposed runtime cushion administration to enhance the execution in unpredictable Network-on-Chip design. The sporadic work NoC where a few connections might be broken or a few switches might be missing. A versatile directing calculation is utilized to course the parcels dependably to any piece of the unpredictable work NoC [2], [8], [12]. One can find congestion avoidance methods for proper link management. There is concept of virtual channel which established which split single channel into two paths for packets to be routed which reduces latency, deadlock avoidance, performance improvement, QoS by means of guaranteed traffic. Hence high number of buffer strength and more number of virtual channels will reduce contentions in network. A. M. Rahmani et al., proposed a proficient design for 3D stacked work NoC to upgrade framework execution, diminish control utilization, enhance the framework

unwavering quality, and alleviate warm issues. The adequacy of the proposed engineering with respect to normal parcel inertness, control utilization, and pinnacle temperature has been exhibited by test comes about utilizing the manufactured and in addition the practical activity loads [9–11]. Adusumilli Vijaya Bhaskar et al. [31], presented an investigation of the impact of virtual channels on the execution of Network-on-Chip. From the recreation comes about one can watch that the system throughput and inertness increments upto a specific number of virtual channels independent of the movement design utilized, past which there is very little change in throughput and dormancy. Mingyang Kyungsu Kang et al., discuss Financially Design of Mesh-of-Tree Interconnect for Multicore Clusters With 3-D Stacked L2 Scratchpad Memory. They exhibited another TSV sharing technique for a financially savvy outline of 3-D MoT interconnect that can be coordinated in a multicore group where a 3-D multibanked shared L2 SPM is stacked on the multicore bite the dust.

D. Packet Loss and Error Over Transmission

While performing congestion management there is every possibility of faults over links. Also the crossover talks across the links in networks can introduce packet loss and hence few researchers have explored the possibility of implementing fault tolerant error detection and correction techniques over transmission links. Lalit Kishore Arora, Rajkumar have examined the parcel misfortune amid the connection down in work interconnection organize topology with source steering utilizing reproduction. Jie Cen and Cheng Li, Paul Gillared have portrayed a reenactment structure for work interconnection arrange, Investigation and assessment has been done on work interconnection arranges on various activity designs utilizing recreation on NS2 [13], [17–19].

E. Energy Optimization and Quality of Service (QoS)

Advance research work is found in latency and energy optimization for Quality of services (QoS). Many researcher have worked on latency of operation and hence various levels of latency matrix are offered. Hence one can find various architectures for optimizing the guaranteed bandwidth and Best effort for QoS using various arbitration algorithms like round robin, FCFS, Priority, and Priority based round robin wherein later are used for guaranteed traffic. Reetuparna Das et al proposed Aéria: Exploiting Packet Latency Slack in On-Chip Networks. They present the idea of bundle slack and describe it with regards to on-chip systems. So as to adventure bundle slack While the proposed topology gives a few enhancements (e.g., expanded data transfer capacity, diminished dormancy) over standard work, it successfully copies the quantity of connections making switches costly [10], [23], [29], [30].

In this paper, we simulate mesh topology of NoC keeping the routing and switching strategies constant and assessing the performance of the said topology in terms of max end-to-end latency, and throughput using a network simulator.

III. MODELLING OF MESH TOPOLOGY

We consider some variants of 2D Mesh topology in this paper for study. In this topology each switch is connected to four neighboring switches and one resource. The number of switches is equal to the number of resources. The resources and the switches are connected through communication channels. A channel consists of two unidirectional links between two switches or between a switch and a resource. We apply the deterministic XY routing algorithm for this topology. Mesh-based NoCs are receiving attention because of their modularity and the ability to expand by adding new nodes and links without any modification of the existing node structure. One advantage of a mesh is that it can be partitioned into smaller meshes, which is a desirable feature for parallel applications. Some of the most important performance parameters that are used in evaluating the NoCs, are defined in this section briefly. Latency over Network, presents the required time to transfer n bytes of payload from its source to its destination. Latency consists of routing delay, contention delay, channel occupancy and overhead. Bandwidth over communication is the amount of data that can be moved using a communication link in a unit time period. Throughput is the total number of received packets by the destinations per time unit. Packet Loss happens when one or more packets do not reach their destination due to the error introduced by the network, the contention for network link or lack of buffer space etc. NS-2 is an open source, object-oriented and Tcl. Its a very common and widely used tool to simulate small and large area networks. Due to similarities between NoCs and networks, NS-2 has been a choice of many NoC researchers to simulate and observe the behavior of a NoC at a higher abstraction level of design. It has a huge variety of protocols and various topologies can be created with little effort. Moreover, customized protocols for NoCs can easily be incorporated into NS-2. The parameters for routers and links can easily be scaled down to reflect the real situation on a chip. Based on this fact, we have successfully simulated a 16 node 2D mesh based NoC using our reliable protocol for safe delivery of packets.

A. Simulation Environment

For the evaluation of event-driven simulator has been developed for the simulator models a 16 and 64-nodes, 256 1024, 4096 nodes 2-D mesh (4×4 and 8×8 , 16×16 , 32×32 , 64×64) in which routing decision will be taken at input node using source routing methodology. Each node is connected with peer-to-peer twodirectional serial links. The connections are resource-router and router-router base having Transmission Control Protocol (TCP) with static routing table which established the path using shortest path algorithm. The Queue is drop tail type. The transport agent attached to source node $N(0)$ is TCP and two different traffic pattern applications namely FTP and CBR were tested. FTP is use to transmit bulk data and CBR is use to generate packet at constant bit rate and transmit to destination node. Here four types of scenarios are modeled as described in Table I. These scenarios are revolving round the parameters by varying CBR or FTP,

TABLE I
VARIOUS SCENARIOS OF 4×4 AND 8×8 , 16×16 , 32×32 , 64×64 MESH TOPOLOGIES OVER FTP AND CBR TRAFFIC APPLICATIONS.

NoC Model Parameter		Parameter Constraint applied in NS2	
Topology		Mesh	
Connections		Resource-router, router-router	
Transmission protocols		Transmission Control Protocol (TCP)	
Routing scheme		Static	
Routing protocol		Shortest path	
Queue mechanism		Drop tail (FIFO)	
Simulation time		20 s	
Number of nodes		4 × 4 (16 nodes) and 8 × 8 (64 nodes), 16 × 16 (256 nodes), 32 × 32 (1024), 64 × 64 (4096)	
Scenario 1	Scenario 2	Scenario 3	Scenario 4
CBR: 10 Mbps; Link delay: 10 ms; Link BW: 10 Mbps Queue size: 100; Varying packet size: 0.1 to 16000 kB	CBR: 10 Mb/s; Link delay: 10 ms; Link BW: 10 Mbps Queue size: 5–200; Fixed packet size: 0.512 and 64 kB	CBR: 10 Mb/s; Link delay: 10 ms; Link BW varying: 10–200; Queue size: 100; Fixed packet size: 0.512 and 64 kB	CBR: 10 Mb/s; Link delay: 10–200 ms; Link BW: 10 Mbps; Queue size: 100; Fixed packet size: 0.512 and 64 kB

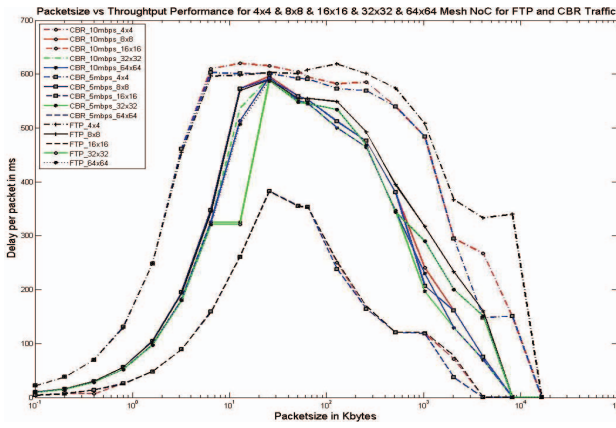


Fig. 1. Throughput vs. packet size for 4×4 and 8×8 , 16×16 , 32×32 , 64×64 Mesh topology for CBR and FTP application.

link delay and bandwidth, queue size and packets size. All these modeled parameters are described as a script file using Tcl. The parameters chosen for simulation are shown in Table I under various scenarios. Here, node N(0) and node N(253) were fixed as source and destination node respectively for simulation.

Scenario-1: Throughput and delay calculation with varying packet size

The link bandwidth and delay of link was kept constant at 10 Mbps and 10 ms, the bulk data size and constant data was generated using FTP and CBR (10 Mbps) rate application with varying packet size generated. It is observed (Fig. 1) that for FTP and CBR application as the packet size increases throughput increases linearly initially and saturates for packet size in range of 6–512 kbps having maximum value of 619 kbps which is corresponding to 4.952 Mbps (close to 50% of the bandwidth since it is simplex link) and later degrades. The throughput for the 4×4 , 8×8 is higher than the 16×16 , 32×32 , 64×64 mesh topology which is due to higher length of path.

Further, we also studied the performance of delay (Fig. 2) using FTP and CBR (10 Mbps) rate application with varying

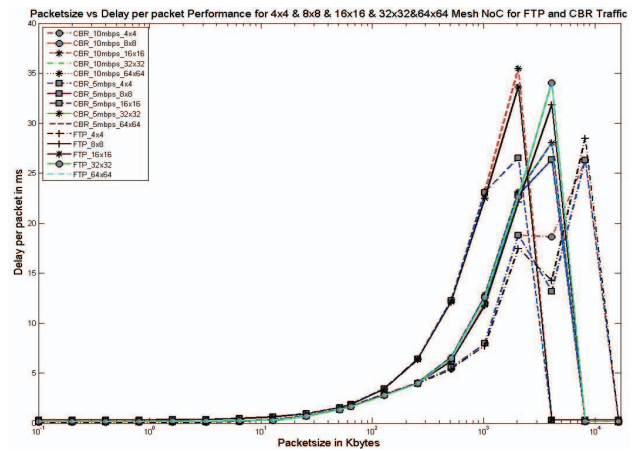


Fig. 2. Delay per packet vs. Packet size for 4×4 and 8×8 , 16×16 , 32×32 , 64×64 Mesh topology for CBR and FTP application.

packet size generated. It is observed (Fig. 1) that for FTP and CBR application as the packet size increases delay slowly increases and is highest from the 1000 to 10,000 packet size and later drop down drastically. This decrease is due to drop in the throughput from 4.952 Mbps to 320 bps. The delay for the 64×64 , 32×32 , 16×16 is higher than the 8×8 , 4×4 mesh topology which is due to higher path length.

Scenario-2: Throughput and delay calculation with varying queue size with low and high load packets

In this scenario we kept each link bandwidth at 10 Mbps, propagation delay of the each link at 10 ms, the bulk data size and constant data was generated using FTP and CBR (10 Mbps) rate application with varying queue size from 5 to 200. It is observed (Fig. 3) that the performance of low load i.e. 0.512 kB is very low as compared to high load of 64 kB having factor of 4–5 times. This is because at low load of 0.512 kB the network resource i.e. queues size is not utilized efficiently. Also it may be noted that the within the low load, the 4×4 topology has higher throughput as compared to 8×8 , 16×16 , 32×32 , 64×64 topology due to short path

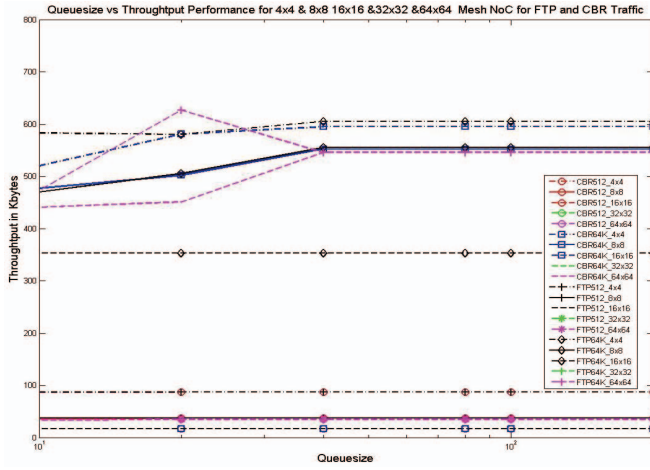


Fig. 3. Throughput vs. queue size.

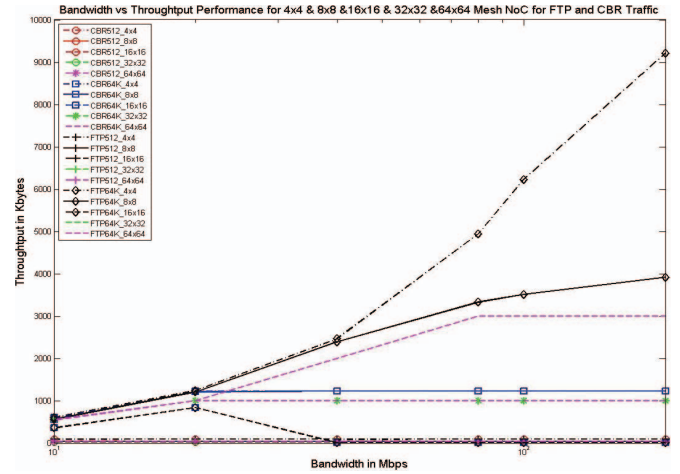


Fig. 5. Throughput vs. bandwidth.

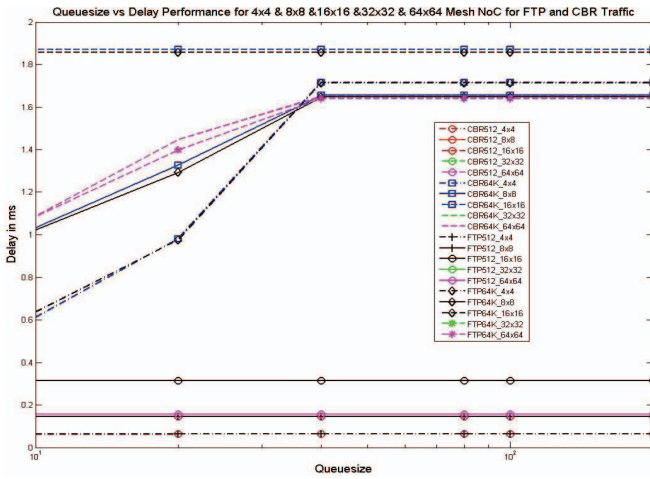


Fig. 4. Delay per packet vs. queue size.

length. This holds same for high load packets wherein the 4×4 topology has higher delay throughput as compared to $8 \times 8, 16 \times 16, 32 \times 32, 64 \times 64$ topology due to short path length.

Similar performance was studied for transmission delay from N(0) to N(15) and N(0) to N(64), N(0) to N(256) source and destination node respectively. It is observed (Fig. 4) that the delay performance of low load i.e. 0.512 kB is very low as compared to high load of 64 kB having factor of 4–5 times on an average. This is because at low load of 0.512 kB the network resource i.e. queues size is not utilized efficiently. Further it may be noted that within the low load, the 4×4 topology has better performance over transmission delay as compared to $8 \times 8, 16 \times 16, 32 \times 32, 64 \times 64$ topology. It may be noted that the delay performance over higher load is saturating at the queue size of 40. This could be the optimized size of the queue at that packets size of 64 kB. It may be noted that from queue size of 10 to 40 the delay performance is gradually increasing linearly and here it is again better performance

for transmission delay over 4×4 topology as compared to $8 \times 8, 16 \times 16$ topology, which is due to higher path length.

Scenario-3: Throughput and delay calculation with varying link Bandwidth for low & high load packets

In this scenario we kept queue size as 100, propagation delay of the each link at 10 ms, the bulk data size and constant data was generated using FTP and CBR (10 Mbps) rate application with varying link bandwidth from 10 to 200. It is observed (Fig. 5) that the throughput performance for low load i.e. 0.512 kB is very low below 100 kB compared to high load of 64 kB having average factor of 20–25 times. This is because at low load of 0.512 kB the bandwidth is not exploited and so throughput remains very low. At the high load of 64kB FTP performs better as compared to CBR, as CBR rate is low to exploit the given bandwidth and hence it remains saturated even after increasing bandwidth. While the FTP application the bandwidth is linearly increasing as the bandwidth increases and it is found to be best for 4×4 topology as compared to $8 \times 8, 16 \times 16, 32 \times 32, 64 \times 64$ topology due to path length.

Similar performance was studied for transmission delay from N(0) to N(15) and N(0) to N(64), N(0) to N(256) source and destination node respectively. It is observed (Fig. 6) that the delay performance of low load i.e. 0.512 kB is better as compared to high load of 64 kB having factored of 4–5 times on an average between bandwidth of 10–40 Mbps. The high performance of transmission delay is due to size of the packets 128 times smaller than high load packet. The initial delay is high for the low link bandwidth within 10–40 Mbps as for the higher load the bandwidth is not enough for transmission, which is satisfies after at 40 Mbps for 64 kB load.

Scenario-4: Throughput and delay calculation with varying propagation delay of link with low & high load packets

In this scenario we kept queue size as 100, link bandwidth from 10 Mbps and the bulk data size and constant data was generated using FTP and CBR (10 Mbps) rate application with varying link propagation delay each link within 10–200 ms. It is observed (Fig. 7) that the throughput performance for

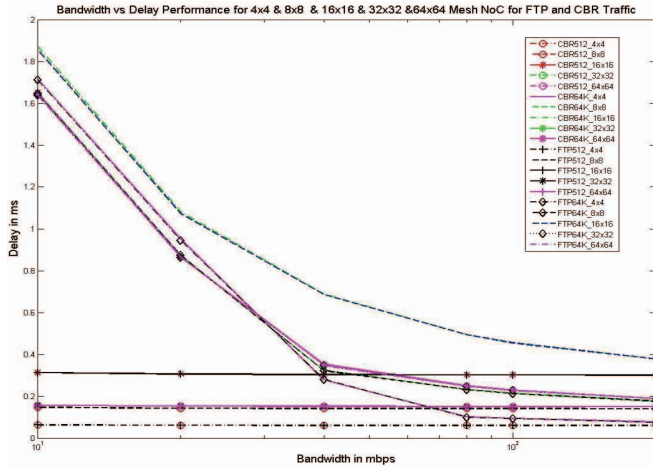


Fig. 6. Delay per packet vs. bandwidth.

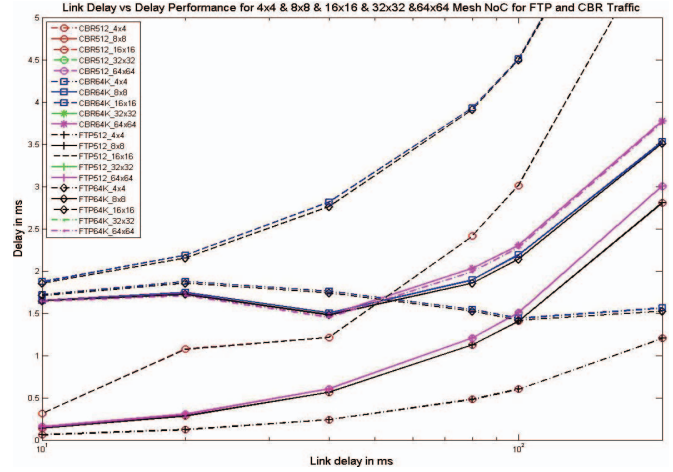


Fig. 8. Delay per packet vs. link delay.

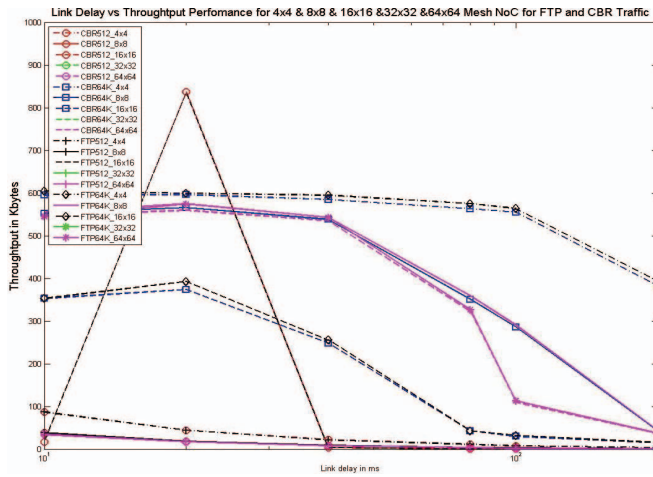


Fig. 7. Throughput vs. link delay.

low load i.e. 0.512 kB is very low below 100 kB compared to high load of 64 kB factor of 4–5 times, having average value of having average of 400 kB. The throughput of the high load decreases as the link propagation delay increases. The 4×4 topology performs better compared to 8×8 , 16×16 , 32×32 , 64×64 due to low path length. The decrease in performance at the higher propagation delay is natural and implicit.

Similar performance was studied for transmission delay from N(0) to N(15) and N(0) to N(64), and N(0) to N(256) source and destination node respectively. It is observed (Fig. 8) that the delay performance is better over topologies as compared to scenarios 2 and 3 which was for high and low loads. It is found that the 8×8 topology the delay performance worst 1.5 factor times. The transmission delay remains within average value of 1.5 ms for high load packets i.e. 64Kbytes; using FTP and CBR (10 Mbps) rate application. This could be because as the propagation delay increases the packets transvers time matches with that of propagation delay and

system is seems to be in unison within specific propagation link days limits. While in other application low load 8×8 , 16×16 topology and 4×4 load topology the packets delay performance degrades.

IV. DISCUSSION AND CONCLUSION

Choosing suitable parameter for NoC architectures is an important issue in NoC design and implementation so as to bringing the NoC paradigm to real applications. Here, we have presented and developed simulation and verification platform to measure the NoC performance in terms of network delay and throughput. The proposed platform has been designed and implemented in mesh topology. Here we have proposed a NoC platform to meet the requirements of the target applications by customizing parameters. The designers can configure various heterogeneous and homogenous network topologies, flow control mechanisms and routing algorithms as well as configure a various regular applications. Here we have evaluated the performance of standard mesh-based NoC architecture. Each node is connected with point-to-point bidirectional serial links. Our work briefly compares the performance of the NoC, for the throughput and delay. Using different attributes, like varying packet size; FTP traffic gives better performance as compared to CBR traffic. The varying packet size has little effect on throughput performance in FTP but significance effect in CBR up to packet size of 25 kB. With respect to delay CBR traffic performance is better than FTP traffic, as packet size increases, the delay increases in FTP but there is not much change in delay in CBR traffic. Varying Queue size with high load packets, FTP traffic gives better performance as compared to CBR traffic, throughput increases with increase in queue size in FTP. Delay increases as queue size increases in FTP and CBR traffic. Link Bandwidth for low load and high load, is total with varying link bandwidth for low and high load FTP traffic, which gives better throughput as compared to CBR traffic and delay decreases as bandwidth increases in both the traffic. Propagation delay of link with low load and high load, Throughput decreases as propagation delay of link

increases for FTP traffic with low and high load. Better in FTP traffic, delay per packet increases as propagation delay of link increases in both the cases. The extension of these work is to evaluate the lowest drop probability using different CLICH, Folded Torus, BFT algorithm, then will be find the good topology of the system.

Hence the simulations, considerable end-to-end throughput enhancement, and a reduction in average delay was measured when using 4×4 , 8×8 , 16×16 , 32×32 , 64×64 mesh topologies. Using such a technologies appropriately, higher service support can be provided to clients with increased throughput while meeting more efficiently QoS requirements demanded by today's applications. Finally a simple sensible situation was exhibited which highlighted how 4×4 , 8×8 , 16×16 , 32×32 , 64×64 work topologies help in the versatility of WMNs. It was highlighted that when WMNs are gently stacked, the future extent of MIMO STBC modes can be used to boost scope utilizing a negligible number of 4×4 , 8×8 , 16×16 , 32×32 , 64×64 work switches. Additionally work, it was noticed that for direct work switch interface separates, the MIMO modes perform best while for longer separation joins, STBC MIMO modes accomplish the best execution because of the accessibility of differing qualities pick up.

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