

A New NoC Architecture Based on Partial Interconnection of Mesh Networks

S. Choudhary and S. Qureshi

Department of Electrical Engineering, Indian Institute of Technology, Kanpur, India-208016.

E-mail: suds@iitk.ac.in and qureshi@iitk.ac.in

Abstract- A new network on chip (NoC) topology called partially interconnected mesh network is proposed and a routing algorithm supporting the proposed architecture is also developed. The proposed architecture is based on standard mesh networks, here four extra bidirectional channels are added which remove the congestion and hotspots compare to standard mesh networks with fewer channels. The proposed architecture and routing algorithm are compared to measure performance benefits over standard mesh network in terms of delay and throughput. Significant improvement in delay (60% reduction) and throughput (60% increased) were observed when using the proposed network. An increase in number of channels makes the switches expensive and could increase the area and power consumption. However, the proposed network can be useful in high speed applications with some compromise in area and power.

I. INTRODUCTION

As reported by the researchers in [1–5], it will not be possible for the dedicated wires and shared busses to fulfill the communication requirements of future ICs. On chip interconnection architecture is commonly based on dedicated wires or shared busses. As the system complexity increases the number of dedicated wires grows which means they are effective only for small core systems. Also there are issues of poor reusability and flexibility with dedicated wires. A shared bus can be more scalable and reusable compared to dedicated wires but they cannot support the communication parallelism and bandwidth requirements of multi core systems [6–7].

NoCs have emerged as a solution to the existing interconnection architecture constraints [8–10] due to the following characteristics: (i) energy efficiency and reliability [3], (ii) scalability of bandwidth when compared to traditional bus architectures, (iii) reusability and (iv) distributed routing decisions [4–5]. NoC is an on-chip interconnection network [4] composed by cores (IP blocks) connected to switches (routers) which are in turn connected among themselves by communication channels. Two main resources that compose NoCs are buffers and channels. To increase the resources allocation for each packet, a physical channel is multiplexed into a number of virtual channels [4, 5]. Each virtual channel has one or more buffers which provide multiple buffers for each physical channel. The performance of NoC with virtual

channels can be evaluated and the important parameters can be fixed by the designers for specific applications [10].

The main steps of a NoC design are architecture specification, traffic modeling, and performance evaluation. Fully adaptive routing is considered the best for mesh networks [11–18], we verified the same using Noxim simulator [19] (details not shown in this paper). The key contribution of this paper is a new NoC architecture (partially interconnected mesh topology) and a suitable routing algorithm for the new design. In section 2, partially interconnected mesh network topology and a routing scheme [20] for this topology is proposed. This proposed architecture and routing algorithm is compared with the best configured ideal mesh network architecture proposed by previous research works [11–18] [20]. We used Nirgam simulator [21] to build the proposed architecture and routing scheme, the simulator was modified to support the new topology and routing scheme. Conclusion is presented in section 3.

II. PROPOSED ARCHITECTURE AND ROUTING

Full mesh topology is a network topology in which all nodes are directly connected to each other. In a fully connected network with n nodes, there are $n(n-1)/2$ direct links. Full mesh networks are very costly to setup, but provide a highly reliable data transfer because of the availability of multiple paths to a node. This topology is used when there are only a small number of nodes to be interconnected. These networks are usually seen in military applications.

Partially connected mesh is a network topology in which some of the nodes of the network are connected to more than one other node in the network with a point-to-point link. This makes it possible to take advantage of some of the redundancy that is provided by a physical fully connected mesh topology without the expense and complexity required for a connection between every node in the network [22]. In this section, a new architecture based on partially connected mesh topology and a routing algorithm for this new topology is proposed. We use Nirgam [21] simulator for evaluation.

This simulator supports both mesh and torus networks. The simulator was modified to support the proposed new architecture, a routing algorithm was also written for the simulator to send packets on the proposed network. In this

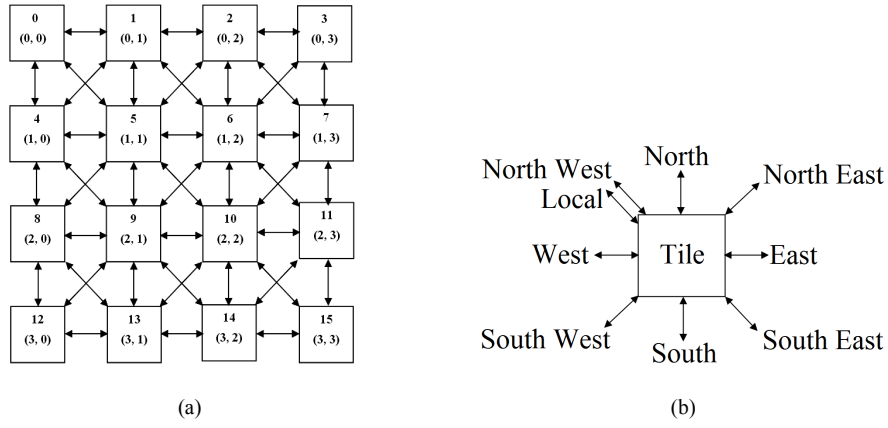


Fig. 1. (a) Proposed partially connected mesh topology where tiles are connected through bidirectional channels (b) Representation of a tile with its bi-directional channels.

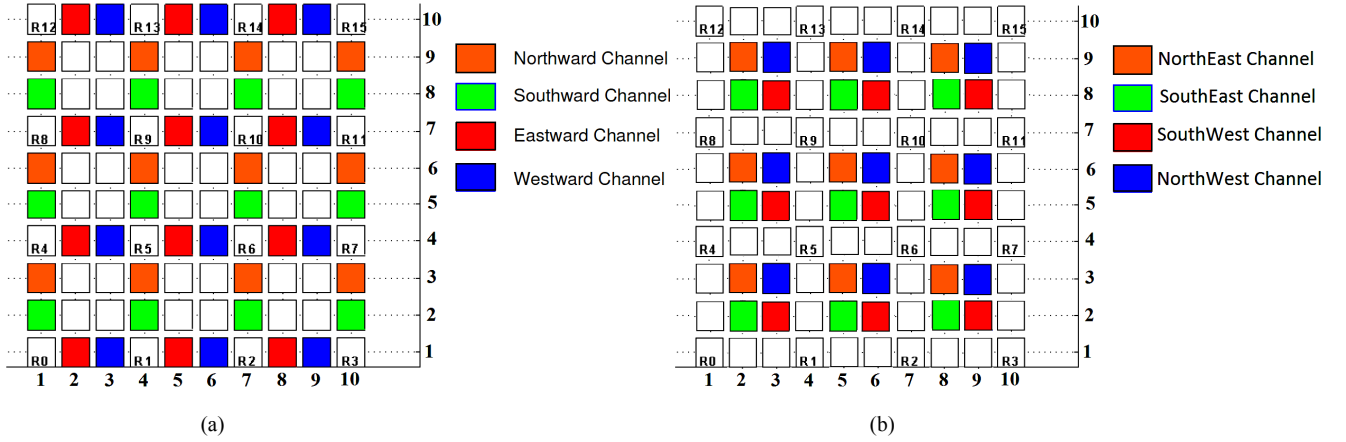


Fig. 2. Representation of Performance metrics on per channel basis (a) North, South, East and West channels (b) North-East, South-East, North-West and South-West channels. R0-R15 represents the routers.

new architecture we add four extra bidirectional channels to each router of the mesh network, so that there are nine bidirectional communication channels in each router namely East, West, North, South, Local, North-East, South-East, North-West and South-West (see Fig. 1).

The performance of NoC is evaluated on per-channel basis. Fig. 2(a) shows representation of performance metrics in matlab generated graphs. R0 - R15 shows the placement of tiles/routers. Red bar between R0 and R1 represents metric for east channel from R0 to R1. Blue bar between R0 and R1 represents metric for west channel from R1 to R0. Green bar between R0 and R4 represents metric for south channel from R0 to R4. Orange bar between R0 and R4 represents metric for north channel from R4 to R0. Similarly in Fig. 2(b), Red bar between R1 and R4 represents metric for South-West channel from R1 to R4. Blue bar between R5 and R0 represents metric for North-West channel from R5 to R0. Green bar between R0 and R5 represents metric for South-East channel from R0 to R5. Orange bar between R4 and R1 represents metric for North-East channel from R4 to R1.

In a standard mesh network each router/tile has four bidirectional ports/channels for communicating other routers in the network and has one bidirectional channel for communicating with the local IP attached to tile. Routing algorithms for such network are mainly based on communication in x-direction and y-direction, using turn models that routes the packet by turning in x-direction (using East or West channel) or y-direction (using North or South channel). Dead-locks in some unique cases in turn models are avoided by prohibiting few turns while routing a packet from source node to destination node. In the new architecture, packets can also be routed in z-direction (NE, SE, NW and SW) along with the usual x and y-directions. This saves the number of routers traversed which in turn applies the use of free router channels by other communications. For example, if a packet has to move from source tile number 12 to destination tile number 7 using standard mesh network, the path could be through tiles 12-13-14-15-11-7. However, the path is through tiles 12-9-6-7 when network of Fig. 1(a) is used, that saves time by routing through fewer tiles and also allows the free channels/paths for other communications. Higher throughput

```

if(dest_yco > yco)           else if(dest_yco < yco)           else if(dest_yco == yco)
{
    if(dest_xco < xco)
        return NE;
    else if(dest_xco > xco)
        return SE;
    else if(dest_xco == xco)
        return E;
}

{
    if(dest_xco < xco)
        return NW;
    else if(dest_xco > xco)
        return SW;
    else if(dest_xco == xco)
        return W;
}

{
    if(dest_xco < xco)
        return N;
    else if(dest_xco > xco)
        return S;
    else if(dest_xco == xco)
        return C;
}

```

Fig. 3. Cross-routing algorithm; 'xco' and 'yco' are x and y-coordinates of source tile; 'dest_xco' and 'dest_yco' are coordinates of destination tile.

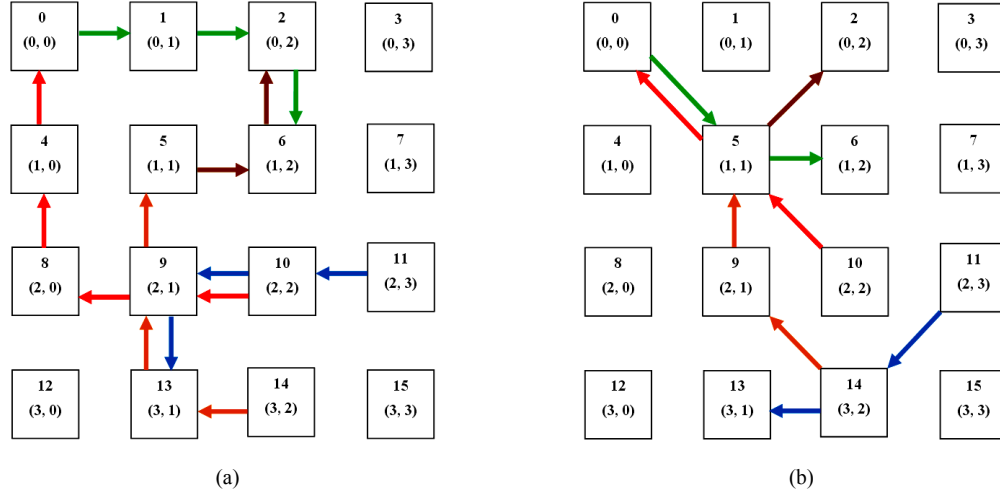
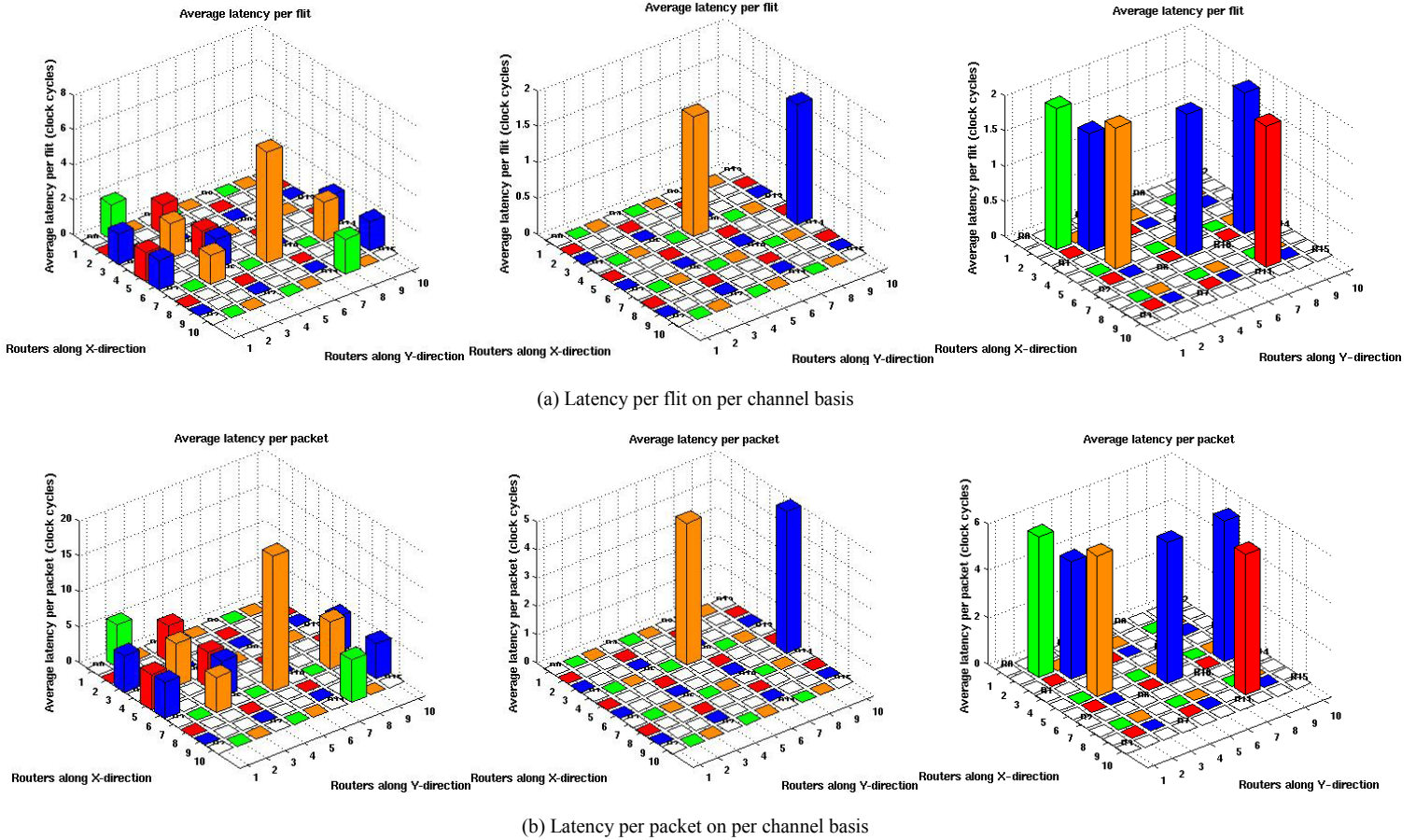
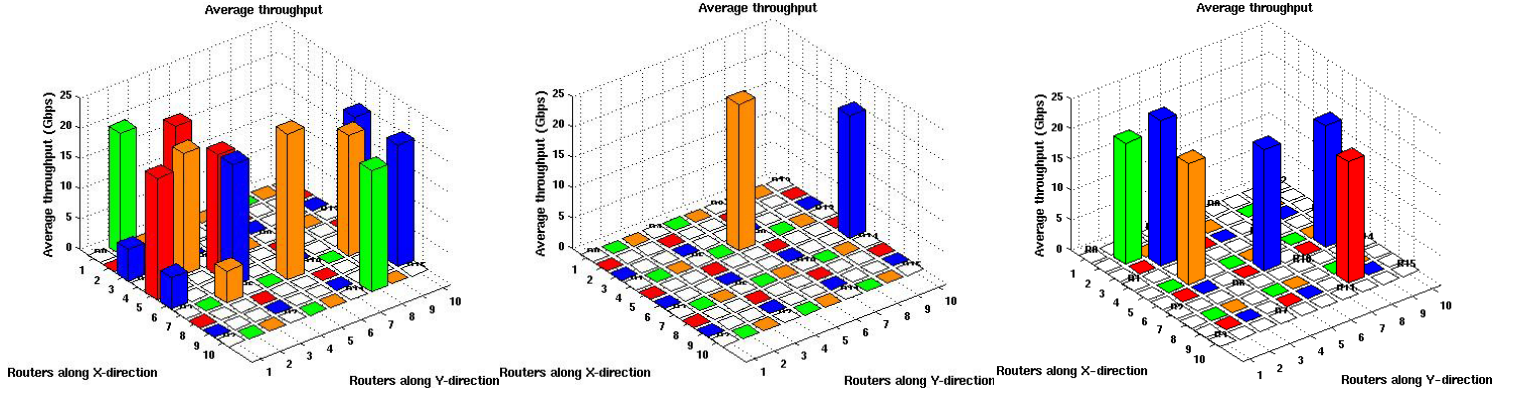


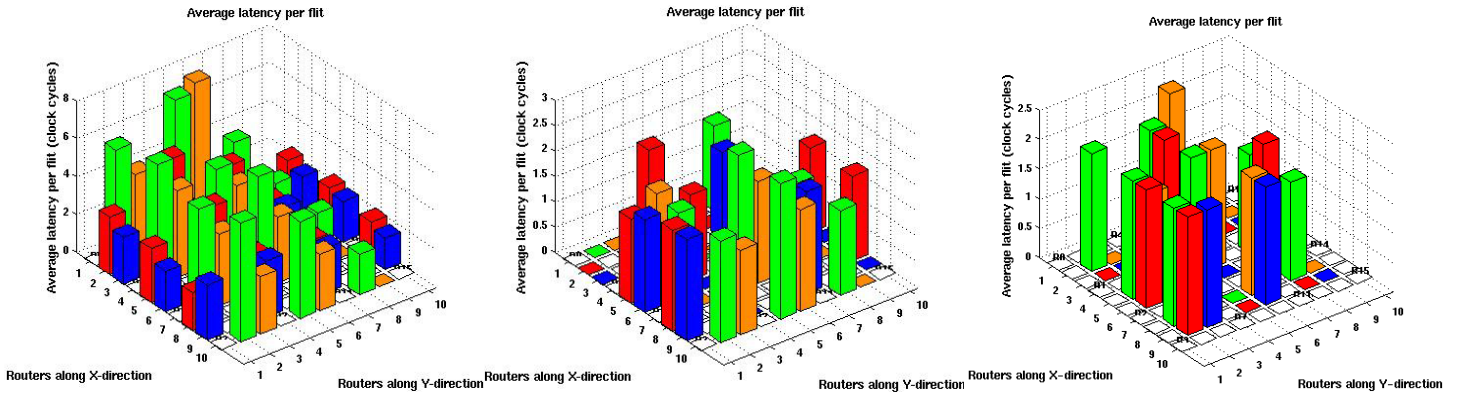
Fig. 4. CBR with fixed destination on (a) standard mesh with fully adaptive routing (b) partially connected mesh with cross-routing





(c) Throughput per channel

Fig. 5. Simulation results for fixed destination corresponding to Fig. 4; (a) latency per flit, (b) latency per packet and (c) Throughput. Three results are shown in each case where first result is obtained for mesh network using fully adaptive routing, second and third results are for the proposed network topology on cross-routing. Also in each case, second result shows measurements on East, West, North and South channel and third result shows measurements on North East, South East, North West and South West channels.



(a) Latency per flit for random destination, other details remain same as in Fig. 5 above.

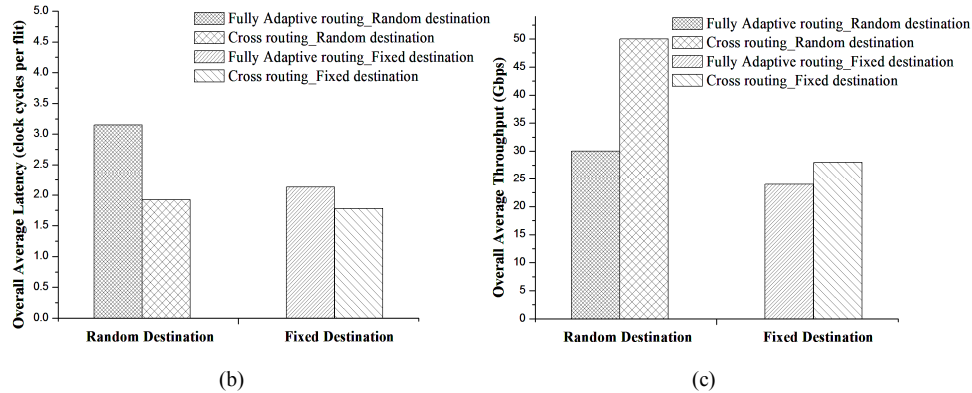


Fig. 6. (a) Latency per flit for random destination, (b) Overall Average latency for fixed and random destination and (c) Overall Average Throughput for fixed and random destination.

and smaller latency is confirmed through simulations on this architecture.

Routing algorithm for this architecture is called cross-routing and is given in Fig. 3. While moving a packet, the x-coordinate and y-coordinate of source and destination tiles are compared. If both x and y-coordinates of source and

destination tiles are not equal, packet is moved in z-direction (using NE, SE, NW or SW channels), else packet moves in either x or y-direction depending on whether the x-coordinate or y-coordinate of source tile is equal to that of destination tile. Cross-routing is free of dead-locks since it does not form loops, third turn is prohibited so that a packet reaches the

destination by taking maximum two turns, one in z-direction and other in x or y-direction. Simulation results using cross-routing on the proposed architecture show significant improvement in latency and throughput when compared to fully adaptive routing on ideal mesh networks.

A. Experimental Results and Discussion

The performance evaluation is based on standard 4x4 mesh network with five bi-directional ports and partially connected mesh network with nine bidirectional channels (see Fig. 1(a)). It was found earlier that fully adaptive routing is superior to all other routing schemes [11-18]. Hence we evaluate and compare the performance of these networks on fully adaptive and cross-routing algorithm. Also, we consider tiles of both the networks transmitting packets at constant bit-rate (CBR) with random destinations and at constant bit-rate with fixed destinations. In CBR with random destinations, each tile behaves as a source as well as sink, implying that it is capable of generating as well as receiving flits. Each tile generates CBR traffic to randomly chosen destination. For CBR with fixed destinations, we consider an example shown in Fig. 4, where, tile 0 sends CBR traffic to tile 6, tile 5 sends CBR traffic to tile 2, tile 10 sends CBR traffic to tile 0, tile 11 sends CBR traffic to tile 13 and tile 14 sends CBR traffic to tile 5. Fig. 4(a) shows the possible path taken by the packets to move from sources to fixed destinations on standard mesh network using fully adaptive routing, while Fig. 4(b) uses partially connected mesh network of Fig. 1(a) with cross-routing.

Performance of both the NoCs are measured on per channel basis. Traffic generation begins after 5 clock cycles, and continues until 300 clock cycles. Simulation stops after 1000 clock cycles. Latency and throughput per-channel for CBR with fixed destination are measured and plotted in Fig. 5. Overall average latency is shown in Fig. 5(a), which is smaller in case of cross-routing (1.78, in clock-cycles per flit) compare to fully adaptive routing on standard mesh NoC (2.13, in clock cycles per flit). Overall average throughput (see Fig. 5(b)) is also higher for cross-routing scheme (28 Gbps) compare to fully adaptive routing on standard mesh NoC (24 Gbps). Similar results are obtained for CBR with random destinations and are shown in Fig. 6. The results in Fig. 6(b) and (c) show that for cross-routing the overall average latency reduces by 60% and the overall average throughput increases by 60% in comparison to fully adaptive routing on standard mesh NoC. This improvement in performance is possible because lesser nodes are traversed during packet transmission thus offering greater number of available free channels which could be utilized by other communications.

III. CONCLUSION

In this paper we have evaluated the performance of standard mesh-based NoC architecture and compared it with the proposed partially interconnected network architecture. We started by evaluating different routing algorithms and switching schemes on a standard mesh topology and then proposed a partially interconnected mesh topology with cross-routing algorithm. From the performance comparison, it was

found that the proposed network and routing algorithm can be efficiently used for future NoCs. The experiments were also performed on larger networks and performance measurements gave significant improvements. While the proposed topology provides some improvements (e.g. increased bandwidth, decreased latency) over standard mesh, it effectively duplicates the number of links making switches expensive. It is also expected that this topology could increase the die area and power consumption but still it can be useful for high speed applications with some compromise in power and area.

ACKNOWLEDGMENT

The authors would like to thank Ministry of Communication and Information Technology, Govt. of India for their support.

REFERENCES

- [1] S. Kumar, A. Jantsch, J. P. Soininen, M. Forsell, M. Millberg, J. Oberg, K. Tiensyrja and A. Hemani, "A network on chip architecture and design methodology," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI'02)*, April 2002, pp. 105-112.
- [2] M. Millberg, E. Nilsson, R. Thid, S. Kumar and A. Jantsch, "The Nostrum backbone—a communication protocol stack for networks on chip," *Proceedings of the VLSI Design Conference*, January 2004.
- [3] L. Benini and G. De Micheli, "Powering networks on chips: energy-efficient and reliable interconnect design for SoCs," *14th International Symposium on Systems Synthesis (ISSS'01)*, October 2001, pp. 33-38.
- [4] L. Benini and G. De Micheli, "Networks on chips: a new SoC paradigm," *IEEE Computer*, vol. 35, no. 1, pp. 70-78, 2002.
- [5] P. Guerrier and A. Greiner, "Ageneric architecture for on-chip packet-switched interconnections," *Design Automation and Test in Europe (DATE'00)*, March 2000, pp. 250-256.
- [6] E. Bolotin, I. Cidon, R. Ginosar and A. Kolodny, "Cost Considerations in Network on Chip," *Integration: The VLSI Journal*, no. 38, pp. 19-42, 2004.
- [7] C.A. Zeferino, M.E. Kreutz, L. Carro and A.A. Susin, "A Study on Communication Issues for Systems-on-Chip," *Symposium on Integrated Circuits and Systems Design*, 2002, pp. 121-126.
- [8] E. Rijpkema, K. Goossens, A. Radulescu, J. Dielissen, J. van Meerbergen, P. Wielage and E. Waterlander, "Tradeoffs in the design of a router with both guaranteed and best-effort services for networks on chip," *Design, Automation and Test in Europe (DATE'03)*, March 2003, pp. 350-355.
- [9] E. Rijpkema, K. Goossens and P. Wielage, "A router architecture for networks on silicon," *2nd Workshop on Embedded Systems (PROGRESS'2001)*, November 2001, pp. 181-188.
- [10] B. S. Feero and P. P. Pande, "Networks-on-Chip in a Three-Dimensional Environment: A Performance Evaluation," *IEEE Trans. on Computers*, vol. 58, no. 1, pp. 32-45, 2009.
- [11] M. Palesi, G. Longo, S. Signorino, S. Kumar, R. Holmark and V. Catania, "Design of Bandwidth Aware and Congestion Avoiding Efficient Routing Algorithms for Networks-on-Chip Platforms," *IEEE International Symposium on Networks-on-Chip*, 7th-11th April 2008, Newcastle University, UK, pp. 97-106.
- [12] G. Longo, S. Signorino, M. Palesi, S. Kumar, R. Holmark and V. Catania, "Bandwidth Aware Routing Algorithms for Networks-on-Chip," *2nd Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip*, Goteborg, Sweden, January 27, 2008.
- [13] R. Tornero, J. M. Orduna, M. Palesi and J. Duato, "A Communication-Aware Task Mapping Technique for NoCs," *2nd Workshop on*

- [14] M. Palesi, S. Kumar, R. Holsmark and V. Catania, "Exploiting Communication Concurrency for Efficient Deadlock Free Routing in Reconfigurable NoC Platforms," *IEEE International Parallel and Distributed Processing Symposium*, Long Beach, CA, March 2007, pp. 1-8.
- [15] G. Ascia, V. Catania, M. Palesi and D. Patti, "Neighbors-on-Path: A New Selection Strategy for On-Chip Networks," *Fourth IEEE Workshop on Embedded Systems for Real Time Multimedia*, Seoul, Korea, October 26-27, 2006, pp. 79-8.
- [16] M. Palesi, R. Holsmark, S. Kumar and V. Catania, "A Methodology for Design of Application Specific Deadlock-free Routing Algorithms for NoC Systems," *International Conference on Hardware-Software Codesign and System Synthesis*, Seoul, Korea, October 22-25, 2006, pp. 142-147..
- [17] M. Palesi, S. Kumar and R. Holsmark, "A Method for Router Table Compression for Application Specific Routing in Mesh Topology NoC Architectures," *SAMOS VI Workshop: Embedded Computer Systems: Architectures, Modeling, and Simulation*, Samos, Greece, July 17-20, 2006, pp. 373-384.
- [18] G. Ascia, V. Catania, M. Palesi and D. Patti, "A New Selection Policy for Adaptive Routing in Network on Chip," *International Conference on Electronics, Hardware, Wireless and Optical Communications*, Madrid, Spain, February 15-17, 2006.
- [19] Noxim-the NoC Simulator, <http://sourceforge.net/projects/noxim/>
- [20] S. Choudhary and S. Qureshi, "Performance Evaluation for Mesh-based NoCs: Implementation of a New Architecture and Routing Algorithm," springer, IJAC, submitted.
- [21] NIRGAM: A Simulator for NoC Interconnect Routing and Application Modeling, <http://www.nirgam.ecs.soton.ac.uk>, 2008.
- [22] http://en.wikipedia.org/wiki/Tree_and_hypertree_networks#Tree