1. **Study of Logic Gates–AND, OR, NOT, NAND, NOR , EX-OR**

AIM: To investigate the logic behavior of AND, OR, NOT, NAND, NOR, EX-OR gates.

APPARATUS REQUIRED: Deeds-DCs simulation kit

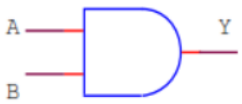
Procedure:

1. Make the connections as per the circuit diagram.
2. Connect the inputs to input switches.
3. Connect the outputs to the output switches or Output LED's.
4. Apply various combinations of inputs according to the truth table and observe conditions of the outputs.

Conclusion: The logic behavior of AND, OR, NOT, NAND, NOR, EX-OR gates is verified.

OBSERVATIONS

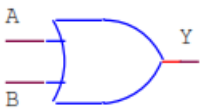
AND Gate



Truth Table

A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

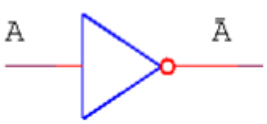
OR Gate



Truth Table

A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

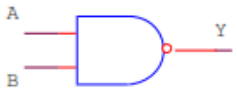
NOT Gate



Truth Table

A	Y=Ā
0	1
1	0

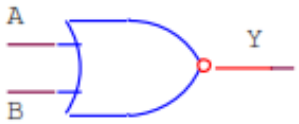
NAND Gate



Truth Table

A	B	$Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

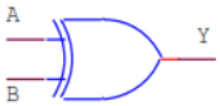
NOR Gate



Truth Table

A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate



Truth Table

A	B	$Y=A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

2. Realization of AND, OR and NOT gates using Universal Gates.

AIM: To Study and Verify NAND and NOR as a Universal Gate.

APPARATUS REQUIRED: Deeds-DCs simulation kit

Procedure:

1. Make the connections as per the circuit diagram.

2. Connect the inputs to input switches.

3. Connect the outputs to the output switches or Output LED's.

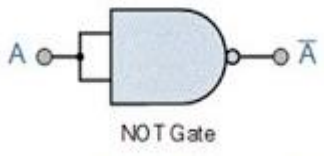
4. Apply various combinations of inputs according to the truth table and observe conditions of the outputs.

5. Note the outputs of NAND as a AND, OR, NOT and NOR as a AND, OR, NOT.

Conclusion: The universal behavior of NAND, NOR gates is verified.

OBSERVATION

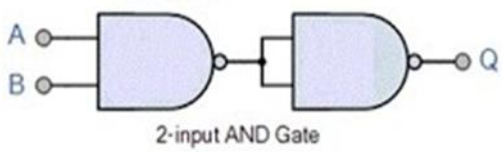
Using NAND Gate



NOT Gate

Truth Table

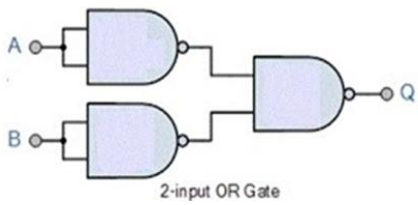
A	Y=$\bar{A}$
0	1
1	0



2-input AND Gate

Truth Table

A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

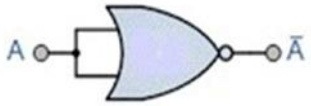


2-input OR Gate

Truth Table

A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

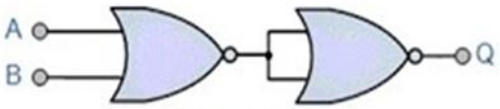
Using NOR Gate



NOT Gate

Truth Table

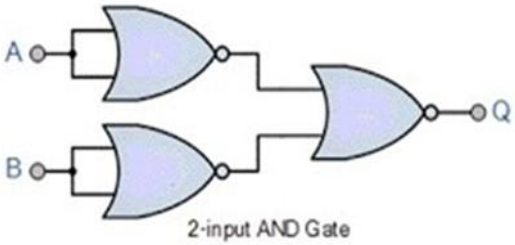
A	Y=Ā
0	1
1	0



2-input OR Gate

Truth Table

A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1



2-input AND Gate

Truth Table

A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

3. Design and Realization of Half Adder using logic gates.

AIM: To design and Verify operation of half adder using logic gates.

APPARATUS REQUIRED: Deeds-DCs simulation kit

Procedure:

1. Make the connections as per the circuit diagram.

2. Connect the inputs to input switches.

3. Connect the outputs to the output switches or Output LED's.

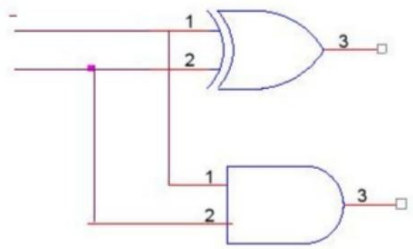
4. Apply various combinations of inputs according to the truth table and observe conditions of the outputs.

5. Note the outputs of sum and carry

Conclusion: The operation of half adder using logic gates is verified.

OBSERVATION:

CIRCUIT DAIGRAM



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

4. Design and Realization of Full Adder using logic gates.

AIM: To design and Verify operation of full adder using logic gates.

APPARATUS REQUIRED: Deeds-DCs simulation kit

Procedure:

1. Make the connections as per the circuit diagram.

2. Connect the inputs to input switches.

3. Connect the outputs to the output switches or Output LED's.

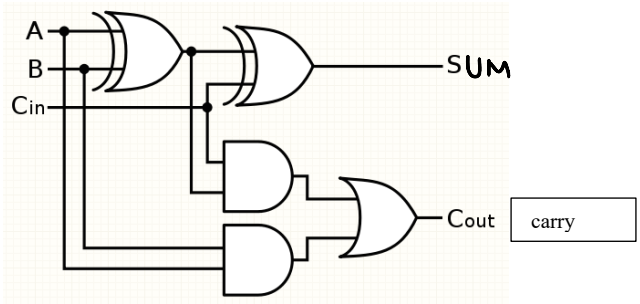
4. Apply various combinations of inputs according to the truth table and observe conditions of the outputs.

5. Note the outputs of sum and carry

Conclusion: The operation of full adder using logic gates is verified.

OBSERVATION:

CIRCUIT DIAGRAM



TRUTH TABLE

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

5. Design and Realization of BCD Adder.

AIM: To design and Verify operation of 4-bit BCD adder.

APPARATUS REQUIRED: Deeds-DCs simulation kit

Procedure:

1. Make the connections as per the circuit diagram.

2. Use Input DIP switches to the 4-bit A and B inputs.

3. Connect these inputs to the 4- bit adder.

4. Connect the output DIP switches RESULT to the output of 4-bit adder.

5.For addition always Ci input of BCD adder should be 0.

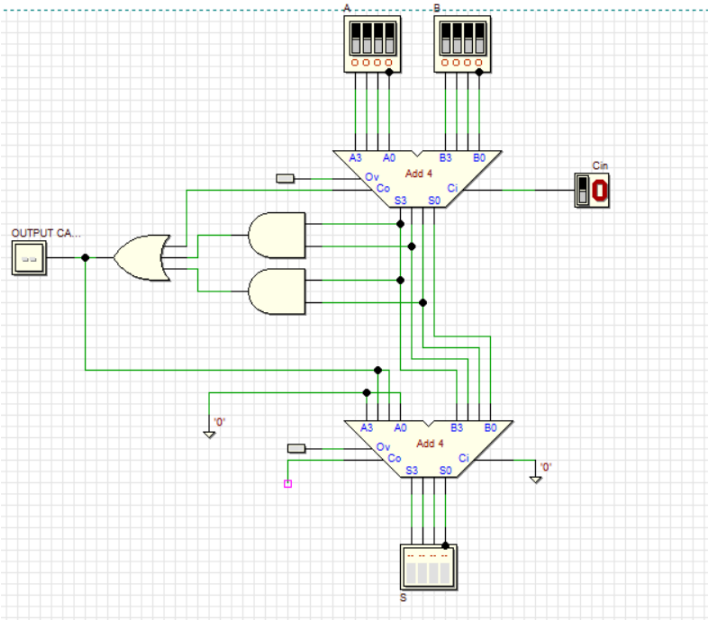
4. Apply various combinations of inputs according to the truth table and observe conditions of the outputs.

5. Note the outputs of sum and carry

Conclusion: The operation of 4-bit BCD adder is verified.

OBSERVATION:

CIRCUIT DIAGRAM



TRUTH TABLE

INPUT A				INPUT B				Output Sum				C
0	1	0	1	0	1	1	0					
1	0	1	1	1	1	0	0					
1	0	0	1	1	0	0	1					
1	0	0	0	1	0	0	0					
1	1	0	0	1	1	1	0					
0	1	1	0	0	0	1	0					
0	0	1	0	0	1	0	0					

6. Design and Realization of SR flip flop.

AIM: To design and Verify operation SR flip flop using NAND gates.

APPARATUS REQUIRED: Deeds-DCs simulation kit

Procedure:

1. Use NAND gates and CLOCK input from input switch from tool bar.

2. Use a CLOCK in between NAND Gates.

3. Join all the components through wires just like the given circuit diagram.

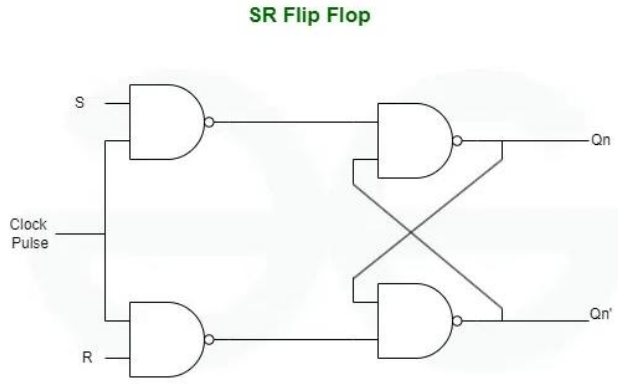
4. Now click on the Play button. Alter the Values of Input and observe all the outputs at each Logic Gate.

5. Apply various combinations of inputs according to the truth table and observe conditions of the outputs.

Conclusion: Design and Realization of SR flip flop is verified.

OBSERVATION

Circuit diagram



Truth table:

CLOCK	S	R	Q	Q’
X	-	-	No change	No change
1	0	0	No change	No change
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid	Invalid

7. Design and Realization of JK flip flop.

AIM: To design and Verify operation JK flip flop using NAND gates.

APPARATUS REQUIRED: Deeds-DCs simulation kit

Procedure:

1. Use NAND gates and CLOCK input from input switch from tool bar.

2. Use a CLOCK in between NAND Gates.

3. the two initialization inputs $\overline{preset}$ and $\overline{clear}$.

4. Join all the components through wires just like the given circuit diagram.

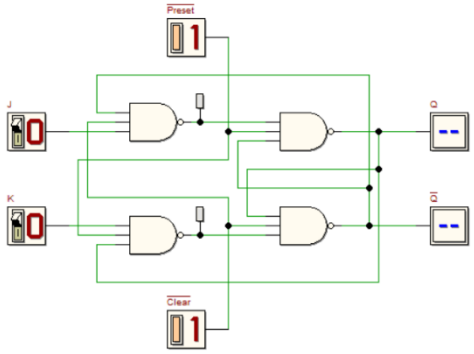
5. Now click on the Play button. Alter the Values of Input and observe all the outputs at each Logic Gate.

6. Apply various combinations of inputs according to the truth table and observe conditions of the outputs.

Conclusion: Design and Realization of JK flip flop is verified.

OBSERVATION

Circuit diagram



Truth table:

CLOCK	J	K	Q	Q’
X	-	-	No change	No change
1	0	0	No change	No change
1	0	1	0	1
1	1	0	1	0
1	1	1	Toggles	Toggles

8. Design and Implementation of PIPO shift registers.

AIM: To design and Verify operation of 4-bit PIPO shift registers.

APPARATUS REQUIRED: Deeds-DCs simulation kit

Procedure:

1. Use 4 number of D flip flops and CLOCK input from input switch from tool bar.

2. Use a CLOCK in between NAND Gates.

3. Join all the components through wires just like the given circuit diagram.

4. Now click on the Play button.

5. Apply the 4 data bits as input to D3, D2, D1, D0. 4.

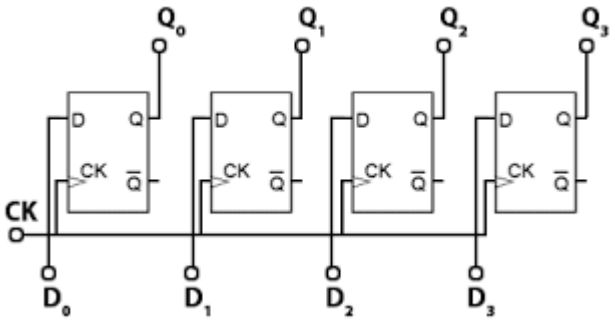
6. Apply one clock pulse

7. Note that the 4-bit data at parallel inputs appears at the parallel output pins Q3, Q2, Q1, Q0 respectively.

Conclusion: Working 4-bit PIPO shift registers is verified.

OBSERVATION

Circuit diagram



Truth table:

	INPUTS				OUTPUTS			
Clock	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3
1	1	0	1	1	1	0	1	1
1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	0	1
1	0	0	0	1	0	0	0	1
1	1	1	1	1	1	1	1	1

9. Realization of Boolean function Y= AB + BC + CA

AIM: Realization of Boolean function Y= AB + BC + CA

APPARATUS REQUIRED: Deeds-DCs simulation kit

Procedure:

1. Make the connections as per the circuit diagram.

2. Connect the inputs to input switches.

3. Connect the outputs to the output switches or Output LED's.

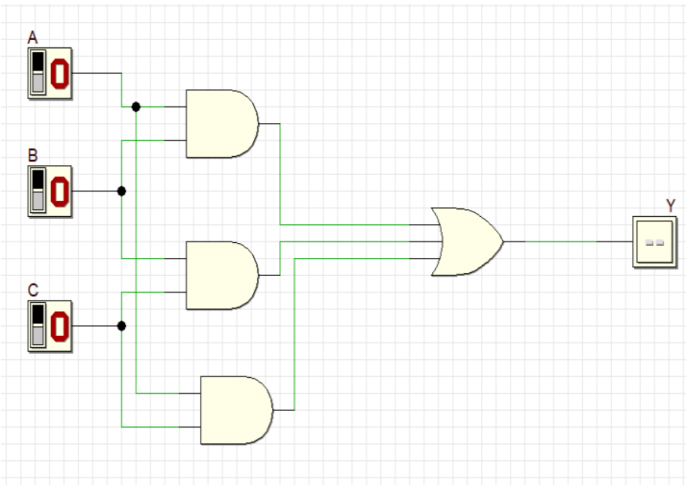
4. Apply various combinations of inputs according to the truth table and observe conditions of the outputs.

5. Note the output Y

Conclusion: The Boolean function Y= AB + BC + CA is verified.

OBSERVATION

Circuit diagram



Truth table:

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

10. Realize Binary to Gray code converter.

AIM: Realize Binary to Gray code converter using basic gates

APPARATUS REQUIRED: Deeds-DCs simulation kit

Procedure:

1. Make the connections as per the circuit diagram.

2. Connect the inputs to input switches.

3. Connect the outputs to the output switches or Output LED's.

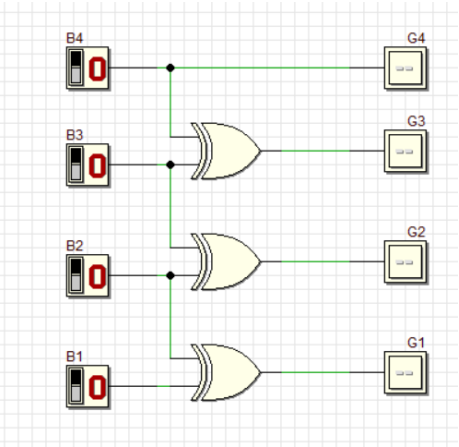
4. Apply various combinations of inputs according to the truth table and observe conditions of the outputs.

5. Note down the outputs.

Conclusion: The realization of binary to gray code is verified.

OBSERVATION

Circuit diagram



Truth table:

Decimal Number	B4	B3	B2	B1	G4	G3	G2	G1
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0