Traffic Light Control System Design

Digital Logic Design Project

September 2, 2025

1 Objective

The objective of this project is to design and simulate a traffic light control system. The system utilizes a clock, D Flip-Flops for sequential logic, and combinational logic for state transitions. The design specifications are as follows:

- Three states for vehicle lights: Red, Yellow, Green.
- Two states for pedestrian lights: Red, Green.

2 State Definitions and Timing

The system operates through three primary states with the following durations:

- **State A:** Vehicle light Green, Pedestrian light Red — 6 seconds.
- **State B:** Vehicle light Yellow, Pedestrian light Red — 2 seconds.
- **State C:** Vehicle light Red, Pedestrian light Green — 2 seconds.

To simplify the circuit design, a clock with a cycle duration of 2 seconds (frequency = 0.5 Hz) is used. The states are mapped to clock cycles as follows:

- `S0`: A (first 2 seconds)
- `S1`: A (second 2 seconds)
- `S2`: A (third 2 seconds)
- `S3`: B (2 seconds)
- `S4`: C (2 seconds)

Thus, State A remains active for 6 seconds (3 clock cycles), while States B and C are active for 2 seconds each.

Note: In the Logisim simulation file, the clock frequency must be set to 0.5 Hz before enabling the clock.

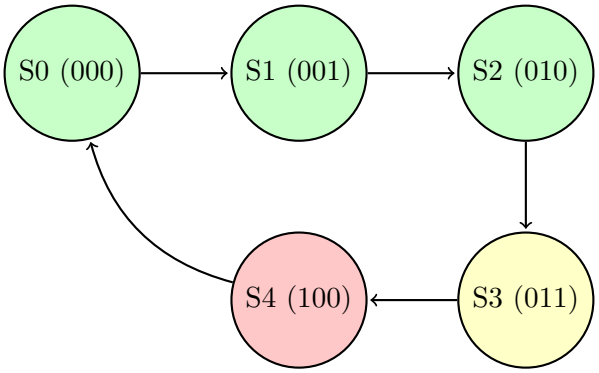
3 State Encoding and Diagram

The system requires 5 states, which are encoded using 3 bits ($Q_2Q_1Q_0$). The state assignments are:

- `S0`: 000
- `S1`: 001
- `S2`: 010
- `S3`: 011
- `S4`: 100

Three D Flip-Flops are used to store the current state ($Q_2Q_1Q_0$) and compute the next state ($D_2D_1D_0$).

3.1 State Diagram



4 Next State Table

The next state and output values are determined from the current state as shown in Table 1.

Table 1: Next State and Output Table

Current State			**Next State**			**Outputs**				
Q_2	Q_1	Q_0	D_2	D_1	D_0	G_v	Y_v	R_v	G_p	R_p
0	0	0	0	0	1	1	0	0	0	1
0	0	1	0	1	0	1	0	0	0	1
0	1	0	0	1	1	1	0	0	0	1
0	1	1	1	0	0	0	1	0	0	1
1	0	0	0	0	0	0	0	1	1	0

Subscripts: v for vehicle, p for pedestrian.

5 Flip-Flop Equations

Using the Sum of Products method on the next state table, the following equations for the D Flip-Flop inputs are derived:

$$
\begin{aligned}
D_2 &= Q_2' \cdot Q_1 \cdot Q_0 \\
D_1 &= Q_2' \cdot Q_1' \cdot Q_0 + Q_2' \cdot Q_1 \cdot Q_0' = Q_2' \cdot (Q_1 \oplus Q_0) \\
D_0 &= Q_2' \cdot Q_1' \cdot Q_0' + Q_2' \cdot Q_1 \cdot Q_0' = Q_2' \cdot Q_0'
\end{aligned}
$$

6 Output Equations

Similarly, the output equations are derived from the next state table:

$$
\begin{aligned}
G_v &= Q_2' \cdot Q_1' \cdot Q_0' + Q_2' \cdot Q_1' \cdot Q_0 + Q_2' \cdot Q_1 \cdot Q_0' \\
&= Q_2' \cdot Q_1' + Q_2' \cdot Q_1 \cdot Q_0' = Q_2'(Q_1' + Q_1 \cdot Q_0) \\
&= Q_2'(Q_1' + Q_0') \\
Y_v &= Q_2' \cdot Q_1 \cdot Q_0 \\
R_v &= Q_2 \cdot Q_1' \cdot Q_0' \\
G_p &= Q_2 \cdot Q_1' \cdot Q_0' \\
R_p &= Q_2' \cdot Q_1' \cdot Q_0' + Q_2' \cdot Q_1 \cdot Q_0 = G_v + Q_2' \cdot Q_1 \cdot Q_0
\end{aligned}
$$

7 System Design and Chronogram

The complete system design, chronogram (timing diagram), simulation examples, and waveform output are detailed in the accompanying documentation.

8 Logical Analysis

Flip-Flops are fundamental components in sequential logic circuits, providing state storage and management. They enable precise state transitions synchronized with clock pulses. The combination of sequential logic (Flip-Flops) and combinational logic (for next-state and output determination) is essential for achieving reliable and efficient circuit behavior in this traffic light control system.