Memory Management-3

CS3600 Spring 2022

Review

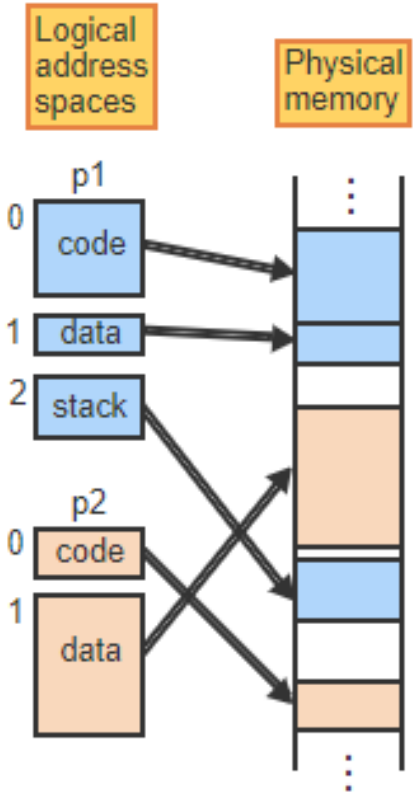
- Paging
  - Pages
  - Frames
- Internal Fragmentation

Segmentation and paging

- Segmentation addresses the problem of variable size, by providing multiple logical address spaces for each process, where each segment can have a different size.

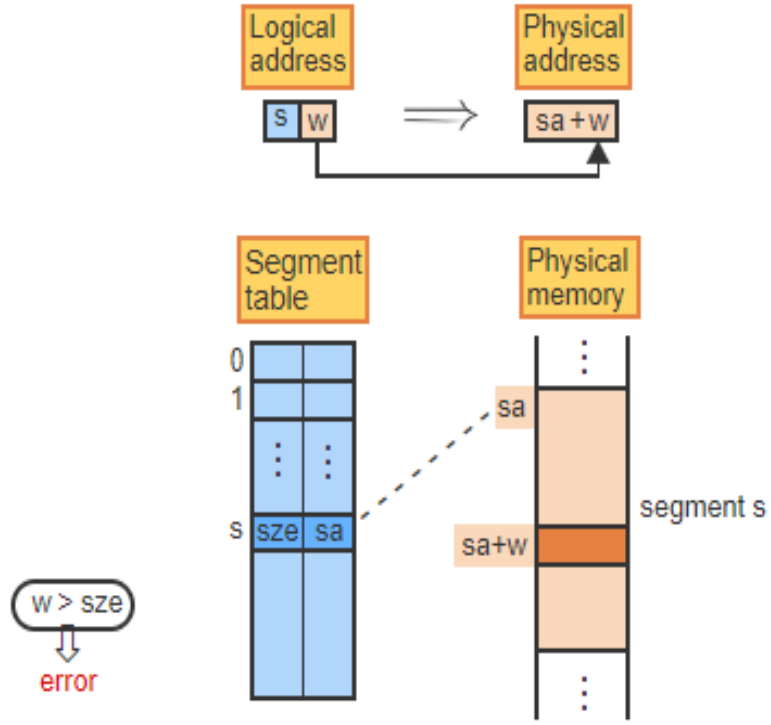
- A ***segment*** is a variable-size block of a logical address space identified by a single number, the segment number.

- A ***segment table*** is an array that keeps track of which segment resides in which area of physical memory. Each entry corresponds to one segment and contains the starting address of the segment.



Segmentation

- **Address translation**
  - Given a logical address (s, w), access the segment table entry at offset s and get the segment's starting address, sa, and size, sze.
  - If w > sze then reject the address as illegal.
  - Otherwise, add w to sa to form the physical address, sa + w, corresponding to the logical address (s, w).



Example

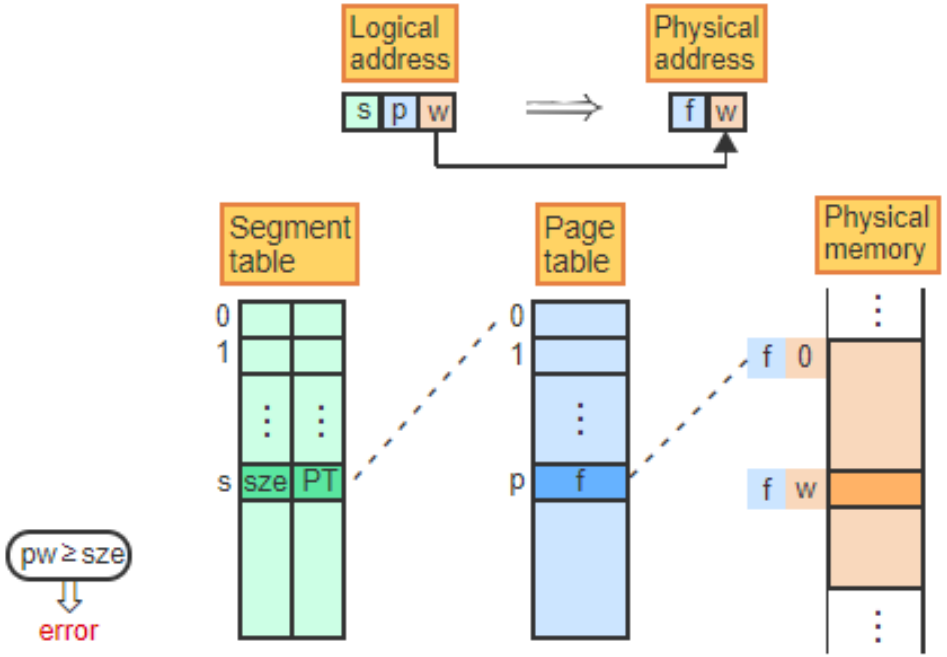
s	size	Address
0	16	30
1	8	5

The logical address (0, 10) will be translated to the physical address _____.

The logical address (0, 16) will be translated to the physical address _____.

Segmentation with paging

- Address translation
  - Given a logical address (s, p, w), access the segment table at s to find the page table and the size, sze, of segment s.
  - If (p, w) > sze then reject the address as illegal. Otherwise, access the page table at p and read the frame number, f, of the frame containing page p.
  - Combine f with the offset w to form the physical address, (f, w).



Example

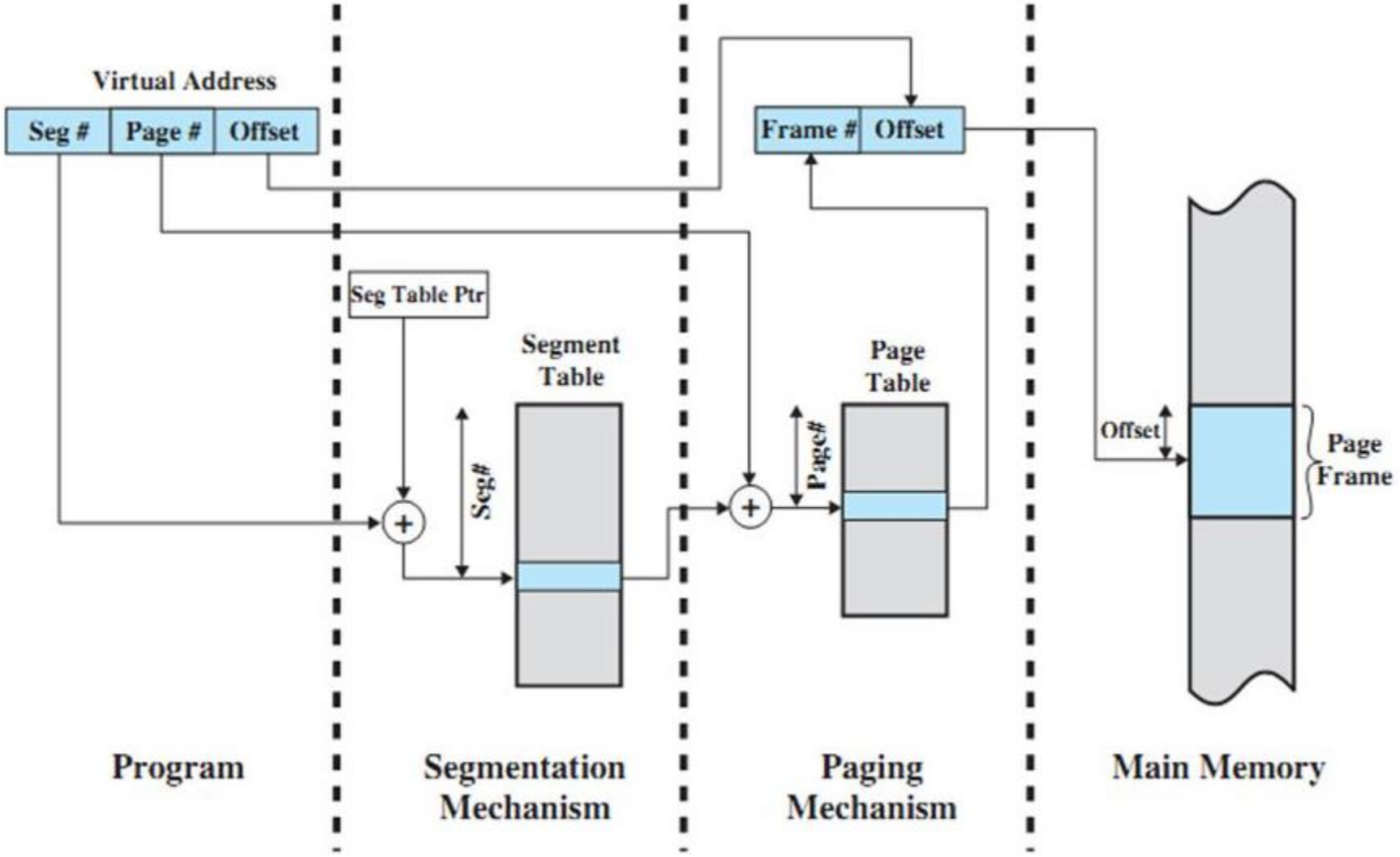
- A logical address has the form (s, p, w), where s consists of 3 bits, p consists of 4 bits, and w consists of 5 bits.

  - The maximum number of segments per process= _____
  - Maximum number of pages per segment=_____
  - Maximum page size (number of words per page) =_____
  - Maximum segment size =_____
  - Maximum size of logical address =_____

Example

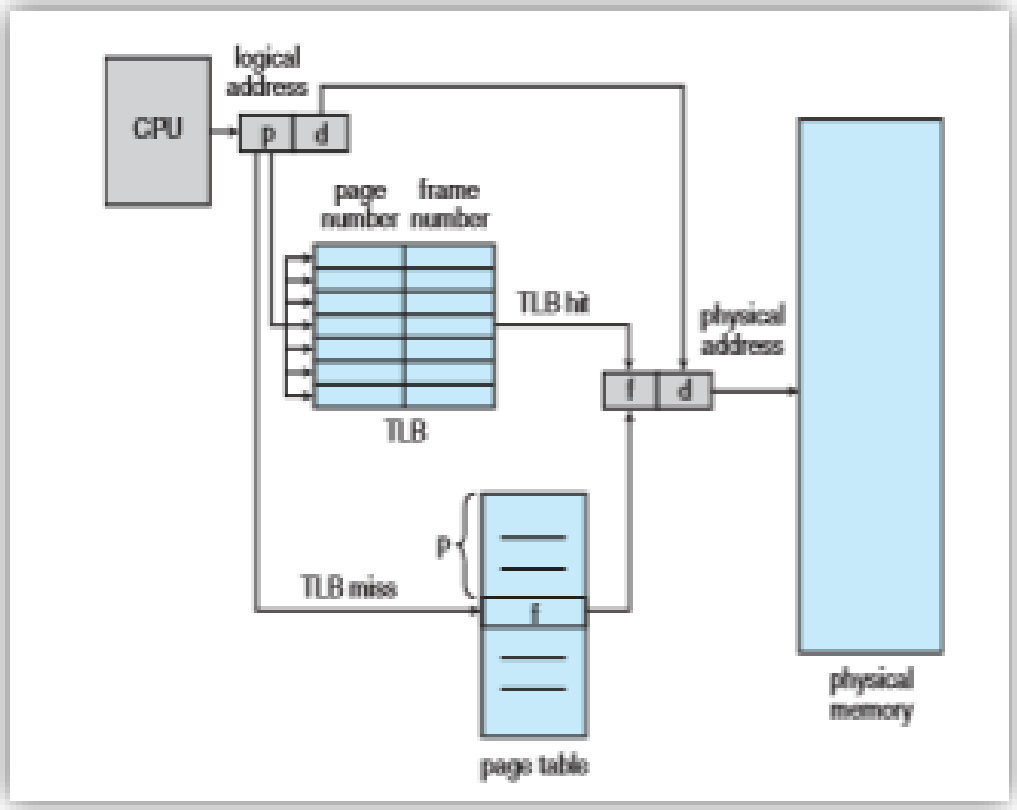
- A segment s has a length of 25 words. The page size is 10 words. Which address is illegal.
  - (s,0,8)
  - (s,1,1)
  - (s,2,1)
  - (s,2,8)

Address Translation



TLB

- Paging and segmentation both double the number of memory accesses because the address translation must first access the segment or page table. When segmentation is combined with paging, the number of memory accesses triples: First the segment table is accessed, then a page table, and finally the page holding the addressed word.
- A ***translation lookaside buffer*** (***TLB***) is a fast associative memory buffer that maintains recent translations of logical addresses to frames in physical memory for faster retrieval.



Worksheet 09

- Complete- Worksheet 09