Stage 5 – CTS

Advvlsi_02

Workarea path:
/project/advvlsi/users/adamsalameh/ws/bitcoin/stage5

Adam Salameh 207534538 adamsalameh@mail.tau.ac.il

Nawaf Gadban 314702705 nawafgadban@mail.tau.ac.il

Anan Break 322663170 ananbreak@mail.tau.ac.il

Sara Abo Salah 208298562 saraabosalah23@mail.tau.ac.il

Lama Metanis 314857152 Lamametanis@mail.tau.ac.il

3.1 Warmup Questions

1. [#P3.1_Q1] What is the main goal of CTS? in your answer also discuss classic CTS and CCD.

Clock Tree Synthesis (CTS) is the process of efficiently distributing the clock signal to sequential elements in an integrated circuit design. The main goals of CTS include achieving uniform clock distribution, minimizing skew (variation in arrival times), optimizing power consumption, and balancing the clock tree. Classic CTS focuses on these objectives. Clock-Clock Distribution (CCD) extends CTS by addressing the distribution of multiple clock domains, handling clock domain crossings, and ensuring domain isolation. CCD aims to accurately route clocks, maintain synchronization during domain transitions, and prevent unwanted interactions between clock domains.

2. [#P3.1_Q2] What is the role of clock buffers in the CTS stage, and how are they optimized to meet design constraints?

Clock buffers play a vital role in Clock Tree Synthesis (CTS) by amplifying and shaping the clock signal for distribution to sequential elements. Optimizing clock buffers in CTS involves several factors. Buffer sizing is adjusted to balance capacitance and delay. Buffer insertion and placement are optimized to minimize delay and skew, while considering power consumption and signal integrity. Clock tree balancing ensures equal delay paths. Power optimization techniques are employed to reduce power consumption. Crosstalk and signal integrity are considered. Overall, optimizing clock buffers in CTS involves sizing, placement, fanout optimization, power reduction, clock tree balancing, and signal integrity considerations.

3. [#P3.1_Q3] Explain the following concepts:

3.1.Skew – global and local

3.2.Jitter

3.3.PLL

Skew: Skew refers to the variation in arrival times of a signal or clock edge. It can be categorized as global skew, which represents the delay difference across the entire chip, and local skew, which represents the delay difference within a specific circuit block. Minimizing skew is important for maintaining synchronization and proper timing in digital circuits.

Jitter: Jitter is the short-term, random variation in the timing of a signal or clock edge. It can be caused by noise, interference, temperature fluctuations, and other factors. Jitter can be classified as random jitter, which is statistically random and follows a Gaussian distribution, and deterministic jitter, which has specific causes and is predictable. Managing jitter is crucial for reliable data transmission and accurate timing in high-speed digital systems.

PLL (Phase-Locked Loop): A PLL is an electronic feedback control system used to generate stable and precise clock signals. It consists of a phase detector, which compares the phase of a reference signal and a VCO output; a VCO, which generates the output clock signal with a frequency controlled by an input voltage; and a low-pass filter, which smooths the error signal from the phase detector. The PLL continuously adjusts the VCO frequency and phase to minimize the phase difference, ensuring stable and synchronized clock signals even in the presence of noise or variations. PLLs are commonly used for clock generation, frequency synthesis, and data communication systems.

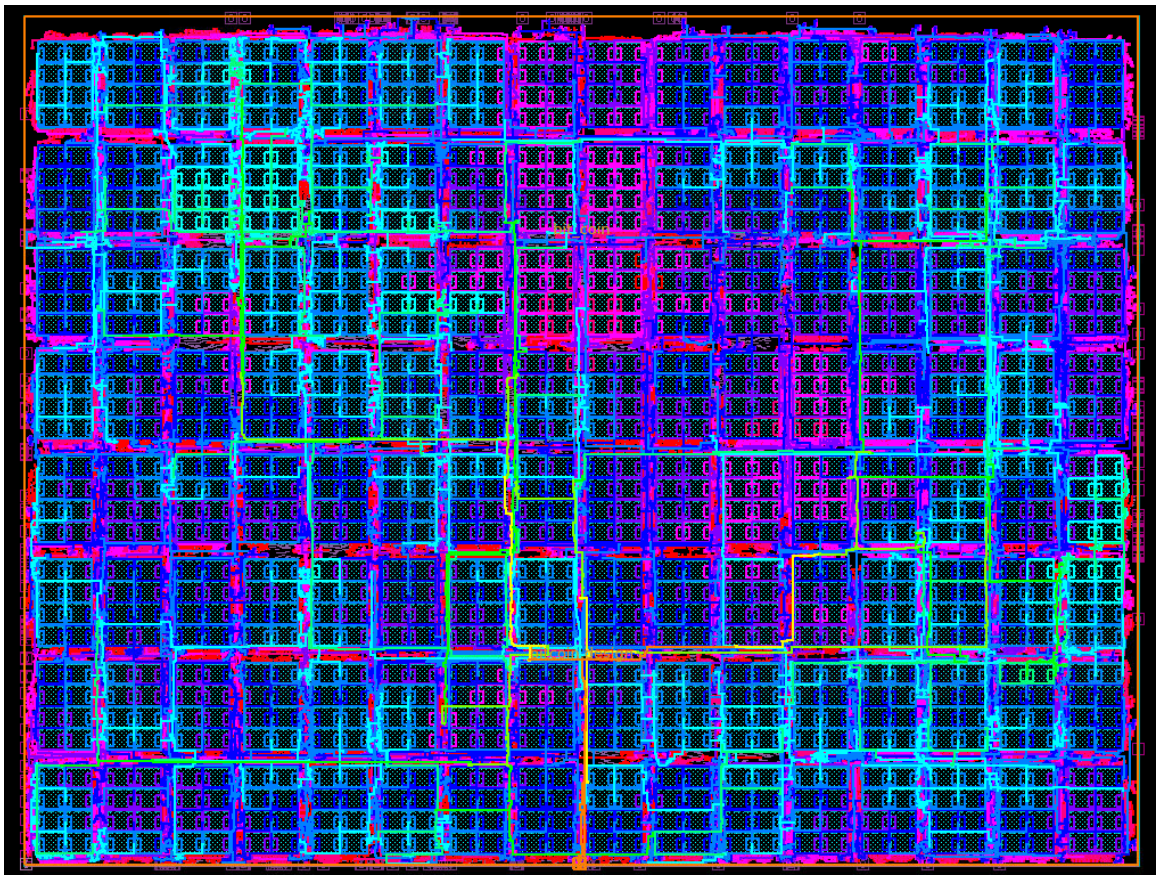
4. [#P3.1_Q4] We discussed during the lecture about several approaches for clock trees. Choose one, describe it and explain its pros and cons (like mesh)

Clock mesh is an alternative clock distribution architecture that replaces the hierarchical clock tree with a mesh network of interconnected clock wires. It offers reduced skew, improved timing, and scalability. However, clock mesh requires more area and power, involves complex design and routing challenges, and may result in potential crosstalk issues. The choice between clock mesh and traditional clock trees depends on specific design requirements and trade-offs.

5. [#P3.1_Q5] What are shielding and spacing techniques regarding the CTS stage?

Shielding and spacing techniques are used in Clock Tree Synthesis (CTS) to mitigate crosstalk and maintain signal integrity. Shielding involves inserting metal layers or ground shields between adjacent clock wires to reduce electromagnetic coupling, while spacing refers to the physical distance between clock wires to minimize coupling capacitance. These techniques are applied during the physical design phase to improve the reliability and accuracy of clock distribution in integrated circuits.

[#P3.2_Q1] Attach a print screen of the clock tree distribution



[#P3.2_Q2] What is the skew of lclk and hclk? Is it high or low in your opinion? Hint: What is the clock period of the design?

```
Report : clock timing
        -type skew
        -nworst 1
        -setup
Design : bit_coin
Version: U-2022.12-SP2
Date   : Tue Jul  4 12:48:30 2023
****************************************
Scenario FUNC_Fast is not configured for setup or hold analysis
Scenario FUNC_Slow is not configured for setup or hold analysis

  Mode: FUNC
  Clock: hclk

  Clock Pin                                          Latency      Skew             Corner
-------------------------------------------------------------------------------------------------
  bit_secure_0/slice_0/hreset_sync/reset_sync_reg/CLK
                                                       0.46              rp-+    Typical
  bit_secure_3/slice_27/sync_add2mem/dut_sync/t_sync_out_reg[2]/CLK
                                                       0.21      0.25    rp-+    Typical

-------------------------------------------------------------------------------------------------

  Mode: FUNC
  Clock: lclk

  Clock Pin                                          Latency      Skew             Corner
-------------------------------------------------------------------------------------------------
  bit_secure_3/slice_14/sipo_bit/tmp_reg[4]/CLK        0.63              rp-+    Typical
  bit_secure_3/slice_14/sipo_bit/pout_reg[4]/CLK       0.30      0.33    rp-+    Typical

-------------------------------------------------------------------------------------------------
1
fc_shell>
```

```
Clock          Period   Waveform            Attrs     Sources
-------------------------------------------------------------------------------
hclk             1.00   {0 0.5}             p         {hclk}
lclk             1.00   {0 0.5}             p         {lclk}
```

CTS aims to minimize skew and achieve a balanced clock distribution.
As we can see the skew of LCLK and HCLK are relatively low. Which indicates a successful and well-optimized CTS process.

[#P3.2_Q3] Attach a print screen of each clock (lclk and hclk).