Stage 4 – Placement

Advvlsi_02

Workarea path: /project/advvlsi/users/adamsalameh/ws/bitcoin/stage4

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3.1 Warmup Questions – Placement

1 .[#P3.1_Q1] What is the difference between Placement and Floorplanning in physical design？

- Floorplanning: It is an early stage in the physical design process that involves dividing the chip area into functional blocks, determining their approximate sizes and locations, and defining interconnections. Floorplanning focuses on macro-level decisions, such as overall chip structure, block partitioning, clock and power distribution, and I/O locations.

- Placement: Placement occurs after floorplanning and involves the detailed positioning of individual components within each block. It determines the precise locations of components, considering timing, power, and area constraints. Placement algorithms aim to minimize wirelength, optimize signal integrity, and meet timing requirements. It focuses on the micro-level decisions of component placement and logical connectivity.

In essence, floorplanning focuses on the high-level organization and partitioning of the chip, while placement deals with the detailed placement of individual components within each block. Both stages are important in achieving an optimal chip layout and ensuring the design meets performance, power, and area goals.

2 .[#P3.1_Q2] What are some of the common techniques used in Placement optimization？

1. Analytical Placement: Mathematical optimization algorithms are used to find an optimal or near-optimal placement solution by considering factors like wirelength, congestion, and timing constraints.

2. Force-Directed Placement: Components are treated as particles connected by springs, and forces such as electrical net forces and repulsive forces are applied to achieve global wirelength minimization and balance.

3. Hybrid Placement: Combining different algorithms or approaches to improve placement results, such as starting with analytical placement and refining with iterative techniques.

4. Congestion-Driven Placement: Considers congestion levels to spread out highly congested areas and optimize routing resources, improving signal integrity and routing quality.

5. Timing-Driven Placement: Focuses on meeting timing constraints by considering interconnect wire delays and using timing analysis data to guide the placement process.

6. Hierarchical Placement: Divides the design into smaller hierarchical blocks or clusters, allowing better control over timing, power, and congestion by optimizing individual blocks first before integrating them.

3 .[#P3.1_Q3] What is simulated annealing in the context of the placement stage? Explain how the algorithm works, what are the hyperparameters included?

Simulated annealing is a metaheuristic optimization algorithm used in the placement stage of physical design. It mimics the annealing process in metallurgy to search for an optimal or near-optimal placement solution.

The algorithm works as follows:

1. Initialization: Generate an initial placement solution.

2. Define a temperature schedule: Gradually decrease the temperature over iterations.

3. Iteration: Perturb the current solution, evaluate the new solution, and accept it based on a probability determined by the temperature and a probability distribution function.

4. Update temperature: Decrease the temperature according to the temperature schedule.

5. Repeat the iteration until a stopping criterion is met.

6. Return the best solution found during the iterations.

Simulated annealing includes hyperparameters such as the initial temperature, cooling schedule, number of iterations, and probability distribution function. Tuning these hyperparameters is important for effective exploration and convergence.

Warmup Questions – Advanced STA

1.1.[#P3.3_Q1] Which type of timing violation can be more critical – setup or hold?

- **Setup Violation**: A setup violation occurs when data is not stable before the clock edge arrives. It can lead to incorrect data capture in flip-flops or latches, causing functional errors. Setup violations are typically considered more critical due to their direct impact on circuit functionality.

- **Hold Violation**: A hold violation occurs when data changes too quickly after the clock edge, potentially causing metastability. While hold violations can lead to unpredictable behavior, their impact is generally less severe than setup violations.

Setup violations are generally considered more critical than hold violations due to their direct impact on functional correctness and the stricter timing requirements. Hold violations may lead to metastability, but their consequences can be mitigated through careful design techniques and timing margins.

1.2.[#P3.3_Q2] Suggest 3 ways to fix a setup violation

1. Clock Skew Adjustment: By adjusting the clock skew, you can control the arrival time of the clock signal at different circuit components, helping to meet the setup requirements. This can involve inserting delay elements or buffering the clock signal strategically to balance the timing paths.

2. Critical Path Optimization: Identify and optimize the critical paths causing the setup violation. Techniques such as gate resizing, gate replacement, or logic restructuring can be employed to reduce overall delay and improve timing.

3. Pipelining: Introduce pipeline stages to break down long combinational paths into smaller segments with flip-flops in between. Pipelining allows more time for data stabilization before being captured, effectively mitigating setup violations.

1.3.[#P3.3_Q3] How can a hold violation be created in a digital design.

1. Unbalanced Delays: Hold violations can arise when there is a significant imbalance in the delays of different paths in the circuit. If the delay of the data path is much smaller than the delay of the clock path, it can lead to hold violations. The data transitions may not be held long enough for proper capture in the flip-flop or latch.

2. Clock Skew: Clock skew, which refers to the variation in arrival times of the clock signal at different elements of the circuit, can contribute to hold violations. If the clock signal arrives at different components at significantly different times, it can result in hold time violations.

3. Synchronous Inputs: Hold violations can occur when synchronous inputs (e.g., enable signals) are changing close to the active edge of the clock. If the setup and hold requirements of these inputs are not met, it can lead to hold violations.

4. Propagation Delays: Hold violations can be created by long combinational paths or logic elements with significant propagation delays. When the data changes shortly after the active edge of the clock, the previous data may not be held long enough for reliable capture.

5. Process Variations: Variations in manufacturing processes can introduce differences in transistor characteristics, resulting in variations in delays. These process variations can contribute to hold violations, especially in cases where the delays are at the edge of meeting hold time requirements.

To address hold violations, various techniques can be employed, such as buffering the data path, balancing delays, optimizing critical paths, adjusting clocking schemes, or introducing additional pipeline stages. The specific approach will depend on the design, constraints, and desired trade-offs between timing, area, and power considerations. Careful analysis, simulation, and optimization are necessary to ensure hold time requirements are met and reliable operation of the circuit is achieved.

1.4.[#P3.3_Q4] Suggest 3 ways to fix a hold violation.

1. Delay Insertion: Adding additional delay elements, such as buffers or inverters, in the data path to increase the propagation delay and satisfy the hold time requirement.

2. Clock Delay: Adjusting the timing of the clock signal by introducing deliberate delays in the clock path to align the arrival times of the data and clock signals, ensuring proper data holding before the clock edge.

3. Pipeline Insertion: Introducing pipeline stages with flip-flops to break down long combinational paths, allowing more time for the data to stabilize before being captured. Pipelining reduces the criticality of hold violations by introducing synchronization points.

3.4 Advanced STA

2 .[#P3.4_Q1] Analyze the timing reports extracted and find 2 problematic paths. For each

path:

3.1.Note the path type (setup / hold).

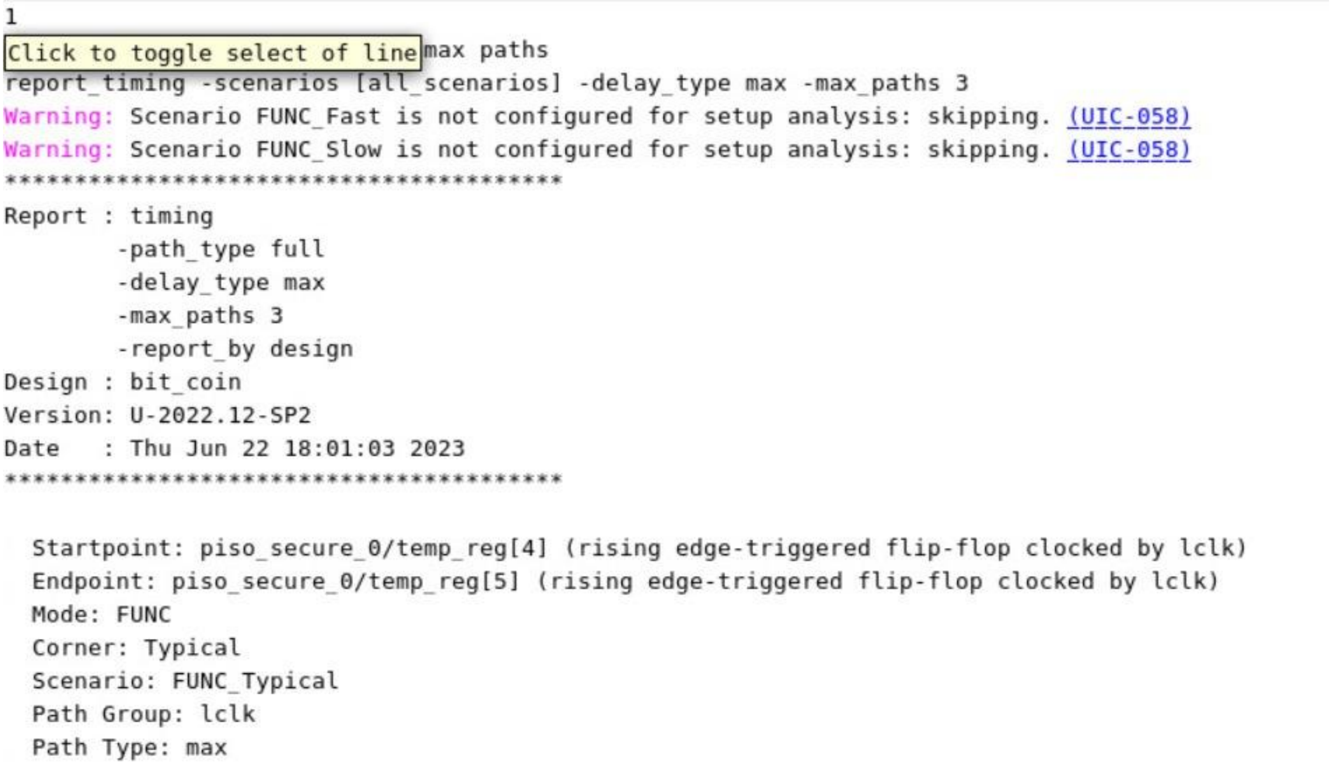
3.2.Add a screenshot of the report [Tip: get the screen shots from shell window and not

from the gui window for better scaling[

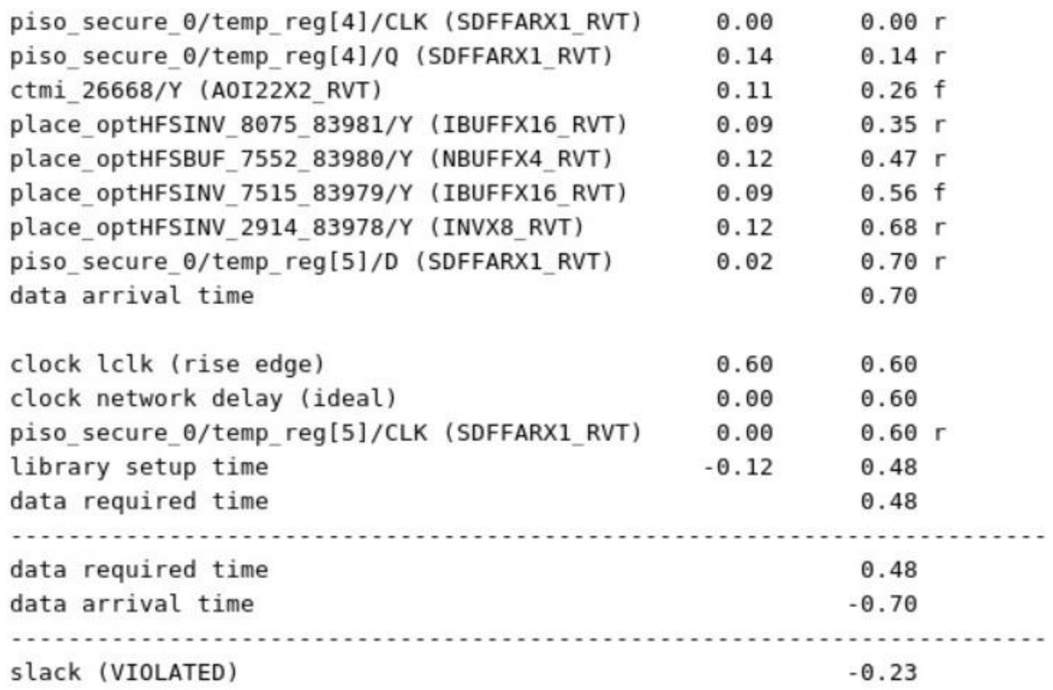
3.3.Add a screen shot of the path over the layout. Use the command from stage 1:

3.4.Add a screen shot of the path as a schematic view.

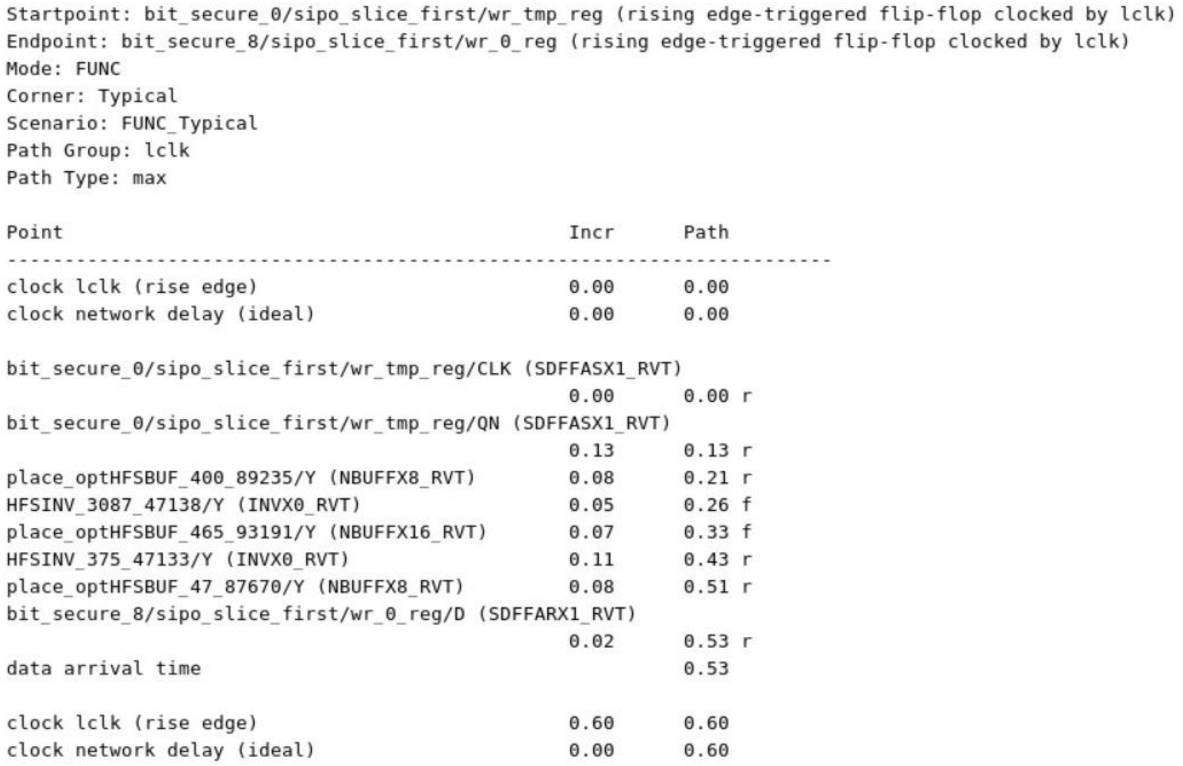
Max delay reports (setup).



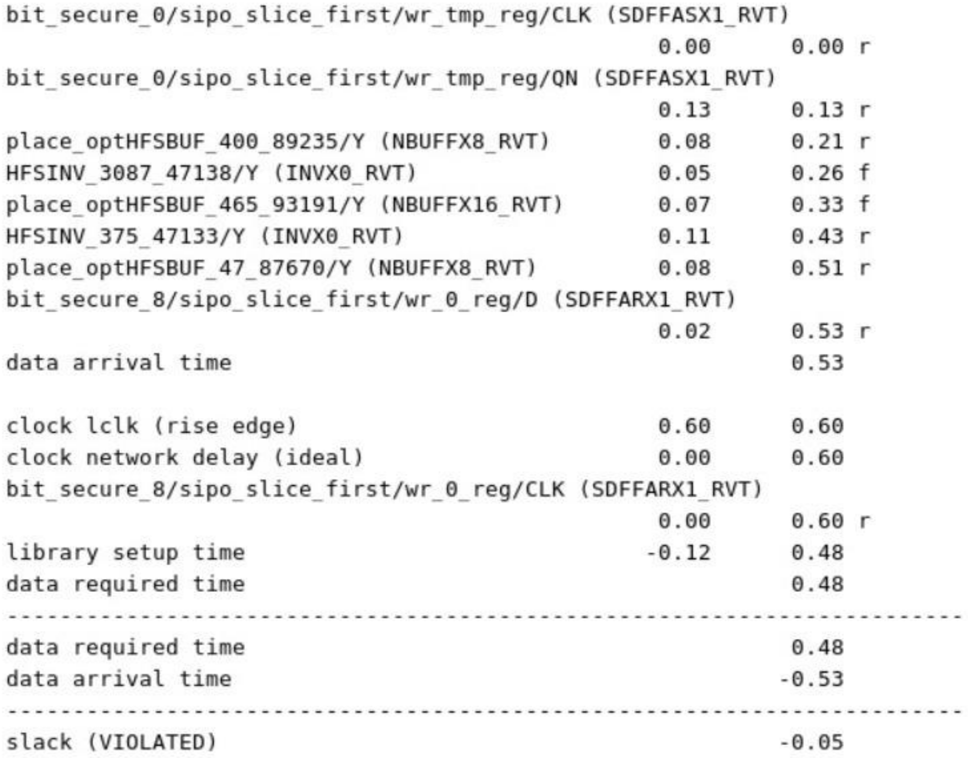
```
1
Click to toggle select of linemax paths
report_timing -scenarios [all_scenarios] -delay_type max -max_paths 3
Warning: Scenario FUNC_Fast is not configured for setup analysis: skipping. (UIC-058)
Warning: Scenario FUNC_Slow is not configured for setup analysis: skipping. (UIC-058)
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 3
        -report_by design
Design : bit_coin
Version: U-2022.12-SP2
Date   : Thu Jun 22 18:01:03 2023
****************************************

  Startpoint: piso_secure_0/temp_reg[4] (rising edge-triggered flip-flop clocked by lclk)
  Endpoint: piso_secure_0/temp_reg[5] (rising edge-triggered flip-flop clocked by lclk)
  Mode: FUNC
  Corner: Typical
  Scenario: FUNC_Typical
  Path Group: lclk
  Path Type: max
```



```
piso_secure_0/temp_reg[4]/CLK (SDFFARX1_RVT)     0.00       0.00 r
piso_secure_0/temp_reg[4]/Q (SDFFARX1_RVT)       0.14       0.14 r
ctmi_26668/Y (AOI22X2_RVT)                       0.11       0.26 f
place_optHFSINV_8075_83981/Y (IBUFFX16_RVT)      0.09       0.35 r
place_optHFSBUF_7552_83980/Y (NBUFFX4_RVT)       0.12       0.47 r
place_optHFSINV_7515_83979/Y (IBUFFX16_RVT)      0.09       0.56 f
place_optHFSINV_2914_83978/Y (INVX8_RVT)         0.12       0.68 r
piso_secure_0/temp_reg[5]/D (SDFFARX1_RVT)       0.02       0.70 r
data arrival time                                           0.70

clock lclk (rise edge)                           0.60       0.60
clock network delay (ideal)                      0.00       0.60
piso_secure_0/temp_reg[5]/CLK (SDFFARX1_RVT)     0.00       0.60 r
library setup time                              -0.12       0.48
data required time                                          0.48
------------------------------------------------------------------------
data required time                                          0.48
data arrival time                                          -0.70
------------------------------------------------------------------------
slack (VIOLATED)                                           -0.23
```

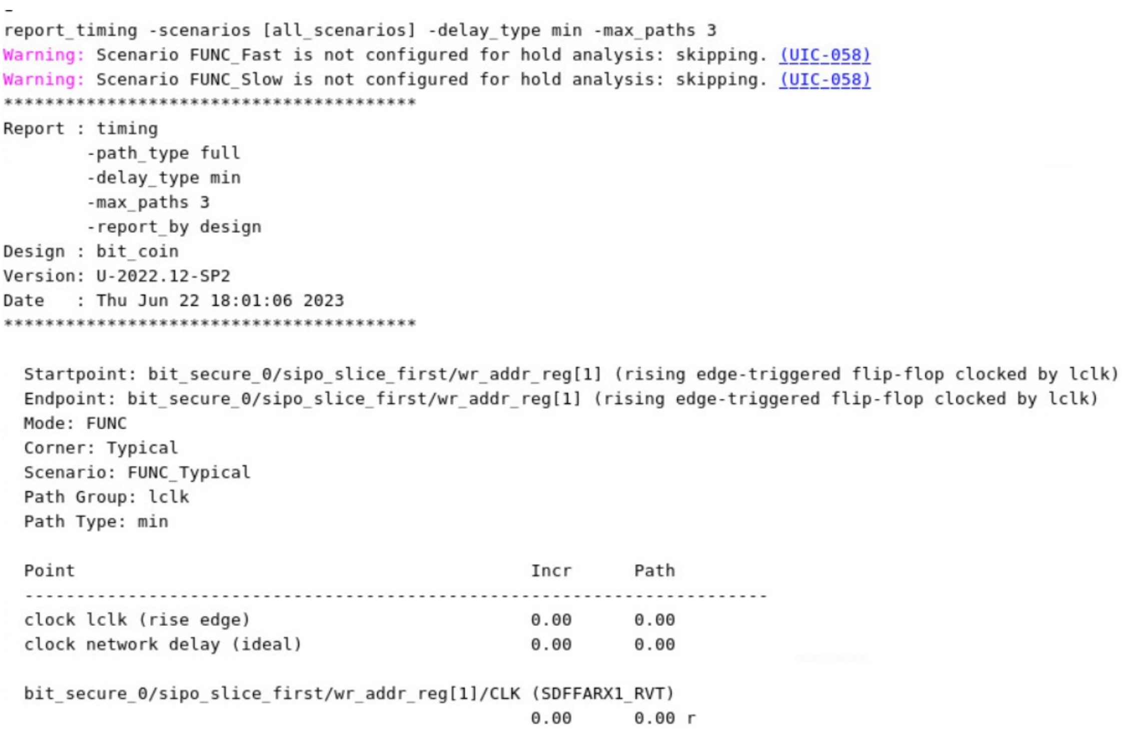


```
Startpoint: bit_secure_0/sipo_slice_first/wr_tmp_reg (rising edge-triggered flip-flop clocked by lclk)
Endpoint: bit_secure_8/sipo_slice_first/wr_0_reg (rising edge-triggered flip-flop clocked by lclk)
Mode: FUNC
Corner: Typical
Scenario: FUNC_Typical
Path Group: lclk
Path Type: max

Point                                            Incr       Path
------------------------------------------------------------------------
clock lclk (rise edge)                           0.00       0.00
clock network delay (ideal)                      0.00       0.00

bit_secure_0/sipo_slice_first/wr_tmp_reg/CLK (SDFFASX1_RVT)
                                                 0.00       0.00 r
bit_secure_0/sipo_slice_first/wr_tmp_reg/QN (SDFFASX1_RVT)
                                                 0.13       0.13 r
place_optHFSBUF_400_89235/Y (NBUFFX8_RVT)        0.08       0.21 r
HFSINV_3087_47138/Y (INVX0_RVT)                  0.05       0.26 f
place_optHFSBUF_465_93191/Y (NBUFFX16_RVT)       0.07       0.33 f
HFSINV_375_47133/Y (INVX0_RVT)                   0.11       0.43 r
place_optHFSBUF_47_87670/Y (NBUFFX8_RVT)         0.08       0.51 r
bit_secure_8/sipo_slice_first/wr_0_reg/D (SDFFARX1_RVT)
                                                 0.02       0.53 r
data arrival time                                           0.53

clock lclk (rise edge)                           0.60       0.60
clock network delay (ideal)                      0.00       0.60
```

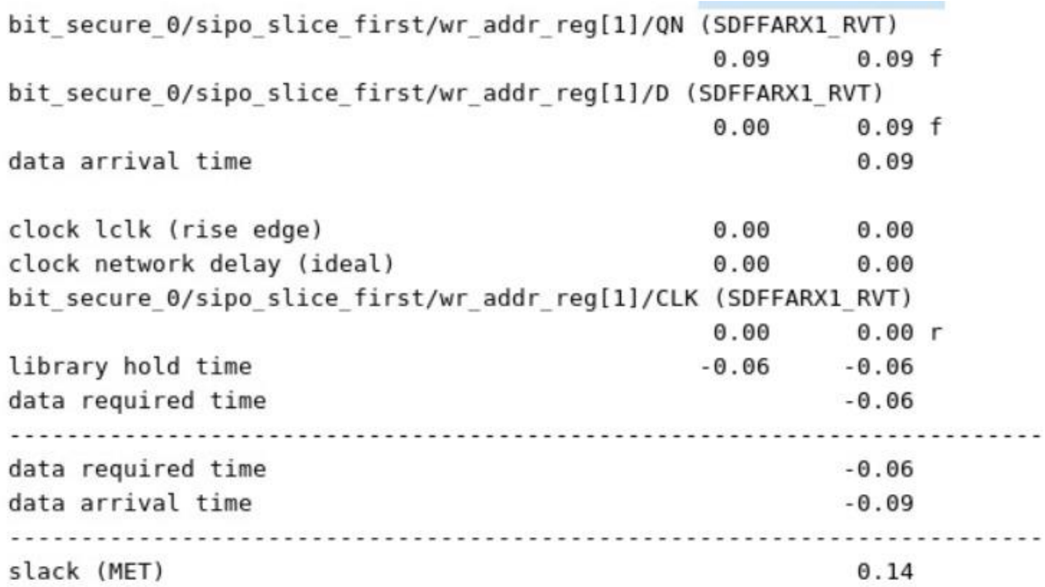


```
bit_secure_0/sipo_slice_first/wr_tmp_reg/CLK (SDFFASX1_RVT)
                                                 0.00      0.00 r
bit_secure_0/sipo_slice_first/wr_tmp_reg/QN (SDFFASX1_RVT)
                                                 0.13      0.13 r
place_optHFSBUF_400_89235/Y (NBUFFX8_RVT)        0.08      0.21 r
HFSINV_3087_47138/Y (INVX0_RVT)                  0.05      0.26 f
place_optHFSBUF_465_93191/Y (NBUFFX16_RVT)       0.07      0.33 f
HFSINV_375_47133/Y (INVX0_RVT)                   0.11      0.43 r
place_optHFSBUF_47_87670/Y (NBUFFX8_RVT)         0.08      0.51 r
bit_secure_8/sipo_slice_first/wr_0_reg/D (SDFFARX1_RVT)
                                                 0.02      0.53 r
data arrival time                                          0.53

clock lclk (rise edge)                           0.60      0.60
clock network delay (ideal)                      0.00      0.60
bit_secure_8/sipo_slice_first/wr_0_reg/CLK (SDFFARX1_RVT)
                                                 0.00      0.60 r
library setup time                              -0.12      0.48
data required time                                         0.48
------------------------------------------------------------------------
data required time                                         0.48
data arrival time                                         -0.53
------------------------------------------------------------------------
slack (VIOLATED)                                          -0.05
```

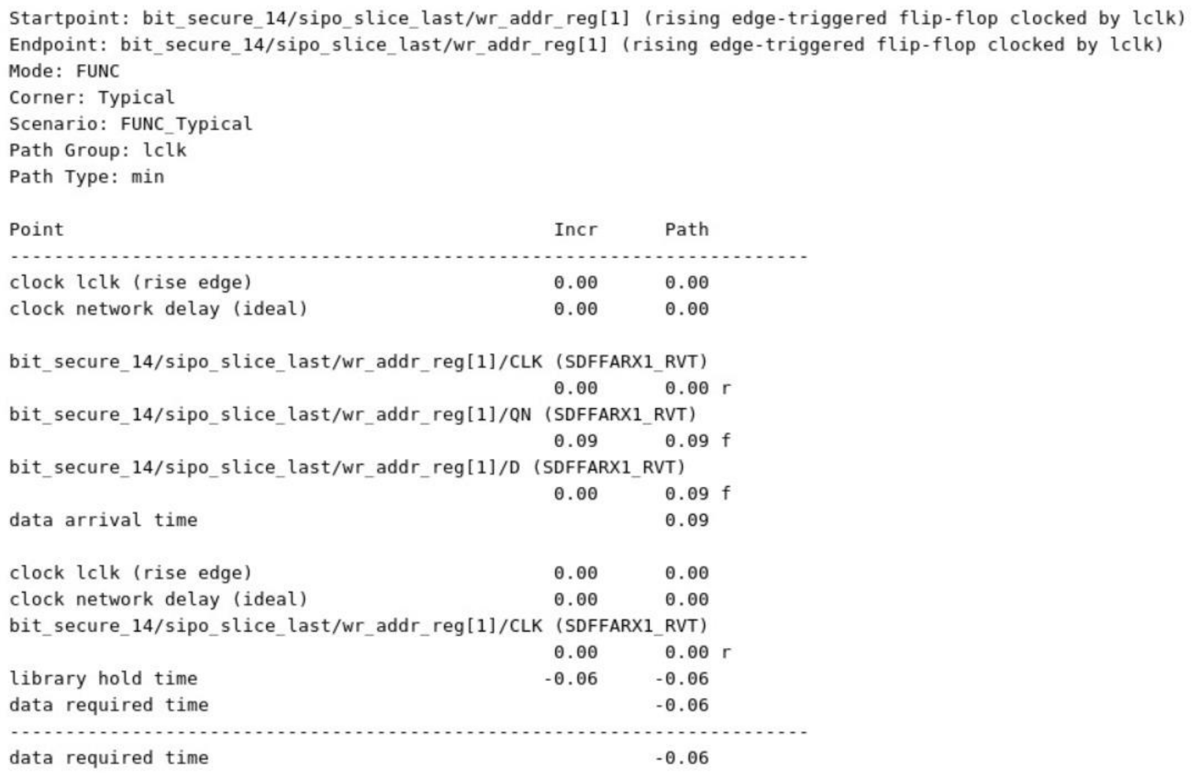
min delay reports (hold).



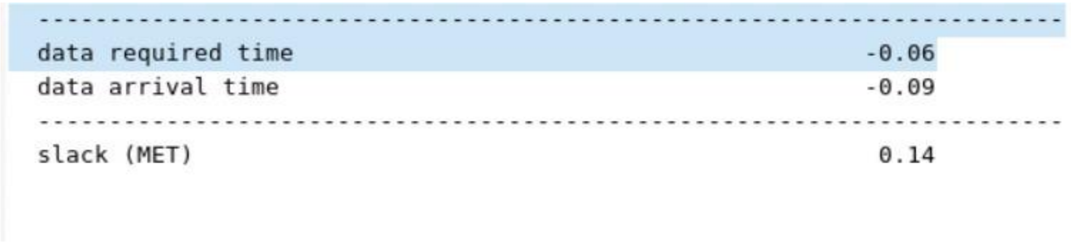
```
-
report_timing -scenarios [all_scenarios] -delay_type min -max_paths 3
Warning: Scenario FUNC_Fast is not configured for hold analysis: skipping. (UIC-058)
Warning: Scenario FUNC_Slow is not configured for hold analysis: skipping. (UIC-058)
****************************************
Report : timing
        -path_type full
        -delay_type min
        -max_paths 3
        -report_by design
Design : bit_coin
Version: U-2022.12-SP2
Date   : Thu Jun 22 18:01:06 2023
****************************************

  Startpoint: bit_secure_0/sipo_slice_first/wr_addr_reg[1] (rising edge-triggered flip-flop clocked by lclk)
  Endpoint: bit_secure_0/sipo_slice_first/wr_addr_reg[1] (rising edge-triggered flip-flop clocked by lclk)
  Mode: FUNC
  Corner: Typical
  Scenario: FUNC_Typical
  Path Group: lclk
  Path Type: min

  Point                                            Incr      Path
  ------------------------------------------------------------------------
  clock lclk (rise edge)                           0.00      0.00
  clock network delay (ideal)                      0.00      0.00

  bit_secure_0/sipo_slice_first/wr_addr_reg[1]/CLK (SDFFARX1_RVT)
                                                   0.00      0.00 r
```



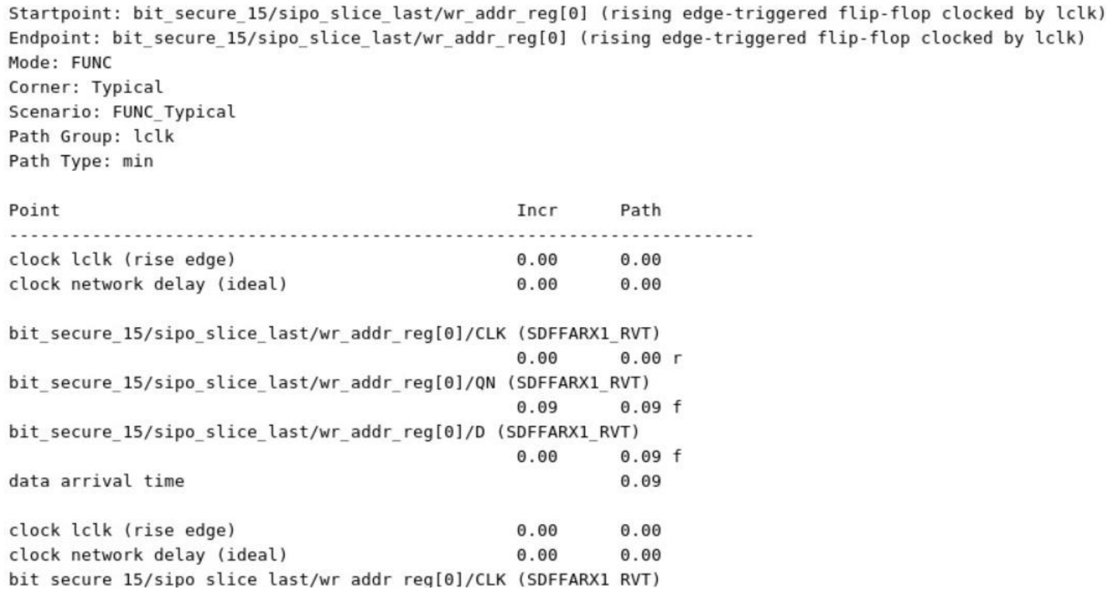
```
  bit_secure_0/sipo_slice_first/wr_addr_reg[1]/QN (SDFFARX1_RVT)
                                                   0.09      0.09 f
  bit_secure_0/sipo_slice_first/wr_addr_reg[1]/D (SDFFARX1_RVT)
                                                   0.00      0.09 f
  data arrival time                                          0.09

  clock lclk (rise edge)                           0.00      0.00
  clock network delay (ideal)                      0.00      0.00
  bit_secure_0/sipo_slice_first/wr_addr_reg[1]/CLK (SDFFARX1_RVT)
                                                   0.00      0.00 r
  library hold time                               -0.06     -0.06
  data required time                                        -0.06
  ------------------------------------------------------------------------
  data required time                                        -0.06
  data arrival time                                         -0.09
  ------------------------------------------------------------------------
  slack (MET)                                                0.14
```



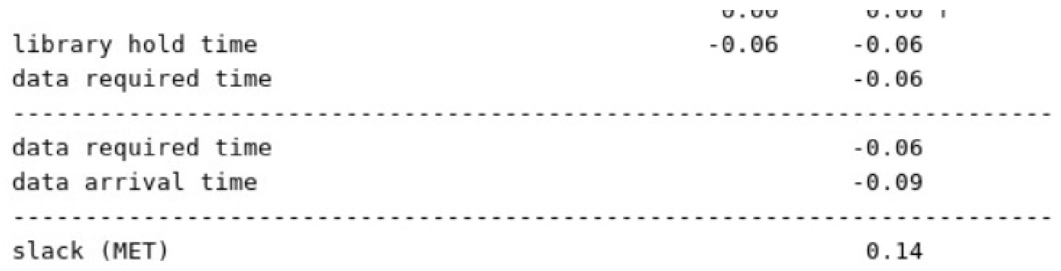
```
Startpoint: bit_secure_14/sipo_slice_last/wr_addr_reg[1] (rising edge-triggered flip-flop clocked by lclk)
Endpoint: bit_secure_14/sipo_slice_last/wr_addr_reg[1] (rising edge-triggered flip-flop clocked by lclk)
Mode: FUNC
Corner: Typical
Scenario: FUNC_Typical
Path Group: lclk
Path Type: min

Point                                               Incr      Path
------------------------------------------------------------------------
clock lclk (rise edge)                              0.00      0.00
clock network delay (ideal)                         0.00      0.00

bit_secure_14/sipo_slice_last/wr_addr_reg[1]/CLK (SDFFARX1_RVT)
                                                    0.00      0.00 r
bit_secure_14/sipo_slice_last/wr_addr_reg[1]/QN (SDFFARX1_RVT)
                                                    0.09      0.09 f
bit_secure_14/sipo_slice_last/wr_addr_reg[1]/D (SDFFARX1_RVT)
                                                    0.00      0.09 f
data arrival time                                             0.09

clock lclk (rise edge)                              0.00      0.00
clock network delay (ideal)                         0.00      0.00
bit_secure_14/sipo_slice_last/wr_addr_reg[1]/CLK (SDFFARX1_RVT)
                                                    0.00      0.00 r
library hold time                                  -0.06     -0.06
data required time                                           -0.06
------------------------------------------------------------------------
data required time                                           -0.06
```



```
------------------------------------------------------------------------
data required time                                           -0.06
data arrival time                                            -0.09
------------------------------------------------------------------------
slack (MET)                                                   0.14
```



```
Startpoint: bit_secure_15/sipo_slice_last/wr_addr_reg[0] (rising edge-triggered flip-flop clocked by lclk)
Endpoint: bit_secure_15/sipo_slice_last/wr_addr_reg[0] (rising edge-triggered flip-flop clocked by lclk)
Mode: FUNC
Corner: Typical
Scenario: FUNC_Typical
Path Group: lclk
Path Type: min

Point                                               Incr      Path
------------------------------------------------------------------------
clock lclk (rise edge)                              0.00      0.00
clock network delay (ideal)                         0.00      0.00

bit_secure_15/sipo_slice_last/wr_addr_reg[0]/CLK (SDFFARX1_RVT)
                                                    0.00      0.00 r
bit_secure_15/sipo_slice_last/wr_addr_reg[0]/QN (SDFFARX1_RVT)
                                                    0.09      0.09 f
bit_secure_15/sipo_slice_last/wr_addr_reg[0]/D (SDFFARX1_RVT)
                                                    0.00      0.09 f
data arrival time                                             0.09

clock lclk (rise edge)                              0.00      0.00
clock network delay (ideal)                         0.00      0.00
bit_secure_15/sipo_slice_last/wr_addr_reg[0]/CLK (SDFFARX1_RVT)
```



```
                                                     0.00      0.00 r
  library hold time                                 -0.06     -0.06
  data required time                                          -0.06
  -----------------------------------------------------------------------
  data required time                                          -0.06
  data arrival time                                           -0.09
  -----------------------------------------------------------------------
  slack (MET)                                                  0.14
```

Just to make sure here is all the timing reports as a text:

report_timing -scenarios [all_scenarios] -delay_type max -max_paths 3

Warning: Scenario FUNC_Fast is not configured for setup analysis: skipping. (UIC-058)

Warning: Scenario FUNC_Slow is not configured for setup analysis: skipping. (UIC-058)

****

Report : timing

path_type full-

delay_type max-

max_paths 3-

report_by design-

Design : bit_coin

Version: U-2022.12-SP2

Date   : Thu Jun 22 18:01:03 2023

****

Startpoint: piso_secure_0/temp_reg[4] (rising edge-triggered flip-flop clocked by lclk)

Endpoint: piso_secure_0/temp_reg[5] (rising edge-triggered flip-flop clocked by lclk)

Mode: FUNC

Corner: Typical

Scenario: FUNC_Typical

Path Group: lclk

Path Type: max

Point   Incr   Path

```
---------------------------------------------------------------------------

clock lclk (rise edge)                        0.00     0.00

clock network delay (ideal)                   0.00     0.00


piso_secure_0/temp_reg[4]/CLK (SDFFARX1_RVT)     0.00     0.00 r

piso_secure_0/temp_reg[4]/Q (SDFFARX1_RVT)       0.14     0.14 r

ctmi_26668/Y (AOI22X2_RVT)                       0.11     0.26 f

place_optHFSINV_8075_83981/Y (IBUFFX16_RVT)      0.09     0.35 r

place_optHFSBUF_7552_83980/Y (NBUFFX4_RVT)       0.12     0.47 r

place_optHFSINV_7515_83979/Y (IBUFFX16_RVT)      0.09     0.56 f

place_optHFSINV_2914_83978/Y (INVX8_RVT)         0.12     0.68 r

piso_secure_0/temp_reg[5]/D (SDFFARX1_RVT)       0.02     0.70 r

data arrival time                                 0.70


clock lclk (rise edge)                        0.60     0.60

clock network delay (ideal)                   0.00     0.60

piso_secure_0/temp_reg[5]/CLK (SDFFARX1_RVT)     0.00     0.60 r

library setup time                           -0.12     0.48

data required time                                0.48

---------------------------------------------------------------------------

data required time                                0.48

data arrival time                                -0.70

---------------------------------------------------------------------------

slack (VIOLATED)                                 -0.23
```

Startpoint: bit_secure_0/sipo_slice_first/wr_tmp_reg (rising edge-triggered flip-flop clocked by lclk)

Endpoint: bit_secure_8/sipo_slice_first/wr_0_reg (rising edge-triggered flip-flop clocked by lclk)

Mode: FUNC

```
Corner: Typical

Scenario: FUNC_Typical

Path Group: lclk

Path Type: max


Point                              Incr      Path

----------------------------------------------------------------------

clock lclk (rise edge)                  0.00      0.00

clock network delay (ideal)                  0.00      0.00


bit_secure_0/sipo_slice_first/wr_tmp_reg/CLK (SDFFASX1_RVT)

r 0.00       0.00

bit_secure_0/sipo_slice_first/wr_tmp_reg/QN (SDFFASX1_RVT)

r 0.13       0.13

place_optHFSBUF_400_89235/Y (NBUFFX8_RVT)       0.08      0.21 r

HFSINV_3087_47138/Y (INVX0_RVT)                0.05      0.26 f

place_optHFSBUF_465_93191/Y (NBUFFX16_RVT)       0.07      0.33 f

HFSINV_375_47133/Y (INVX0_RVT)                 0.11      0.43 r

place_optHFSBUF_47_87670/Y (NBUFFX8_RVT)        0.08      0.51 r

bit_secure_8/sipo_slice_first/wr_0_reg/D (SDFFARX1_RVT)

r 0.53       0.02

data arrival time                              0.53


clock lclk (rise edge)                  0.60      0.60

clock network delay (ideal)                  0.00      0.60

bit_secure_8/sipo_slice_first/wr_0_reg/CLK (SDFFARX1_RVT)

r 0.60       0.00

library setup time                     -0.12      0.48

data required time                               0.48

----------------------------------------------------------------------

data required time                               0.48
data arrival time                              -0.53
---------------------------------------------------------------------
slack (VIOLATED)                                -0.05



Startpoint: bit_secure_0/sipo_slice_first/wr_tmp_reg (rising edge-triggered flip-flop clocked by lclk)
Endpoint: bit_secure_6/sipo_slice_first/wr_0_reg (rising edge-triggered flip-flop clocked by lclk)
Mode: FUNC
Corner: Typical
Scenario: FUNC_Typical
Path Group: lclk
Path Type: max

Point                                   Incr     Path
---------------------------------------------------------------------
clock lclk (rise edge)                       0.00     0.00
clock network delay (ideal)                     0.00     0.00

bit_secure_0/sipo_slice_first/wr_tmp_reg/CLK (SDFFASX1_RVT)
r 0.00      0.00
bit_secure_0/sipo_slice_first/wr_tmp_reg/QN (SDFFASX1_RVT)
r 0.13      0.13
place_optHFSBUF_400_89235/Y (NBUFFX8_RVT)       0.08     0.21 r
HFSINV_3087_47138/Y (INVX0_RVT)                0.05     0.26 f
place_optHFSBUF_465_93191/Y (NBUFFX16_RVT)      0.07     0.33 f
HFSINV_375_47133/Y (INVX0_RVT)                 0.11     0.43 r
place_optHFSBUF_47_87670/Y (NBUFFX8_RVT)        0.08     0.51 r
bit_secure_6/sipo_slice_first/wr_0_reg/D (SDFFARX1_RVT)
r 0.53      0.02
```

```
data arrival time                              0.53


clock lclk (rise edge)                   0.60      0.60

clock network delay (ideal)                   0.00      0.60

bit_secure_6/sipo_slice_first/wr_0_reg/CLK (SDFFARX1_RVT)

r 0.60       0.00

library setup time                      -0.12      0.48

data required time                                0.48

--------------------------------------------------------------------

data required time                                0.48

data arrival time                             -0.53

--------------------------------------------------------------------

slack (VIOLATED)                                -0.05



1

report_timing -scenarios [all_scenarios] -delay_type min -max_paths 3

Warning: Scenario FUNC_Fast is not configured for hold analysis: skipping. (UIC-058)

Warning: Scenario FUNC_Slow is not configured for hold analysis: skipping. (UIC-058)

**************

Report : timing

path_type full-

delay_type min-

max_paths 3-

report_by design-

Design : bit_coin

Version: U-2022.12-SP2

Date   : Thu Jun 22 18:01:06 2023

**************


Startpoint: bit_secure_0/sipo_slice_first/wr_addr_reg[1] (rising edge-triggered flip-flop
clocked by lclk)
```

```
Endpoint: bit_secure_0/sipo_slice_first/wr_addr_reg[1] (rising edge-triggered flip-flop
clocked by lclk)

Mode: FUNC

Corner: Typical

Scenario: FUNC_Typical

Path Group: lclk

Path Type: min


Point                                    Incr     Path

----------------------------------------------------------------------

clock lclk (rise edge)                      0.00     0.00

clock network delay (ideal)                     0.00     0.00


bit_secure_0/sipo_slice_first/wr_addr_reg[1]/CLK (SDFFARX1_RVT)

r 0.00      0.00

bit_secure_0/sipo_slice_first/wr_addr_reg[1]/QN (SDFFARX1_RVT)

f 0.09      0.09

bit_secure_0/sipo_slice_first/wr_addr_reg[1]/D (SDFFARX1_RVT)

f 0.09      0.00

data arrival time                                    0.09


clock lclk (rise edge)                      0.00     0.00

clock network delay (ideal)                     0.00     0.00

bit_secure_0/sipo_slice_first/wr_addr_reg[1]/CLK (SDFFARX1_RVT)

r 0.00      0.00

library hold time                         -0.06    -0.06

data required time                                   -0.06

----------------------------------------------------------------------

data required time                                   -0.06

data arrival time                                   -0.09

----------------------------------------------------------------------

slack (MET)                                        0.14
```

```
Startpoint: bit_secure_14/sipo_slice_last/wr_addr_reg[1] (rising edge-triggered flip-flop
clocked by lclk)

Endpoint: bit_secure_14/sipo_slice_last/wr_addr_reg[1] (rising edge-triggered flip-flop
clocked by lclk)

Mode: FUNC

Corner: Typical

Scenario: FUNC_Typical

Path Group: lclk

Path Type: min


Point                                Incr      Path

------------------------------------------------------------------------

clock lclk (rise edge)                     0.00      0.00

clock network delay (ideal)                     0.00      0.00


bit_secure_14/sipo_slice_last/wr_addr_reg[1]/CLK (SDFFARX1_RVT)

r 0.00       0.00

bit_secure_14/sipo_slice_last/wr_addr_reg[1]/QN (SDFFARX1_RVT)

f 0.09       0.09

bit_secure_14/sipo_slice_last/wr_addr_reg[1]/D (SDFFARX1_RVT)

f 0.09       0.00

data arrival time                                    0.09


clock lclk (rise edge)                     0.00      0.00

clock network delay (ideal)                     0.00      0.00

bit_secure_14/sipo_slice_last/wr_addr_reg[1]/CLK (SDFFARX1_RVT)

r 0.00       0.00

library hold time                          -0.06     -0.06

data required time                                    -0.06

------------------------------------------------------------------------
```

```
data required time                       -0.06

data arrival time                       -0.09

-----------------------------------------------------------------------

slack (MET)                             0.14




Startpoint: bit_secure_15/sipo_slice_last/wr_addr_reg[0] (rising edge-triggered flip-flop
clocked by lclk)

Endpoint: bit_secure_15/sipo_slice_last/wr_addr_reg[0] (rising edge-triggered flip-flop
clocked by lclk)

Mode: FUNC

Corner: Typical

Scenario: FUNC_Typical

Path Group: lclk

Path Type: min


Point                              Incr     Path

-----------------------------------------------------------------------

clock lclk (rise edge)                  0.00     0.00

clock network delay (ideal)                 0.00     0.00


bit_secure_15/sipo_slice_last/wr_addr_reg[0]/CLK (SDFFARX1_RVT)

r 0.00      0.00

bit_secure_15/sipo_slice_last/wr_addr_reg[0]/QN (SDFFARX1_RVT)

f 0.09      0.09

bit_secure_15/sipo_slice_last/wr_addr_reg[0]/D (SDFFARX1_RVT)

f 0.09      0.00

data arrival time                        0.09


clock lclk (rise edge)                  0.00     0.00

clock network delay (ideal)                 0.00     0.00
```

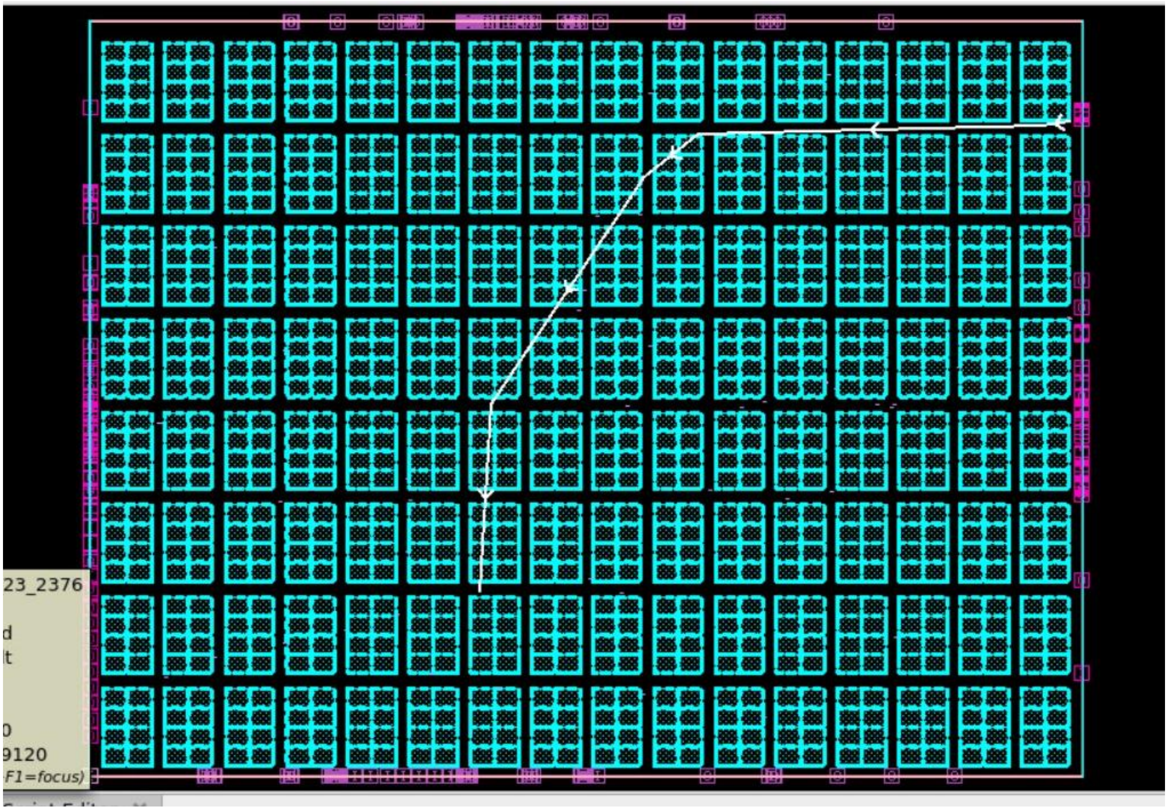
```
bit_secure_15/sipo_slice_last/wr_addr_reg[0]/CLK (SDFFARX1_RVT)

r 0.00    0.00

library hold time               -0.06   -0.06

data required time                     -0.06

----------------------------------------------------------------------

data required time                     -0.06

data arrival time                     -0.09

----------------------------------------------------------------------

slack (MET)                          0.14
```

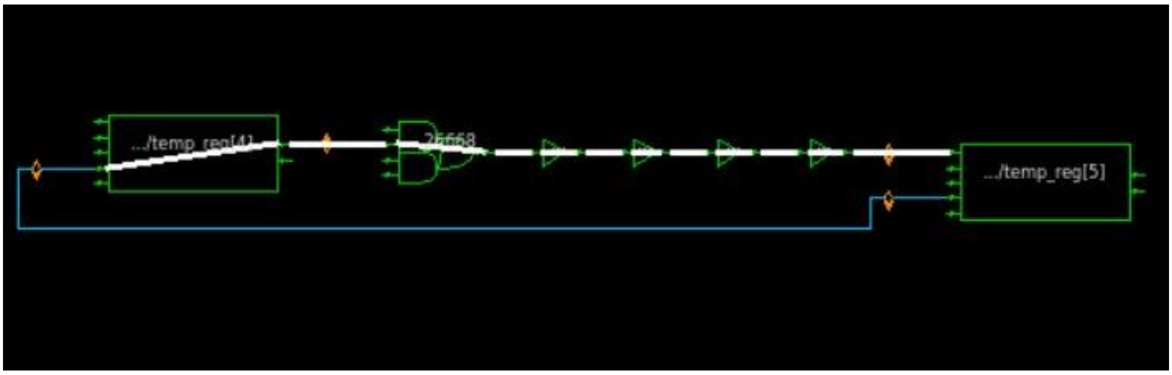
As we can see from the reports above we can execute the following 2 problematic paths (both are setup violations)

1.

START: piso_secure_0/temp_reg[4]

END: piso_secure_0/temp_reg[5]

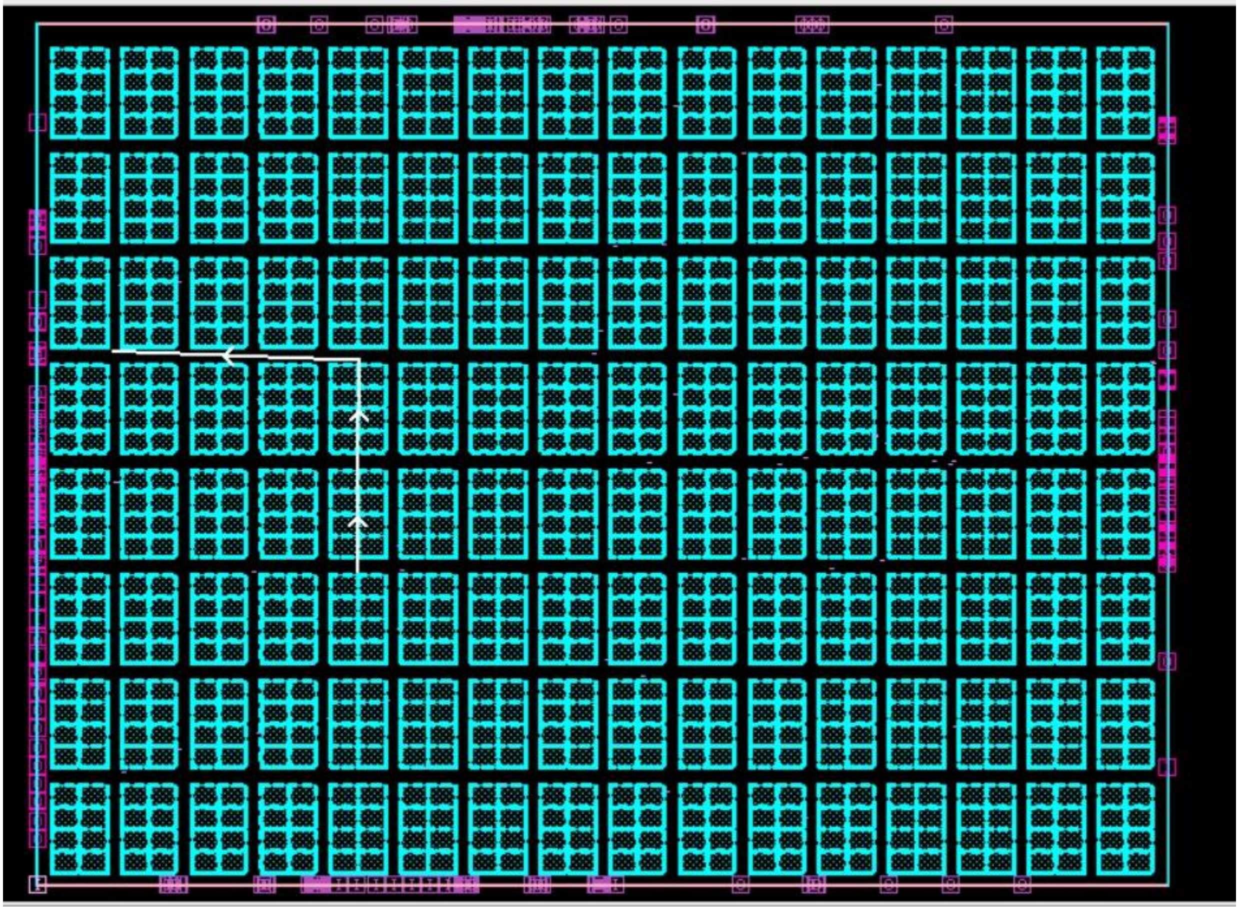


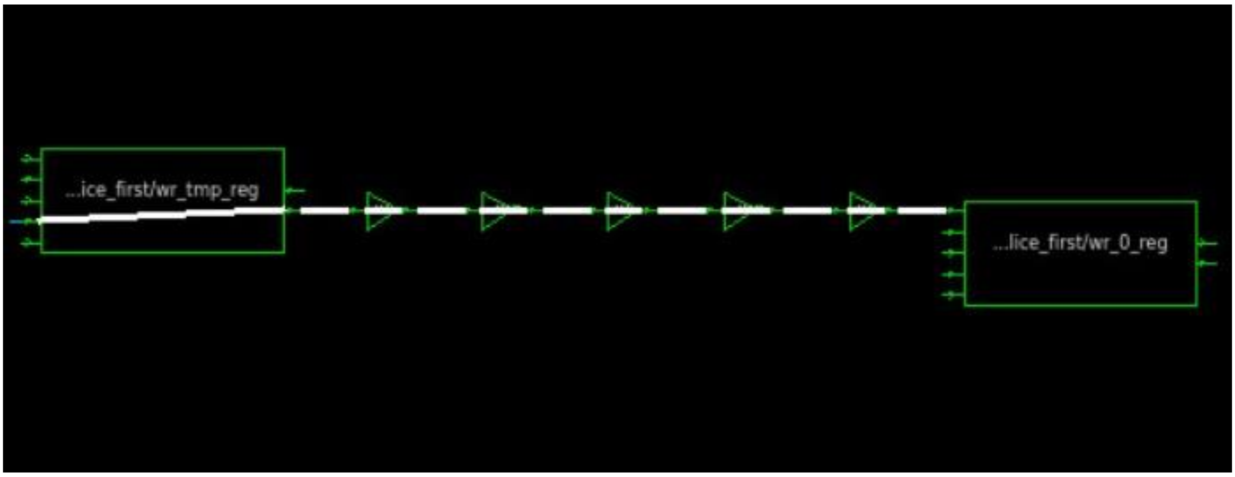


2.

START: bit_secure_0/sipo_slice_first/wr_tmp_reg

END: bit_secure_8/sipo_slice_first/wr_0_reg]





3.5.Explain the main problem of the path that causes the negative slack

Hints: which cells have the highest delay? How many cells are in the path? What can be inferred from the screenshots above?

The main problem in the path that causes the negative slack is the cumulative delay introduced by several cells along the path.

The cells with the highest delay along the path are:

- ctmi_26668/Y (AOI22X2_RVT) with an incremental delay of 0.11

- place_optHFSBUF_7552_83980/Y (NBUFFX4_RVT) with an incremental delay of 0.12

- place_optHFSINV_2914_83978/Y (INVX8_RVT) with an incremental delay of 0.12

The path consists of a total of 8 cells.

From the given report, it can be inferred that the negative slack is caused by a combination of multiple cells with significant delays. These delays accumulate along the path, resulting in a violation of the required timing constraints. To improve the slack, you may need to optimize the critical cells or the routing to reduce the overall delay along the path.

3.6.Suggest 1-2 ways to fix the timing path.

1. Reduce the delay in critical cells: Identify the cells with the highest delay in the path and try to optimize them. In the first timing path, some of the cells with relatively high delay. Analyze these cells and see if there are any optimization techniques or alternative cell options that can reduce their delay.

2. Adjust clock timing or buffering: If optimizing the individual cells is not sufficient, you can consider adjusting the clock timing or inserting additional buffering elements along the path. By modifying the clock skew or inserting buffers strategically, you can balance the delays and improve the slack.