Problem 1:

A carry lookahead adder computes $G = G_3 + P_3(G_2 + P_2(G_1 + P_1G_0))$. Consider designing a compound gate to compute $\overline{G}$.

a) sketch a transistor-level schematic

b) sketch a stick diagram

c) estimate the area from the stick diagram

Problem 2:

Consider an nMOS transistor in a 0.6 μm process with $W/L = 4/2\ \lambda$ (i.e., 1.2/0.6 μm). In this process, the gate oxide thickness is 100 Å and the mobility of electrons is 350 $cm^2/V \cdot s$. The threshold voltage is 0.7 V. Plot I_{ds} vs. V_{ds} for $V_{gs} = 0, 1, 2, 3, 4,$ and 5 V.

Problem 3:

Show that the current through two transistors in series is equal to the current through a single transistor of twice the length if the transistors are well described by the Shockley model. Specifically, show that $I_{DS1} = I_{DS2}$ in Figure 2.32 when the transistors are in their linear region: $V_{DS} < V_{DD} - V_t$, $V_{DD} > V_t$ (this is also true in saturation). *Hint*: Express the currents of the series transistors in terms of V_1 and solve for V_1.

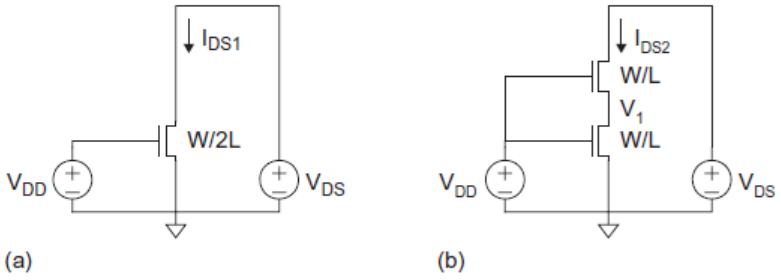

FIGURE 2.32 Current in series transistors

Problem 4:

A 90 nm long transistor has a gate oxide thickness of 16 Å. What is its gate capacitance per micron of width?

Problem 5:

An nMOS transistor has a threshold voltage of 0.4 V and a supply voltage of $V_{DD} = 1.2$ V. A circuit designer is evaluating a proposal to reduce V_t by 100 mV to obtain faster transistors.

a) By what factor would the saturation current increase (at $V_{gs} = V_{ds} = V_{DD}$) if the transistor were ideal?

b) By what factor would the subthreshold leakage current increase at room temperature at $V_{gs} = 0$? Assume $n = 1.4$.

c) By what factor would the subthreshold leakage current increase at 120 °C? Assume the threshold voltage is independent of temperature.

Problem 6:

Give an expression for the output voltage for the pass transistor networks shown in Figure 2.35. Neglect the body effect.

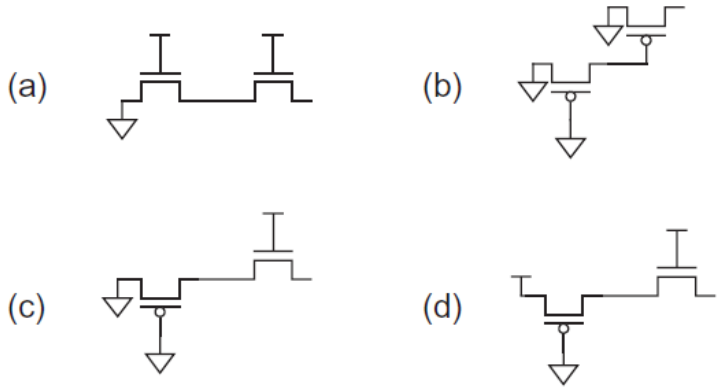

FIGURE 2.35 Pass transistor networks

Problem 7: Design a CMOS circuit with the minimum possible number of **transistors** for each of the expression below:

a. F = ((a + b + c).d.e)'
b. F = (((a + b) . c) + d)'
c. F = (x + y).(x + z)
d. F = a.b + a'.c + b.c.d