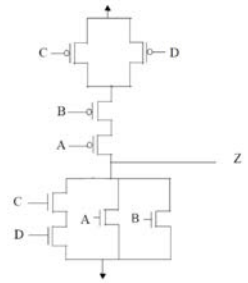
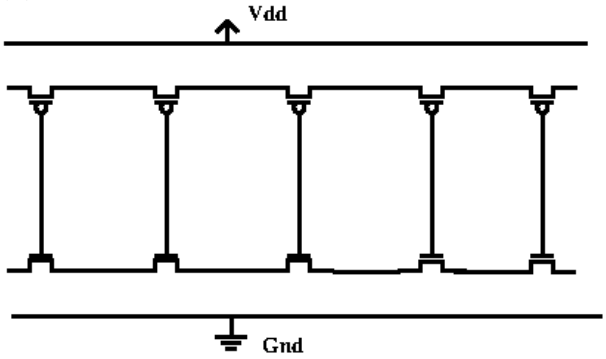
Problem 1 (25 points):

Complete the diagram in (b) so it implements the transistor circuit shown in (a)

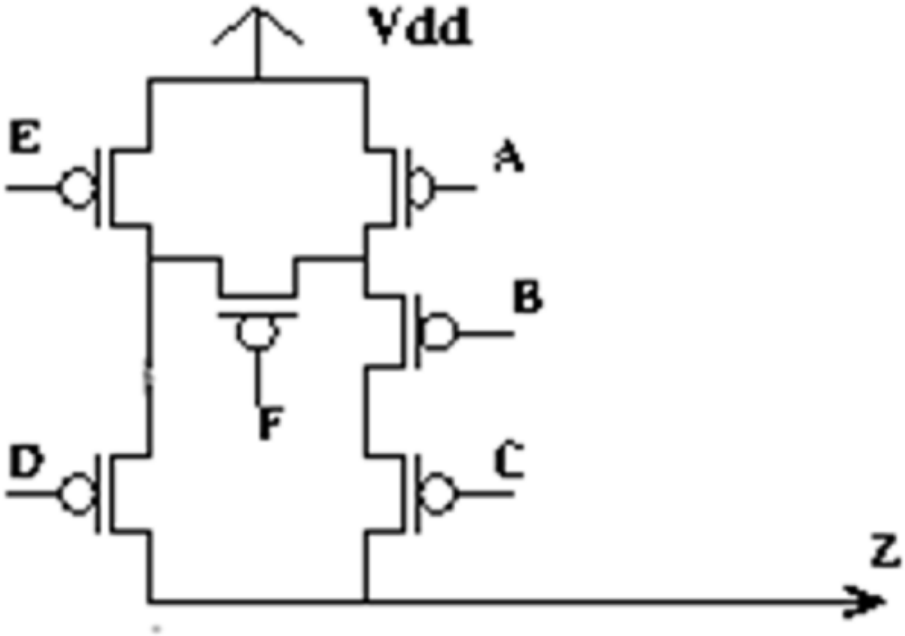


(a)

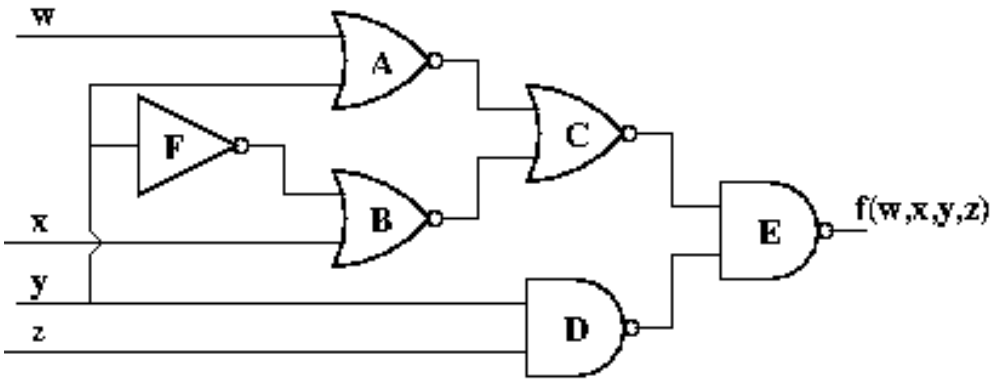


(b)

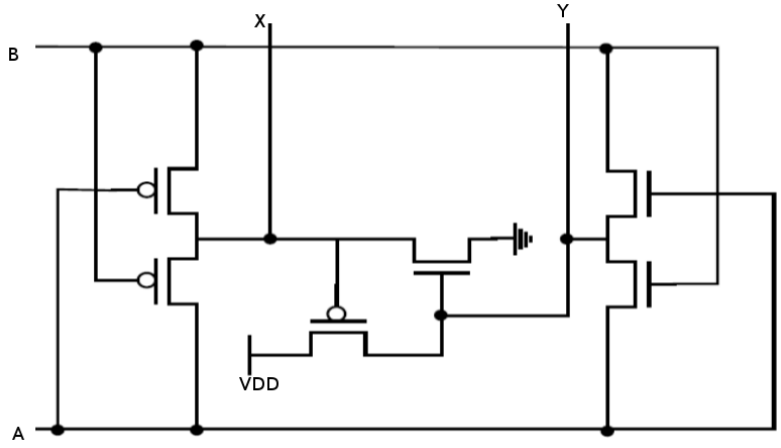
Given the P-network below for a complex static CMOS gate, derive the N-network and show the complete transistor-level diagram?



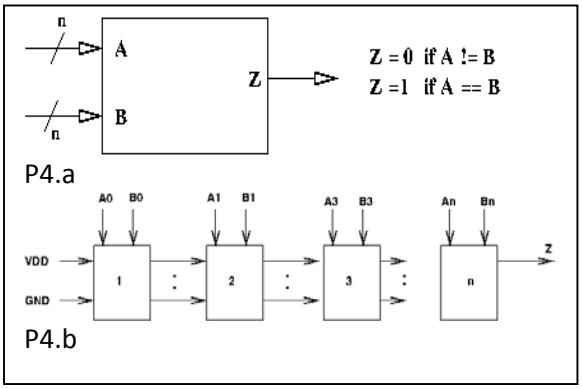
Problem 2 (25 points): For the circuit shown below design: Derive a static CMOS gate.



Problem 3 (25 points): Find the functions X and Y implemented by the following circuit.



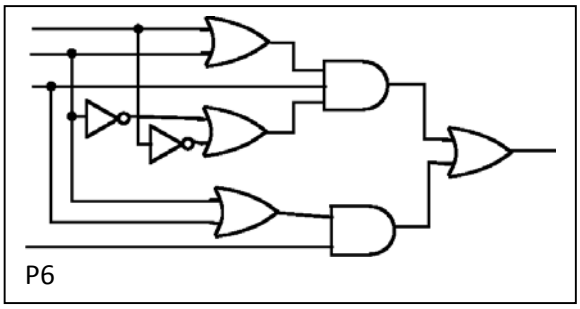
Problem 4 (25 points): This problem relates to the design of equality functions in CMOS. The function takes two **n** input variables **A** and **B** and produces an output Z as shown in P4.a.



A solution to the realization of the equality function for two **n** input variables would be to repeat a single variable **cell N** times. Appropriate information is transmitted between cells as shown in the figure P4.b. Design a cell in static CMOS at the transistor level which, when repeated as above, implements the equality function.

Problem 5(15 points): Minimize the given Boolean equations to eliminate redundancy (a' means the complement of a)

1) ab + bdc + ca'
2) (x+y)(x+z)
3) a(b+c+d) + b(c+d+a) + c(d+a+b) + d(a+b+c)



Problem 6 (25 points): Label the inputs of the circuit P6 so that it implements the function: **d (b + b' c) + a b c' + a' b c**

Problem 7(15points): This problem relates to the design of circuits using multiplexer modules. Three 2-to1 multiplexer modules can be combined to produce a 4-to-1 multiplexer. Any 2-input logic function can be implemented using this 4-to-1 multiplexer with the two inputs fed to the select line and the truth table entries appropriately fed to the input lines. However, a 4-to-1 multiplexer can also implement a 3-input logic function if the complement of one of the inputs is also available. Can you figure this out? You are to implement the logic function F(a,b,c)= ∑(0,2,7) using three of the 2-to-1 multiplexer modules.

1. Design a gate-level implementation of the above function using multiplexer modules made of NAND/NOR gates.
2. How many transistors are needed for the gate level implementation?
3. If the same function is implemented using multiplexers with transmission gates, what would be the number of transistors needed for this implementation?

Problem 7(15): Draw the transistor schematic representing the circuit below. Can you describe the function of the circuit?