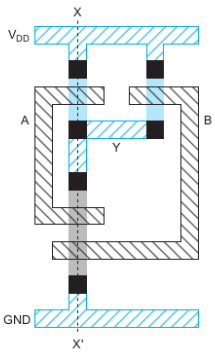
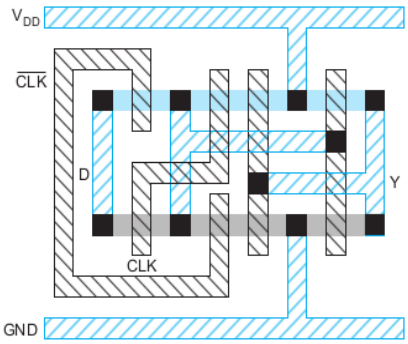
Problem 1 (15pts): For the stick diagram shown in P1, sketch a side view (cross-section) of the gate from X to X'.



P1

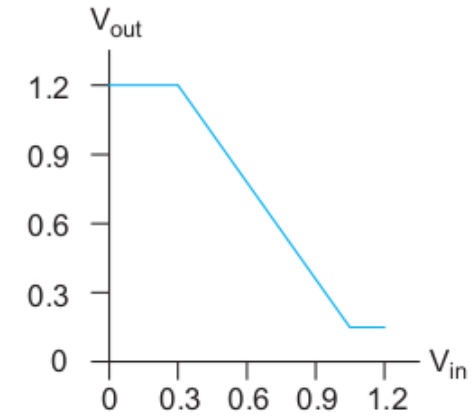
Problem 2 (12pts): For the stick diagram shown in P2, Estimate the area of the design.



P2

Problem 3 (15pts): Consider the design of a CMOS compound OR-AND-INVERT (OAI21) gate computing F = ((A + B) · C)'.

a) Sketch a transistor-level schematic
b) Sketch a stick diagram
c) Estimate the area from the stick diagram



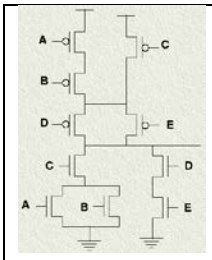
P3

Problem 4 (14pts): A novel inverter has the transfer characteristics shown in P3. What are the values of V_{IL} , V_{IH} , V_{OL} , and V_{OH} that give best noise margins? What are these high and low noise margins?

Problem 5 (14pts): Find the rising and falling propagation delays of an unloaded AND-OR-INVERT (AOI21) gate using the Elmore delay model. Estimate the diffusion capacitance based on a stick diagram of the layout.

Problem 6 (14pts): Find the worst-case Elmore parasitic delay of an n-input NOR gate.

Problem 7 (14pts): Size the gate, in P4, so that it has the same drive strength as an inverter with pMOS transistor width=3 and an nMOS transistor width=2.



P4