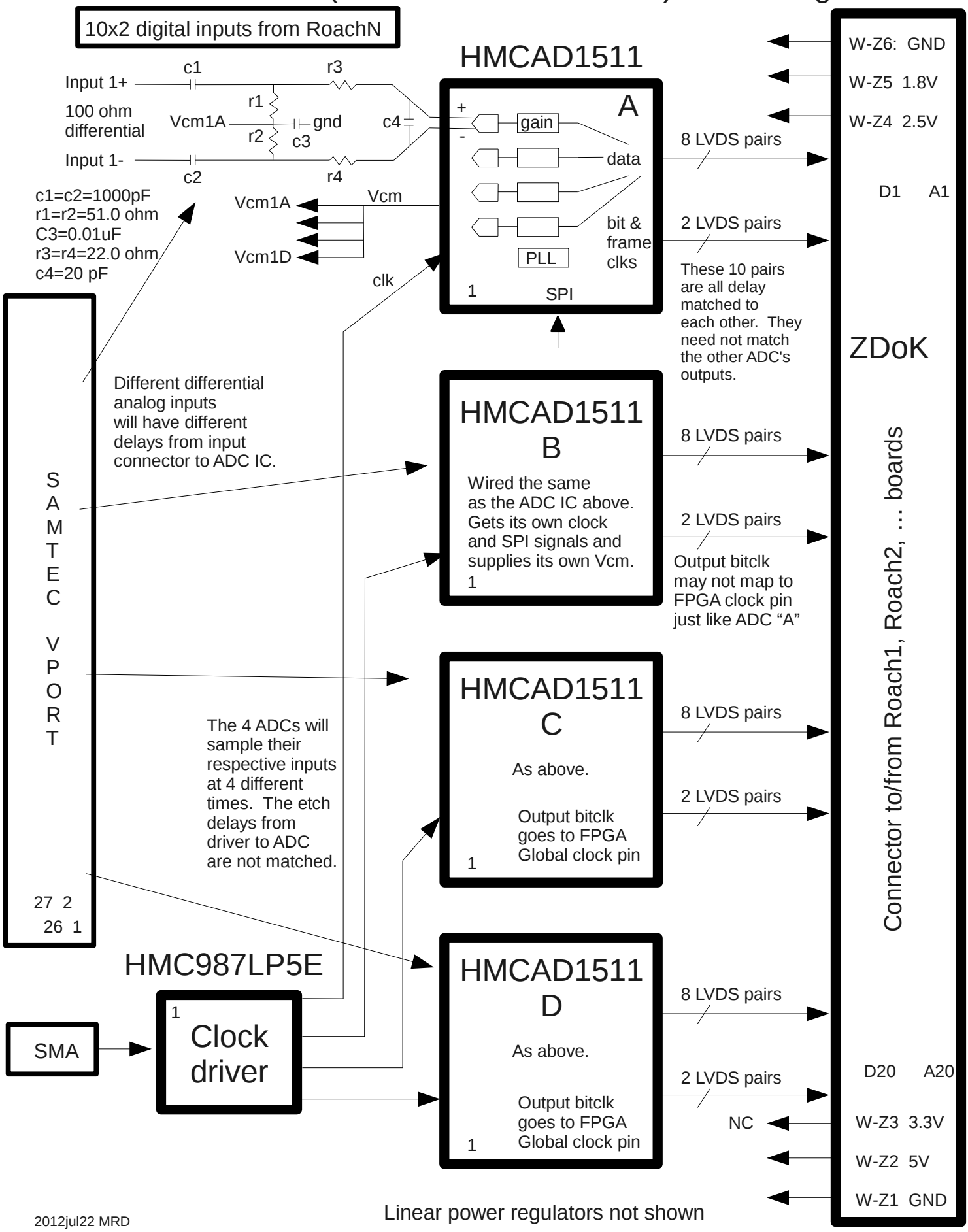
ADC 16x250-8 (or 8x500-8 or 4x1000-8) Block Diagram



ADC 16x250-8 (or 8x500-8 or 4x1000-8) Power distribution

10x2 Digital inputs from RoachN

SPI 10x2 header HostVio →
- 10X2 header pin 1 is output voltage for the to SN74AVC8T245PW Translator. Pin 19 is an unused supply HostVaux.
- There are no added inductors on these 2 nets – just bypass caps.
- Estimate of Amps required : 0.001 Amp found from
  - 4 ADC ICs * 3 SPI pins * 10 uA + translator's 15 uA
- Measured: TBD

Zdok 1.8V →
- Zdok pin is the digital_1.8V sent via a (shared) plane to
  - load 1 → ADC 1
  - load 2 → ADC 2
  - load 3 → ADC 3
  - load 4 → ADC 4
  - load 5 → SN74AVC8T245PW (TTL level translator)
- There are no added inductors on the 1.8VD net – just bypass caps
- Estimate of Amps required : 0.8 Amps found from
  - 4 ADC ICs * 0.2 Amp where 0.2 is rounded up from 0.125 Amp typical
  - The level translator load is small 15uA or 1mA w/ loads included.
- Measurements 2012jul26: 0.58 Amps
  - 0.304 A @ 150 MHz, 0.373 A @ 250 MHz, 0.580 A @ 500 and 1000 MHz

Zdok 2.5V → two TDK NLC453232T-1R0K-PF 1uH inductors in parallel →
- LP3856ES-1.8 regulator to generate analog_1.8V for ADC ICs.
- This regulator has 4 outputs
  - load 1 → TDK NLC453232T-1R0K-PF 1uH inductor to ADC A
  - load 2 → TDK NLC453232T-1R0K-PF 1uH inductor to ADC B
  - load 3 → TDK NLC453232T-1R0K-PF 1uH inductor to ADC C
  - load 4 → TDK NLC453232T-1R0K-PF 1uH inductor to ADC D
- Estimate of Amps required :
  - 4 ADC ICs * 0.3 Amp where 0.3 is rounded up from 0.270 Amp typical
- Measurements 2012jul26 : 1.37 Amps
  - 0.61 A @ 150 MHz, 0.98 A @ 250 MHz, 1.370 A @ 500 and 1000 MHz

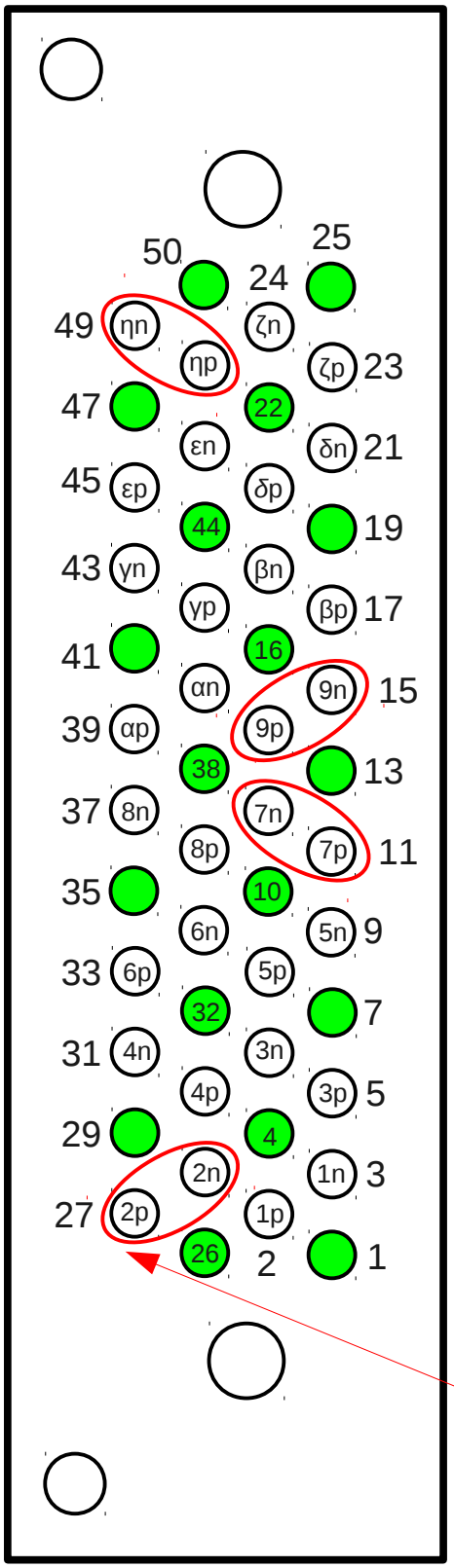
Zdok 3.3V → is not used. It is NOT connected to the clean_3.3V generated on this board.

Zdok 5V → TDK NLC453232T-150K-PF 15 uH →
- HMC976LP3E regulator to generate clean_3.3V
- This regulator has 1 load
  - load 1 → TDK NLC453232T-1R0K-PF 1 uH inductor to the clock driver HMC987LP5E.
- Conservative est of Amps required: 0.3 Amp
- Measured 2012jul26: 0.25 Amp
  - 0.25 A @ 150, 250, 500 and 1000 MHz

2012jul27 MRD

ADC 16x250-8 (or 8x500-8 or 4x1000-8) Block Diagram
analog input connector pinout

Samtec VRDPC-50-01-M-RA2 aka VPORT



Analog input pairs

Pair	neg	pos
ADC IC A		
η=A4	49	48
ζ=A3	24	23
ε=A2	46	45
δ=A1	21	20
ADC IC B		
γ=B4	43	42
β=B3	18	17
α=B2	40	39
9=B1	15	14
ADC IC C		
8=C4	37	36
7=C3	11	12
6=C2	34	33
5=C1	9	8
ADC IC D		
4=D4	31	30
3=D3	6	5
2=D2	28	27
1=D1	3	2

Positive/negative to pin location mapping on this connector was chosen to match the orientation of the ADC IC's P,N pins.

All 4 ADC ICs have the negative input pins of each pair always towards the top edge of the PCB. Thus, by setting the neg pin on the connector towards the top the input circuitry for each input could be almost an exact copy of each other. And with a minimum of routing complexity

This mapping may impose a sign flip on the input depending on the mapping of the connector at the TX side of the cable. Any such reversal will be taken out by the ADC IC's programmable input polarity register, the downstream FPGA or in the science product calibration.

Ground pins shown in green:
Pins 1, 4, 7, 10, 13, 16, 19, 22, 25, 26, 29, 32, 35, 38, 41, 44, 47 and 50.
Samtec tested these exact connectors and cables with 12, not 16, differential pairs and 8 additional grounds. Those pins are shown by the red ovals.

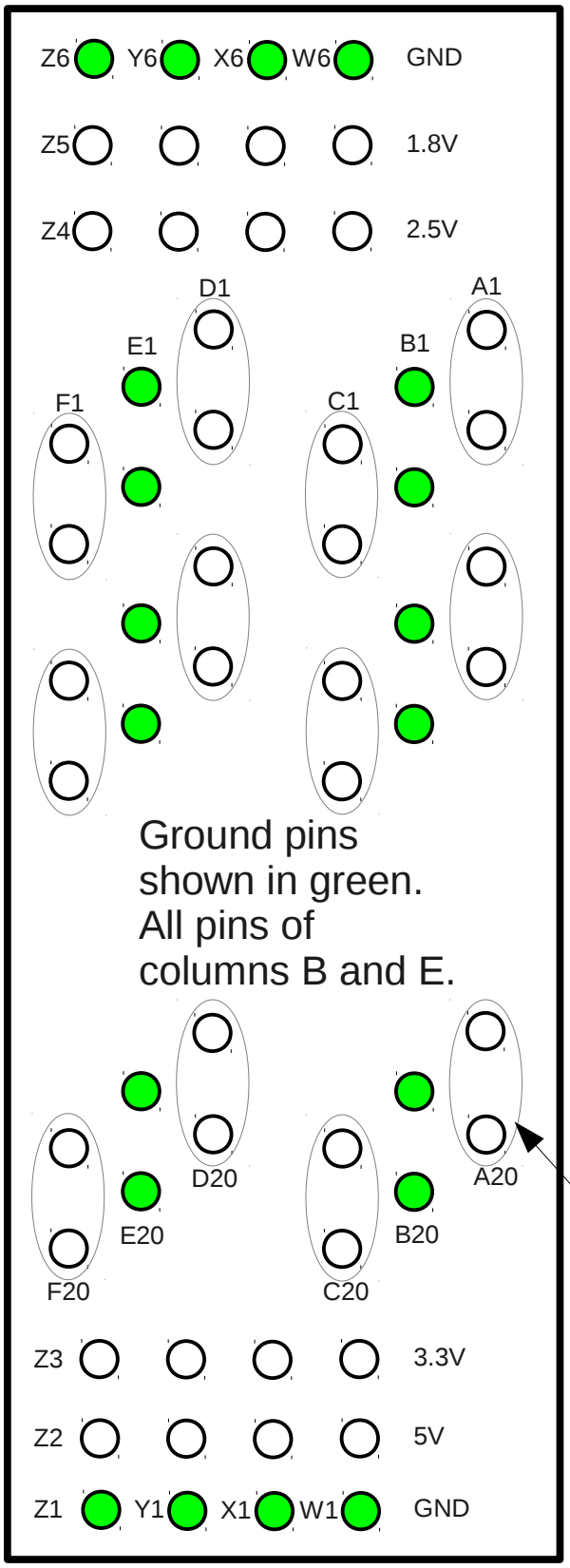
See page 7 of the Samtec VPSTP datasheet and page 12 of the VPSTP HSC report

NOT TO SCALE

2013mar02 MRD

ADC 16x250-8 (or 8x500-8 or 4x1000-8) Block Diagram digital output connector pinout. Tyco 6367555-3

http://www.te.com/catalog/pn/en/6367555-1
http://tycoelectronics.custhelp.com/app/answers/list/kw/zdok



Board edge of side to host RoachN Board here.

For each of the 4 ADC ICs the general pattern may be as shown. BUT changes to use the FPGA's Global clock pins and to ease routing, if need be. will be made.

D1Ap-n: D5-6
D1Bp-n: A5-6
D2Ap-n: F3-4
D2Bp-n: C3-4
D3Ap-n: F1-2
D3Bp-n: D1-2
D4Ap-n: C1-2
D4Bp-n: A1-2
LCLKp-n: A3-4
FCLKp-n: D3-4

See the Separate Zdok connector pinout mapping document as there are lots of details to get right..

Trace length matching rules:

The host board this ADC16 mates with does not include the its Zdok connector pin length differences in its etch length matching. The etch lengths on this board must i ADCMP605BCPZ znclude those length differences as well as for its own Zdok connector pin length differences.

Tyco's propagation Delay values
Page 12 of Z-dok-epr.pdf
A: 145.2ps
C: 196.8ps
D: 213.3ps
F: 264.8ps

Thus the time of flight for the signals on the ADC16 board for the ADC IC 1 to
1) F column pins will be TOF-ADC1
2) D column pins will be TOF-ADC1+51.5 ps
3) C column pins will be TOF-ADC1+68 ps
4) A column pins will be TOF-ADC1+120 ps

Using the generic rates of 1.72 ns/ft or 0.143 ns/in for microstrip and 1.98 ns/ft or 0.165 ns/in for stripline
If for example external layer (microstrip) etch Delivered the ADC IC outputs to the F column pins then microstrip etch runs for that same ADC IC A column pins would need to be extended by 0.834 inches. For internal layer stripline runs to F and A column pins then the A pin etch would need to be extended by 0.725 inches. When mapping from stripline etch to 1 column vs microstrip etch to another column have to use the time of flight. Not the physical distance.

It's the time to match; not the distance.

See the Zdok_pins.pdf
The P,N flips on all these pins are compensated for in the VHDL library block

Note: oval differential antipads for all the signal differential pairs. This is for electrical signal Integrity.
No nets to be routed between the two pins of 1 pair; instead route in the space between 2 pairs.

Board edge

NOT TO SCALE

2012jdec04 MRD

Zdok connector etch matching continued

Trace length matching rules:

The host board, such as the Roach1 and Roach2, this ADC16 mates with does not include its Zdok connector pin length differences in its etch length matching. The etch lengths on this board must include those length differences as well as for its own Zdok connector pin length differences.

Tyco's propagation Delay values from Page 12 of Z-dok-epr.pdf
A: 145.2ps
C: 196.8ps
D: 213.3ps
F: 264.8ps

Try to sanity check Tyzo's number via physical measurements of the connectors as well as dimensions From the datasheets.

bottom of PCB to A,C,D,F pins measured at the ADC16 Zdok mating face
0.16, 0.20, 0.282 and 0.322” (measured).

Other dimensions from the Tyco datasheets.

Use the common generic stripline rate of 1.72 ns/ft or 0.143 ns/inch

Mated A pins: .6102+2*.16”	= 0.930”	or 0.133 ns or 12 ps away from Tyco's
Mated C pins: .6102+2*(2*.0689+.2)	= 1.286”	or 0.184 ns or 12 ps away from Tyco's
Mated D pins: .6102+2*(2*.0689+.0984+.282)	= 1.647”	or 0.239 ns or 26 ps away from Tyco's
Mated F pins: .6102+2*(4*.0689+.0984+.322)	= 2.002”	or 0.286 ns or 21 ps away from Tyco's

Thus, by simpling using the physical dimensions the errors are about 10 % off from Tyco's published time of flights. Not too bad all in all.

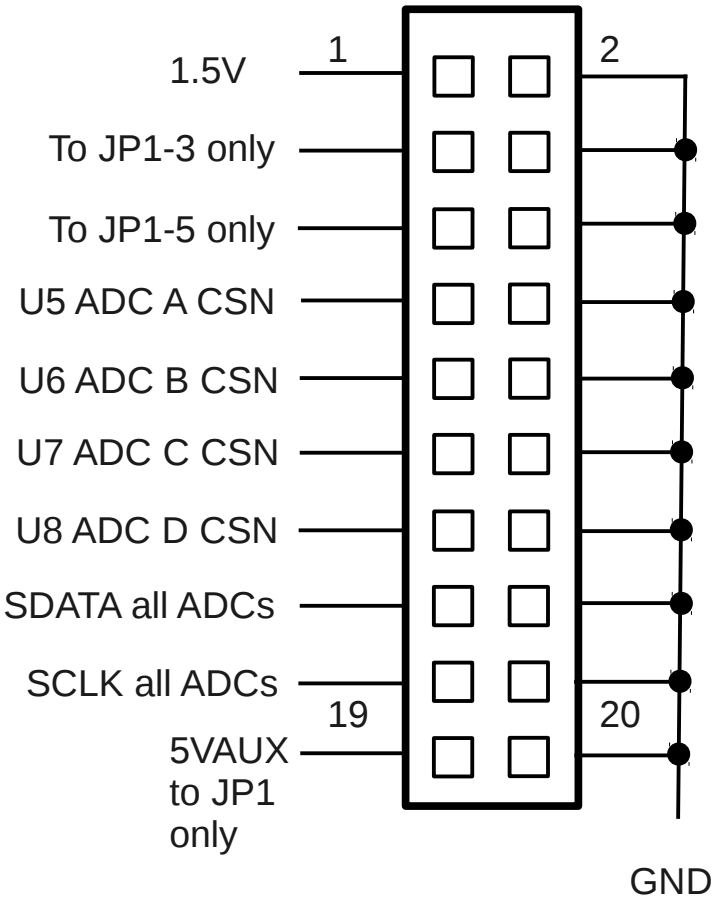
Tyco's specified time differences will be use when routing the ADC16 board.

Roach2 rev1 and Roach2 rev2
TTL programming

Roach2 connector and FPGA pins

for ADC at P10 “ZDok0” P13 pin	FPGA pin	for ADC at P11 “ZDok1” P15 pin	FPGA pin
1V5		1V5	
V6_GPIO15	M27	V6_GPIO7	J30
V6_GPIO14	E29	V6_GPIO6	M29
V6_GPIO13	F16	V6_GPIO5	H30
V6_GPIO12	H18	V6_GPIO4	L30
V6_GPIO11	N20	V6_GPIO3	AG33
V6_GPIO10	N19	V6_GPIO2	AF32
V6_GPIO9	K30	V6_GPIO1	H31
V6_GPIO8	M28	V6_GPIO0	G31
5VAUX		5VAUX	

ADC16x250 JP2

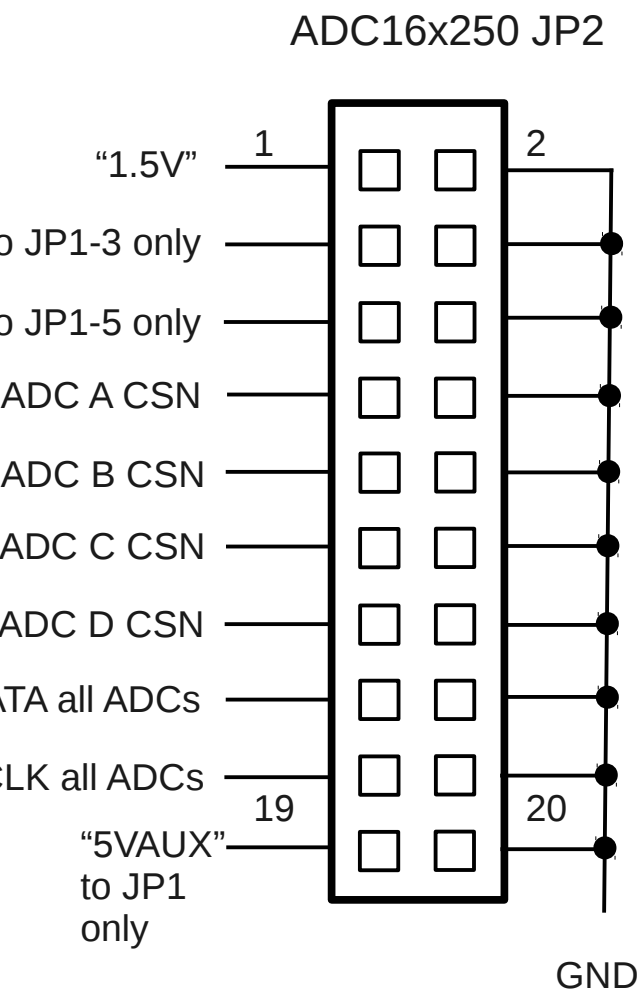


Note there is a 1V5 / 3V3 level translator U68 attached to the V6_GPIO7..0 pins and LEDs hang off the other side of the translator. Thus, if someone where playing with LEDs and the ADC16 were connected via P15 they'd also might be changing the ADC16's configuration.

Roach1 TTL programming

Roach1 connector and FPGA pins

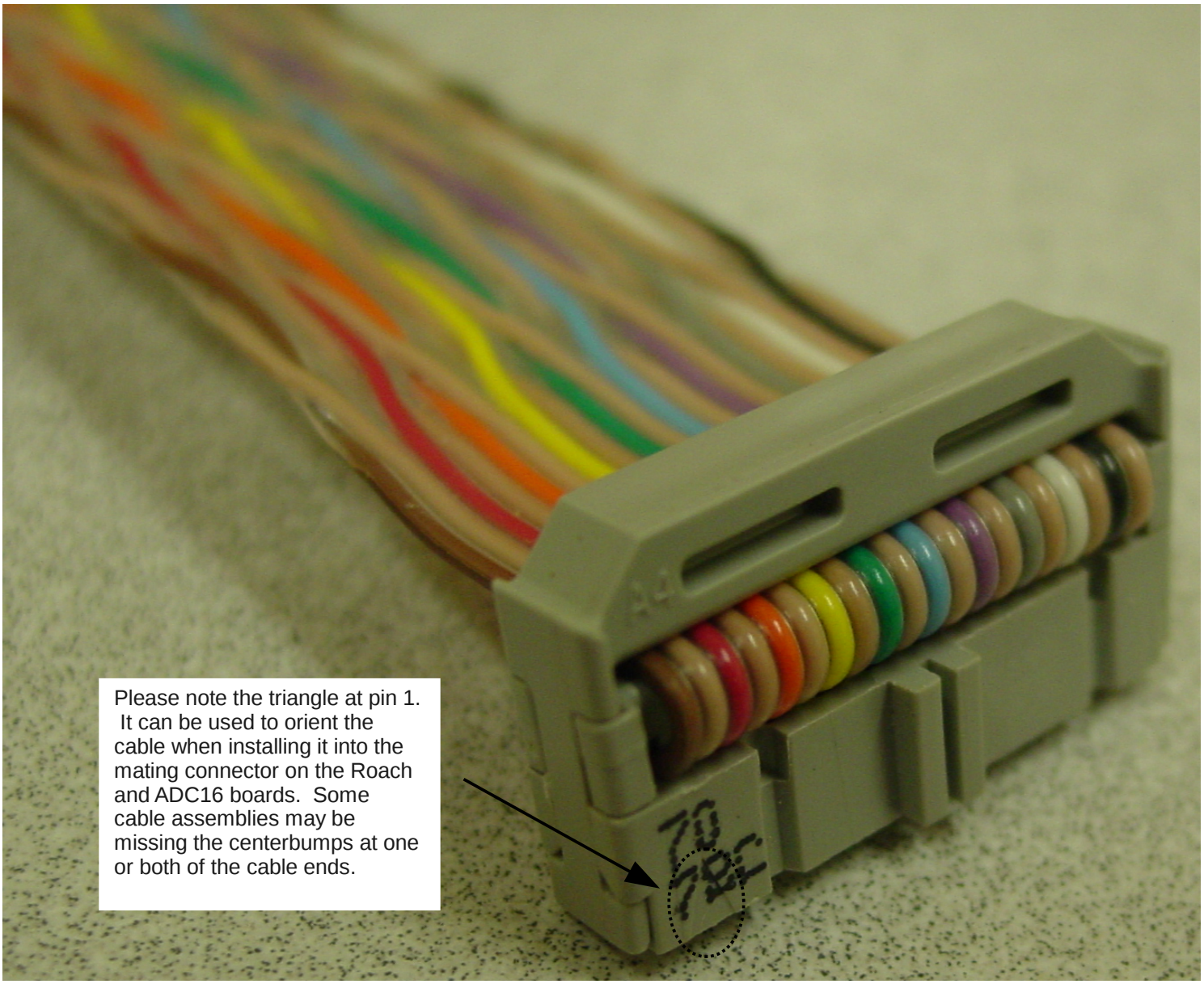
for ADC at P5 "ZDok0" J9 pin	FPGA pin	for ADC at P7 "ZDok1" J2 pin	FPGA pin
3V3		3V3	
GPIOLVC25[4]	R33	GPIOLVC15[4]	J10
GPIOLVC25[3]	P34	GPIOLVC15[5]	J9
GPIOLVC25[2]	N34	GPIOLVC15[6]	H7
GPIOLVC25[1]	N33	GPIOLVC15[7]	J7
GPIOLVC25[8]	N32	GPIOLVC15[0]	A26
GPIOLVC25[7]	P32	GPIOLVC15[1]	E24
GPIOLVC25[6]	L33	GPIOLVC15[2]	D24
GPIOLVC25[5]	M33	GPIOLVC15[3]	B27
GND		GND	



The net names on the ADC16x250-8 card are confusing. They were selected with the Roach2 rev2 in mind. Thus, the so called "1V5" net will actually be 3.3 VDC and the "5VAUX" net will actually be 0.0 VDC.

Note there is a bi-directional 2.5V to/from 3.3V level translator ICs between the Roach1 FPGA pins and the J9 connector. The bi-directional control signals must be set to the output mode (Roach1 as source). Same idea for the Roach1 FPGA pins and the J2 connector but that level translation is between 1.5V and 3.3V. See page 13 of 25 of Roach1 rev3 schematics.

TTL programming cable assembly



Using ADC16x250-8 pin names for the connector pins:

Pin 1: 1.5V	brown	pin 2: GND	tan
Pin 3: To JP1-3 only	red	pin 4: GND	tan
Pin 5: To JP1-5 only	orange	pin 6: GND	tan
Pin 7: U5 ADC A CSN	yellow	pin 8: GND	tan
Pin 9: U6 ADC B CSN	green	pin 10: GND	tan
Pin 11: U7 ADC C CSN	blue	pin 12: GND	tan
Pin 13: U8 ADC D CSN	purple	pin 14: GND	tan
Pin 15: SDATA all ADCs	grey	pin 16: GND	tan
Pin 17: SCLK all ADCs	white	pin 18: GND	tan
Pin 19: 5VAUX to JP1 only	black	pin 20: GND	tan

Roach2