# The Design of Snap2 System

Jie Hao, Qiuxiang Fan, Liangtian Zhao, Jingbin Mu, Hui Feng, Lin Shu

Institute of Automation, Chinese Academy of Sciences

## Contents

# 1 System overview

The Snap2 system provides a hardware environment for developing designs targeting the Ultrascale XCKU115-FLVF1924 FPGA. The Snap2 System contains a Zynq AP SoC XC7Z010, four QDR component memories, a DDR3 component memory, four Quad Small Form-factor Pluggable (QSFP) connectors, two Ethernet PHY, an USB interface, a ZD+ connector, some general purpose I/Os. Other features can be added by using VITA-57 FPGA mezzanine cards (FMC) attached to two high pin count (HPC) FMC connectors in the system.

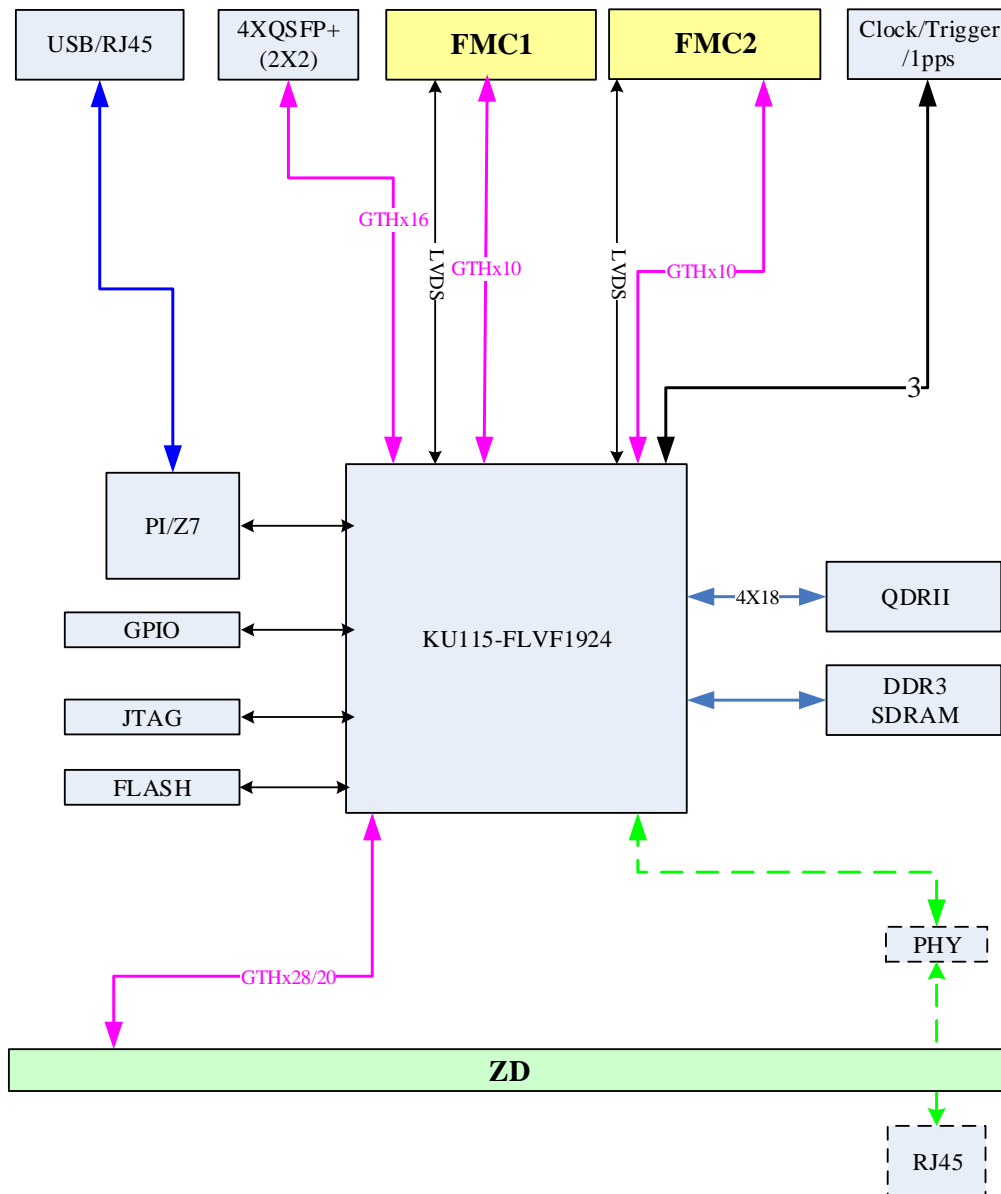The Snap2 system diagram is shown in Figure 1-1.



Figure 1-1 Snap2 System Block Diagram

The key features of the system are listed in following:

• Ultrascale XCKU115-FLVF1924 FPGA is used for high-speed operation and high-speed

interconnect.

- Zynq AP Soc XC7Z010 based system controller.

- Four 36Mb QDR component memories.

- A 1GB DDR3 component memory.

- Two 1Gb serial peripheral interface flash memory (Quad SPI) is used to configure FPGA and Z7.

- 64 GTH transceivers (16 Quads).

- Four QSFP connectors and cages.

- Two Ethernet PHY SGMII interface with RJ-45 connectors.

- Two VITA 57.1 FMC HPC connectors.

- A ZD connector.

- JTAG interface.

- Some SMA connectors. The input trigger signal, external clock and 1pps signal are from SMA connectors.

- An USB interface.

Existing FMC module that can be attached to FMC connectors including: HMCAD1520_FMC，EV10AD190_FMC, ADC12D_FMC, ADS62P49, ADC1X26G_FMC and MD657B_FMC.

## 1.1 Key device

### 1.1.1 FPGA

Table 1-1: Device Resources of FPGA

| Logic Cells | 1,160,880 |
|---|---|
| CLB Flip-Flops | 1,326,720 |
| CLB LUTS | 663,360 |
| Distributed RAM(Mb) | 18.3 |
| Block RAM(36Kb each) | 2,160 |
| Total Block RAM(Mb) | 75.9 |
| CMTs(1 MMCM,2 PLLs) | 24 |
| I/O DLLs | 64 |
| HP I/Os | 624 |
| HR I/Os | 104 |
| DSP Slices | 5,520 |
| System Monitor | 2 |
| PCIe Gen3 x8 | 6 |
| GTH 16.3Gb/s Transceivers | 64 |

The XCKU115-FLVF1924 FPGA is based on the Xilinx Ultrascale architecture. Ultrascale architecture is a revolutionary approach to creating programmable devices capable of addressing the massive I/O and memory bandwidth requirements of next generation applications while efficiently

routing and processing the data brought on-chip. UltraScale devices address a vast spectrum of high-bandwidth, high-utilization system requirements through industry-leading technical innovations.

XCKU115-FLVF1924 FPGA has 64 GTH transceivers and 14 general I/O banks, among which 12 are1.8v-capable high-performance (HP) bank and the other 2 banks are 3.3v-capable high-range bank. There are 52 I/Os in each bank. The device resources are listed in Table 1-1.

### 1.1.2 Z7

The Zynq AP Soc XC7Z010 is based on the Xilinx All Programmable SoC architecture. These products integrate a feature-rich dual-core ARM Corte-A9 based processing system (PS) and 28 nm Xilinx programmable logic (PL) in a single device. The ARM Cortex-A9 CPUs are the heart of the PS and also include on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces. The features of Zynq AP Soc XC7Z010 are listed in Table 1-2.

Table 1-2 Zynq-7000 All Programmable SoC

| PS(processing System) | |
|---|---|
| Processor Core | Dual ARM Cortex-A9MPCore with CoreSight |
| Processor Extensions | NEON &Single/Double Precision Floating Point for each processor |
| Maximum Frequency | 667MHz(-1);766MHz(-2);866MHz(-3) |
| L1 Cache | 32KB Instruction,32KB Data per processor |
| L2 Cache | 512KB |
| On-chip Memory | 256KB |
| External Memory Support | DDR3,DDR3L,DDR2,LPDDR2 |
| External Static Memory Support | 2xQSPI,NAND,NOR |
| DMA Channels | 8(4 dedicated to PL) |
| Peripherals | 2xUART,2x CAN 2.0B,2x I2C,2xSPI,4x 32b GPIO |
| Peripherals w/built-in DMA | 2x USB2.0,2xTri-mode Gigabit Ethernet,2x SD/SDIO |
| Processing System to Programmable Logic Interface Ports | |
| AXI 32b Master | 2 |
| AXI 32b Slave | 2 |
| AXI 64-bit/32-bit Memory | 4 |
| AXI 64-bit ACP | 1 |
| Interrupts | 16 |
| Programmable Logic | |
| Logic Cells | 28k |
| LUTs | 17,600 |
| Flip-Flops | 35,200 |
| Block RAM(36Kb each) | 240KB(60) |
| DSP Slices | 80 |

## 2   The hardware design

### 2.1   Configuration circuit

In Snap2 system, the Z7 and FPGA need to be configured after power up. The process whereby the defining data is loaded or programmed into the FPGA/Z7 is called configuration. Configuration is

designed to be flexible to accommodate different application needs and, wherever possible, to leverage existing system resources to minimize system costs.

Zynq-7000 All Programmable SoC devices can be configured in secure mode using static memories only (JTAG disabled) or in non-secure mode using either JTAG or static memories. In secure mode, NAND, parallel NOR, serial NOR (Quad-SPI), and Secure Digital (SD) flash memories are used for booting the device. JTAG mode is primarily used for development and debug.

XCKU115-FLVF1924 FPGA supports a variety of configuration mode, including JTAG、Master Serial、Master SPI、Master BPI、Master select MAP、Slave select MAP、Slave serial mode。

In addition to the ways introduced above, the Ultrascale based FPGA and Zynq-7000 All Programmable SoC devices also supports Multiboot mode, which enables user update bitstream images dynamically in the field. By the Multiboot mode, user can reconfigure FPGA remotely through Ethernet.

Figure 2-1 shows the configuration circuit of the Snap2 system.
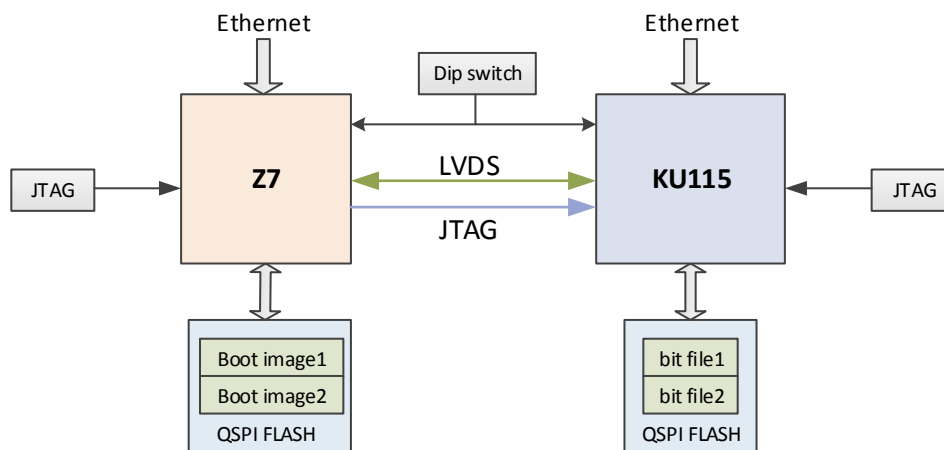


Figure 2-1 Configuration Circuit of the Snap2 System

The configuration circuit of Snap2 system is highly flexible: 1) User can configure the FPGA and Z7 through JTAG respectively for development and debug; 2) Both FPGA and Z7 have a QSPI flash for configuration. After power up, FPGA and Z7 can load or boot themselves automatically from QSPI flash; 3) User can reconfigure FPGA through the Ethernet port connected to FPGA; 4) User can reconfigure Z7 through the Ethernet port connected to Z7; 5) Z7 can configure FPGA through the JTAG interface of FPGA.

## 2.2 FPGA external interface

The Pin usage statistics of FPGA is listed in Table 2-1.

Table 2-1 Pin usage statistics of FPGA

| Object | Number | I/O | GTH | I/O voltage |
|--------|--------|-----|-----|-------------|
| QDR | 4 | 210 | 0 | 1.8v |
| DDR3 | 1 | 42 | 0 | 1.5v |
| ZD | 8 | | 28 | -- |
| QSFP | 4 | 30 | 16 | 2.5v |
| FMC(HPC) | 2 | 320 | 20 | 1.8v/2.5v |
| Z7 | 1 | 20 | 0 | 1.8v |
| PHY | 1 | 4 | 0 | 1.8v |

| SMA | 3 | 3 | 0 | |
|---|---|---|---|---|
| JTAG | 1 | 4 | 0 | 1.8 |
| FLASH | 1 | 6 | 0 | 1.8 |
| GPIO | 10 | 10 | 0 | |

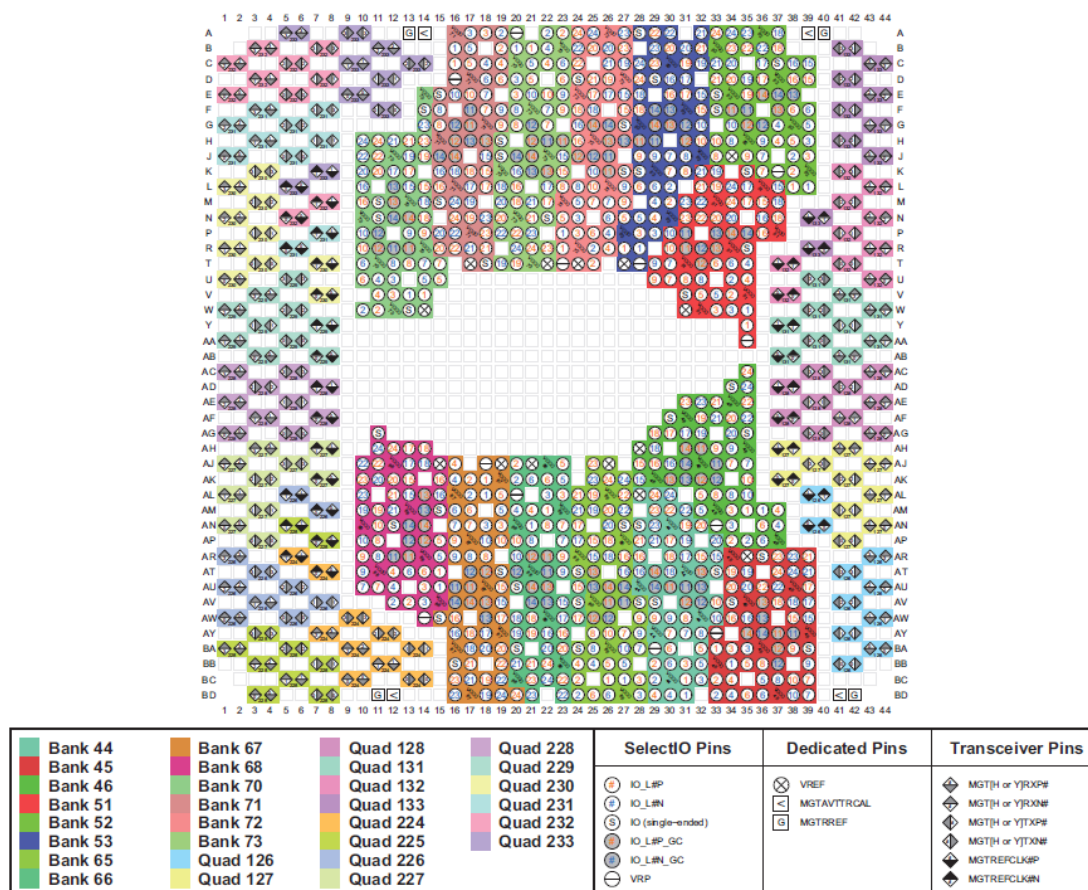The Bank diagram of XCKU115-FLVF1924 FPGA is shown in Figure 2-2.



Figure 2-2 Bank Diagram of XCKU115-FLVF1924 FPGA

According to the needs of peripheral interface, the FPGA bank assignment is listed in Table 2-2.

Table 2-2 FPGA bank assignment

| BANK | Type | Use | VCCO |
|---|---|---|---|
| 0 | HR | FPGA configuration | 1.8v |
| 65 | HR | GPIO/QSFP | 2.5v |
| 70 | HR | FMC2 | 2.5v |
| 44 | HP | QDR1/QDR2/PHY | 1.8v |
| 45 | HP | QDR1/QDR2/Z7 | 1.8v |
| 46 | HP | QDR1/QDR2 | 1.8v |
| 51 | HP | QDR3/QDR4 | 1.8v |
| 52 | HP | QDR3/QDR4 | 1.8v |
| 53 | HP | QDR3/QDR4 | 1.8v |

| 66 | HP | FMC1 | 1.8v |
|---|---|---|---|
| 67 | HP | FMC1 | 1.8v |
| 68 | HP | FMC1 | 1.8v |
| 71 | HP | FMC2 | 1.8v |
| 72 | HP | FMC2 | 1.8v |
| 73 | HP | DDR3 | 1.5v |
| 126 | GTH | FMC1 | -- |
| 127 | GTH | FMC1 | -- |
| 128 | GTH | FMC1/FMC2 | -- |
| 131 | GTH | FMC2 | -- |
| 132 | GTH | FMC2 | -- |
| 133 | GTH | ZD | -- |
| 224 | GTH | QSFP1 | -- |
| 225 | GTH | QSFP2 | -- |
| 226 | GTH | QSFP3 | -- |
| 227 | GTH | QSFP4 | -- |
| 228 | GTH | ZD | -- |
| 229 | GTH | ZD | -- |
| 230 | GTH | ZD | -- |
| 231 | GTH | ZD | -- |
| 232 | GTH | ZD | -- |
| 233 | GTH | ZD | -- |

Notes: As related banks doesn't have enough I/O pins, some devices' interface spread over several banks.

### 2.2.1  Design of FPGA external interface

2.2.1.1    GTH interface

The GTH transceivers in the UltraScale architecture are power-efficient transceivers, supporting line rates from 500 Mb/s to 16.375 Gb/s. The GTH transceiver is highly configurable and tightly integrated with the programmable logic resources of the UltraScale architecture. The GTH transceiver supports PCI Express, SFF-8431 (SFP+), 10GBASE-R/KR, Serial RapidIO (SRIO), etc.

XCKU115-FLVF1924 FPGA has 64 GTH modules. 16 of GHTs are wired to the QSFP connectors, 20 wired to the FMC HPC connectors, while the other 28 GTHs are wired to the ZD connectors

2.2.1.2    Interface to QSPI FLASH

The Quad-SPI flash memory provides nonvolatile storage that can be used for configuration and data storage. As the Bitstream Length of XCKU115-FLVF1924 FPGA is 386,012,160 bits, in order to support the Multiboot mode, the flash capacity should be more than 772,024,320 bits. This system uses N25Q00AA11GSF40G 1Gb flash of micron company. The datapath width of N25Q00AA11GSF40G is 4, and the supply voltage is 1.8v.

### 2.2.1.3    Interface to FMC

FMC is an ANSI/VITA standard that defines I/O mezzanine modules with connection to an FPGA or other device with reconfigurable I/O capability. The focus is to create a mezzanine module that minimizes the handling and formatting of the transceived data. The FMC mezzanine module uses a high-pin count 400 pin high-speed array connector, HPC. A mechanically compatible low-pin count, LPC, connector with 160 pins can also be used with any of the form factors detailed in this standard. Both FMC connectors in this system are HPC. There are 78 pairs of LVDS signal pins and 10 GTH pins in HPC and all of them are wired to FPGA directly.

### 2.2.1.4    Interface to QDR

This system uses four 36Mb QDR component memories. The part number is CY7C2263KV18 (CYPRESS). The datapath width of QDR is 18 bits and the supply voltage is 1.8v. The working frequency can be up to 550MHz.

The QDR pins are wired to bank 44/45/46/51/52/53. As the QDR uses HSTL standard, the VCCO of the banks above is 1.8v.

### 2.2.1.5    Interface to DDR3

This system uses MT41J1GB 1GB ddr3 component memory. The datapath width of this component is 8 bits and the supply voltage is 1.5v.

The DDR3 pins is wired to bank 73. As the DDR3 uses SSTL-15 standard, the VCCO of bank 73 is 1.5v.

### 2.2.1.6    Interface to PHY

The Snap2 system uses the Marvell Alaska PHY device (88E1111) for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The system supports SGMII mode only. The PHY connection to a user-provided Ethernet cable is through RJ-45 connector.

The PHY device is wired to bank44. The VCCO of bank44 is 1.8v.

### 2.2.1.7    Interface to QSFP

The Snap2 system hosts four Quad Small Form-factor Pluggable (QSFP) that accept QSFP modules. The data path of QSFP connectors is wired to GTH module and the control path is wired to bank 65 of FPGA.

### 2.2.1.8    Interface to ZD

The ZD connector is wired to 28 GTH modules of FPGA.

### 2.2.1.9    Interface to Z7

The Zynq-7000 AP SoC XC7Z010 implements interfaces to: 1) Programmable user clock; 2) USB; 3) RJ-45; 4) I2C bus to current/power monitor and temperature sensor.

The interface between FPGA and Z7 is user defined. In snap2 system, there are 10 pairs of LVDS signals between FPGA and Z7.

## 2.3 Clock circuit

### 2.3.1 Clock requirement

The FPGA need three types of clock: 1) the clock for inner temporal logic; 2) the peripheral interface clock; 3) the reference clock of GTH module. The peripheral interface clock includes the reference clock for four QDRs and a DDR3 controllers. XCKU115-FLVF1924 FPGA has 64 GTH transceivers, which is divided into 16 Quads. Each Quad needs two reference clocks in different frequency. Thus, the system needs 32 clocks for GTH module. Besides, the Z7 needs a working clock of 33MHz and two FMC connectors need some reference clocks. The other devices' clock can be generated from FPGA directly.

The system needs to be synchronous in some applications, and the whole system should have same clock source. The source can be from external though SMA connector or in the Snap2 board.

### 2.3.2 Design of clock circuit

To meet the requirement introduced above, a simple design based on oscillator is shown in the Figure 2-3.
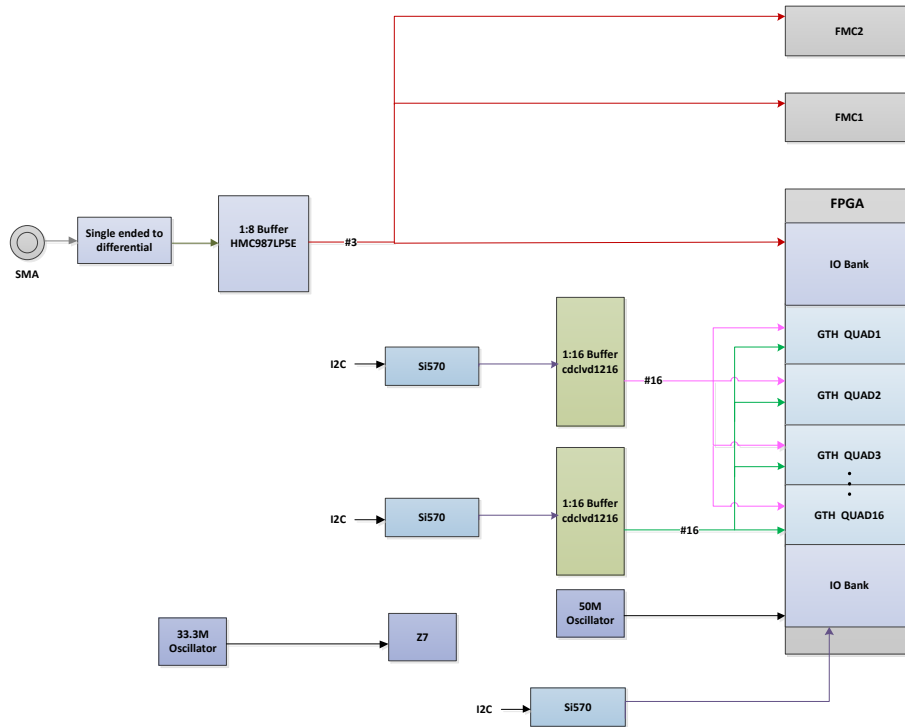


Figure 2-3 Clock Circuit Based on Oscillator

The features of the design are listed in following:

1) The external clock source is input from SMA connector. Through a clock buffer, the external clock divide into three channels, which provide clock to FMC1, FMC2 and FPGA.

2) Si570 is a 10 MHz to 1.4 GHz I2C programmable crystal oscillator. The output of Si570 is divided into 16 channels by a 1:16 clock buffer CDCLVD1216, which provide reference clocks to the GTH module of FPGA.

3) The internal clock including: A 33.3MHz oscillator for Z7, a 50MHz oscillator and a Si570

for FPGA.

To increase the flexibility of the system, another design uses a five/fen output clock generator/jitter cleaner CDCE62005 in the system. The block diagram of circuit is shown in Figure 2-4.
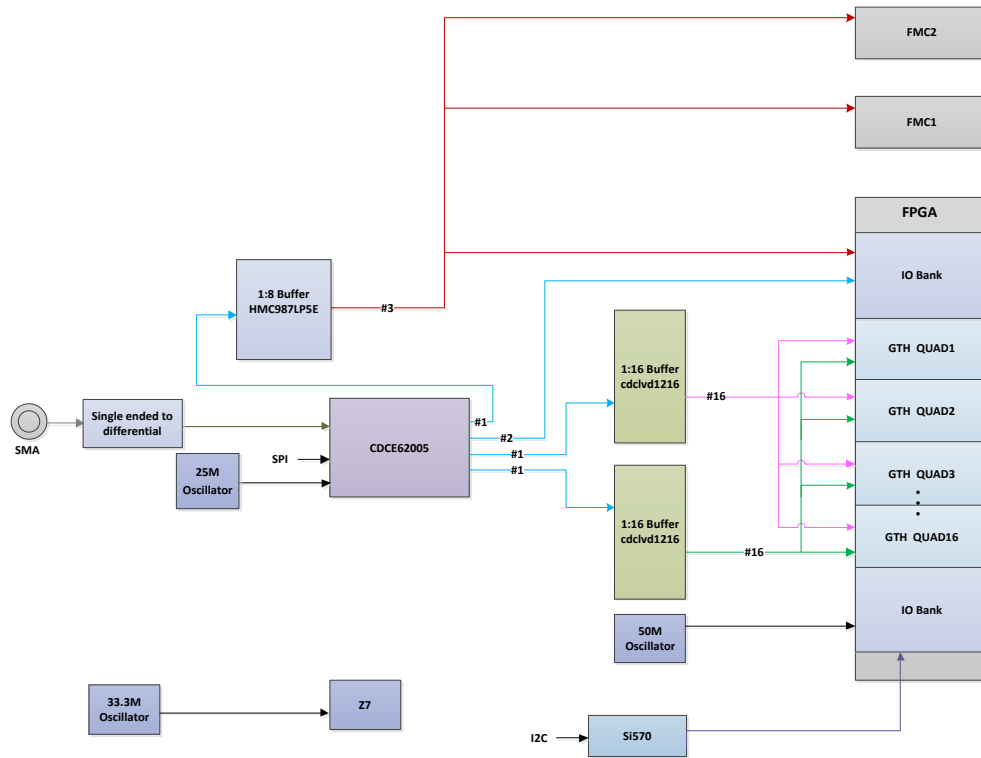


Figure 2-4 Clock Circuit Based on CECD62005

The features of CDCE62005 include: 1) Fully configurable outputs including frequency, output format, and output skew; 2) Smart input multiplexer automatically switches between one of three reference inputs; 3) Multiple operational modes include clock generation via crystal, SERDES startup mode, jitter cleaning, and oscillator holdover mode; 4)Integrated EEPROM determines device configuration at power-up; 5) Excellent jitter performance. In this design, the input of CDCE62005 is from SMA connector or the output of the crystal oscillator on board. The five outputs of CDCE62005 is distributed to FMC1, FMC2 and FPGA through clock buffers.

Comparing the two designs above, the first one is simple but it is inflexible. The second design increases the flexibility of system, but in this design, all clocks are generated from CDCE62005, which lead to a poor reliability of system. The Snap2 system synthesizes the advantages of the two design above. The block diagram of clock circuit in Snap2 system is shown in Figure 2-5.
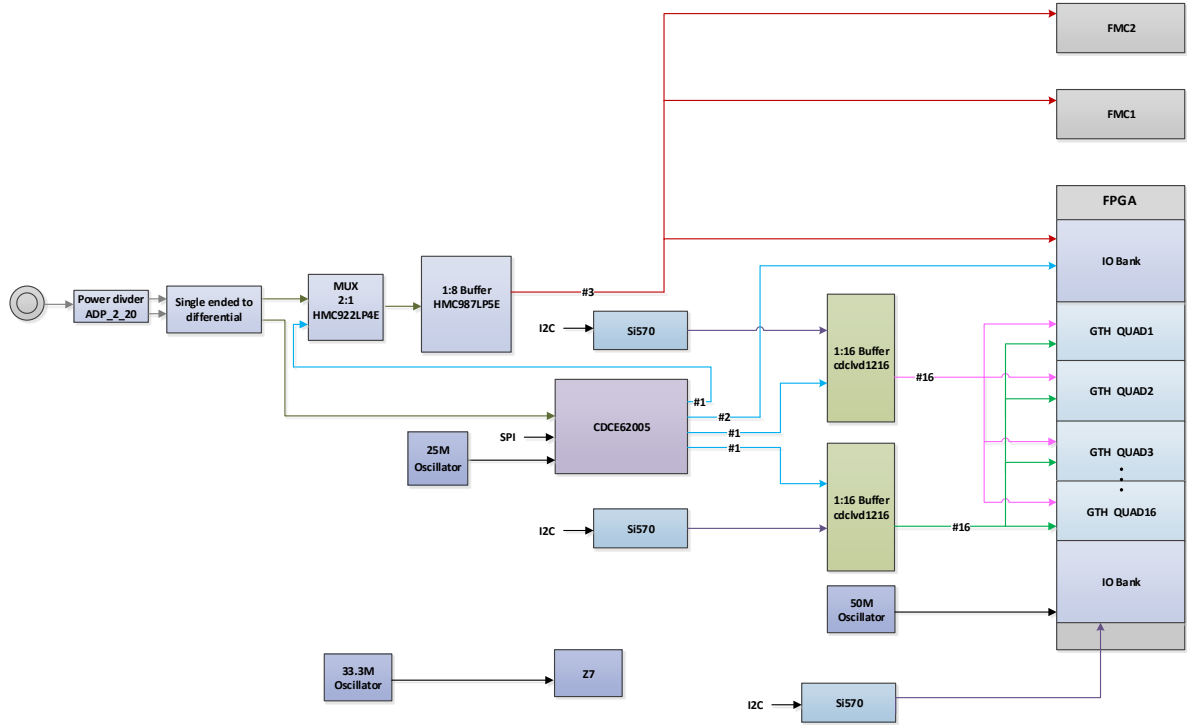
Figure 2-5 Clock Circuit Block Diagram of Snap2

CDCE62005 has five Differential outputs. Two of them are used as reference clock of QDR controllers, while two are wired to the input of CDCLVD1216. The other one is wired to a 2:1 multiplexer. The CDCLVD1216 clock buffer distributes one of two selectable clock inputs to 16 pairs of differential LVDS clock outputs. This system uses two CDCLVD1216 and has 32 Differential outputs in total. The 32 output clocks of CDCLVD1216 are used as reference clock of GTH module. One of the two selectable clock inputs is from CDCE62005, while the other one is from si570 programmable crystal oscillator. As both CDCE62005 and si570 are programmable, the frequency of GTH module reference clock is flexible.

The clock distribution of this system is listed in Table 2-3.

Table 2-3 Clock Distribution of Snap2 System

| Object | Number | Source |
|---|---|---|
| FPGA logic clock | 2 | Crystal oscillator |
| QDR controller | 2 | CDCE62005 |
| DDR3 controller | 1 | SI570 |
| GTH | 32 | CDCLVD1216 |
| FMC | 2 | HMC987LP5E |

External global user clocks must be brought into the UltraScale device on differential clock pin pairs called global clock inputs (GC). There are four GC pin pairs in each bank that have direct access to the global clock buffers, MMCMs, and PLLs that are in the CMT adjacent to the same I/O bank.

## 2.4 Power

### 2.4.1 FPGA power requirement

In this system, we estimate the FPGA power by The Xilinx Power Estimator (XPE) spreadsheet, which is a power estimation tool typically used in the pre-design and pre-implementation phases of a

project. XPE considers design's resource usage, toggle rates, I/O loading, and many other factors which it combines with the device models to calculate the estimated power distribution. In this system we set the resource utilization as 80%, the FPGA working clock as 250MHz and the estimated power distribution of XCKU115-FLVF1924 FPGA is shown in Figure 2-6.



Figure 2-6 Estimated Power Distribution of XCKU115-FLVF1924 FPGA

The power requirement of FPGA is listed in Table 2-4.

Table 2-4 FPGA power requirement

| Voltage rail | Voltage requirement（V） | current requirement（A） |
|---|---|---|
| $V_{CCINT}$ | 0.95±3%（±28mV） | 18.904 |
| $V_{CCBRAM}$ | 0.95±3%（±28mV） | 0.943 |
| $V_{CCINT\_IO}$ | 0.95±3%（±28mV） | 0.253 |
| $V_{CCAUX}$ | 1.8±3%（±54mV） | 0.571 |
| $V_{CCAUX\_IO}$ | 1.8±3%（±54mV） | 0.603 |
| $V_{CCO\_2.5V}$ | 2.5±5%（±125mV） | |
| $V_{CCO\_1.8V}$ | 1.8±5%（±90mV） | |
| $V_{CCO\_1.5V}$ | 1.5±5%（±75mV） | |
| $MGTV_{CCAUX}$ | 1.8±2.7%（±50mV） | 0.218 |
| $MGTAV_{CC}$ | 1.0±3%（±30mV） | 9.455 |
| $MGTAV_{TT}$ | 1.2±2.5%（±30mV） | 3.568 |

### 2.4.2 Other device power requirement

The power requirement of other device in system is listed in Table 2-5.

Table 2-5 Other Device Power Requirement

| Device | Part number | Power supply |
|--------|-------------|--------------|
| QDR | CY7C2263KV18 | VDD=1.8v |
| | | VREF=0.9v |
| DDR3 | MT41J1GB | VDD=1.5v |
| | | VREF=0.75v |
| FMC | ASP_134486_01 | 12P0V=12v |
| | | 3P3V=3.3v |
| | | VADJ=1.8v,2.5v |
| PHY | 88E1111 | VDD/AVDD=2.5v |
| | | DVDD=1.0v |
| RJ45 | | 2.5v |
| QSFP | | VCC=3.3v |
| FLASH | N25Q256 | VCC=1.8v |
| USB | | |

### 2.4.3 Design of power supply circuit

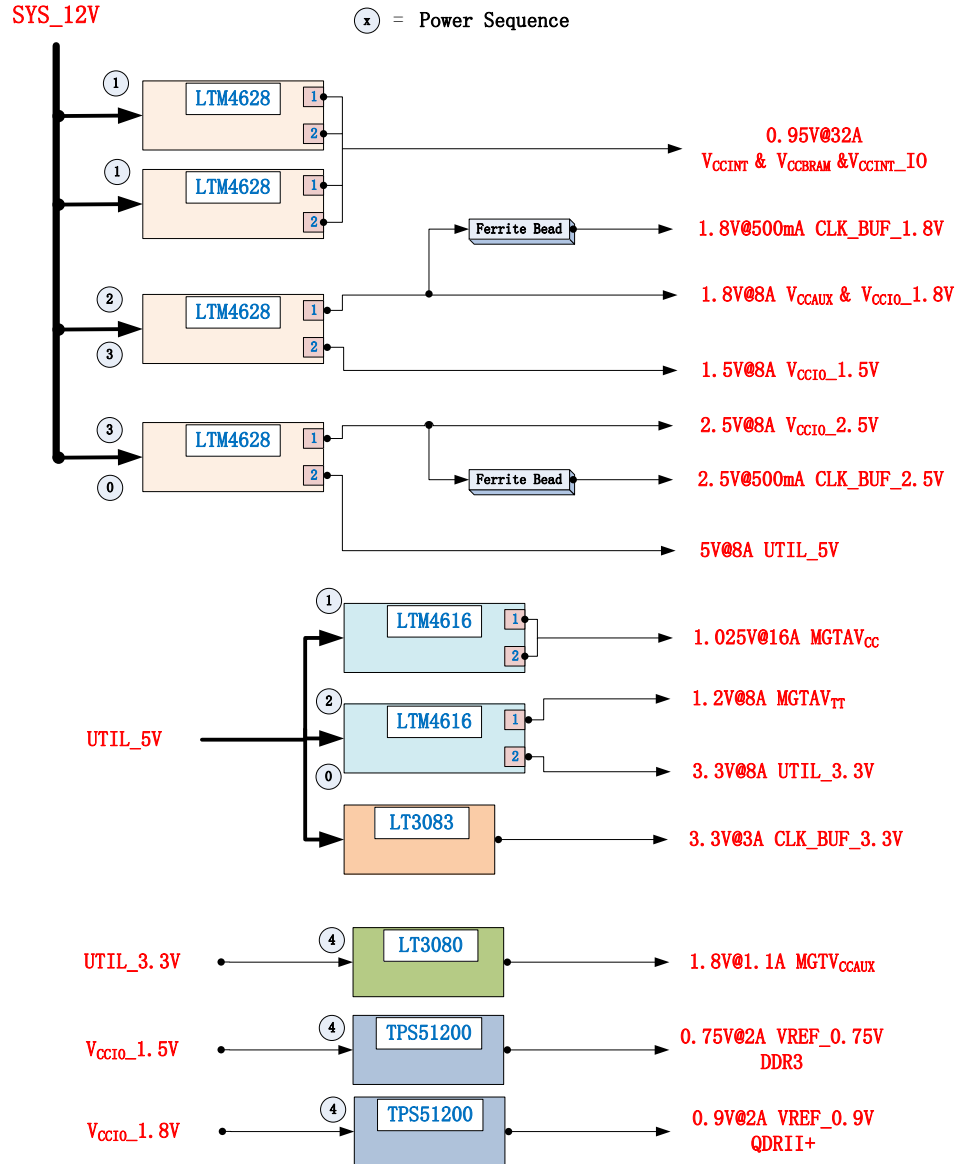The block diagram of power supply circuit is shown in **Figure 2-7**.

**Figure 2-7 Power Supply Circuit Block Diagram**

The LTM4628 is a complete dual 8A output switching mode DC/DC power supply and can be easily configured to provide a single 2-phase 16A output. Operating from an input voltage range of 4.5V to 26.5V, the LTM4628 supports two outputs each with an output voltage range of 0.6V to 5.5V. In this system, we use two LTM4628 providing a 4-phase 32A output to power the FPGA VCCINT.

The LTM4616 is a complete dual 2-phase 8A per channel switch mode DC/DC power regulator. Operating from an input voltage range of 2.7V to 5.5V, the LTM4616 supports two outputs within a voltage range of 0.6V to 5V.

The LT3080 is a 1.1A low dropout linear regulator that can be paralleled to increase output current or spread heat in surface mounted boards. The LT3080 has a wide input voltage range: 1.2V to 36V, and the dropout voltage can be down to 350 millivolts.

The LT3083 is a 3A low dropout linear regulator that can be paralleled to increase output current or spread heat on surface mounted boards. The input voltage range of LT3083 is 1.2V to 23V, and the dropout voltage can be down to 310 millivolts.

The TPS51200 is a sink/source double data rate (DDR) termination regulator specially designed for low input voltage, low-noise, low-cost systems. The TPS51200 supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, and low power DDR3/DDR4 VTT bus termination.

# 3  Board specifications

The size of Roach2 is 305X244mm. The Snap2 has s smaller size, which is 233X160mm (6U standard). There are two ZDOK connectors in Roach2, which wired 80 pairs of LVDS signals to FPGA. There is not enough I/O pins in Snap2 system for ZDOK connectors. In order to plug Z-DOK cards, we design a dedicated FMC-to-ZDOK board. The mechanical dimension diagram of Snap2 Board, Roach2 board, ADC1X26G (FMC) and FMC-to-ZDOK board (FMC) are shown in Figure 3-1.
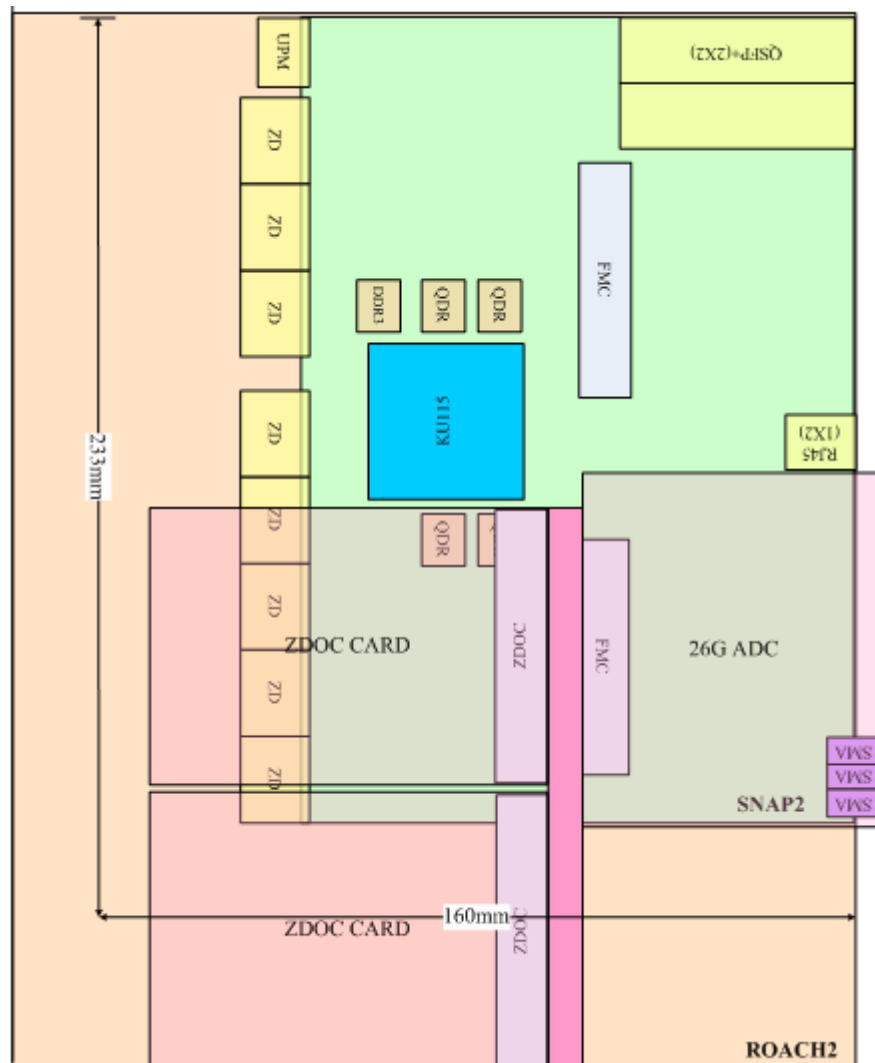


Figure 3-1 Mechanical Dimension of Snap2