WRC iBo										
	ob jumper set	ettings								
07jul24		MRD	2006dec28 cr	eated; revised	d to include D MacMahon	's DDC related function	ns			
-			2007may31 a	dd in phase s	witch and TCP/IP address	functions.				
					colored shunts for the MAC					
					of TCP/IP and Mac ID add					
es	dofault cotti	tings are in bo l	Id							
		less otherwise			+					
Shunts a	are black unit	less offerwise	designated							
mper	pins	Pitch	size	Vendor	Part	Shunt to	signal name	shunt installed	shunt gone	notes
- 1					number	use	or function	shorted pins	not connected	
					namo.	400	or randing.	Chorton pino		
	1, 2	0.1"	1 x 2	Samtec	TSW_102_26_G_S	SNT_100_BK_G	PROG (active low)	Program the FPGA	FPGA operational	in parallel with the push button switch SW1
	1, 2	0.1	1 1 2	Samec	1347_102_20_G_3	SINT_TOU_BR_G	FROG_ (active low)	Flogram the F GA	rroa operational	In paraller with the push button switch SW i
	4.0	0.4"	1.0		TOW 400 00 0 0	ONT. 400 DIC O	V004 5 to V000 BANK04	\(\(\text{OOQ}\) \(\text{DANKO4}\) \(\text{is a set to 4.5}\)	V000 DANKOA ' (bar - (b 10 14 15	
	1, 2	0.1"	1 x 2	Samtec	TSW_102_26_G_S	SNT_100_BK_G	VCC1_5 to VCCO_BANK01	VCCO_BANK01 is set to 1.5V	VCCO_BANK01 is set by other J3,J4 or J5	
	1, 2	0.1"	1 x 2	Samtec	TSW_102_26_G_S	SNT_100_BK_G	VCC1_8 to VCCO_BANK01	VCCO_BANK01 is set to 1.8V	VCCO_BANK01 is set by other J2,J4 or J5	
,										
	1, 2	0.1"	1 x 2	Samtec	TSW_102_26_G_S	SNT_100_BK_G	VCC2_5 to VCCO_BANK01	VCCO_BANK01 is set to 2.5V; this is the default	VCCO_BANK01 is set by other J2, J3 or J5	
						·		·		
	1, 2	0.1"	1 x 2	Samtec	TSW 102 26 G S	SNT_100_BK_G	VCC3 3 to VCCO BANK01	VCCO BANK01 is set to 3.3V	VCCO BANK01 is set by other J2, J3 or J4	
	i , -				1211_102_20_0_0					
	See the con-	nector page of	s not all 17 pins o	re defined for	mode/configuration jumpe	are				
	5.6	0.1"	2 x 20	Samtec	inoue/comiguration jumpe	,10	GPIO1 2; Msbit walsh sel: input 0	Input O wolch coloct Mobit is a logic 1: upless accommittee by cofficers	Input 0 walsh select Msbit is a logic 0	For all walsh select signals :
	-							Input 0 walsh select Msbit is a logic 1; unless overwritten by software		
	3,4	0.1"	2 x 20	Samtec			GPIO1_1; midbit walsh sel: input 0	Input 0 walsh select midbit is a logic 1; unless overwritten by software	Input 0 walsh select midbit is a logic 0	Shunt installed shorts PCB signal to GND
	1,2	0.1"	2 x 20	Samtec			GPIO1_0; Lsbit walsh sel: input 0	Input 0 walsh select Lsbit is a logic 1; unless overwritten by software	Input 0 walsh select Lsbit is a logic 0	FPGA inverts signal so PCB 0V = logic 1.
	13,14	0.1"	2 x 20	Samtec			GPIO1_6; Msbit walsh sel: input 1	Input 1 walsh select Msbit is a logic 1; unless overwritten by software	Input 1 walsh select Msbit is a logic 0	May be overwritten by software
,	11,12	0.1"	2 x 20	Samtec			GPIO1_5; midbit walsh sel: input 1	Input 1 walsh select midbit is a logic 1; unless overwritten by software	Input 1 walsh select midbit is a logic 0	
,	9,10	0.1"	2 x 20	Samtec			GPIO1_4; Lsbit walsh sel: input 1	Input 1 walsh select Lsbit is a logic 1; unless overwritten by software	Input 1 walsh select Lsbit is a logic 0	
,	21,22	0.1"	2 x 20	Samtec			GPIO1 10; Msbit walsh sel: input 2	Input 2 walsh select Msbit is a logic 1; unless overwritten by software	Input 2 walsh select Msbit is a logic 0	
	19,20	0.1"	2 x 20	Samtec			GPIO1_9; midbit walsh sel: input 2	Input 2 walsh select midbit is a logic 1; unless overwritten by software	Input 2 walsh select midbit is a logic 0	
	17,18	0.1"	2 x 20	Samtec			GPIO1_8; Lsbit walsh sel: input 2	Input 2 walsh select Lsbit is a logic 1; unless overwritten by software	Input 2 walsh select Lsbit is a logic 0	
	29,30	0.1"	2 x 20	Samtec			GPIO1_14; Msbit walsh sel: input 3	Input 3 walsh select Msbit is a logic 1; unless overwritten by software	Input 3 walsh select Msbit is a logic 0	
	27,28	0.1"	2 x 20	Samtec			GPIO1_14; Misbit walsh sel: input 3	Input 3 walsh select misbit is a logic 1; unless overwritten by software	Input 3 walsh select midbit is a logic 0	
	25,26	0.1"	2 x 20	Samtec			GPIO1_12; Lsbit walsh sel: input 3	Input 3 walsh select Lsbit is a logic 1; unless overwritten by software	Input 3 walsh select Lsbit is a logic 0	
ish sele	ect = 0b111 =	=/ is the highe	est frequency wal	sh signal; wal	sh select = $0b000 = 0$ is t	the slowest frequency	walsh signal			
l										
!	33,34	0.41	2 x 20	Samtec			GPIO1_16; walsh unswitch enable	Disable walsh phase Unswitching on all inputs	Enable walsh phase unswitching (all inputs)	
		0.1"	Z X Z0							
	See the con			re defined for	mode/configuration jumpe	ers				
	See the con			re defined for	mode/configuration jumpe	ers				
		nector page as	s not all J8 pins a				P address			
,2 thru	ı 27, 28 are d	nector page as	s not all J8 pins a	run and seria	I numbers and are used to	o set the MAC ID and				
,2 thru	27, 28 are d	nector page as derived from the 2:1b:AB:CD w	s not all J8 pins a e PCB, assembly here AB:CD is 0b	run and seria	I numbers and are used to 3. BPIO2_12: BPIO2_11.	o set the MAC ID and .8: BPIO2_74: BPIO2				
2 thru ID wil will be	27, 28 are d ill be 00:6d:12 ie 169.254.AE	nector page as derived from the 2:1b:AB:CD will B.CD where Al	s not all J8 pins a e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 B	run and seria o 1 0 BPIO2_1 PIO2_13. BPI	I numbers and are used to 3. BPIO2_12: BPIO2_11. D2_12: BPIO2_11.8: BPI	o set the MAC ID and .8: BPIO2_74: BPIO2				
,2 thru ID wil	27, 28 are d ill be 00:6d:12 ie 169.254.AE	derived from the 2:1b:AB:CD will B.CD where All Shunt insta	s not all J8 pins a e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Bi	run and seria o 1 0 BPIO2_1 PIO2_13. BPIO signal to GND	I numbers and are used to 3. BPIO2_12: BPIO2_11. D2_12: BPIO2_11.8: BPI	o set the MAC ID and .8: BPIO2_74: BPIO2				
,2 thru C ID wil O will be	27, 28 are d ill be 00:6d:12 ie 169.254.AE	derived from the 2:1b:AB:CD will B.CD where All Shunt insta	s not all J8 pins a e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 B	run and seria o 1 0 BPIO2_1 PIO2_13. BPIO signal to GND	I numbers and are used to 3. BPIO2_12: BPIO2_11. D2_12: BPIO2_11.8: BPI	o set the MAC ID and .8: BPIO2_74: BPIO2				
,2 thru C ID wil O will be	u 27, 28 are d ill be 00:6d:12 e 169.254.AB address bits:	derived from the 2:1b:AB:CD w B.CD where AB Shunt insta FPGA inver	e PCB, assembly here AB:CD is 0b 1 0 B:CD is 0b 1 0 Billed shorts PCB strs signal so PCB	run and seria o 1 0 BPIO2_1 PIO2_13. BPIO signal to GND 0V = logic 1.	Il numbers and are used to 3. BPIO2_12: BPIO2_11. D2_12: BPIO2_118: BPI	o set the MAC ID and .8: BPIO2_74: BPIO2_ O2_74: BPIO2_30	2_30	MAC ID odds bit 40 std. is a tarie d	MAC ID odds bit 42 st in a lessis 0	Obrt O in the register a warker of the DOD
,2 thru ID wil will be	u 27, 28 are d ill be 00:6d:12 e 169.254.AE address bits:	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver	s not all J8 pins a e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 B Illed shorts PCB tts signal so PCB	r run and seria of 1 0 BPIO2_1 PIO2_13. BPI0 signal to GND 0V = logic 1.	Il numbers and are used to 3. BPIO2_12: BPIO2_118: BPIO2_11	o set the MAC ID and a.8: BPIO2_74: BPIO2_02_74: BPIO2_30	Q_30 GPIO2_13; Lsbit 13 of MAC & IP addr, r1	MAC, IP addr bit 13, r1 is a logic 1	MAC, IP addr bit 13, r1 is a logic 0	Obr1r0 is the revision number of the PCB
,2 thru ID wil will be	u 27, 28 are d ill be 00:6d:12 e 169.254.AB address bits:	derived from the 2:1b:AB:CD w B.CD where AB Shunt insta FPGA inver	e PCB, assembly here AB:CD is 0b 1 0 B:CD is 0b 1 0 Billed shorts PCB strs signal so PCB	run and seria o 1 0 BPIO2_1 PIO2_13. BPIO signal to GND 0V = logic 1.	Il numbers and are used to 3. BPIO2_12: BPIO2_11. D2_12: BPIO2_118: BPI	o set the MAC ID and .8: BPIO2_74: BPIO2_ O2_74: BPIO2_30	2_30	MAC, IP addr bit 13, r1 is a logic 1 MAC, IP addr bit 12, r0 is a logic 1	MAC, IP addr bit 13, r1 is a logic 0 MAC, IP addr bit 12, r0 is a logic 0	0br1r0 is the revision number of the PCB And is 03
,2 thru CID will Will be	27, 28 are d ill be 00:6d:12 e 169.254.AB address bits: 27,28 25,26	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Billed shorts PCB strassignal so PCB 2 x 20 2 x 20	run and seria o 1 0 BPIO2_1 PIO2_13. BPI0 signal to GND 0V = logic 1. Samtec Samtec	Il numbers and are used to 3. BPIO2_12: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_138: BPIO2_13	3/M 929953-30 5 set the MAC ID and a.8: BPIO2_74: BPIO2_30 3/M 929953-30	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0	MAC, IP addr bit 12, r0 is a logic 1	MAC, IP addr bit 12, r0 is a logic 0	And is 03
,2 thru C ID wil D will be	u 27, 28 are d ill be 00:6d:12 e 169.254.AE address bits:	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver	s not all J8 pins a e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 B Illed shorts PCB tts signal so PCB	r run and seria of 1 0 BPIO2_1 PIO2_13. BPI0 signal to GND 0V = logic 1.	Il numbers and are used to 3. BPIO2_12: BPIO2_118: BPIO2_11	aset the MAC ID and as: BPIO2_74: BPIO2_02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser	Q_30 GPIO2_13; Lsbit 13 of MAC & IP addr, r1		1 1 2	
,2 thru C ID wil D will be	27, 28 are d ill be 00:6d:12 e 169.254.AB address bits: 27,28 25,26	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Billed shorts PCB strassignal so PCB 2 x 20 2 x 20	run and seria o 1 0 BPIO2_1 PIO2_13. BPI0 signal to GND 0V = logic 1. Samtec Samtec	Il numbers and are used to 3. BPIO2_12: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_138: BPIO2_13	3/M 929953-30 5 set the MAC ID and a.8: BPIO2_74: BPIO2_30 3/M 929953-30	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0	MAC, IP addr bit 12, r0 is a logic 1	MAC, IP addr bit 12, r0 is a logic 0	And is 03
,2 thru CID will Will be	27, 28 are d ill be 00:6d:12 e 169.254.AB address bits: 27,28 25,26	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Billed shorts PCB strassignal so PCB 2 x 20 2 x 20	run and seria o 1 0 BPIO2_1 PIO2_13. BPI0 signal to GND 0V = logic 1. Samtec Samtec	I numbers and are used to 3. BPIO2_12: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_13: BPIO2_148: BPIO2_148: BPIO2_15: BPIO2	aset the MAC ID and as: BPIO2_74: BPIO2_02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0	MAC, IP addr bit 12, r0 is a logic 1	MAC, IP addr bit 12, r0 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number
,2 thru C ID will D will be all IP ad	27, 28 are d ill be 00:6d:12 e 169.254.AR address bits: 27,28 25,26	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1" 0.1 x 0.1"	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Billed shorts PCB strs signal so PCB	r run and seria of 1 0 BPIO2_1 PIO2_13. BPIO signal to GND 0V = logic 1. Samtec Samtec Samtec	I numbers and are used to 3. BPIO2_12: BPIO2_118: BPIO2	aset the MAC ID and as: BPIO2_74: BPIO2_02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number
,2 thru	27, 28 are d ill be 00:6d:12 e 169.254.AE address bits: 27,28 25,26 23,24	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1" 0.1 x 0.1" 0.1 x 0.1"	e PCB, assembly here AB:CD is 0b 1 0 B:CD is 0b 1 0 B:B:CD is 0b 1 0 B:B:CD is 0b 2 x 20	run and seria of 1 0 BPIO2_1 PIO2_13. BPIC signal to GND 0V = logic 1. Samtec Samtec Samtec Samtec	I numbers and are used to 3. BPIO2_12: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_11	aset the MAC ID and .8: BPIO2_74: BPIO2_02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8003	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3 GPIO2_8; Lsbit 8 of MAC & IP addr, a0	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1 MAC, IP addr bit 8, a0 is a logic 1	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0 MAC, IP addr bit 8, a0 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015
,2 thru	27, 28 are d ill be 00:6d:12 e 169.254.AR address bits: 27,28 25,26	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1" 0.1 x 0.1"	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Billed shorts PCB strs signal so PCB	r run and seria of 1 0 BPIO2_1 PIO2_13. BPIO signal to GND 0V = logic 1. Samtec Samtec Samtec	I numbers and are used to 3. BPIO2_12: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_118	aset the MAC ID and .8: BPIO2_74: BPIO2_02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8003	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015 Obs7s6s5s4s3s2s1s0 is the serial number of the
2 thru	27, 28 are d ill be 00:6d:12 e 169.254.AE address bits: 27,28 25,26 23,24 17,18	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1"	e PCB, assembly here AB:CD is 0b 1 0 B:CD is 0b 1 0 B:CD is 0b 10 B:CD i	run and seria of 1 0 BPIO2_1 PIO2_13. BPIC signal to GND 0V = logic 1. Samtec Samtec Samtec Samtec Samtec Samtec	Inumbers and are used to a BPIO2_12: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_11	aset the MAC ID and .8: BPIO2_74: BPIO2_02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8003	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3 GPIO2_8; Lsbit 8 of MAC & IP addr, a0 GPIO2_0; Lsbit 0 of MAC and IP addr, s7	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1 MAC, IP addr bit 8, a0 is a logic 1 MAC, IP addr bit 0, s7 is a logic 1	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0 MAC, IP addr bit 8, a0 is a logic 0 MAC, IP addr bit 7, s7 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015
,2 thru	27, 28 are d ill be 00:6d:12 e 169.254.AE address bits: 27,28 25,26 23,24	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1" 0.1 x 0.1" 0.1 x 0.1"	e PCB, assembly here AB:CD is 0b 1 0 B:CD is 0b 1 0 B:B:CD is 0b 1 0 B:B:CD is 0b 2 x 20	run and seria of 1 0 BPIO2_1 PIO2_13. BPIC signal to GND 0V = logic 1. Samtec Samtec Samtec Samtec	I numbers and are used to 3. BPIO2_12: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_118	aset the MAC ID and .8: BPIO2_74: BPIO2_02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8003	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3 GPIO2_8; Lsbit 8 of MAC & IP addr, a0	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1 MAC, IP addr bit 8, a0 is a logic 1	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0 MAC, IP addr bit 8, a0 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015 Obs7s6s5s4s3s2s1s0 is the serial number of the
,2 thru	27, 28 are d ill be 00:6d:12 e 169.254.AE address bits: 27,28 25,26 23,24 17,18 15,16	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1"	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Billed shorts PCB sts signal so PCB 2 x 20 2	run and seria of 1 0 BPIO2_1 PIO2_13. BPIO Signal to GND OV = logic 1. Samtec Samtec Samtec Samtec Samtec Samtec Samtec	Inumbers and are used to a BPIO2_12: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_11	aset the MAC ID and as: BPIO2_74: BPIO2_02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8003	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3 GPIO2_8; Lsbit 8 of MAC & IP addr, a0 GPIO2_0; Lsbit 0 of MAC and IP addr, s7 GPIO2_0; Lsbit 0 of MAC and IP addr, s0	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1 MAC, IP addr bit 8, a0 is a logic 1 MAC, IP addr bit 0, s7 is a logic 1 MAC, IP addr bit 0, s0 is a logic 1	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0 MAC, IP addr bit 8, a0 is a logic 0 MAC, IP addr bit 7, s7 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015 Obs7s6s5s4s3s2s1s0 is the serial number of the
,2 thru	27, 28 are d ill be 00:6d:12 e 169.254.AE address bits: 27,28 25,26 23,24 17,18	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1"	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 B B:CD is 0b 10 B B:CD is 0b 1	run and seria of 1 0 BPIO2_1 PIO2_13. BPIO Signal to GND OV = logic 1. Samtec Samtec Samtec Samtec Samtec Samtec Samtec TCP/IP	Inumbers and are used to a BPIO2_12: BPIO2_118: BPIO2_12: BPIO2_118: BPIO2_11	set the MAC ID and 8: BPIO2_74: BPIO2 02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8003 Mouser 151-8001 rev;run;S/N	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3 GPIO2_8; Lsbit 8 of MAC & IP addr, a0 GPIO2_0; Lsbit 0 of MAC and IP addr, s7 GPIO2_0; Lsbit 0 of MAC and IP addr, s0 TCP/IP address	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1 MAC, IP addr bit 8, a0 is a logic 1 MAC, IP addr bit 0, s7 is a logic 1 MAC, IP addr bit 0, s0 is a logic 1 HCRO iBob "hardware" names (hcro.org suffix not shown)	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0 MAC, IP addr bit 8, a0 is a logic 0 MAC, IP addr bit 7, s7 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015 Obs7s6s5s4s3s2s1s0 is the serial number of the
,2 thru	27, 28 are d ill be 00:6d:12 e 169.254.AB address bits: 27,28 25,26 23,24 17,18 15,16 1,2 iBob rev	Derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1" 0.1 x 0	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Billed shorts PCB strs signal so PCB 2 x 20 2	run and seria of 1 0 BPIO2_1 PIO2_13. BPIO Signal to GND OV = logic 1. Samtec Samtec Samtec Samtec Samtec Samtec Samtec TCP/IP Address	I numbers and are used to 3. BPIO2_12: BPIO2_11. BPIO2_1	set the MAC ID and 8: BPIO2_74: BPIO2_ O2_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8003 Mouser 151-8001	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3 GPIO2_8; Lsbit 8 of MAC & IP addr, a0 GPIO2_0; Lsbit 0 of MAC and IP addr, s7 GPIO2_0; Lsbit 0 of MAC and IP addr, s0 TCP/IP address 169.254.129.N	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1 MAC, IP addr bit 8, a0 is a logic 1 MAC, IP addr bit 0, s7 is a logic 1 MAC, IP addr bit 0, s0 is a logic 1 HCRO iBob "hardware" names (hcro.org suffix not shown) ibob-aN	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0 MAC, IP addr bit 8, a0 is a logic 0 MAC, IP addr bit 7, s7 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015 Obs7s6s5s4s3s2s1s0 is the serial number of the
,2 thru	27, 28 are d ill be 00:6d:12 e 169.254.AE address bits: 27,28 25,26 23,24 17,18 15,16	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1"	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 B B:CD is 0b 10 B B:CD is 0b 1	run and seria of 1 0 BPIO2_1 PIO2_13. BPIO Signal to GND OV = logic 1. Samtec Samtec Samtec Samtec Samtec Samtec Samtec TCP/IP	I numbers and are used to 3. BPIO2_12: BPIO2_11. BPIO2_1	set the MAC ID and 8: BPIO2_74: BPIO2 02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8003 Mouser 151-8001 rev;run;S/N	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3 GPIO2_8; Lsbit 8 of MAC & IP addr, a0 GPIO2_0; Lsbit 0 of MAC and IP addr, s7 GPIO2_0; Lsbit 0 of MAC and IP addr, s0 TCP/IP address 169.254.129.N 169.254.145.N	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1 MAC, IP addr bit 8, a0 is a logic 1 MAC, IP addr bit 0, s7 is a logic 1 MAC, IP addr bit 0, s0 is a logic 1 HCRO iBob "hardware" names (hcro.org suffix not shown)	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0 MAC, IP addr bit 8, a0 is a logic 0 MAC, IP addr bit 7, s7 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015 Obs7s6s5s4s3s2s1s0 is the serial number of the
,2 thru	27, 28 are d ill be 00:6d:12 e 169.254.AB address bits: 27,28 25,26 23,24 17,18 15,16 1,2 iBob rev	Derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1" 0.1 x 0	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Billed shorts PCB strs signal so PCB 2 x 20 2	run and seria of 1 0 BPIO2_1 PIO2_13. BPIO Signal to GND OV = logic 1. Samtec Samtec Samtec Samtec Samtec Samtec Samtec TCP/IP Address	I numbers and are used to 3. BPIO2_12: BPIO2_11. BPIO2_1	set the MAC ID and 8: BPIO2_74: BPIO2_ O2_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8003 Mouser 151-8001	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3 GPIO2_8; Lsbit 8 of MAC & IP addr, a0 GPIO2_0; Lsbit 0 of MAC and IP addr, s7 GPIO2_0; Lsbit 0 of MAC and IP addr, s0 TCP/IP address 169.254.129.N	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1 MAC, IP addr bit 8, a0 is a logic 1 MAC, IP addr bit 0, s7 is a logic 1 MAC, IP addr bit 0, s0 is a logic 1 HCRO iBob "hardware" names (hcro.org suffix not shown) ibob-aN	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0 MAC, IP addr bit 8, a0 is a logic 0 MAC, IP addr bit 7, s7 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015 Obs7s6s5s4s3s2s1s0 is the serial number of the
,2 thru	27, 28 are d ill be 00:6d:12 e 169.254.AB address bits: 27,28 25,26 23,24 17,18 15,16 1,2 iBob rev	Derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1" 0.1 x 0	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Billed shorts PCB strs signal so PCB 2 x 20 2 x 30 2 x 30 2 x 30 3 2 x 30 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	run and seria of 1 0 BPIO2_1 PIO2_13. BPIO pio2_14. BPIO2_15 pio2_15.	I numbers and are used to 3. BPIO2_12: BPIO2_11. 8: BPIO2_11. 8: BPIO2_12: BPIO2_11. 8: BPIO2_11	D set the MAC ID and B: BPIO2_74: BPIO2_02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8001 rev;run;S/N 0; 1; N 1; 1; N 2; 1; N	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3 GPIO2_8; Lsbit 8 of MAC & IP addr, a0 GPIO2_0; Lsbit 0 of MAC and IP addr, s7 GPIO2_0; Lsbit 0 of MAC and IP addr, s0 TCP/IP address 169.254.129.N 169.254.145.N 169.254.161.N	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1 MAC, IP addr bit 8, a0 is a logic 1 MAC, IP addr bit 0, s7 is a logic 1 MAC, IP addr bit 0, s0 is a logic 1 HCRO iBob "hardware" names (hcro.org suffix not shown) ibob-aN ibob-bN ibob-cN	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0 MAC, IP addr bit 8, a0 is a logic 0 MAC, IP addr bit 7, s7 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015 Obs7s6s5s4s3s2s1s0 is the serial number of the
,2 thru	127, 28 are d ill be 00:6d:12 e 169.254.AE ddress bits: 27,28 25,26 23,24 17,18 15,16 1,2 iBob rev 1 2 2	Derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1" 0.1 x 0.1 1 0.1 1 0.1 x 0.1 1	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Billed shorts PCB strs signal so PCB 2 x 20 2	run and seria of 1 0 BPIO2_1 PIO2_13. BPIO pio2_14. BPIO2_14 pio2_15. BPIO2_15 pio2_15 pio2_	I numbers and are used to 3. BPIO2_12: BPIO2_11. 8: BPIO2_11. 8: BPIO2_12: BPIO2_11. 8: BPIO2_11	Diset the MAC ID and .8: BPIO2_74: BPIO2_02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8003 Mouser 151-8001 rev;run;S/N 0; 1; N 1; 1; N 2; 1; N 2; 2; N	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3 GPIO2_8; Lsbit 8 of MAC & IP addr, a0 GPIO2_0; Lsbit 0 of MAC and IP addr, s7 GPIO2_0; Lsbit 0 of MAC and IP addr, s0 TCP/IP address 169.254.129.N 169.254.145.N 169.254.161.N 169.254.162.N	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1 MAC, IP addr bit 8, a0 is a logic 1 MAC, IP addr bit 0, s7 is a logic 1 MAC, IP addr bit 0, s0 is a logic 1 HCRO iBob "hardware" names (hcro.org suffix not shown) ibob-aN ibob-bN ibob-cN ibob-dN	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0 MAC, IP addr bit 8, a0 is a logic 0 MAC, IP addr bit 7, s7 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015 Obs7s6s5s4s3s2s1s0 is the serial number of the
1,2 thru C ID will D will be all IP ac	127, 28 are d ill be 00:6d:12 ie 169.254.AE iddress bits: 27,28 25,26 23,24 17,18 15,16 1,2 iBob rev 1 2 2 3	derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1" 0.1 x 0.1 1 0.1 1 0.1 x 0.1 1 0.	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Billed shorts PCB sts signal so PCB 2 x 20 2	run and seria of 1 0 BPIO2_1 PIO2_13. BPIC gignal to GND OV = logic 1. Samtec Samtec Samtec Samtec Samtec TCP/IP Address 169.254.14 169.254.16 169.254.16	Inumbers and are used to 3. BPIO2_12: BPIO2_11. BPIO2_11	Diset the MAC ID and .8: BPIO2_74: BPIO2_02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8003 Mouser 151-8001 rev;run;S/N 0; 1; N 1; 1; N 2; 1; N 2; 2; N 3; 1; N	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3 GPIO2_8; Lsbit 8 of MAC & IP addr, a0 GPIO2_0; Lsbit 0 of MAC and IP addr, s7 GPIO2_0; Lsbit 0 of MAC and IP addr, s0 TCP/IP address 169.254.129.N 169.254.145.N 169.254.161.N 169.254.162.N 169.254.177.N	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1 MAC, IP addr bit 8, a0 is a logic 1 MAC, IP addr bit 0, s7 is a logic 1 MAC, IP addr bit 0, s0 is a logic 1 HCRO iBob "hardware" names (hcro.org suffix not shown) ibob-aN ibob-bN ibob-cN ibob-dN ibob-dN ibob-eN	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0 MAC, IP addr bit 8, a0 is a logic 0 MAC, IP addr bit 7, s7 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015 Obs7s6s5s4s3s2s1s0 is the serial number of the
1,2 thru	127, 28 are d ill be 00:6d:12 e 169.254.AE ddress bits: 27,28 25,26 23,24 17,18 15,16 1,2 iBob rev 1 2 2	Derived from the 2:1b:AB:CD where AB Shunt insta FPGA inver 0.1 x 0.1" 0.1 x 0.1 1 0.1 1 0.1 x 0.1 1	e PCB, assembly here AB:CD is 0b B:CD is 0b 1 0 Billed shorts PCB strs signal so PCB 2 x 20 2	run and seria of 1 0 BPIO2_1 PIO2_13. BPIO pio2_14. BPIO2_14 pio2_15. BPIO2_15 pio2_15 pio2_	Inumbers and are used to 3. BPIO2_12: BPIO2_11. BPIO2_11	Diset the MAC ID and .8: BPIO2_74: BPIO2_02_74: BPIO2_30 3/M 929953-30 517-953-30 Mouser 151-8003 Mouser 151-8001 rev;run;S/N 0; 1; N 1; 1; N 2; 1; N 2; 2; N	GPIO2_13; Lsbit 13 of MAC & IP addr, r1 GPIO2_12; Lsbit 12 of MAC & IP addr, r0 GPIO2_11; Lsbit 11 of MAC & IP addr, a3 GPIO2_8; Lsbit 8 of MAC & IP addr, a0 GPIO2_0; Lsbit 0 of MAC and IP addr, s7 GPIO2_0; Lsbit 0 of MAC and IP addr, s0 TCP/IP address 169.254.129.N 169.254.145.N 169.254.161.N 169.254.162.N	MAC, IP addr bit 12, r0 is a logic 1 MAC, IP addr bit 11, a3 is a logic 1 MAC, IP addr bit 8, a0 is a logic 1 MAC, IP addr bit 0, s7 is a logic 1 MAC, IP addr bit 0, s0 is a logic 1 HCRO iBob "hardware" names (hcro.org suffix not shown) ibob-aN ibob-bN ibob-cN ibob-dN	MAC, IP addr bit 12, r0 is a logic 0 MAC, IP addr bit 11, a3 is a logic 0 MAC, IP addr bit 8, a0 is a logic 0 MAC, IP addr bit 7, s7 is a logic 0	And is 03 Oba3a2a1a0 is the assembly run number And is 015 Obs7s6s5s4s3s2s1s0 is the serial number of the

J10	1,2	0.1"x0.1"	2 x 8			SNT_100_BK_G	DIPSW_SIGS<0>	DIPSW_SIGS<0> is shorted to GND.	DIPSW_SIGS<0> is pulled to 2.5V	
110	3,4					SNT_100_BK_G	DIPSW_SIGS<1>	DIPSW_SIGS<1> is shorted to GND.	DIPSW_SIGS<1> is pulled to 2.5V	
10	5,6					SNT_100_BK_G	DIPSW_SIGS<2>	DIPSW_SIGS<2> is shorted to GND.	DIPSW_SIGS<2> is pulled to 2.5V	
10	7,8					SNT_100_BK_G	DIPSW_SIGS<3>	DIPSW_SIGS<3> is shorted to GND.	DIPSW_SIGS<3> is pulled to 2.5V	
10	9,10					SNT_100_BK_G	DIPSW_SIGS<4>	DIPSW_SIGS<4> is shorted to GND.	DIPSW_SIGS<4> is pulled to 2.5V	
10	11,12					SNT_100_BK_G	DIPSW_SIGS<5>	DIPSW_SIGS<5> is shorted to GND.	DIPSW_SIGS<5> is pulled to 2.5V	
J10	13,14					SNT_100_BK_G	DIPSW_SIGS<6>	DIPSW_SIGS<6> is shorted to GND.	DIPSW_SIGS<6> is pulled to 2.5V	
J10	15,16					SNT_100_BK_G	DIPSW_SIGS<7>	DIPSW_SIGS<7> is shorted to GND.	DIPSW_SIGS<7> is pulled to 2.5V	
J11	1,2	0.1"	1 x 3		SIP 1x3	SNT 100 BK G	MGT BOTTOM CLK M	XTAL2 125.00 Mhz; note many boards do NOT have 125MHz XTALs	pin 2 must be	J11 and J12 shunts must be in same position!
J12	1,2	0.1"	1 x 3		SIP 1x3	SNT_100_BK_G		XTAL2 125.00 Mhz; installed and thus this mode may be nonfunctional.	tied to pin 1 or	pin 3s are labled
J11	2,3	0.1"	1 x 3		SIP 1x3	SNT_100_BK_G	MGT BOTTOM CLK M	XTAL3 156.25 Mhz; many boards only have 156.25 Mhz XTALs	pin 2 must be	J11 and J12 shunts must be in same position!
J12	2,3	0.1"	1 x 3		SIP 1x3	SNT_100_BK_G		XTAL3 156.25 Mhz;thus jumpers must be in these positions	tied to pin 3 (or pin 1 shown above)	pin 3s are labled
J13	1,2	0.1"	1 x 3		SIP 1x3	SNT_100_BK_G	MGT TOP CLK M	XTAL2 125.00 Mhz; note many boards do NOT have 125MHz XTALs	pin 2 must be	J13 and J14 shunts must be in same position!
J14	1,2	0.1"	1 x 3		SIP 1x3	SNT_100_BK_G		XTAL2 125.00 Mhz; installed and thus this mode may be nonfunctional.	tied to pin 1 or	pin 3s are labled
J13	2,3	0.1"	1 x 3		SIP 1x3	SNT_100_BK_G	MGT_TOP_CLK_M	XTAL3 156.25 Mhz; many boards only have 156.25 Mhz XTALs	pin 2 must be	J13 and J14 shunts must be in same position!
J14	2,3	0.1"	1 x 3		SIP 1x3	SNT_100_BK_G	MGT_TOP_CLK_P	XTAL3 156.25 Mhz;thus jumpers must be in these positions	tied to pin 3 (or pin 1 shown above)	pin 3s are labled
J15 J15	1,2 3,4	0.1" x 0.1"	2 x 3		SIP 2x3		FPGA_CFGMODE0; U1.AF26 FPGA_CFGMODE1:U1.AE26	M0 = 0 M1 = 0	M0 = 1 M1 = 1	See table below See table below
J15 J15	5,6						FPGA_CFGMODE1,01.AE25	M2 = 0	M2 = 1	See table below
10) = 0b110 = Sla	ve SelectMap Mo	ode. Virtex II I	Pro FPGA is programmed		memory mapped writes over the cPCI bus.		1012 - 1	Occ table below
	M2:M1:M0) = 0b111 = Sla	ve Serial Mode. \	Virtex II Pro F	PGA is programmed 1bit	at a time from memo	ry mapped writes over the cPCI bus (saves	s 7 pins over Slave Select Map).		
							and is specified in the official iBob initial to	est procedure		
	M2:M1:M0) = 0b011 = Ma	ster SelectMAP n	node; This is	s the default. FPGA is the	e source of CCLK,DO	NE and INIT_B(to PROM's RESET_/OE)			
J16	1,2	0.1" x 0.1"	2 x 3		SIP 2x3	SNT_100_BK_G		design revision set by REV_SEL_MODE1:2 bits	internal revision select control bits	EN_EXT_SEL_ on the flash PROM
J16 J16	3,4 5.6					SNT_100_BK_G SNT 100 BK G	REV_SEL_MODE1: U2-26 REV SEL MODE2: U2-27	MODE[1:0] = select 1 of 4 unique designs stored within the 1 PROM IC when enabled by REV_SEL_MODE0 shunt installed; otherwise ignored.	ignored due to MODE0; do not install ignored due to MODE0; do not install	REV_SEL0 on the flash PROM REV_SEL1 on the flash PROM
10	- / -	ision set by PE	V SEL MODE1:2	2 hits		SINT_TOU_DR_G	INL V_SEL_IVIODE2. U2-21	when chapted by KEV_SEL_INODED SHufft Installed, Otherwise Ignored.	ignored due to MODEO, do not install	INL V_SELT OIT THE HASH PROM
			unique designs s		the 1 PROM IC					
	when enah	oled by RFV SF	I MODEO shun	t installed oth	nerwise they are ignored.					
	WINGIT GITAL	JIGG DY INE V_OL	WODEO SHUII	i i i i i i i i i i i i i i i i i i i	ior moc they are ignored.					

	b jumper se									
2006dec28		created								
These ar	en't jumpe	ers exactly b	out they are	e connectors and have Jxx refere	ence designators.					
Jumper	nins	Pitch	size	PCB conn.	Connector	Connector	signal name	Mating connector		notes
bumper	piiis	1 1011	3120		Vendor	Part number	or function			Hotes
				type	Vendor	Part Humber	or function	Vendor	Part Number	
J6	1 to 40	0.1 x 0.1"	2 x 20	DIP 2 x 20			GPIO0_[019]			closest to the FPGA, pin 1 marked with "o"; all even pins=GND
16	1,5,9,13,17,	,21,25,29					LVTTL; GPIO0_0,2,4,6,8,10,	12,14 External sync	out signals; for sync	cing standalone iBobs when no external sync signal is available.
	4 . 40	0.4.0.4"	0.00	DID 0 00			00004 50 40			in the American Court of the Co
J7	1 to 40	0.1 x 0.1"	2 x 20	DIP 2 x 20			GPIO1_[019]			just closer to PCB edge than J6, pin 1 marked with "o"; all even pins=GND
										See the Jumper page as well; part of J7 is used for mode/config jumpers
J8	1 to 40	0.1 x 0.1"	2 x 20	DIP 2 x 20			GPIO2_[019]			closest to PCB edge, pin 1 marked with "o"; all even pins=GND
,,,	1 10 10	0.1 × 0.1	2 x 20	DII Z X Z O			G1 102_[010]			See the Jumper page as well; part of J8 is used for mode/config jumpers
										, , , , , , , , , , , , , , , , , , ,
J9	1 to 40	0.1 x 0.1"	2 x 20	DIP 2 x 20			GPIO3_[019]			just farther from PCB edge than J8, pin 1 marked with "o"; all even pins=GND
9	33						LVTTL; GPIO3_16; Walsh ou	tput for input 0; for r	monitoring or driving	g level shifters/mixers etc
9	35						LVTTL; GPIO3_17; Walsh ou			
9	37						LVTTL; GPIO3_18; Walsh ou			
19	39						LVTTL; GPIO3_19; Walsh ou	tput for input 3; for r	monitoring or driving	g level shifters/mixers etc
244	4.1-0	0.4"	4 0	OID 4 · · · O	0	TOW 400 00 0 0	-5\/DQ ((NA-1	00 50 0444	(0) I/// Oction (const. 00 00AM/Oction (const.)
D11	1 to 2	0.1"	1 x 2	SIP 1 x 2	Samtec	TSW_102_26_G_S	+5VDC for fan	Molex Molex	08-50-0114	two (2) KK-Series female 22-30AWG crimp terminals
								IVIOIEX	22-01-3037	KK-series 3-pin housing
J17	1 to 9	0.1"	1 x 9	SIP 1 x 9	Samtec	TSW_109_14_G_S	JTAG			VCC2_5, GND, NC, JTAG_TCK, NC, JTAG_TDO, JTAG_TDI, NC, JTAG_TMS
, , ,	1 10 0	0.1	1 7 3	CII 1 X O	Carried	1011_100_14_0_0	01710			V002_0, 0115, 110, 01110_1011, 110, 01110_150, 01110_151, 110, 01110_1111
J18	1 to 5	0.1"	1 x 5	sip 1 x 5			RS232 link			RS232 RX,TX,GND,CTS, RTS
				·						
J19	1 to 2			50A Power	Molex	42820-2212	VCC5	Molex	42815-0011	two (2) 10 AWG Mini-Fit Sr. power cable crimp terminals
								Molex	42816-0212	2-pos Mini-Fit Sr power cable housing
100	4			INFINIDAND (IV		04004.0412	T . ()			
J20	1 to 25			INFINIBAND 4X	Molex	91804-0410	Top infiniband link 0			also has 6 mounting pins; this connector gets screwed to the PCB
J21	1 to 25			INFINIBAND 4X	Molex	91804-0410	bottom infiniband link 1			also has 6 mounting pins; this connector gets screwed to the PCB
14 1	1 10 23			INCINIDAND 4A	IVIOIEX	31004-0410	DOLLOTT ITTITIDATIO IITK 1			also has a mounting pins, this connector gets screwed to the PCB
J22	1 to 144			40-PAIR LVDS Z-DOK+ Host	Tyco	6367550-5	ADC0 diff. inputs			J22 is closer to the 100 Mbit connector
				.5 / / 2 / 2 / 2 / 2 / 1 / 1050	1,500	300,000 0				SEE 15 5.5501 to the 100 max controller
J23	1 to 144			40-PAIR LVDS Z-DOK+ Host	Тусо	6367550-5	ADC1 diff inputs			J23 is closer to the VDC input power connector
-					, , , ,	1 2 2 2 2 2	1, 555			
J24	1 to 80		MDR	80-PIN MINI D RIBBON RA	3M	N10280-52E2VC	LVDS_GPIO_M/P[039]			
J115	1 to 12	.072"	RJ45	MAGJACK SMT 10/100Mbit	Pulse	J3011G21D	PHY_TPO, TPI, LAN_LED,	CAT-5e, cable		only available on v1_rev2 and v1_rev3 boards
				with LEDs						some of the v1_rev2 iBobs have faults that cause Ethernet failures