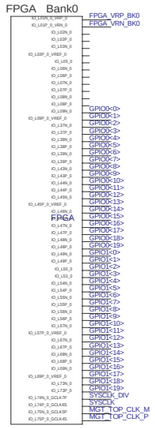
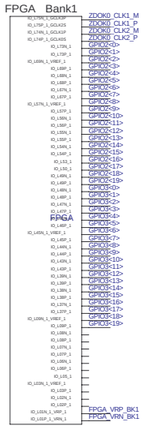
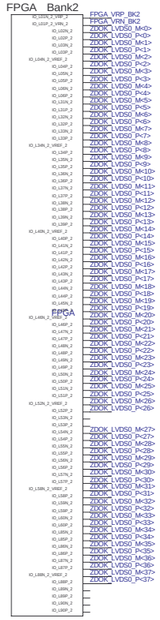
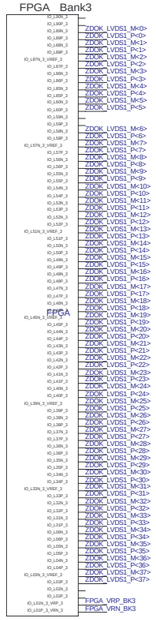
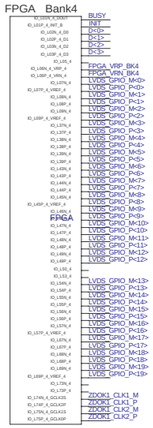
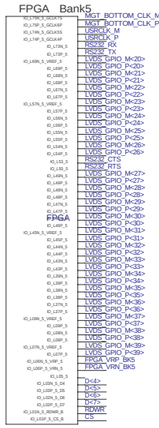


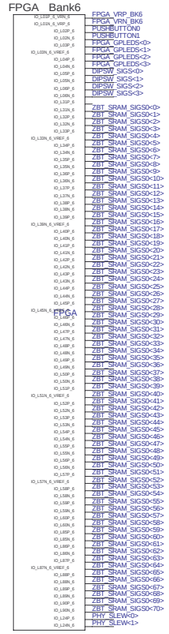


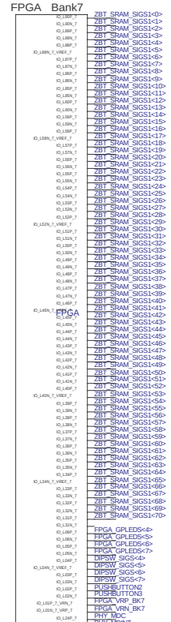


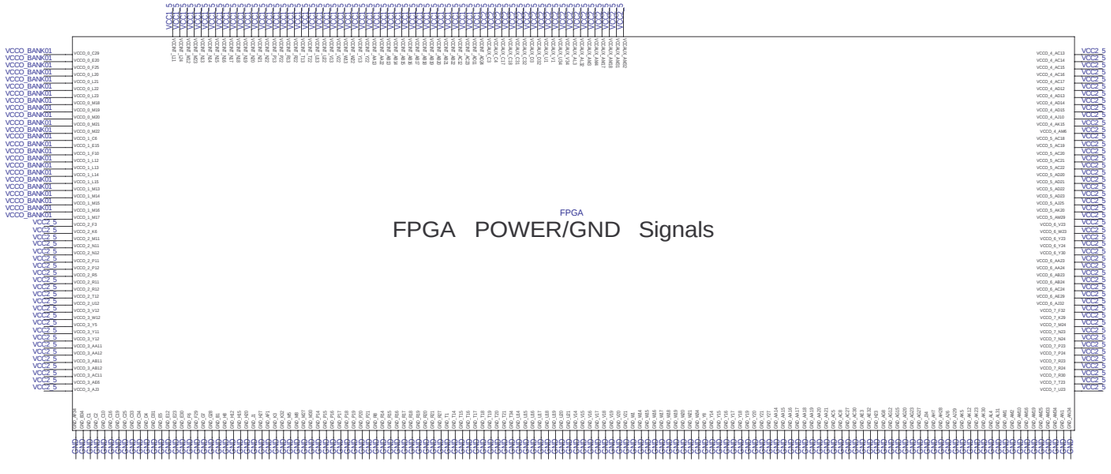


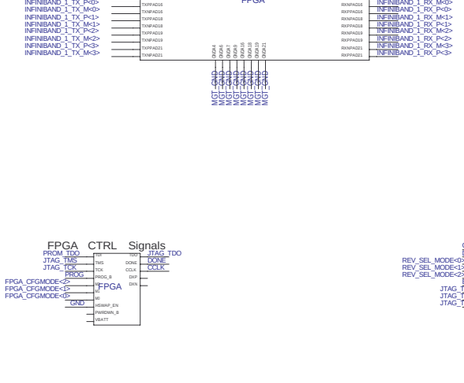


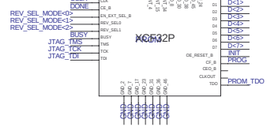












CHEN CHANG
EECS UC BERKELEY
BEE2 GROUP

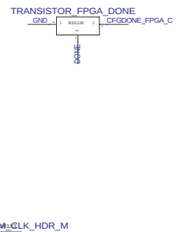
BERKELEY WIRELESS RESEARCH CENTER
2108 ALLSTON WAY
BERKELEY, CA 94704-1302
HTTP://BWRC.EECS.BERKELEY.EDU

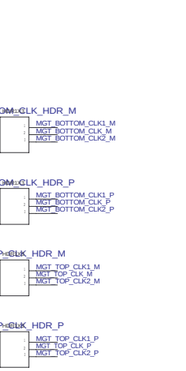
FPGA

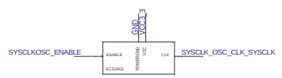
BEE2 DIC BOARD

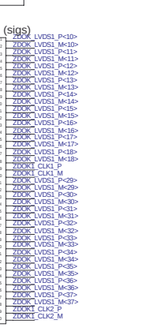
SIZE D

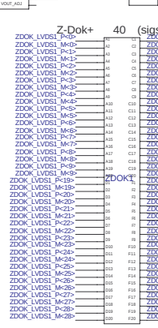
SHEET 1 OF 4

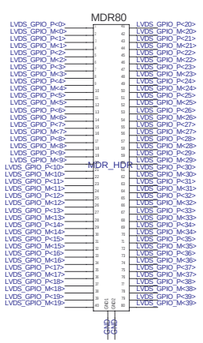


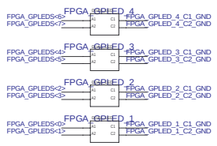


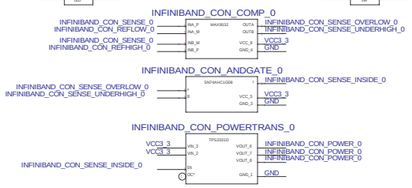


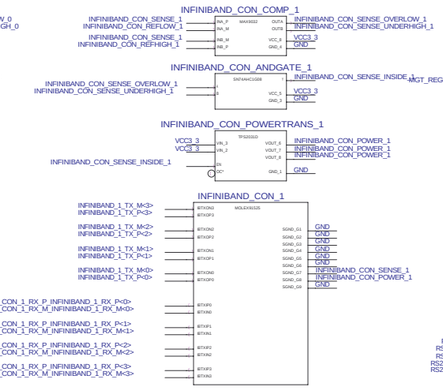


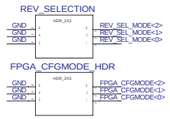


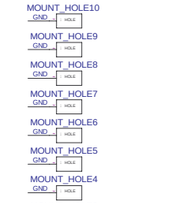


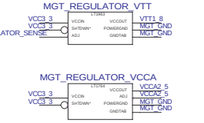


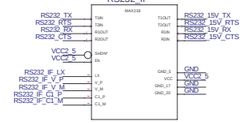


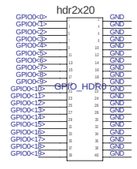


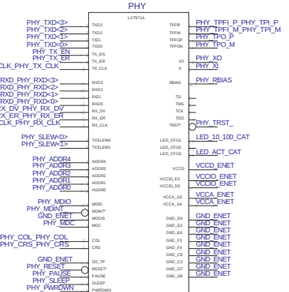


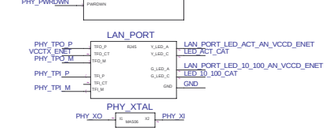












CHEN CHANG
EECS UC BERKELEY
BEE2 GROUP
BERKELEY WIRELESS RESEARCH CENTER
2108 ALLSTON WAY
BERKELEY, CA 94704-1302
HTTP://BWRC.EECS.BERKELEY.EDU

CONNECTORS

BEE2 DIC BOARD

SIZE D

SHEET 2 OF 4

INFINIBAND_CON_BYPASS_SENSE_1_0
INFINIBAND_CON_SENSE_1 GND
CAP_0402_INFINIBAND_CON_0_RX_M_INFINIBAND_0_RX_M_TS_3
INFINIBAND_CON_0_RX_M_INFINIBAND_0_RX_M<3> INFINIBAND_0_RX_M<3>
CAP_0402_INFINIBAND_CON_0_RX_M_INFINIBAND_0_RX_M_TS_2
INFINIBAND_CON_0_RX_M_INFINIBAND_0_RX_M<2> INFINIBAND_0_RX_M<2>
CAP_0402_INFINIBAND_CON_0_RX_M_INFINIBAND_0_RX_M_TS_1
INFINIBAND_CON_0_RX_M_INFINIBAND_0_RX_M<1> INFINIBAND_0_RX_M<1>
CAP_0402_INFINIBAND_CON_0_RX_M_INFINIBAND_0_RX_M_TS_0
INFINIBAND_CON_0_RX_M_INFINIBAND_0_RX_M<0> INFINIBAND_0_RX_M<0>
CAP_0402_INFINIBAND_CON_0_RX_P_INFINIBAND_0_RX_P_TS_3
INFINIBAND_CON_0_RX_P_INFINIBAND_0_RX_P<3> INFINIBAND_0_RX_P<3>
CAP_0402_INFINIBAND_CON_0_RX_P_INFINIBAND_0_RX_P_TS_2
INFINIBAND_CON_0_RX_P_INFINIBAND_0_RX_P<2> INFINIBAND_0_RX_P<2>
CAP_0402_INFINIBAND_CON_0_RX_P_INFINIBAND_0_RX_P_TS_1
INFINIBAND_CON_0_RX_P_INFINIBAND_0_RX_P<1> INFINIBAND_0_RX_P<1>
CAP_0402_INFINIBAND_CON_0_RX_P_INFINIBAND_0_RX_P_TS_0
INFINIBAND_CON_0_RX_P_INFINIBAND_0_RX_P<0> INFINIBAND_0_RX_P<0>
INFINIBAND_CON_HSPEED_BYPASS_POWER_0_0
INFINIBAND_CON_POWER_0 GND
INFINIBAND_CON_BYPASS_SENSE_0_0
INFINIBAND_CON_SENSE_0 GND
BYPASS_CAP_25_MGT_BOTTOM_OSC2_HSPEED_100NF_0
VCC2_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_21
VCC1_5 GND
BYPASS_CAP_25_MGT_BOTTOM_OSC1_HSPEED_100NF_0
VCC2_5 GND
BYPASS_CAP_25_MGT_TOP_OSC2_HSPEED_100NF_0
VCC2_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_20
VCC1_5 GND
BYPASS_CAP_25_MGT_TOP_OSC1_HSPEED_100NF_0
VCC2_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_19
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_18
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_0
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_17
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_16
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_15
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_14
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_13
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_12
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_11
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_10
VCC1_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_35
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_34
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_33
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_32
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_31
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_30
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_29
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_28
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_27
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_26
VCC2_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_9
VCC1_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_25
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_24
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_23
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_22
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_21
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_20
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_19
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_18
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_17
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_16
VCC2_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_8
VCC1_5 GND
PHY_BYPASS_VCCIO_3_2
VCCIO_ENET GND
PHY_BYPASS_VCCIO_3_1
VCCIO_ENET GND
PHY_BYPASS_VCCIO_3_0
VCCIO_ENET GND
BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_2
VCC2_5 GND
PHY_BYPASS_VCCIO_0_0
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_1
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_0
VCC2_5 GND
PHY_CAP_TERM_TPI_COMMON_0
GND_ENET PHY_TPI_COMMON
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_2
VCC1_5 GND
CAP_0402_FPGA_PUSHBUTTON3_GND_TD_0
PUSHBUTTON3 GND
CAP_0402_FPGA_PUSHBUTTON2_GND_TD_0
PUSHBUTTON2 GND
CAP_0402_FPGA_PUSHBUTTON1_GND_TD_0
PUSHBUTTON1 GND
CAP_0402_FPGA_PUSHBUTTON0_GND_TD_0
PUSHBUTTON0 GND
CAP_0402_FPGA_PROG_B_GND_TD_0
PROG GND
BYPASS_CAP_33_SYSCLK_OSC_HSPEED_100NF_0
VCC3_3 GND
CAP_0402_FPGA_SYSCLK_M_GND_TD_0
SYSCLK_DIV GND
BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_11
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_10
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_9
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_8
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_7
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_6
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_5
VCC2_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_1
VCC1_5 GND
BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_4
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_3
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_2
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_1
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_0
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_HSPEED_100NF_11
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_HSPEED_100NF_10
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_HSPEED_100NF_9
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_HSPEED_100NF_8
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_HSPEED_100NF_7
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_HSPEED_100NF_6
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_HSPEED_100NF_5
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_HSPEED_100NF_4
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_HSPEED_100NF_3
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_HSPEED_100NF_2
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_HSPEED_100NF_1
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_HSPEED_100NF_0
VCC2_5 GND
CAP_0402_INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M_TS_3
INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M<3> INFINIBAND_1_RX_M<3>
CAP_0402_INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M_TS_2
INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M<2> INFINIBAND_1_RX_M<2>
CAP_0402_INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M_TS_1
INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M<1> INFINIBAND_1_RX_M<1>
CAP_0402_INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M_TS_0
INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M<0> INFINIBAND_1_RX_M<0>
CAP_0402_INFINIBAND_CON_1_RX_P_INFINIBAND_1_RX_P_TS_3
INFINIBAND_CON_1_RX_P_INFINIBAND_1_RX_P<3> INFINIBAND_1_RX_P<3>
CAP_0402_INFINIBAND_CON_1_RX_P_INFINIBAND_1_RX_P_TS_2
INFINIBAND_CON_1_RX_P_INFINIBAND_1_RX_P<2> INFINIBAND_1_RX_P<2>
CAP_0402_INFINIBAND_CON_1_RX_P_INFINIBAND_1_RX_P_TS_1
INFINIBAND_CON_1_RX_P_INFINIBAND_1_RX_P<1> INFINIBAND_1_RX_P<1>
CAP_0402_INFINIBAND_CON_1_RX_P_INFINIBAND_1_RX_P_TS_0
INFINIBAND_CON_1_RX_P_INFINIBAND_1_RX_P<0> INFINIBAND_1_RX_P<0>
INFINIBAND_CON_HSPEED_BYPASS_POWER_1_0
INFINIBAND_CON_POWER_1 GND
BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_11
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_10
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_9
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_8
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_7
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_6
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_5
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_4
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_3
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_2
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_1
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_0
VCCO_BANK01 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_4
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_5
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_7
VCC1_5 GND
BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_4
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_3
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_2
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_1
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_0
VCC2_5 GND
PHY_BYPASS_VCCA_2_1
VCCA_ENET GND_ENET
PHY_BYPASS_VCCA_2_0
VCCA_ENET GND_ENET
PHY_BYPASS_VCCIO_4_1
VCCIO_ENET GND
PHY_BYPASS_VCCIO_4_0
VCCIO_ENET GND
CAP_0603_PHY_TPFI_M_PHY_TPI_M_TS_0
PHY_TPFI_M_PHY_TPI_M PHY_TPI_M
CAP_0603_PHY_TPFI_P_PHY_TPI_P_TS_0
PHY_TPFI_P_PHY_TPI_P PHY_TPI_P
CAP_0603_PHY_XTAL_XTAL2_GND_TD_0
PHY_XI GND
CAP_0603_PHY_XTAL_XTAL1_GND_TD_0
PHY_XO GND
RS232_IF_CAP_CHARGPUMP0_0
RS232_IF_C1_P RS232_IF_C1_M
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_10
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_9
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_8
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_7
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_6
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_5
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_4
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_3
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_2
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_1
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_0
VCC1_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_17
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_16
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_15
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_14
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_13
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_12
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_11
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_10
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_9
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_8
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_7
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_6
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_5
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_4
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_3
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_2
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_1
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_0
VCC2_5 GND
BYPASS_CAP_BK01_FPGA_VCCO_BULK_4UF7_2
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_BULK_4UF7_1
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_BULK_4UF7_0
VCCO_BANK01 GND
BYPASS_CAP_25_FPGA_VCCAUX_BULK_4UF7_1
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCAUX_BULK_4UF7_0
VCC2_5 GND
PHY_BYPASS_VCCD_3_0
VCCD_ENET GND_ENET
PHY_BYPASS_VCCD_2_0
VCCD_ENET GND_ENET
PHY_BYPASS_VCCD_1_0
VCC3_3 GND
PHY_BYPASS_VCCIO_2_0
VCCIO_ENET GND
PHY_BYPASS_VCCIO_1_0
VCCIO_ENET GND
BYPASS_CAP_25_RS232_IF_BULK_1UF_0
VCC2_5 GND
BYPASS_CAP_15_FPGA_VCCINT_BULK_4UF7_5
VCC1_5 GND
RS232_CAP_CHARGEPUMP2_0
GND RS232_IF_V_M
RS232_CAP_CHARGEPUMP1_0
RS232_IF_V_P GND
BYPASS_CAP_15_FPGA_VCCINT_BULK_4UF7_4
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_BULK_4UF7_3
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_BULK_4UF7_2
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_BULK_4UF7_1
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_BULK_4UF7_0
VCC1_5 GND
BYPASS_CAP_25_ZBT_SRAM1_BULK_10UF_1
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM1_BULK_10UF_0
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_BULK_10UF_1
VCC2_5 GND
BYPASS_CAP_25_ZBT_SRAM0_BULK_10UF_0
VCC2_5 GND
INFINIBAND_CON_BULK_BYPASS_POWER_1_0
INFINIBAND_CON_POWER_1 GND
INFINIBAND_CON_BULK_BYPASS_POWER_0_0
INFINIBAND_CON_POWER_0 GND
BYPASS_CAP_25_MGT_BOTTOM_OSC2_BULK_10UF_0
VCC2_5 GND
BYPASS_CAP_25_MGT_BOTTOM_OSC1_BULK_10UF_0
VCC2_5 GND
BYPASS_CAP_25_MGT_TOP_OSC2_BULK_10UF_0
VCC2_5 GND
BYPASS_CAP_25_MGT_TOP_OSC1_BULK_10UF_0
VCC2_5 GND
BYPASS_CAP_33_18_REGULATION_IN_0
VCC3_3 MGT_GND
BYPASS_CAP_33_25_REGULATION_IN_0
VCC3_3 MGT_GND
BYPASS_CAP_25_FPGA_VCCO_BULK_4UF7_8
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_BULK_4UF7_7
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_BULK_4UF7_6
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_BULK_4UF7_5
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_BULK_4UF7_4
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_BULK_4UF7_3
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_BULK_4UF7_2
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_BULK_4UF7_1
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_BULK_4UF7_0
VCC2_5 GND
BYPASS_CAP_ISR3_3IN_BULK_0
VCC3 GND
BYPASS_CAP_ISR3_3OUT_BULK_0
VCC3_3 GND
BYPASS_CAP_ISR2_5IN_BULK_0
VCC5 GND
BYPASS_CAP_ISR2_5OUT_BULK_0
VCC2_5 GND
BYPASS_CAP_ISR1_8IN_BULK_0
VCC5 GND
BYPASS_CAP_ISR1_8OUT_BULK_0
VCC1_8 GND
BYPASS_CAP_ISR1_5IN_BULK_0
VCC5 GND
BYPASS_CAP_ISR1_5OUT_BULK_0
VCC1_5 GND
BYPASS_CAP_18_18_REGULATION_OUT2_0
VTT1_8 MGT_GND
BYPASS_CAP_25_25_REGULATION_OUT2_0
VCC2_5 MGT_GND
BYPASS_CAP_BK01_FPGA_VCCO_BULK_47UF_1
VCCO_BANK01 GND
BYPASS_CAP_BK01_FPGA_VCCO_BULK_47UF_0
VCCO_BANK01 GND
BYPASS_CAP_25_FPGA_VCCAUX_BULK_47UF_0
VCC2_5 GND
BYPASS_CAP_15_FPGA_VCCINT_BULK_47UF_1
VCC1_5 GND
BYPASS_CAP_15_FPGA_VCCINT_BULK_47UF_0
VCC1_5 GND
BYPASS_CAP_18_18_REGULATION_OUT1_0
VTT1_8 MGT_GND
BYPASS_CAP_25_25_REGULATION_OUT1_0
VCC2_5 MGT_GND
BYPASS_CAP_25_FPGA_VCCO_BULK_47UF_3
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_BULK_47UF_2
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_BULK_47UF_1
VCC2_5 GND
BYPASS_CAP_25_FPGA_VCCO_BULK_47UF_0
VCC2_5 GND

CHEN CHANG
EECS UC BERKELEY
BEE2 GROUP
BERKELEY WIRELESS RESEARCH CENTER
2108 ALLSTON WAY
BERKELEY, CA 94704-1302
HTTP://BWRC.EECS.BERKELEY.EDU

CAPS

BEE2 DIC BOARD

SIZE D

SHEET 3 OF 4

PULLUP_JTAG_TMS_0_0
JTAG_TMS — RES — VCC2_5

PULLUP_JTAG_TCK_0_0
JTAG_TCK — RES — VCC2_5

RES_0603_FPGA_GPLED_4_C2_GND_TS_0
FPGA_GPLED_4_C2_GND — RES — GND

RES_0603_FPGA_GPLED_4_C1_GND_TS_0
FPGA_GPLED_4_C1_GND — RES — GND

RES_0603_FPGA_GPLED_3_C2_GND_TS_0
FPGA_GPLED_3_C2_GND — RES — GND

RES_0603_FPGA_GPLED_3_C1_GND_TS_0
FPGA_GPLED_3_C1_GND — RES — GND

RES_0603_FPGA_GPLED_2_C2_GND_TS_0
FPGA_GPLED_2_C2_GND — RES — GND

RES_0603_FPGA_GPLED_2_C1_GND_TS_0
FPGA_GPLED_2_C1_GND — RES — GND

RES_0603_FPGA_GPLED_1_C2_GND_TS_0
FPGA_GPLED_1_C2_GND — RES — GND

RES_0603_FPGA_GPLED_1_C1_GND_TS_0
FPGA_GPLED_1_C1_GND — RES — GND

RES_0603_SMA_CLK_REF_M_SIGNAL_GND_TD_0
USRCLK_M — RES — GND

RES_0603_SMA_CLK_REF_P_SIGNAL_GND_TD_0
USRCLK_P — RES — GND

RES_0603_SYSCLK_OSC_CLK_SYSCLK_TS_0
SYSCLK_OSC_CLK_SYSCLK — RES — SYSCLK

PULLUP_SYSCLKOSC_ENABLE_0_0
SYSCLKOSC_ENABLE — RES — VCC3_3

PULLDOWN_SYSCLK_DIV_0_0
SYSCLK_DIV — RES — GND

PULLUP_SYSCLK_DIV_0_0
SYSCLK_DIV — RES — VCC3_3

RES_0603_INFINIBAND_CON_ANDGATE_1_Y_GND_TD_0
INFINIBAND_CON_SENSE_INSIDE_1 — RES — GND

INFINIBAND_CON_REFRES_MIDDLE_SENSE_1_0
INFINIBAND_CON_REFLOW_1 — RES — INFINIBAND_CON_REFHIGH_1

INFINIBAND_CON_REFRES_LOW_SENSE_1_0
INFINIBAND_CON_REFLOW_1 — RES — GND

INFINIBAND_CON_REFRES_HIGH_SENSE_1_0
INFINIBAND_CON_REFHIGH_1 — RES — VCC3_3

INFINIBAND_CON_PULLUP_SENSE_1_0
INFINIBAND_CON_SENSE_1 — RES — VCC3_3

RES_0603_INFINIBAND_CON_ANDGATE_0_Y_GND_TD_0
INFINIBAND_CON_SENSE_INSIDE_0 — RES — GND

INFINIBAND_CON_REFRES_MIDDLE_SENSE_0_0
INFINIBAND_CON_REFLOW_0 — RES — INFINIBAND_CON_REFHIGH_0

INFINIBAND_CON_REFRES_LOW_SENSE_0_0
INFINIBAND_CON_REFLOW_0 — RES — GND

INFINIBAND_CON_REFRES_HIGH_SENSE_0_0
INFINIBAND_CON_REFHIGH_0 — RES — VCC3_3

INFINIBAND_CON_PULLUP_SENSE_0_0
INFINIBAND_CON_SENSE_0 — RES — VCC3_3

PULLUP_MGT_BOTTOM_OSC2_OE_0_0
MGT_BOTTOM_OSC2_OE — RES — VCC2_5

PULLUP_MGT_BOTTOM_OSC1_OE_0_0
MGT_BOTTOM_OSC1_OE — RES — VCC2_5

PULLUP_MGT_TOP_OSC2_OE_0_0
MGT_TOP_OSC2_OE — RES — VCC2_5

PULLUP_MGT_TOP_OSC1_OE_0_0
MGT_TOP_OSC1_OE — RES — VCC2_5

RES_0603_MGT_REGULATOR_VTT_ADJ_MGT_GND_TD_0
MGT_REGULATOR_SENSE — RES — MGT_GND

RES_0603_MGT_REGULATOR_VTT_ADJ_VTT1_8_TD_0
MGT_REGULATOR_SENSE — RES — VTT1_8

LVDS_TERM_MGT_BOTTOM_CLK_0_0
MGT_BOTTOM_CLK_P — RES — MGT_BOTTOM_CLK_M

LVDS_TERM_MGT_TOP_CLK_0_0
MGT_TOP_CLK_P — RES — MGT_TOP_CLK_M

RES_0603_FPGA_VRP_BK7_GND_TD_0
FPGA_VRP_BK7 — RES — GND

RES_0603_FPGA_VRN_BK7_VCC2_5_TD_0
FPGA_VRN_BK7 — RES — VCC2_5

RES_0603_FPGA_VRP_BK6_GND_TD_0
FPGA_VRP_BK6 — RES — GND

RES_0603_FPGA_VRN_BK6_VCC2_5_TD_0
FPGA_VRN_BK6 — RES — VCC2_5

RES_0603_FPGA_VRP_BK5_GND_TD_0
FPGA_VRP_BK5 — RES — GND

RES_0603_FPGA_VRN_BK5_VCC2_5_TD_0
FPGA_VRN_BK5 — RES — VCC2_5

RES_0603_FPGA_VRP_BK4_GND_TD_0
FPGA_VRP_BK4 — RES — GND

RES_0603_FPGA_VRN_BK4_VCC2_5_TD_0
FPGA_VRN_BK4 — RES — VCC2_5

RES_0603_FPGA_VRP_BK3_GND_TD_0
FPGA_VRP_BK3 — RES — GND

RES_0603_FPGA_VRN_BK3_VCC2_5_TD_0
FPGA_VRN_BK3 — RES — VCC2_5

RES_0603_FPGA_VRP_BK2_GND_TD_0
FPGA_VRP_BK2 — RES — GND

RES_0603_FPGA_VRN_BK2_VCC2_5_TD_0
FPGA_VRN_BK2 — RES — VCC2_5

RES_0603_FPGA_VRP_BK1_GND_TD_0
FPGA_VRP_BK1 — RES — GND

RES_0603_FPGA_VRN_BK1_VCCO_BANK01_TD_0
FPGA_VRN_BK1 — RES — VCCO_BANK01

RES_0603_FPGA_VRP_BK0_GND_TD_0
FPGA_VRP_BK0 — RES — GND

RES_0603_FPGA_VRN_BK0_VCCO_BANK01_TD_0
FPGA_VRN_BK0 — RES — VCCO_BANK01

RES_0603_PHY_PWRDWN_GND_ENET_TD_0
PHY_PWRDWN — RES — GND_ENET

RES_0603_PHY_PAUSE_GND_ENET_TD_0
PHY_PAUSE — RES — GND_ENET

RES_0603_PHY_SLEEP_GND_ENET_TD_0
PHY_SLEEP — RES — GND_ENET

PULLUP_PHY_TRST__0_0
PHY_TRST — RES — VCC2_5

RES_0603_PHY_CRS_PHY_CRS_TS_0
PHY_CRS_PHY_CRS — RES — PHY_CRS

RES_0603_PHY_COL_PHY_COL_TS_0
PHY_COL_PHY_COL — RES — PHY_COL

RES_0603_PHY_RX_ER_PHY_RX_ER_TS_0
PHY_RX_ER_PHY_RX_ER — RES — PHY_RX_ER

RES_0603_PHY_TX_CLK_PHY_TX_CLK_TS_0
PHY_TX_CLK_PHY_TX_CLK — RES — PHY_TX_CLK

RES_0603_PHY_RX_CLK_PHY_RX_CLK_TS_0
PHY_RX_CLK_PHY_RX_CLK — RES — PHY_RX_CLK

RES_0603_PHY_RX_DV_PHY_RX_DV_TS_0
PHY_RX_DV_PHY_RX_DV — RES — PHY_RX_DV

RES_0603_PHY_RXD_PHY_RXD_TS_3
PHY_RXD_PHY_RXD<3> — RES — PHY_RXD<3>

RES_0603_PHY_RXD_PHY_RXD_TS_2
PHY_RXD_PHY_RXD<2> — RES — PHY_RXD<2>

RES_0603_PHY_RXD_PHY_RXD_TS_1
PHY_RXD_PHY_RXD<1> — RES — PHY_RXD<1>

RES_0603_PHY_RXD_PHY_RXD_TS_0
PHY_RXD_PHY_RXD<0> — RES — PHY_RXD<0>

PHY_RES_TERM_TPI_M_0
PHY_TPI_M — RES — PHY_TPI_COMMON

PHY_RES_TERM_TPI_P_0
PHY_TPI_P — RES — PHY_TPI_COMMON

PHY_RES_RBIAS_0
PHY_RBIAS — RES — GND_ENET

PULLDOWN_PHY_ADDR4_0_0
PHY_ADDR4 — RES — GND

PULLDOWN_PHY_ADDR3_0_0
PHY_ADDR3 — RES — GND

PULLDOWN_PHY_ADDR2_0_0
PHY_ADDR2 — RES — GND

PULLDOWN_PHY_ADDR1_0_0
PHY_ADDR1 — RES — GND

PULLDOWN_PHY_ADDR0_0_0
PHY_ADDR0 — RES — GND

PULLUP_PHY_RESET__0_0
PHY_RESET — RES — VCC2_5

RES_0603_LAN_PORT_LED_10_100_AN_VCCD_ENET_TS_0
LAN_PORT_LED_10_100_AN_VCCD_ENET — RES — VCCD_ENET

RES_0603_LAN_PORT_LED_ACT_AN_VCCD_ENET_TS_0
LAN_PORT_LED_ACT_AN_VCCD_ENET — RES — VCCD_ENET

ISR1_5_SET_RES_0
ISR1_5_ADJUST — RES — GND

RES_0603_VCC5_LED_A_VCC5_TS_0
VCC5_LED_A_VCC5 — RES — VCC5

PULLUP_PUSHBUTTON3_0_0
PUSHBUTTON3 — RES — VCC2_5

PULLUP_PUSHBUTTON2_0_0
PUSHBUTTON2 — RES — VCC2_5

PULLUP_PUSHBUTTON1_0_0
PUSHBUTTON1 — RES — VCC2_5

PULLUP_PUSHBUTTON0_0_0
PUSHBUTTON0 — RES — VCC2_5

PULLUP_DIPSW_SIGS_0_7
DIPSW_SIGS<7> — RES — VCC2_5

PULLUP_DIPSW_SIGS_0_6
DIPSW_SIGS<6> — RES — VCC2_5

PULLUP_DIPSW_SIGS_0_5
DIPSW_SIGS<5> — RES — VCC2_5

PULLUP_DIPSW_SIGS_0_4
DIPSW_SIGS<4> — RES — VCC2_5

PULLUP_DIPSW_SIGS_0_3
DIPSW_SIGS<3> — RES — VCC2_5

PULLUP_DIPSW_SIGS_0_2
DIPSW_SIGS<2> — RES — VCC2_5

PULLUP_DIPSW_SIGS_0_1
DIPSW_SIGS<1> — RES — VCC2_5

PULLUP_DIPSW_SIGS_0_0
DIPSW_SIGS<0> — RES — VCC2_5

PULLUP_FPGA_CFGMODE_0_2
FPGA_CFGMODE<2> — RES — VCC2_5

PULLUP_FPGA_CFGMODE_0_1
FPGA_CFGMODE<1> — RES — VCC2_5

PULLUP_FPGA_CFGMODE_0_0
FPGA_CFGMODE<0> — RES — VCC2_5

RES_0603_DONE_LED_A_VCC2_5_TS_0
DONE_LED_A_VCC2_5 — RES — VCC2_5

PULLUP_JTAG_TDO_0_0
JTAG_TDO — RES — VCC2_5

PULLDOWN_CS_0_0
CS — RES — GND

PULLDOWN_RDWR_0_0
RDWR — RES — GND

PULLUP_DONE_0_0
DONE — RES — VCC2_5

PULLUP_INIT_0_0
INIT — RES — VCC2_5

PULLUP_PROG_0_0
PROG — RES — VCC2_5

PULLUP_PROM_TDO_0_0
PROM_TDO — RES — VCC2_5

PHY_IND_FILTER_GND_0
GND_ENET — IND — GND

PHY_IND_FILTER_VCCTX_0
VCCA_ENET — IND — VCCTX_ENET

PHY_IND_FILTER_VCCA_0
VCCA_ENET — IND — VCCD_ENET

PHY_IND_FILTER_VCCD_0
VCCD_ENET — IND — VCC3_3

PHY_IND_FILTER_VCCIO_0
VCCIO_ENET — IND — VCC2_5

IND_1812_RS232_IF_LX_VCC2_5_TD_0
RS232_IF_LX — IND — VCC2_5

FILTER_IND_MGT_GND_0
GND — IND — MGT_GND

FILTER_IND_MGT_VTRX_7
VTRX<7> — IND — VTT1_8

FILTER_IND_MGT_VTRX_6
VTRX<6> — IND — VTT1_8

FILTER_IND_MGT_VTRX_5
VTRX<5> — IND — VTT1_8

FILTER_IND_MGT_VTRX_4
VTRX<4> — IND — VTT1_8

FILTER_IND_MGT_VTRX_3
VTRX<3> — IND — VTT1_8

FILTER_IND_MGT_VTRX_2
VTRX<2> — IND — VTT1_8

FILTER_IND_MGT_VTRX_1
VTRX<1> — IND — VTT1_8

FILTER_IND_MGT_VTRX_0
VTRX<0> — IND — VTT1_8

FILTER_IND_MGT_VTTX_7
VTTX<7> — IND — VTT1_8

FILTER_IND_MGT_VTTX_6
VTTX<6> — IND — VTT1_8

FILTER_IND_MGT_VTTX_5
VTTX<5> — IND — VTT1_8

FILTER_IND_MGT_VTTX_4
VTTX<4> — IND — VTT1_8

FILTER_IND_MGT_VTTX_3
VTTX<3> — IND — VTT1_8

FILTER_IND_MGT_VTTX_2
VTTX<2> — IND — VTT1_8

FILTER_IND_MGT_VTTX_1
VTTX<1> — IND — VTT1_8

FILTER_IND_MGT_VTTX_0
VTTX<0> — IND — VTT1_8

FILTER_IND_MGT_AVCCAUXRX_7
AVCCAUXRX<7> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXRX_6
AVCCAUXRX<6> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXRX_5
AVCCAUXRX<5> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXRX_4
AVCCAUXRX<4> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXRX_3
AVCCAUXRX<3> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXRX_2
AVCCAUXRX<2> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXRX_1
AVCCAUXRX<1> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXRX_0
AVCCAUXRX<0> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXTX_7
AVCCAUXTX<7> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXTX_6
AVCCAUXTX<6> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXTX_5
AVCCAUXTX<5> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXTX_4
AVCCAUXTX<4> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXTX_3
AVCCAUXTX<3> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXTX_2
AVCCAUXTX<2> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXTX_1
AVCCAUXTX<1> — IND — VCCA2_5

FILTER_IND_MGT_AVCCAUXTX_0
AVCCAUXTX<0> — IND — VCCA2_5

CHEN CHANG
EECS UC BERKELEY
BEE2 GROUP

BERKELEY WIRELESS RESEARCH CENTER
2108 ALLSTON WAY
BERKELEY, CA 94704-1302

HTTP://BWRC.EECS.BERKELEY.EDU

MISC

BEE2 DIC BOARD

SIZE D

SHEET 4 OF 4