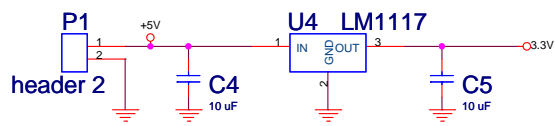
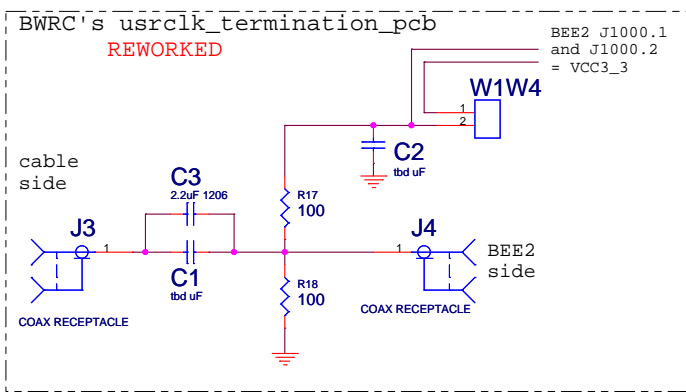
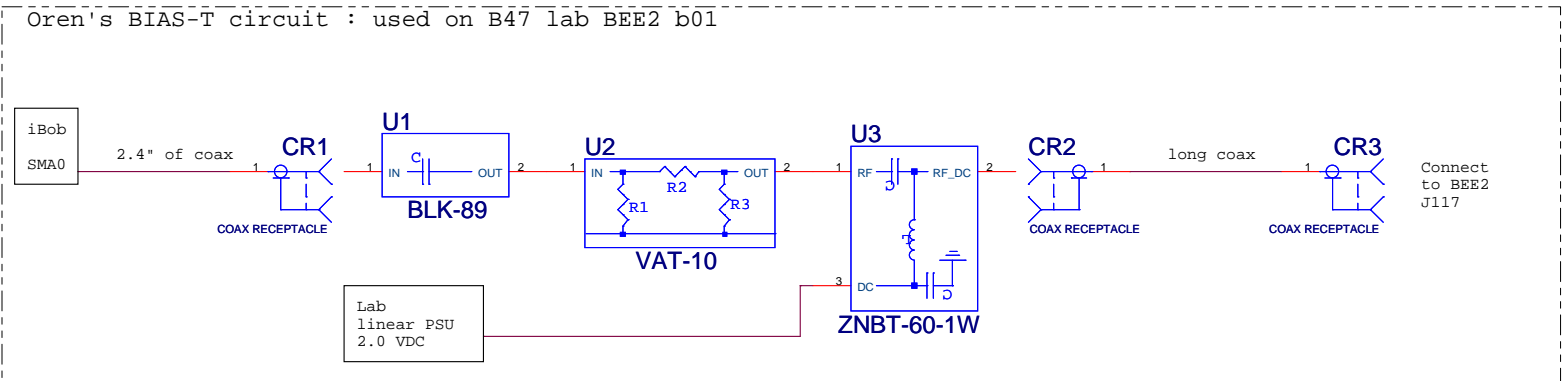
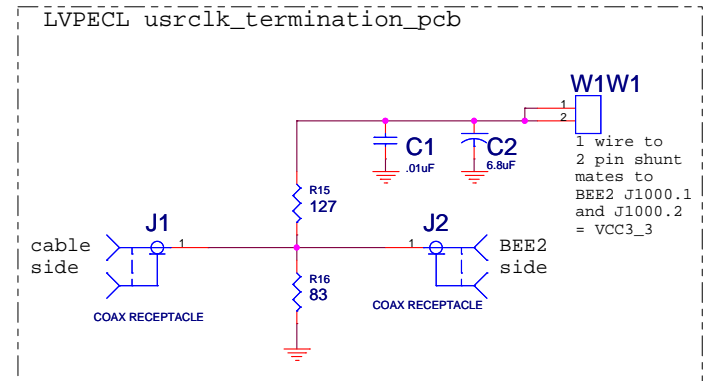
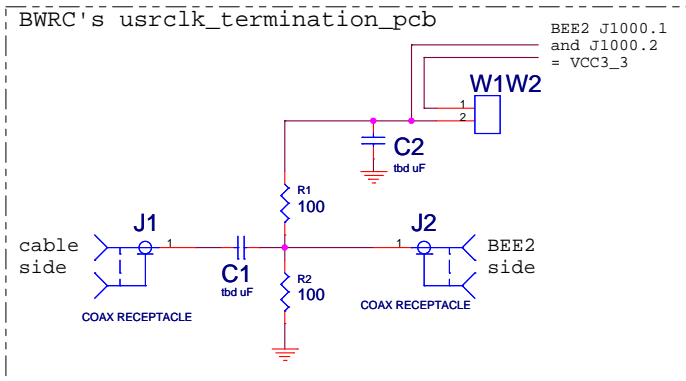
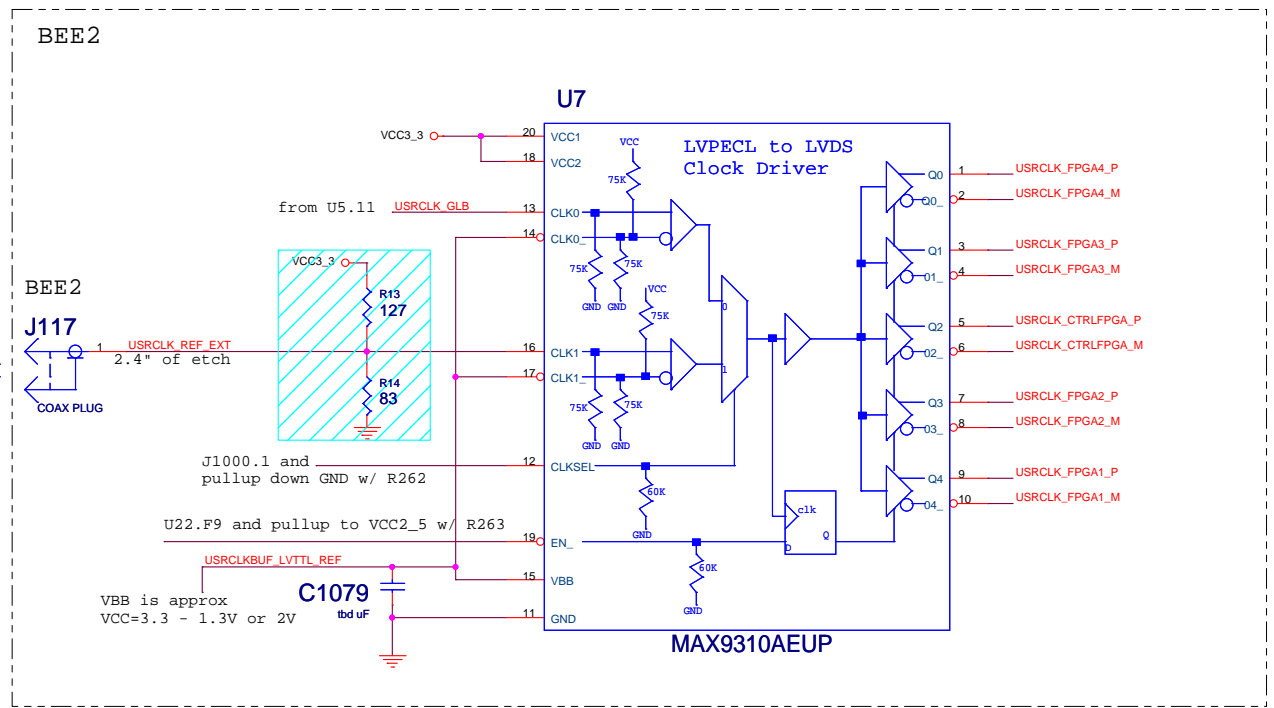


LVTTTL inputs
(eg from iBob)



- BEE2 usrclok options
- A) CW synthesizer
use the usrclok_termination_pcb.
power it from BEE2 Jxxx
 - B) LVPECL source
B.1) remove the 120 ohm pulldowns on the clock driver
and add at BEE2 end the 127 pull up to VCC3_3 at
U7.18 and 83 ohm pulldown to GND at R262.2
This removes 2.4" stub but means modifying the BEE2
Not yet tested.
B2.) make a new termination board with the 127/83
terminating resistor pair (not AC coupled)
This leaves the 2.4" stub but the BEE2 is not modified.
 - C) Oren's DC Block, Attenuator, and BIAS T scheme



Based on my version of the
Corr Clk Buffer schematics for readability:
Calvin has the actual design files.

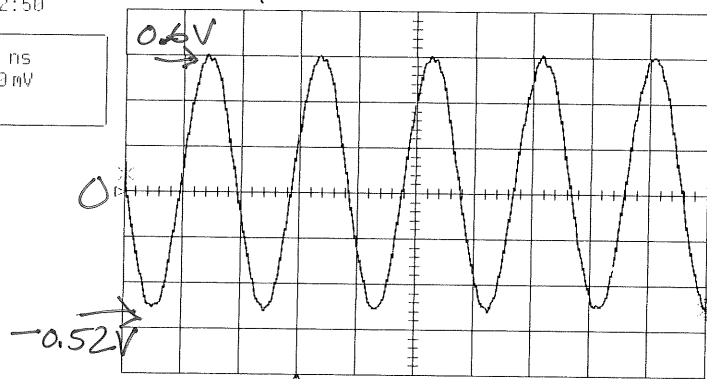
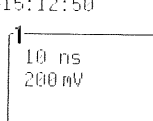
c:\ata\correlator\production\clock_translator\			
Title Clock Distributor for BEE2			
Size Custom	Document Number Clock_buff_to_bee2.opj: clock_buff_to_bee2.dsn	Rev 1.0	
Date: Thursday, September 20, 2007	Sheet 1	of 1	

IC

20-Sep-07
15:12:50

Theory is
0.63V up to
into 50 Ω load.
the BEE2 input
U7.16 isn't
50 Ω load

07.16



	average	low	high	sigma
pkpk(1)	1.125 V	1.100	1.144	0.009
mean(1)	40.4 mV	27.9	53.4	7.2
sdev(1)	391.7 mV	389.8	393.6	0.7
rmsf(1)	393.4 mV	391.2	396.0	1.0
ampl(1)	1.081 V	1.038	1.115	0.013

10 ns

1 20 mV DC $\times 10$

2 20 mV DC

1 DC -0.008 V

☐ NORMAL

5 GS/s

MEASURE

Parameters

made

Std Voltage

Std Time

Custom

Pass

Fail

- statis

OFF

CH

on die

-011 0151
(+200)

Trace

U

from

0.00 0

Track **OF**

_____ to _____

10.00

500 P

Downloaded from ascelibrary.org by University of California, San Diego on 06/01/15. Copyright ASCE. For personal use only; all rights reserved.

NORMAI

$\Gamma = O(1/\epsilon)$

5 GS/S

MAX9310A = U7 min input voltage is -0.1V

This probably turns on diode in protection circuit and if drive too hard one can blow out that diode.

~~Here is the output -~~

V7 outputs don't toggle until
~ + 7 dBm input

+7dBm
 1.416V_{ptp}
 into 50Ω
 load.

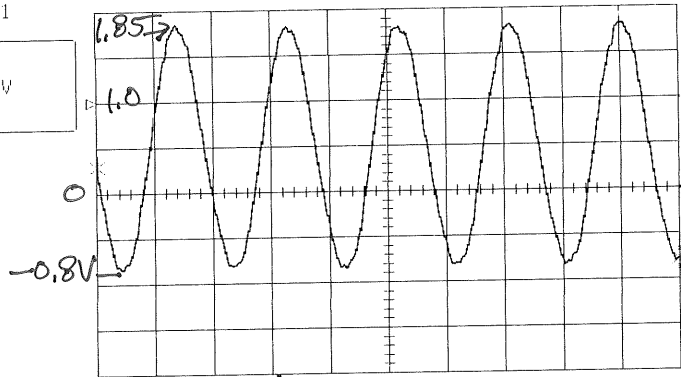
NOTE shift from
 0VDC
 probably due to
 receiver U7 input
 circuit

cwgen → ~~0.1~~ over 18" coax
 J117

2C

20-Sep-07
 15:42:41

1
 10 ns
 0.50 V



	142 sweeps:	average	low	high	sigma
pkpk(1)		2.688 V	2.641	2.734	0.021
mean(1)		492.5 mV	471.7	519.2	11.3
sdev(1)		937.7 mV	933.6	945.1	1.9
rmst(1)		1.0581 V	1.0479	1.0728	0.0054
ampl(1)		2.58 V	2.49	2.69	0.04

10 ns
 1 50 mV DC

2 20 mV DC

1 DC 1.00 V

MEASURE

OFF Cursors
 Parameters

mode

Std Voltage

Std Time

Custom

Pass

Fail

statistics

OFF On

on displayed
 (trace)

1

from

0.00 div

Track OFF On

to

10.00 div

500 points

STOPPED

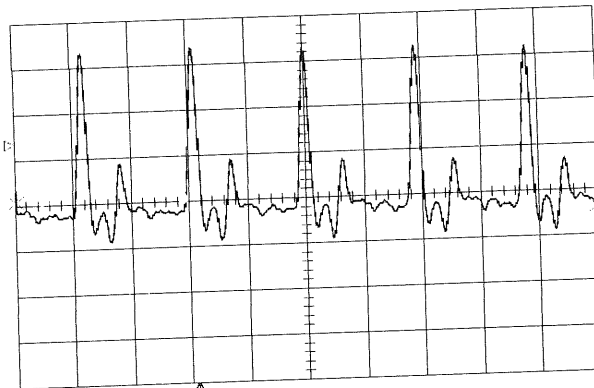
5 Gs/s

cwgen @ +7dBm → 18" coax → ~~0.1~~
 J117

3C

20-Sep-07
 15:41:18

1
 10 ns
 100 mV



	119 sweeps:	average	low	high	sigma
period(1)		19.07 ns	19.03	19.09	0.01
width(1)		1.60 ns	1.45	1.79	0.08
rise(1)		1.10 ns	1.02	1.18	0.04
fall(1)		0.93 ns	0.85	1.03	0.04
delay(1)		-19.96 ns	-20.10	-19.85	0.05

10 ns
 1 10 mV DC

2 20 mV DC

1 DC 1.268 V

MEASURE

OFF Cursors
 Parameters

mode

Std Voltage

Std Time

Custom

Pass

Fail

statistics

OFF On

on displayed
 (trace)

1

from

0.00 div

Track OFF On

to

10.00 div

500 points

AUTO

5 Gs/s

U7.1
 output

lousy duty
 cycle

CW gen @ +10dBm \rightarrow 18' coax \rightarrow J117
 +10dBm is 2V ptp into 50 Ω load.

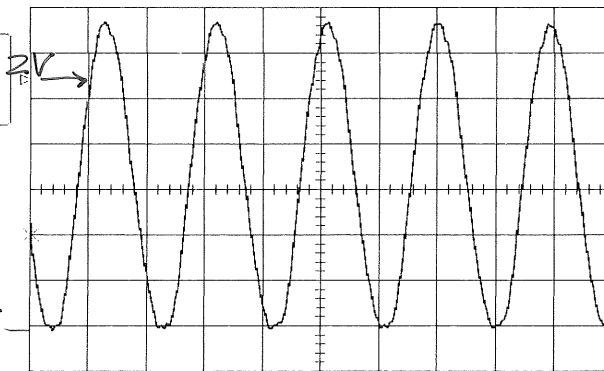
4C

U7.16
input

Note large shift
from DC.

20-Sep-07
15:50:40

1 10 ns
0.50 V



112 sweeps:	average	low	high	sigma
pkpk(1)	3.391 V	3.344	3.438	0.022
mean(1)	898.7 mV	884.7	915.7	6.6
sdev(1)	1.2030 V	1.1978	1.2082	0.0018
rms(1)	1.5004 V	1.4919	1.5103	0.0039
ampl(1)	3.28 V	3.21	3.38	0.04

10 ns
1 50 mV DC ∞

2 20 mV DC

1 DC 2.00 V

MEASURE

OFF Cursors
Parameters

mode
Std Voltage
Std Time
Custom
Pass
Fail

statistics
OFF On

on displayed
(trace)
1

from
0.00 div
Track OFF On

to
10.00 div
500 points

☐ NORMAL
5 6s/s

CW gen @ +10dBm \rightarrow 18' coax \rightarrow J117

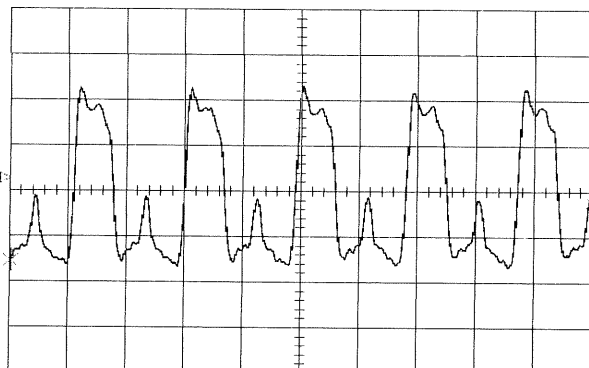
5C

U7.1
output

duty cycle not so good
but much better
than @ +7dBm input

20-Sep-07
15:51:54

1 10 ns
100 mV



106 sweeps:	average	low	high	sigma
pkpk(1)	407 mV	394	419	6
mean(1)	1.23576 V	1.22614	1.24733	0.00507
sdev(1)	140.09 mV	137.93	142.26	0.97
rms(1)	1.24366 V	1.23391	1.25523	0.00507
ampl(1)	311 mV	300	321	5

10 ns
1 10 mV DC ∞

2 20 mV DC

1 DC 1.276 V

MEASURE

OFF Cursors
Parameters

mode
Std Voltage
Std Time
Custom
Pass
Fail

statistics
OFF On

on displayed
(trace)
1

from
0.00 div
Track OFF On

to
10.00 div
500 points

☐ AUTO
5 6s/s

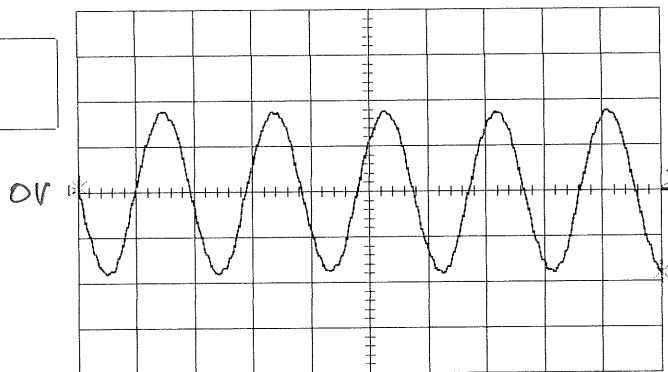
cw gen -10dBm @ 52.4288MHz

1B

18" coax
to BWRC
clk term
cw gen side

20-Sep-07
11:16:47

1 10 ns
100 mV



117 sweeps:	average	low	high	sigma
pkpk(1)	363 mV	353	372	3
mean(1)	-1.94 mV	-6.86	2.28	1.85
sdev(1)	124.80 mV	123.91	125.57	0.31
rms(1)	124.67 mV	123.77	125.46	0.31
ampl(1)	342 mV	331	361	6

10 ns

1 10 mV DC

2 20 mV DC

1 DC 8 mV

MEASURE

OFF Cursors
Parameters

mode

Std Voltage

Std Time

Custom

Pass

Fail

statistics

OFF On

on displayed
(trace)

1

from

0.00 div

Track OFF On

to

10.00 div

500 points

AUTO

5 GS/s

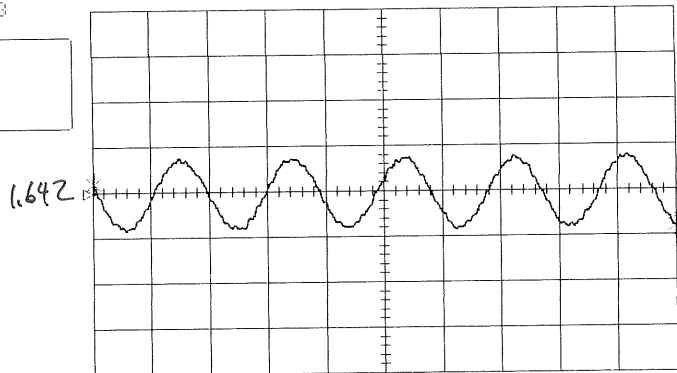
cw gen @ 52.4288MHz (not locked to 10MHz)
-10dBm = 200mV ptp

2B

18" coax
to BWRC
clk term
J117 side

20-Sep-07
11:14:03

1 10 ns
100 mV



110 sweeps:	average	low	high	sigma
pkpk(1)	171 mV	159	181	6
mean(1)	1.63986 V	1.63124	1.64791	0.00347
sdev(1)	56.35 mV	53.32	58.66	1.99
rms(1)	1.64083 V	1.63228	1.64894	0.00347
ampl(1)	155 mV	139	178	9

10 ns

1 10 mV DC

2 20 mV DC

1 DC 1.642 V

MEASURE

OFF Cursors
Parameters

mode

Std Voltage

Std Time

Custom

Pass

Fail

statistics

OFF On

on displayed
(trace)

1

from

0.00 div

Track OFF On

to

10.00 div

500 points

AUTO

5 GS/s

CW gen → 18" coax BWRC CLK term

3B

u7.16

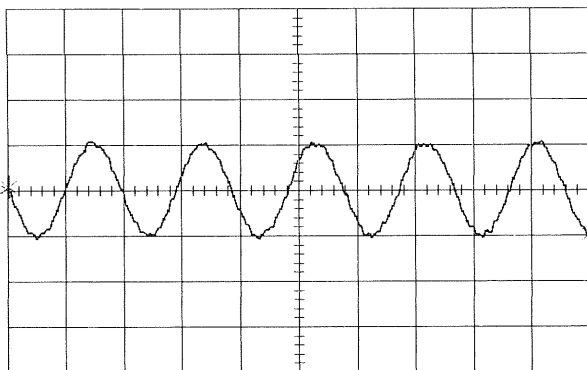
20-Sep-07
11:25:20

-10dBm @ 52.4288 MHz

MEASURE

10 ns
100 mV

1.652



OFF Cursors
Parameters

mode
Std Voltage
Std Time
Custom
Pass
Fail

statistics
OFF On

on displayed
(trace)

from
0.00 div
Track Off On

to
10.00 div
500 points

This is about smallest
swing that could work
but DC offset isn't
right.

u7 outputs NOT
toggling
pin 2 high
pin 1 low

10 ns
1 10 mV DC

2 20 mV DC

	99 sweeps:	average	low	high	sigma
pkpk(1)		213 mV	187	222	5
mean(1)		1.64065 V	1.63017	1.65417	0.00627
sdev(1)		71.01 mV	61.25	72.51	1.41
rms(1)		1.64218 V	1.63173	1.65569	0.00627
ampl(1)		194 mV	165	216	8

1 DC 1.652 V

☐ AUTO
5 Gs/s

look at outputs while ever increasing
the input power

- ⑤ +9 dBm outputs would occasionally toggle
- ⑥ +10 dBm $V_{p\text{top}}(\text{theory}) = 2V_{p\text{top}}$
outputs toggle repeatedly (regularly) but
waveform is NOT good duty cycle
due to wrong DC shift

CW gen +10dBm \rightarrow 18" coax BWRC clk term 4B

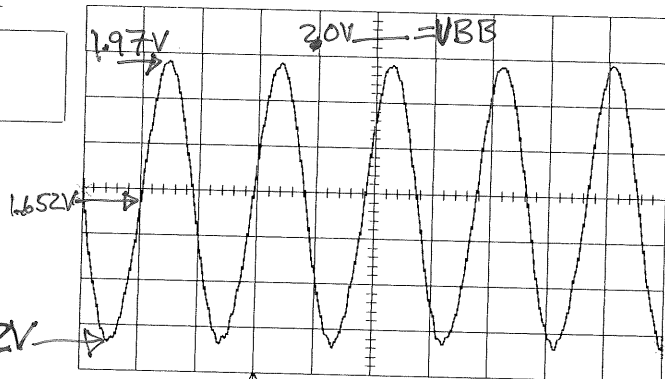
U7.16

20-Sep-07
11:40:32

this is lowest
level input
which causes output
to toggle.

this is same (about)
as J117 input.
Input to BWRC
clk term is much
larger ~3.5V ptp
difference
due to poor
AC-coupling

1
10 ns
100 mV



pkpk(1)	1.970V	1.628mV	616	641	5
mean(1)	1.63902 V	1.62092	1.65458	0.00755	
sdev(1)	216.00mV	215.03	216.98	0.46	
rms(1)	1.65316 V	1.63527	1.66862	0.00747	
ampl(1)	603mV	570	626	8	

10 ns
1 10 mV DC \times

2 20 mV DC

1 DC 1.652 V

MEASURE

OFF Cursors
Parameters

mode
Std Voltage
Std Time
Custom
Pass
Fail

statistics
OFF On

on displayed
(trace)

from
0.00 div
Track OFF On

to
10.00 div
500 points

STOPPED
5 Gs/s

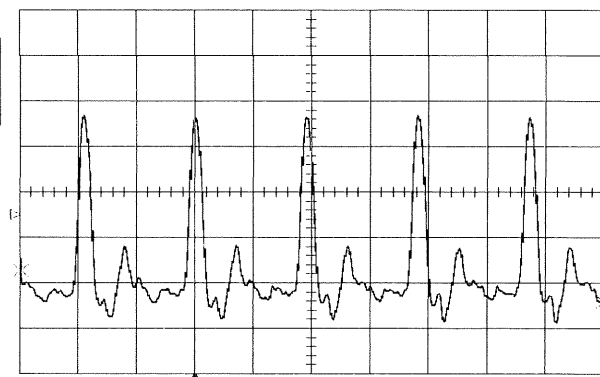
5B

U7.1

20-Sep-07
11:35:48

very uneven duty cycle!!

1
10 ns
100 mV



period(1)	19.07 ns	19.02	19.10	0.01
width(1)	2.27 ns	1.87	2.69	0.19
rise(1)	1.19 ns	1.10	1.34	0.05
fall(1)	1.28 ns	1.05	1.58	0.11
delay(1)	-19.93 ns	-20.07	-19.77	0.05

10 ns
1 10 mV DC \times

2 20 mV DC

1 DC 1.272 V

MEASURE

OFF Cursors
Parameters

mode
Std Voltage
Std Time
Custom
Pass
Fail

statistics
OFF On

on displayed
(trace)

from
0.00 div
Track OFF On

to
10.00 div
500 points

AUTO
5 Gs/s

2007 SEP 20

68

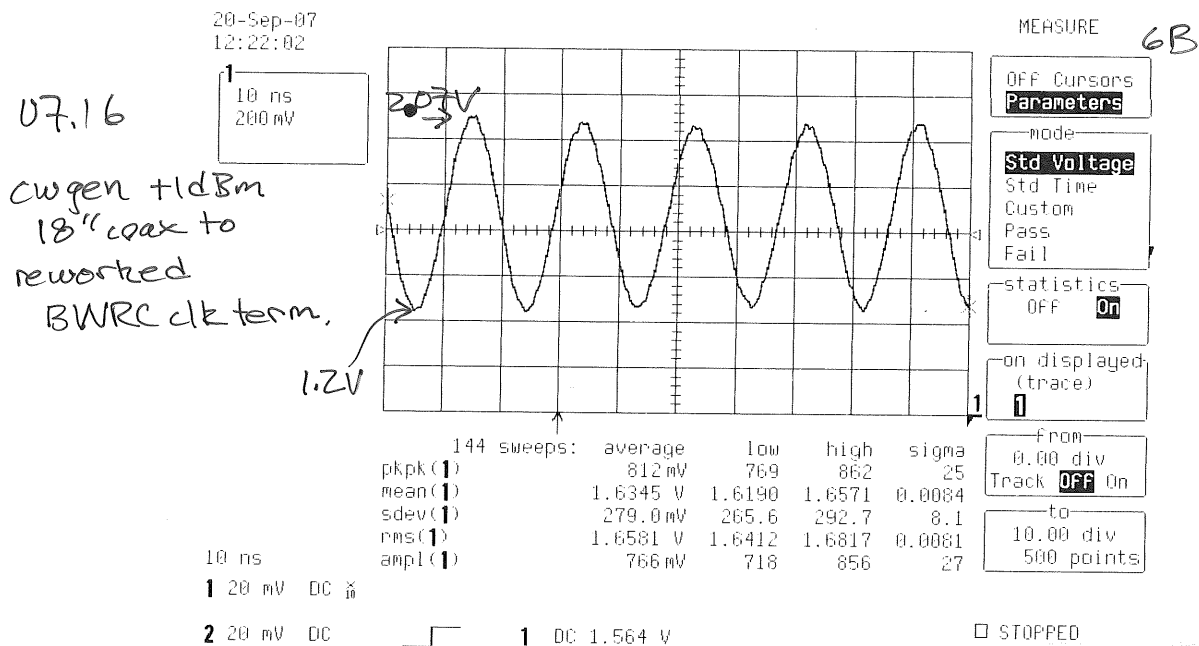
Rework BWRC clk term board:

Add $2.2\mu\text{F}$ 1206 decoupling cap in parallel. 16V rated part to whatever was there already.

$XX\mu\text{F}$ 0805 I think. I don't know $XX\mu\text{F}$.

Now much more signal gets thru to J117.

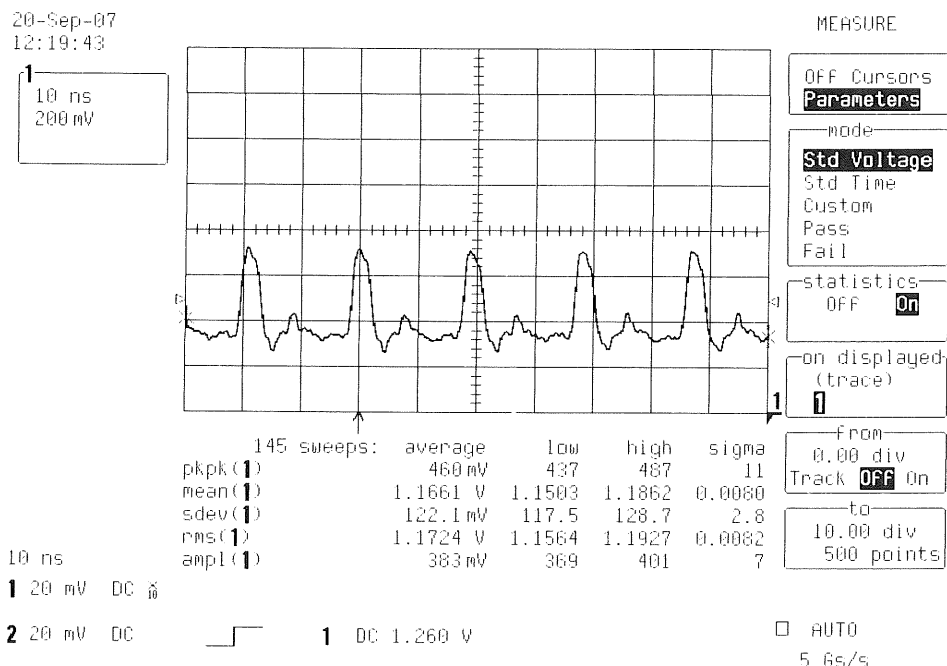
Now see what lowest level input is required to get valid output if not valid then at least toggling. 0dBm input was a little flakey. so go with $+1\text{dBm}$.



cw gen $+1\text{dBm} = .7(V_{\text{top}}(\text{Theory}))$

7B

07.1



2007SEP20

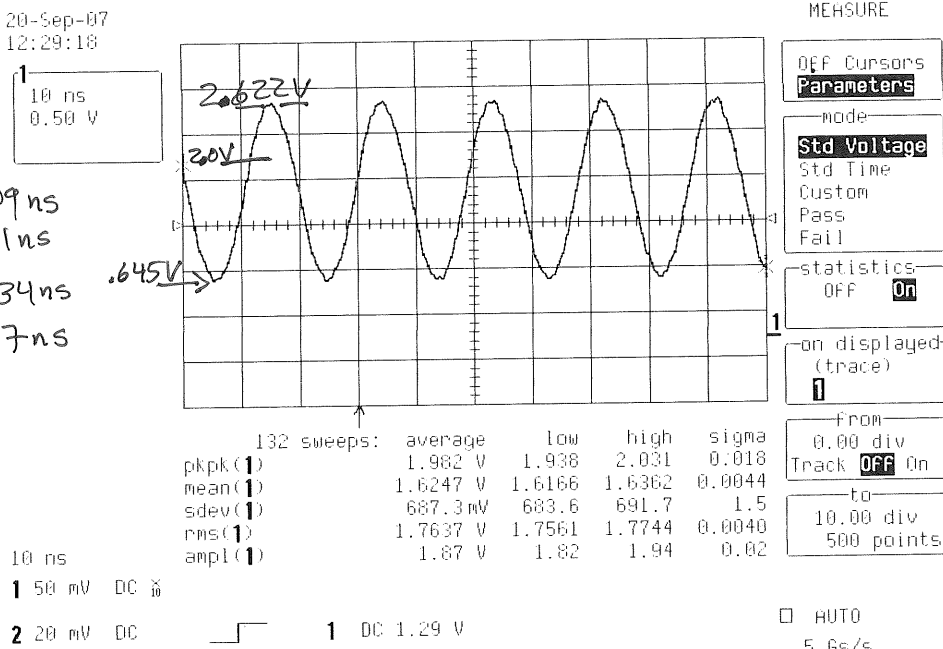
Now look to see what input level gets a better duty cycle...
(at U7, ~~xxx~~ outputs)

cu gen +10dBm 18' coax reworked
BWRC clk term

8B

20-Sep-07
12:29:18
U7.16

period = 19.09 ns
high = 9.31 ns
rise = 5.34 ns
fall = 5.57 ns

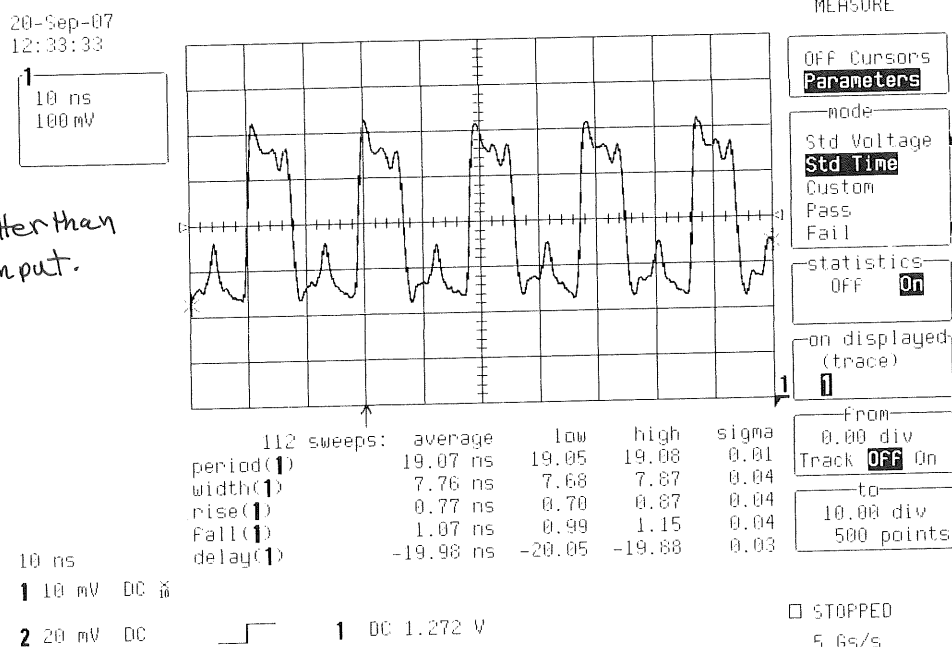


cu gen +10dBm 18' coax reworked
BWRC clk term

9B

U7.1

NOT 50%
duty cycle
but much better than
w/ +10dBm input.



Correlk translator
right into scope 4ft coax.

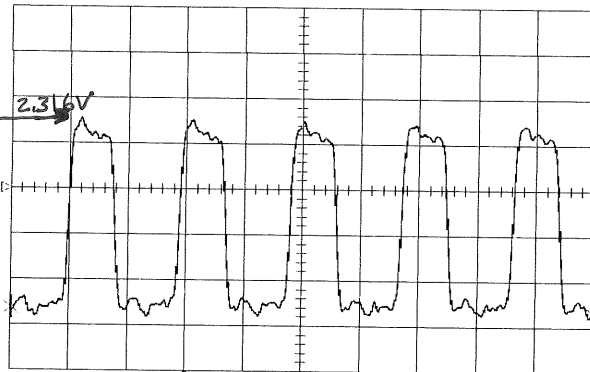
ka

Nice sharp
edges.

This output doesn't have
120 Ω pull down to gnd
but its complimentary
inverted output does

19-Sep-07
16:02:17

1
10 ns
200 mV



1.447V

280 sweeps:	average	low	high	sigma
period(1)	19.07 ns	19.04	19.09	0.01
width(1)	7.93 ns	7.85	8.04	0.04
rise(1)	1.23 ns	1.11	1.34	0.06
Fall(1)	1.22 ns	1.12	1.36	0.06
delay(1)	-20.16 ns	-20.27	-20.07	0.04

10 ns

1.2 V 50 Ω 50 Ω

2 20 mV DC

1 DC 2.000 V

MEASURE

OFF Cursors
Parameters

mode
Std Voltage
Std Time
Custom
Pass
Fail

statistics
OFF On

on displayed
(trace)

from
0.00 div
Track OFF On

to
10.00 div
500 points

☐ AUTO

5 Gs/s

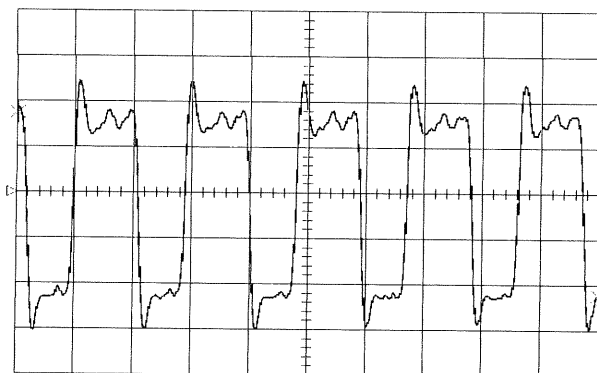
Correlk
translator
unused
output.
(No path to
BEEZ)

New 1M//11pF scope probe "500MHz"
and better GND

2a

19-Sep-07
16:13:06

1
10 ns
200 mV



233 sweeps:	average	low	high	sigma
period(1)	19.07 ns	19.05	19.09	0.01
width(1)	7.89 ns	7.80	7.98	0.04
rise(1)	0.93 ns	0.85	1.02	0.05
Fall(1)	0.91 ns	0.85	0.99	0.04
delay(1)	-28.03 ns	-28.12	-27.92	0.04

10 ns

1 20 mV DC

2 20 mV DC

1 DC 2.000 V

MEASURE

OFF Cursors
Parameters

mode
Std Voltage
Std Time
Custom
Pass
Fail

statistics
OFF On

on displayed
(trace)

from
0.00 div
Track OFF On

to
10.00 div
500 points

☐ NORMAL

5 Gs/s

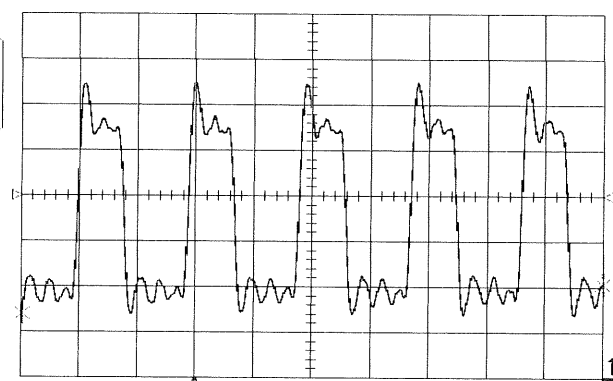
correct
translator
output
used to
drive BEEZ

better probe

3a

19-Sep-07
16:16:16

1
10 ns
200 mV



	146 sweeps:	average	low	high	sigma
period(1)		19.07 ns	19.05	19.10	0.01
width(1)		7.96 ns	7.89	8.06	0.04
rise(1)		0.90 ns	0.81	0.98	0.04
Fall(1)		1.03 ns	0.96	1.13	0.04
delay(1)		-20.14 ns	-20.24	-20.07	0.04

10 ns
1 20 mV DC
2 20 mV DC

1 DC 2.000 V

MEASURE

OFF Cursors
Parameters

mode
Std Voltage
Std Time
Custom
Pass
Fail

statistics
OFF On

on displayed
(trace)
1

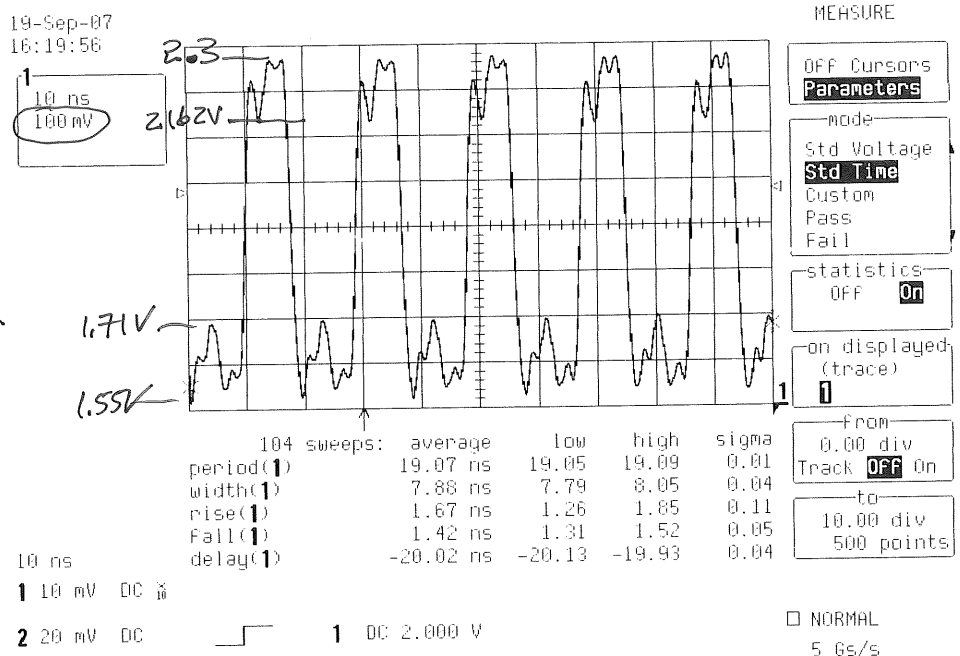
from
0.00 div
Track OFF On

to
10.00 div
500 points

☐ NORMAL
5 Gs/s

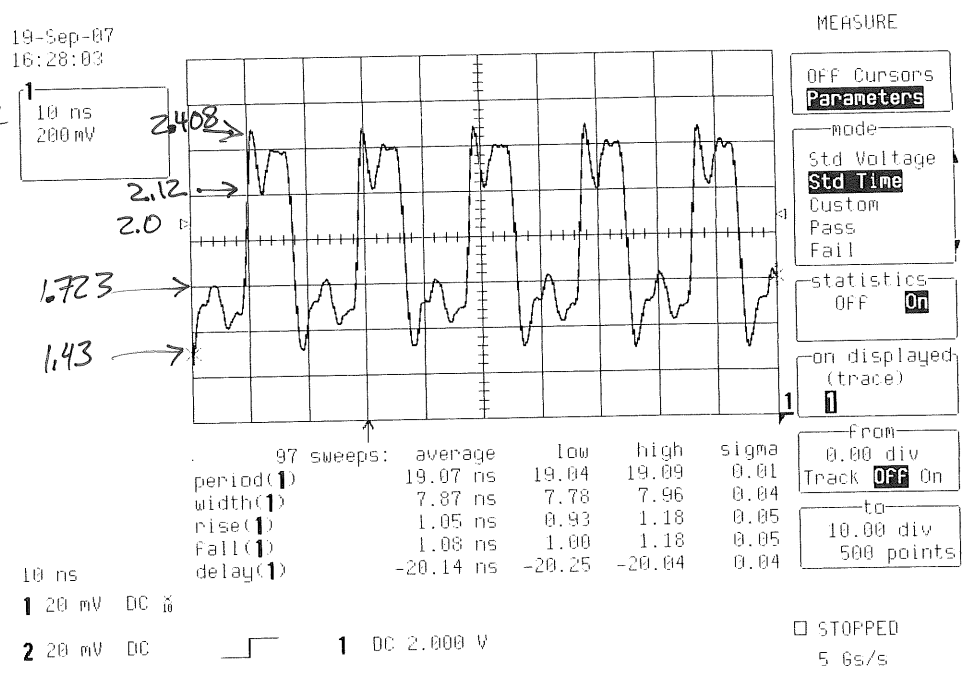
4a

BEEZ
input
J117
better probe
with
WRPECL
termination
kludge



5a

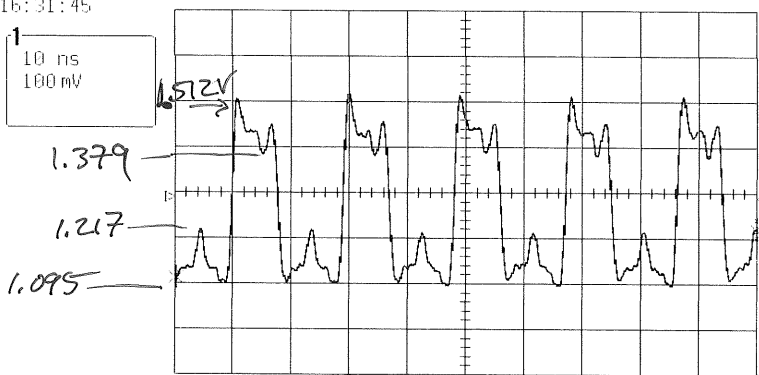
U7.16
Betterprobe
input
to clock
driver



U7.1
better probe
LVDS

19-Sep-07
16:31:45

1
10 ns
100 mV



117 sweeps:	average	low	high	sigma
period(1)	19.07 ns	19.03	19.09	0.01
width(1)	7.99 ns	7.91	8.10	0.05
rise(1)	0.78 ns	0.71	0.87	0.04
fall(1)	1.01 ns	0.92	1.10	0.04
delay(1)	-20.01 ns	-20.11	-19.89	0.04

10 ns
1 10 mV DC

2 20 mV DC

1 DC 1.280 V

MEASURE

OFF Cursors
Parameters

mode
Std Voltage
Std Time
Custom
Pass
Fail

statistics
OFF On

on displayed
(trace)
1

from
0.00 div
Track OFF On

to
10.00 div
500 points

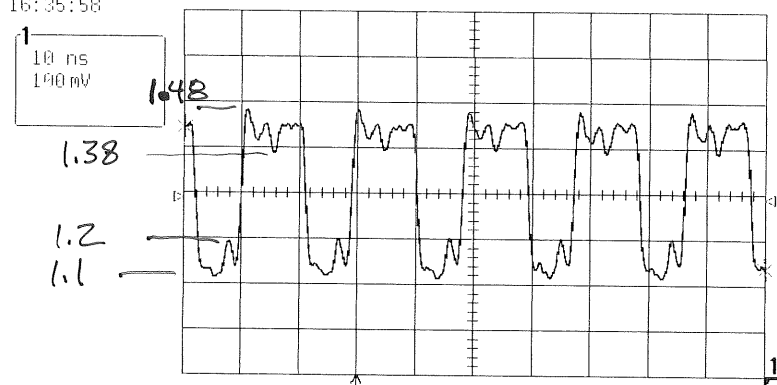
☐ AUTO
5 6s/s

6a

U7.2
better probe
LVDS

19-Sep-07
16:35:58

1
10 ns
100 mV



154 sweeps:	average	low	high	sigma
period(1)	19.07 ns	19.05	19.10	0.01
width(1)	7.75 ns	7.66	7.87	0.04
rise(1)	0.97 ns	0.87	1.22	0.06
fall(1)	1.16 ns	1.03	1.34	0.07
delay(1)	-27.73 ns	-27.84	-27.64	0.04

10 ns
1 10 mV DC

2 20 mV DC

1 DC 1.280 V

MEASURE

OFF Cursors
Parameters

mode
Std Voltage
Std Time
Custom
Pass
Fail

statistics
OFF On

on displayed
(trace)
1

from
0.00 div
Track OFF On

to
10.00 div
500 points

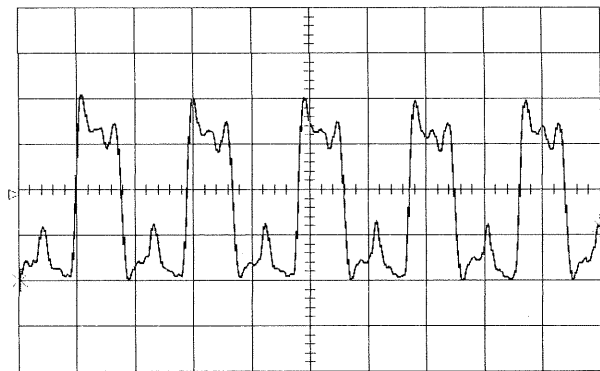
☐ NORMAL
5 6s/s

7a

U7.3
better probe

19-Sep-07
16:39:11

1
10 ns
100 mV



111 sweeps:	average	low	high	sigma
period(1)	19.07 ns	19.04	19.10	0.01
width(1)	7.99 ns	7.92	8.08	0.04
rise(1)	0.80 ns	0.72	0.87	0.04
fall(1)	1.00 ns	0.94	1.07	0.04
delay(1)	-20.00 ns	-20.11	-19.90	0.04

10 ns
1 10 mV DC

2 20 mV DC



1 DC 1.280 V

☐ NORMAL
5 GS/s

MEASURE

OFF Cursors
Parameters

mode
Std Voltage
Std Time
Custom
Pass
Fail

statistics
OFF On

on displayed
(trace)
1

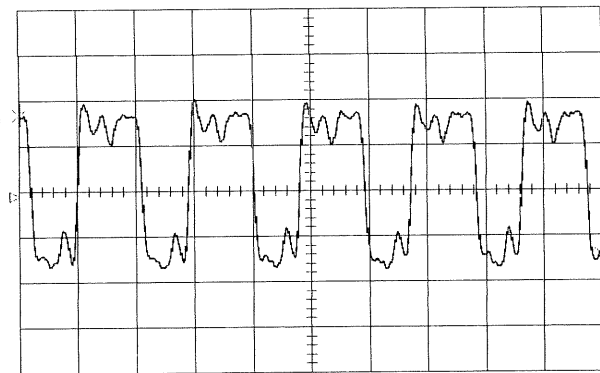
from
0.00 div
Track OFF On

to
10.00 div
500 points

U7.4
better probe

19-Sep-07
16:40:28

1
10 ns
100 mV



106 sweeps:	average	low	high	sigma
period(1)	19.07 ns	19.04	19.09	0.01
width(1)	7.80 ns	7.74	7.89	0.04
rise(1)	0.97 ns	0.90	1.08	0.04
fall(1)	1.18 ns	1.03	1.31	0.06
delay(1)	-27.78 ns	-27.90	-27.67	0.05

10 ns
1 10 mV DC

2 20 mV DC



1 DC 1.280 V

☐ AUTO
5 GS/s

MEASURE

OFF Cursors
Parameters

mode
Std Voltage
Std Time
Custom
Pass
Fail

statistics
OFF On

on displayed
(trace)
1

from
0.00 div
Track OFF On

to
10.00 div
500 points

other
U7 outputs
match
U7d → U7.4
No need to plot.

9a

OREN'S Lab Setup

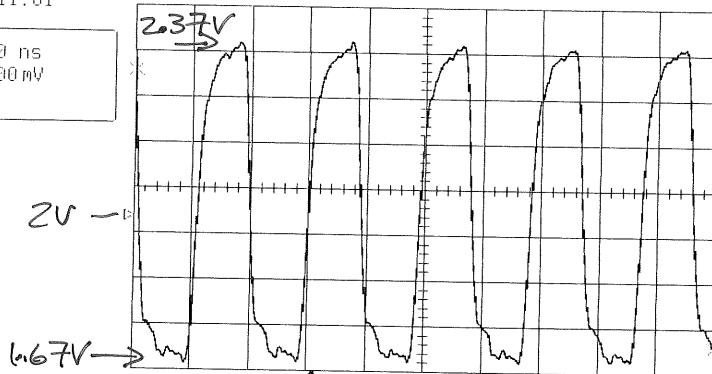
ID

U7.16
input

period = 19.07 ns
width = 9.12 ns
rise = 3.4 ns
fall = 2.9 ns

20-Sep-07
16:11:01

1 10 ns
100 mV



132 sweeps:	average	low	high	sigma
pkpk(1)	710 mV	691	731	10
mean(1)	2.00452 V	1.98838	2.02830	0.00958
sdev(1)	286.02 mV	283.63	288.01	0.87
rms(1)	2.02477 V	2.00852	2.04832	0.00949
ampl(1)	668 mV	646	681	7

10 ns
1 10 mV DC

2 20 mV DC

1 DC 2.000 V

MEASURE

OFF Cursors
Parameters

Mode
Std Voltage
Std Time
Custom
Pass
Fail

Statistics
OFF On

on displayed
(trace)
1

from
0.00 div
Track OFF On

to
10.00 div
500 points

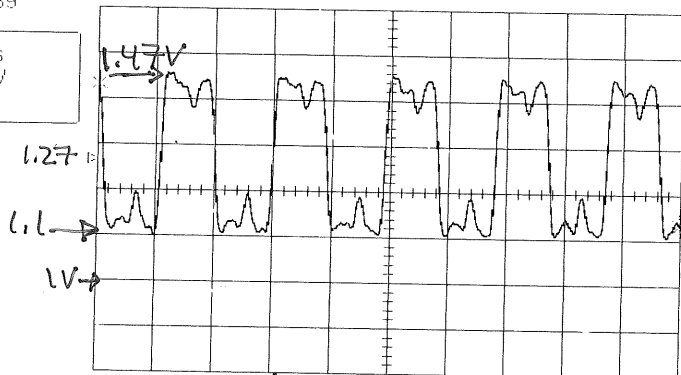
AUTO
5 Gs/s

1 Bob SMA0 → 24" about coax → DC Block BLK-89 → 10dB PAD → BIAS T (IF) → long coax → BEEZ J17

2V linear supply (DC) ↑

20-Sep-07
16:18:39

1 10 ns
100 mV



122 sweeps:	average	low	high	sigma
period(1)	19.07 ns	19.05	19.10	0.01
width(1)	9.96 ns	9.01	10.08	0.15
rise(1)	0.96 ns	0.89	1.04	0.03
fall(1)	1.13 ns	1.00	1.25	0.05
delay(1)	-29.64 ns	-30.02	-19.84	1.56

10 ns
1 10 mV DC

2 20 mV DC

1 DC 1.266 V

MEASURE

OFF Cursors
Parameters

Mode
Std Voltage
Std Time
Custom
Pass
Fail

Statistics
OFF On

on displayed
(trace)
1

from
0.00 div
Track OFF On

to
10.00 div
500 points

AUTO
5 Gs/s

U7.1
output