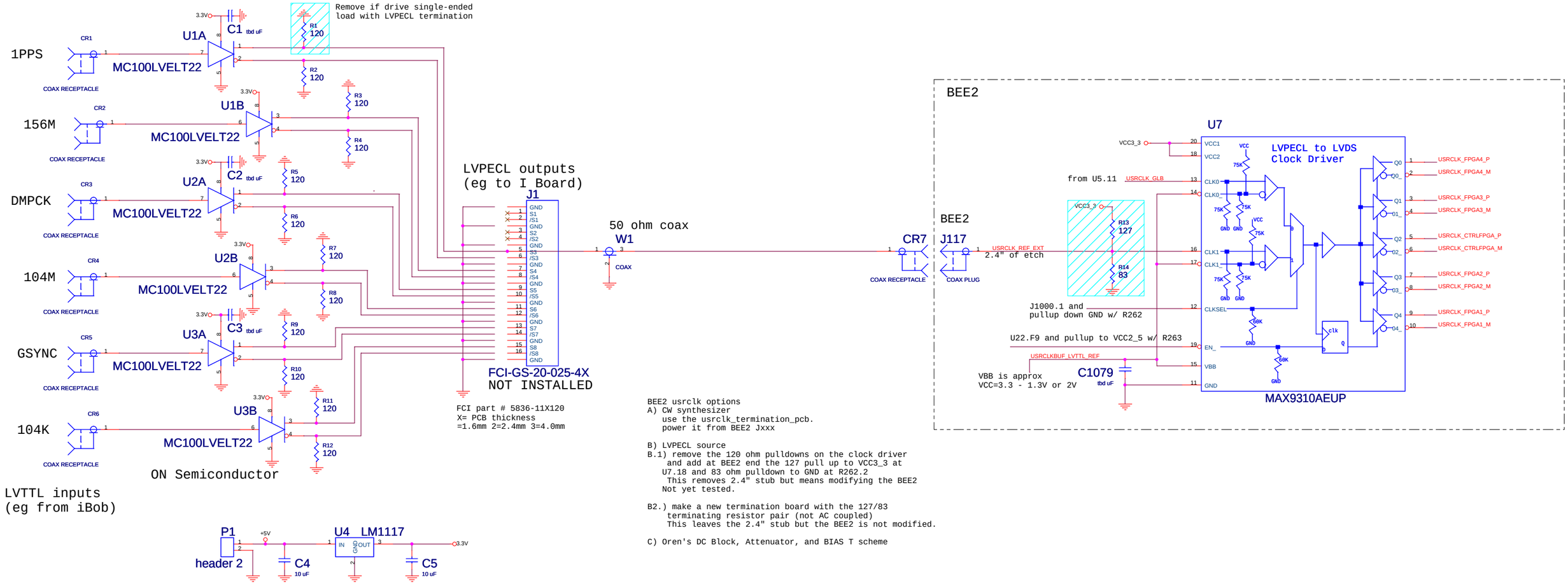
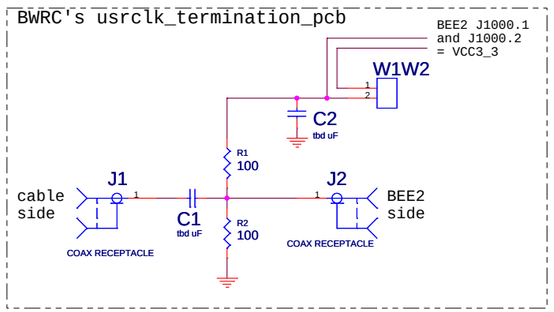


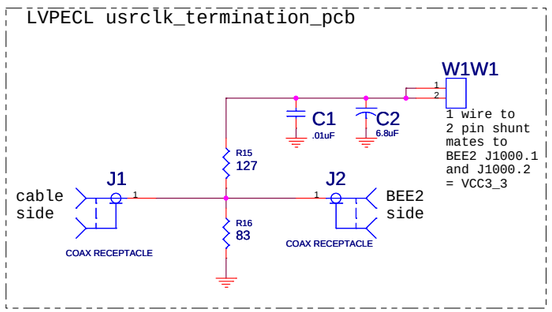
BEE2 usrclk options
A) CW synthesizer
use the usrclk_termination_pcb.
power it from BEE2 Jxxx

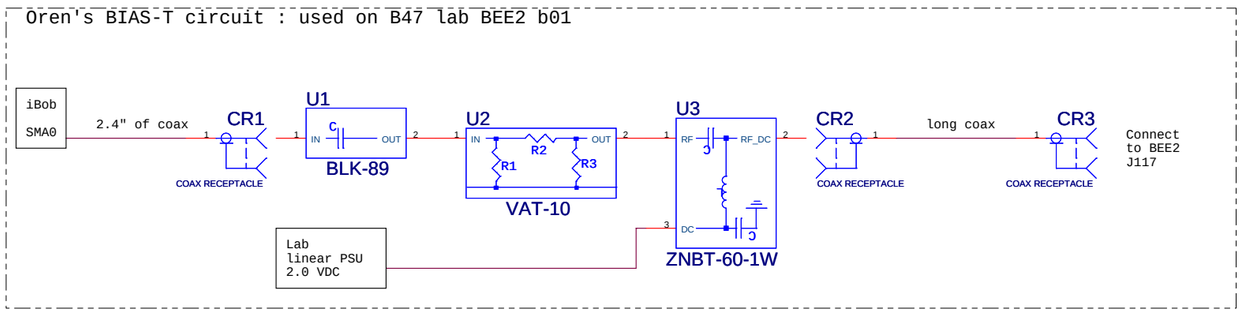
B) LVPECL source
B.1) remove the 120 ohm pulldowns on the clock driver
and add at BEE2 end the 127 pull up to VCC3_3 at
U7.18 and 83 ohm pulldown to GND at R262.2
This removes 2.4" stub but means modifying the BEE2
Not yet tested.

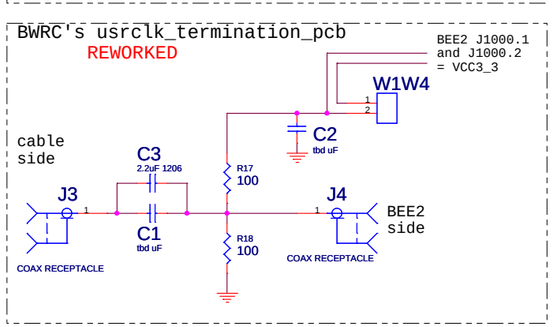
B2.) make a new termination board with the 127/83
terminating resistor pair (not AC coupled)
This leaves the 2.4" stub but the BEE2 is not modified.

C) Oren's DC Block, Attenuator, and BIAS T scheme









Based on my version of the Corr Clk Buffer schematics for readability: Calvin has the actual design files.

c:\ata\correlator\production\clock_translator\

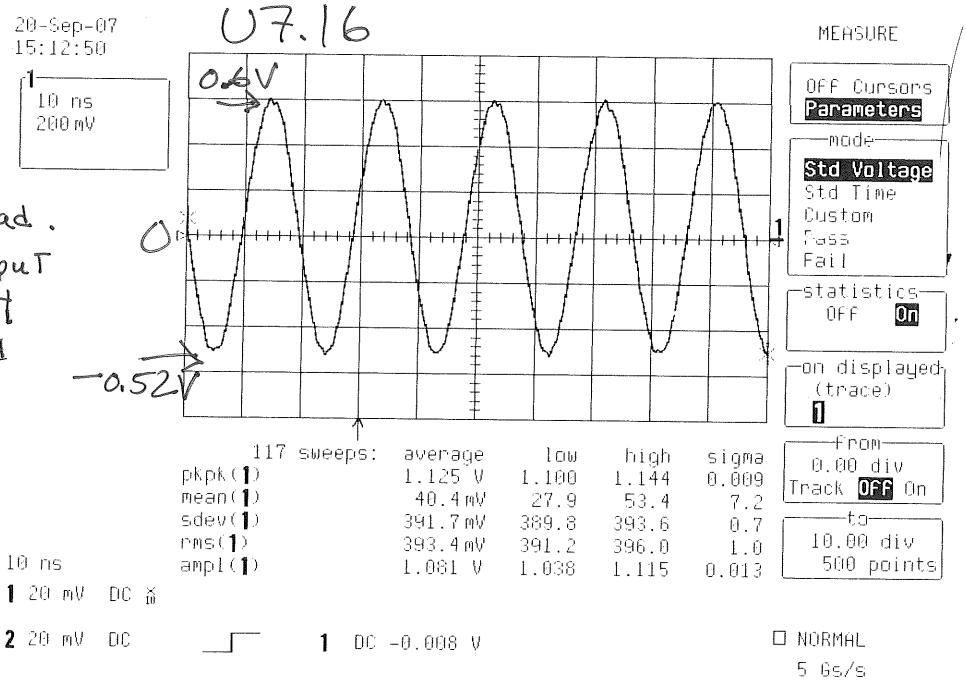
Title: Clock Distributer for BEE2			
Size: Custom	Document Number: Clock_buff_to_bee2.opj: clock_buff_to_bee2.dsn		Rev: 1.0
Date: Thursday, September 20, 2007	Sheet 1 of 1		

CW gen 18" coax → #J117 1C.

cw gen 0dBm

Theory is 0.63V ptop into 50Ω load. the BEE2 input U7.16 isn't 50Ω load

U7.16



MAX9310A = U7 min input voltage is -0.4V

This probably turns on diode in protection circuit and if drive too hard one can blow out that diode.

Here is the output – [redacted]

U7 outputs don't toggle until ~ +7dBm input

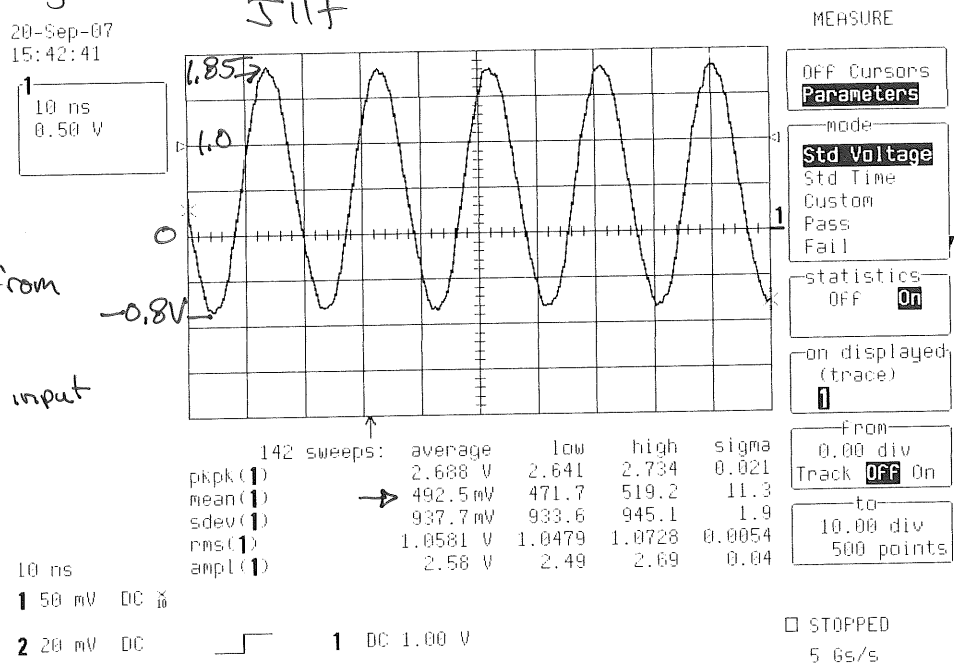
2C

cwgen → ~~DUT~~ J117 over 18" coax

+7dBm

1.416 Vptp into 50Ω load.

NOTE shift from 0VDC probably due to receiver U7 input circuit

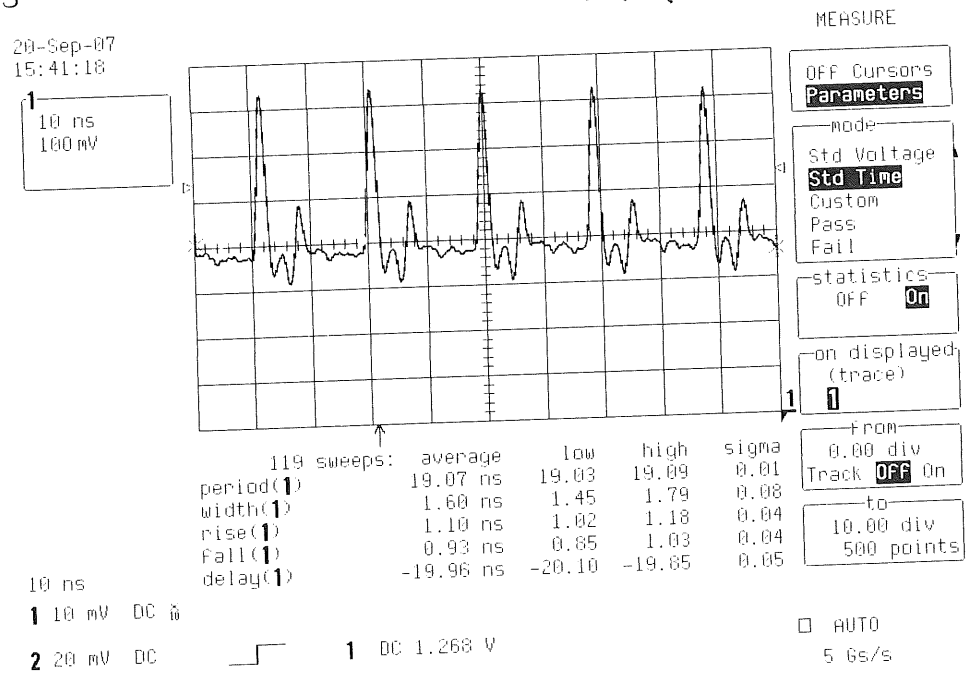


3C

cwgen @ +7dBm → 18" coax → J117

U7.1 output

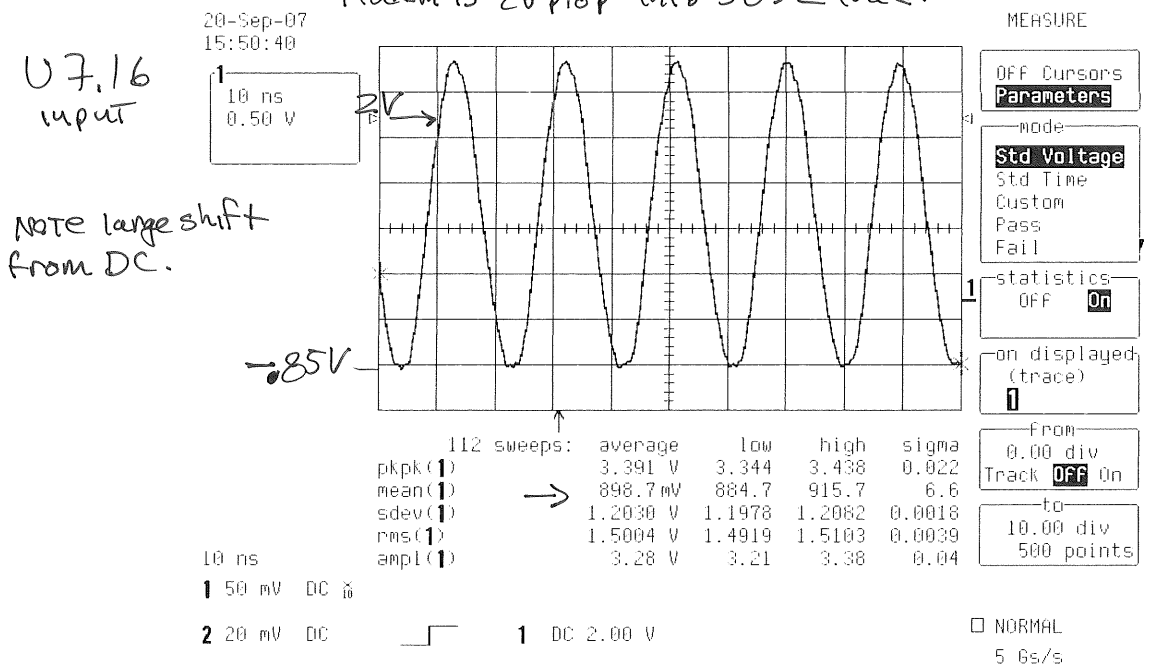
lousy duty cycle



CW gen @ +10dBm → 18" coax → J117 4C

+10dBm is 2V ptop into 50Ω load.

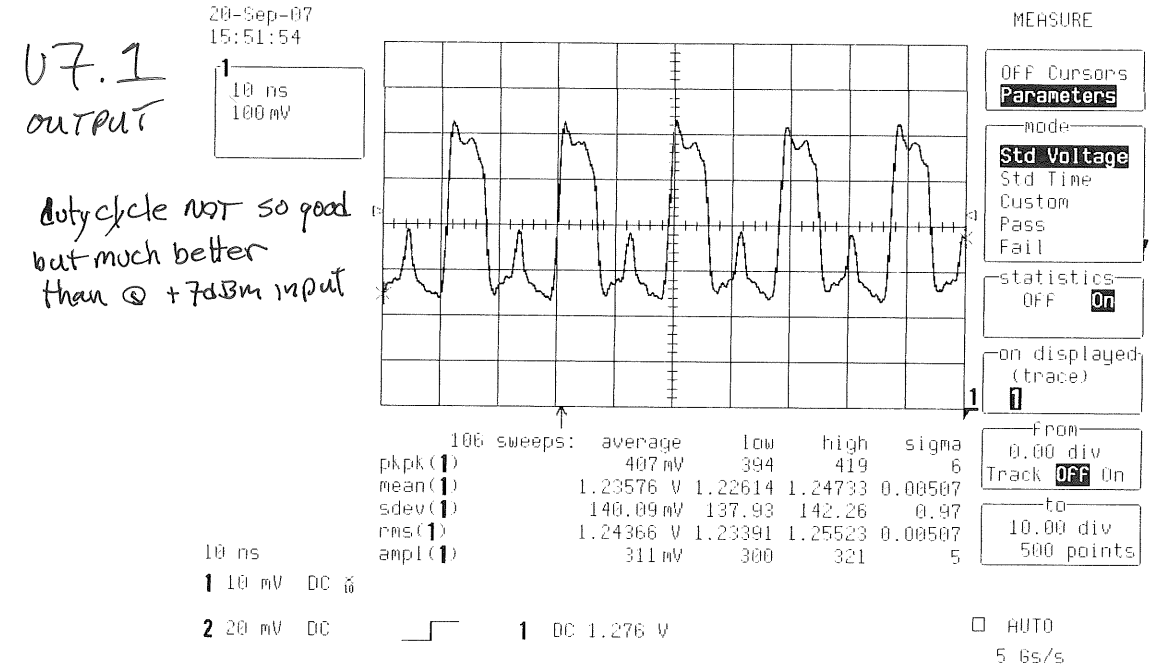
U7.16 input



NOTE large shift from DC.

CW gen @ +10dBm → 18" coax → J117 5C

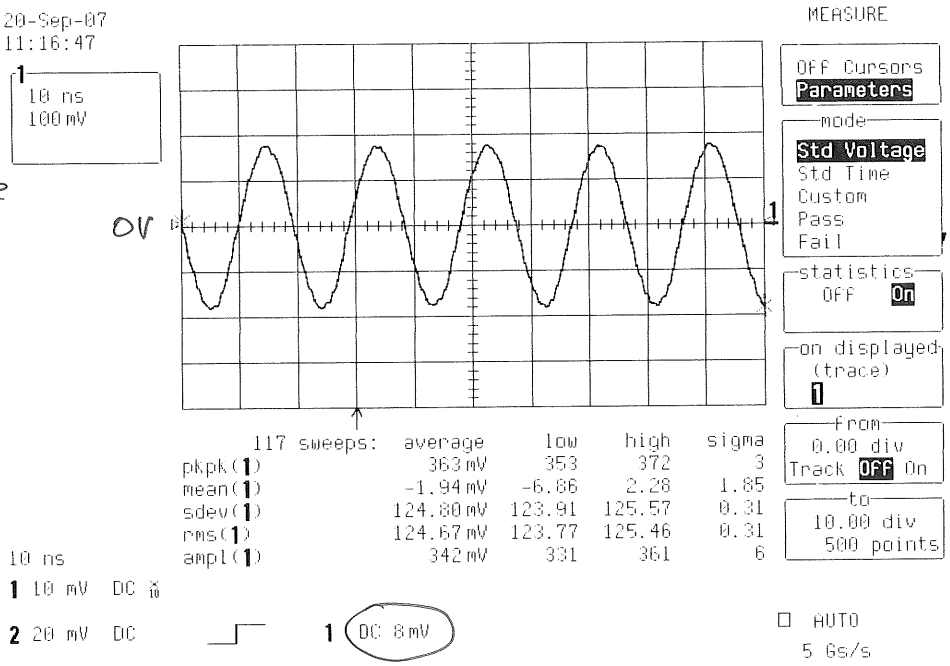
U7.1 output



duty cycle NOT so good but much better than @ +7dBm input

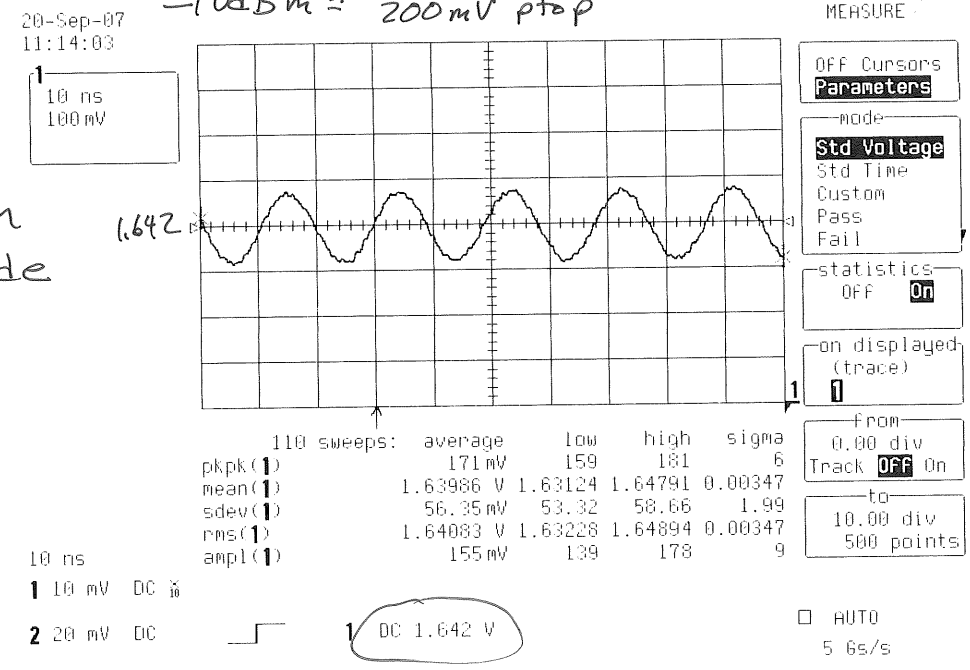
cw gen -10dBm @ 52.4288MHz 1B

18" coax to BWRC clkterm cwgen side



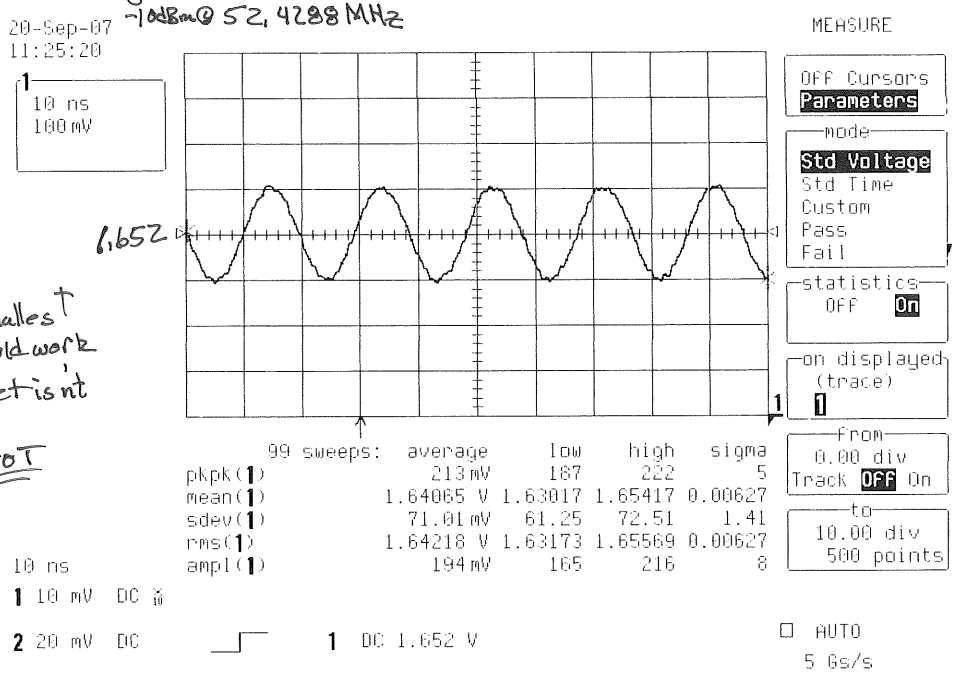
cw gen @ 52.4288MHz (not locked to 10MHz) 2B
-10dBm = 200mV ptop

18" coax to BWRC clkterm J117 side



CW gen → 18" coax BWRC clk term 3B

U7.16



This is about smallest swing that could work but DC offset is not right.

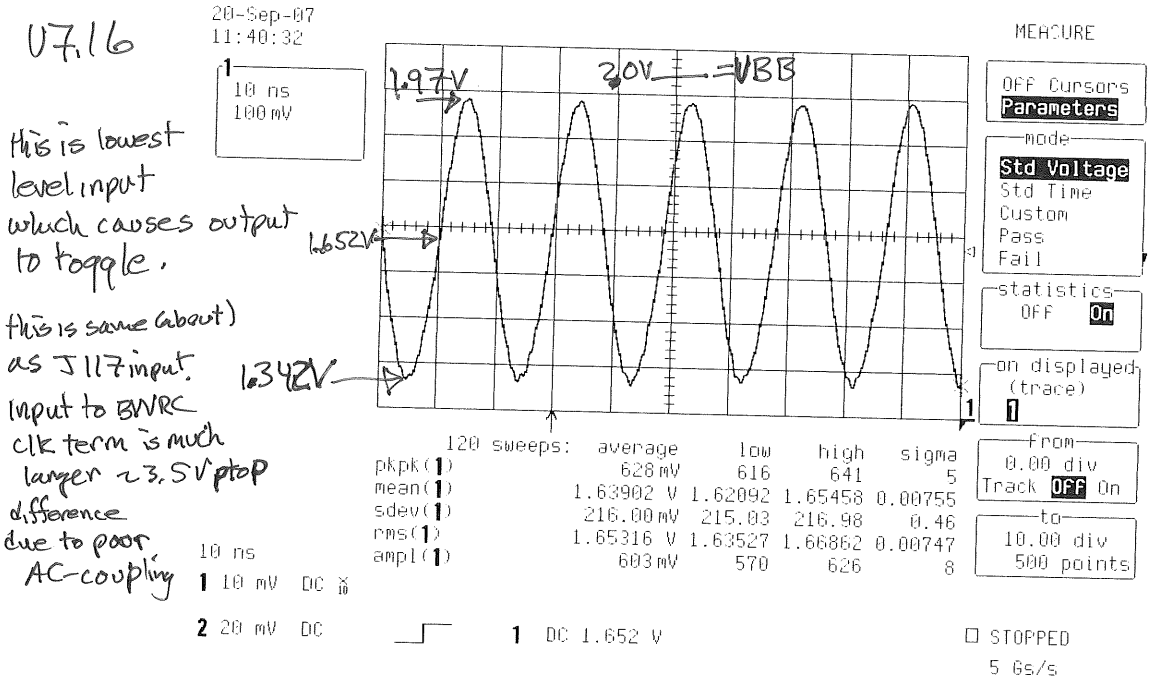
U7 outputs NOT toggling
pin 2 high
pin 1 low

look at outputs while ever increasing the input power

- ⑨ +9 dBm outputs would occoassionaly toggle
- ⑩ +10 dBm Vptop (Theory) = 2Vptop
  outputs toggle repeatedly (regularly) but waveform is NOT good duty cycle due to wrong DC shift

CW gen +10dBm → 18" coax BWRC clk term 4B

U7.16



This is lowest level input which causes output to toggle.

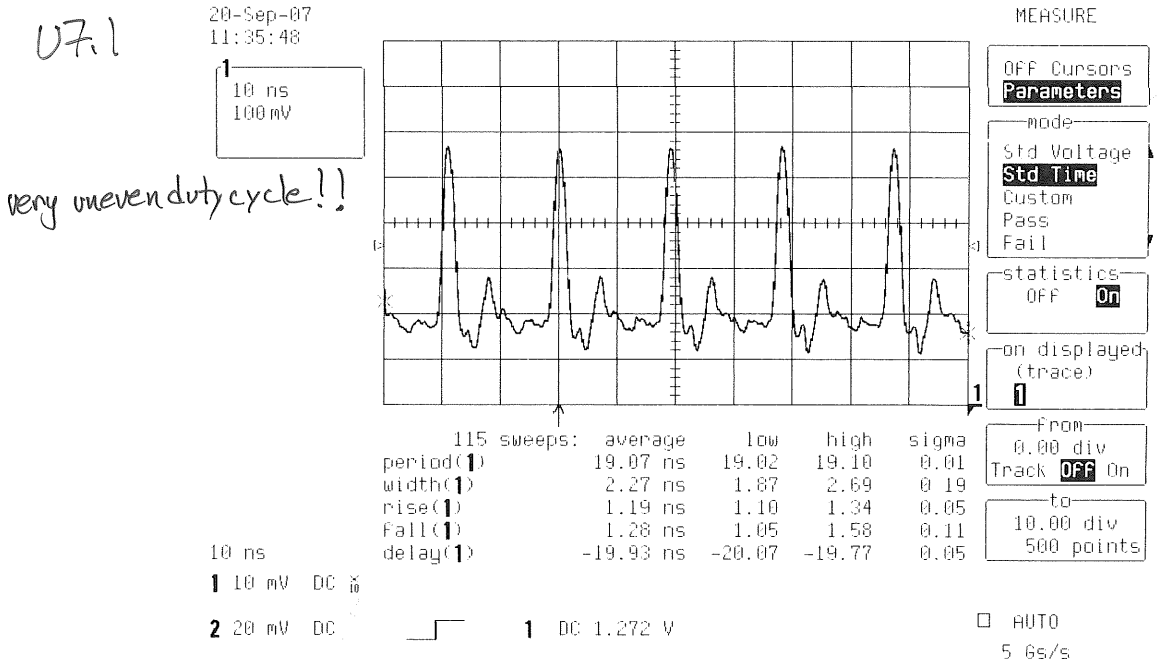
This is same (about) as J117 input.

Input to BWRC clk term is much larger ~3.5V ptop

difference due to poor AC-coupling

5B

U7.1



very uneven duty cycle!!

2007SEP20

Rework BWRC clkterm board:

Add 2.2μF 1206 decoupling cap in parallel. 16V rated part to whatever was there already.

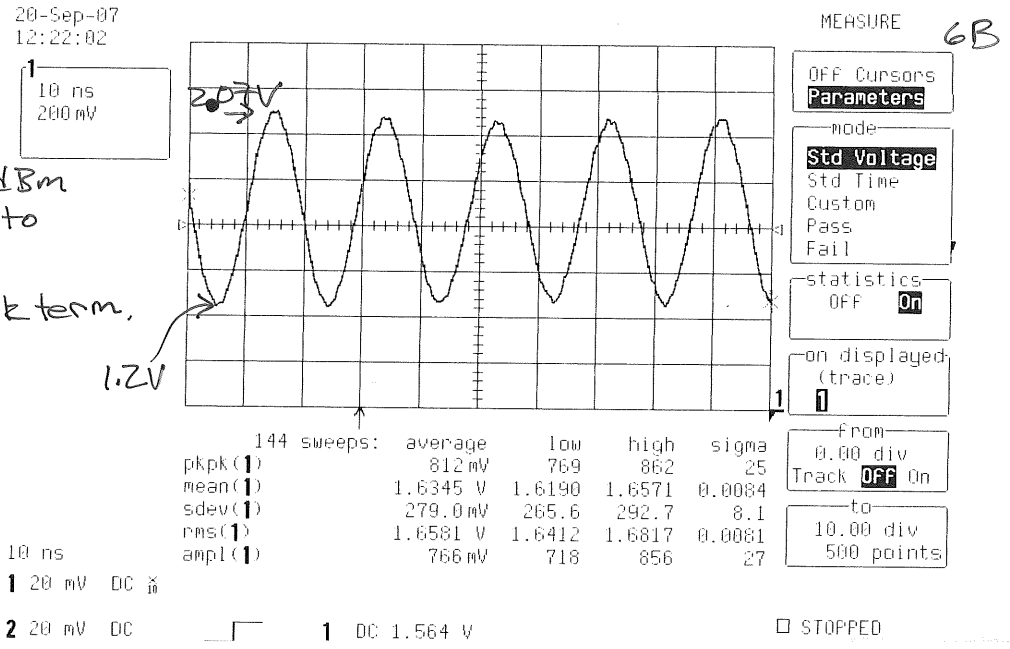
XX μF 0805 I think. I don't know XX μF.

Now much more signal gets thru to J117.

Now see what lowest level input is required to get valid output if not valid then at least toggling. 0dBm input was a little flakely. So go with +1dBm.

U7.16

cw gen +1dBm 18" coax to reworked BWRC clkterm.

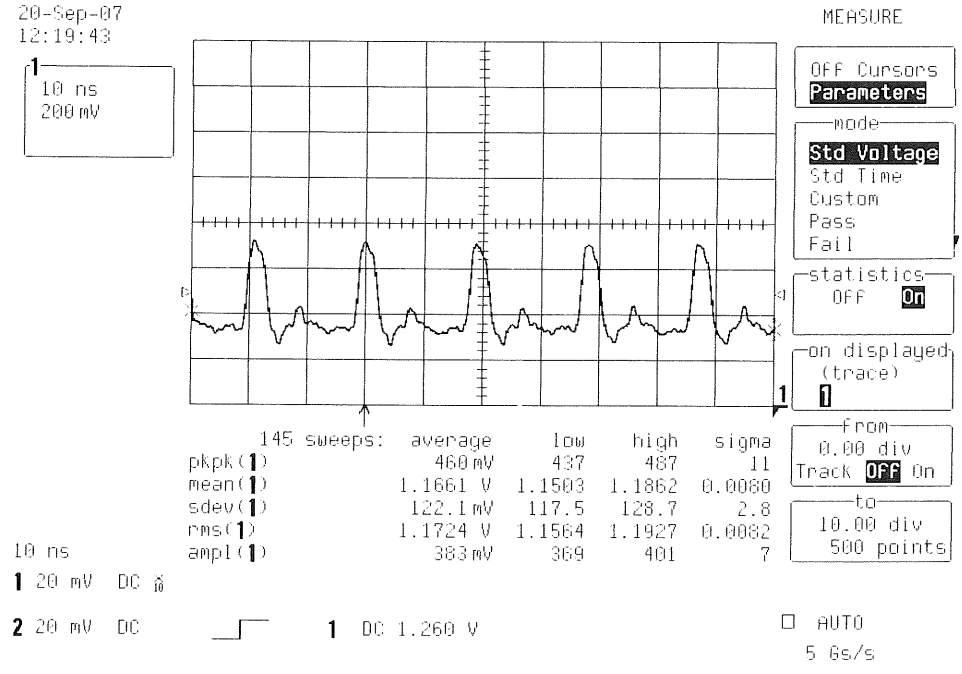


6B

cw gen +1 dBm = .7 (Vptop (theory)

7B

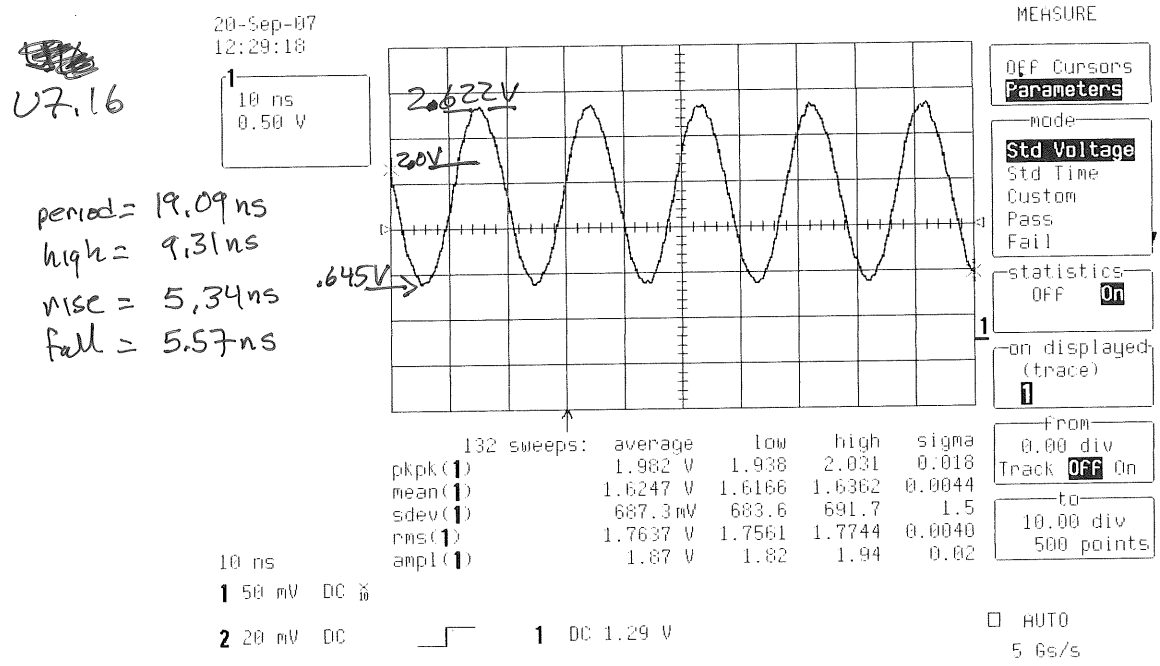
U7.1



2007SEP20

Now look to see what input level gets a better duty cycle...
(at U7, ~~xx~~ outputs)

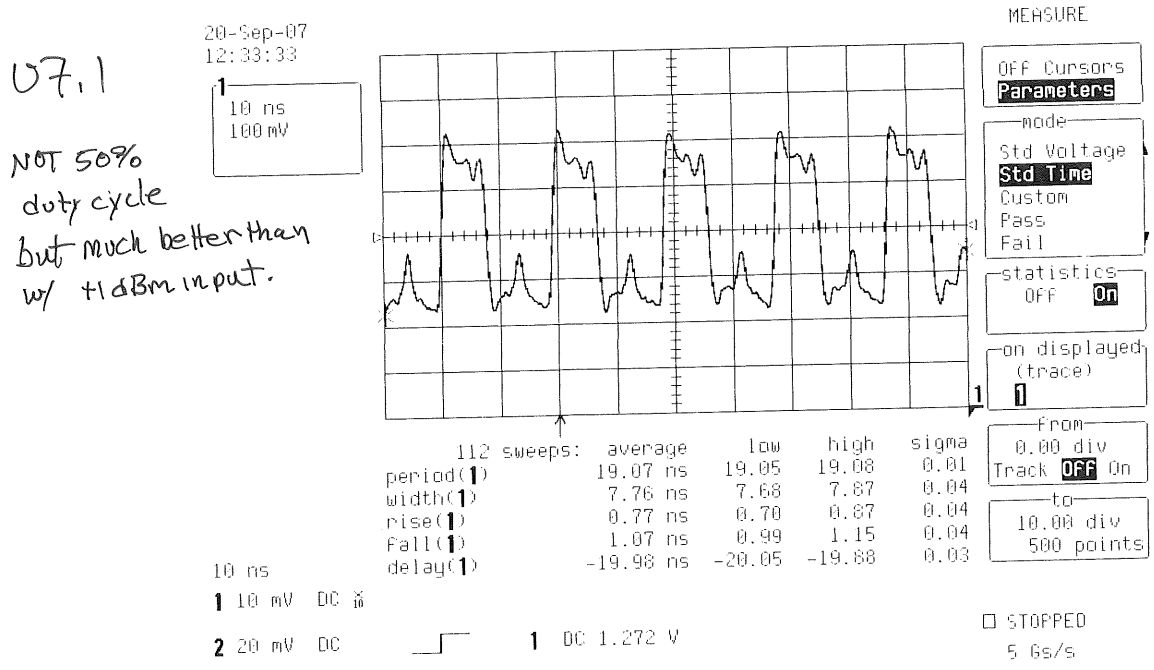
CW gen +10dBm 18" coax reworked BWRC clkterm 8B



U7.16

period = 19.09 ns
high = 9.31 ns
rise = 5.34 ns
fall = 5.57 ns

CW gen +10dBm 18" coax reworked BWRC clkterm 9B

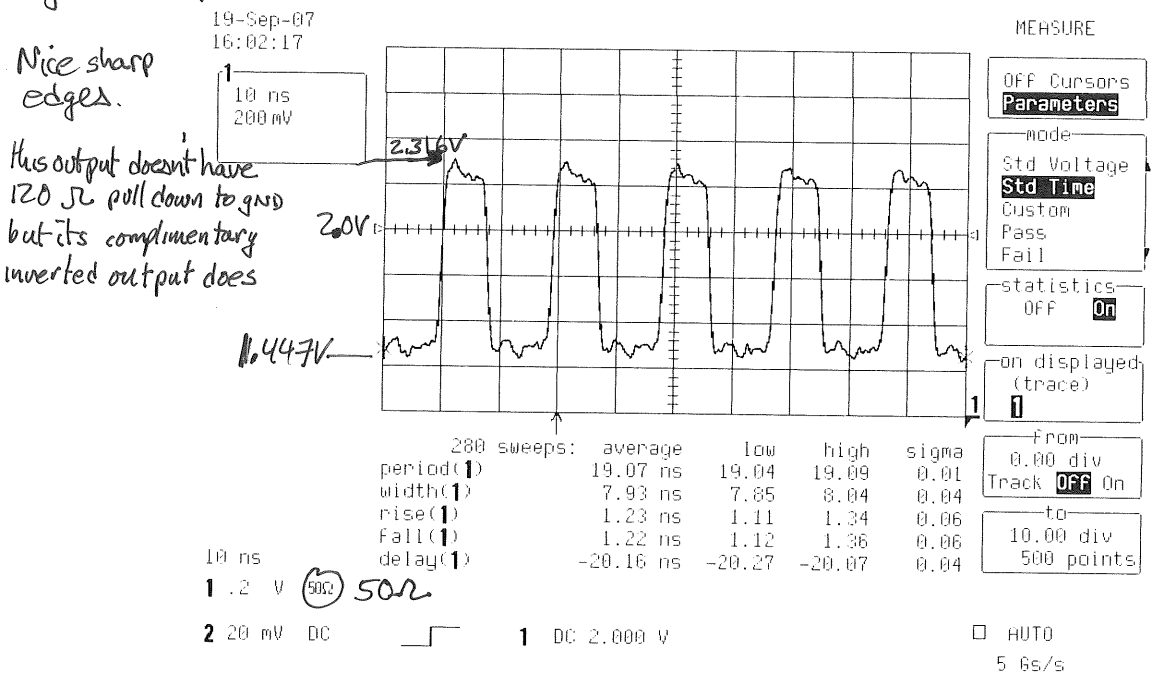


U7.1

NOT 50% duty cycle
But much better than w/ +1dBm input.

Corrclk translator
right into scope 4ft coax.

1a



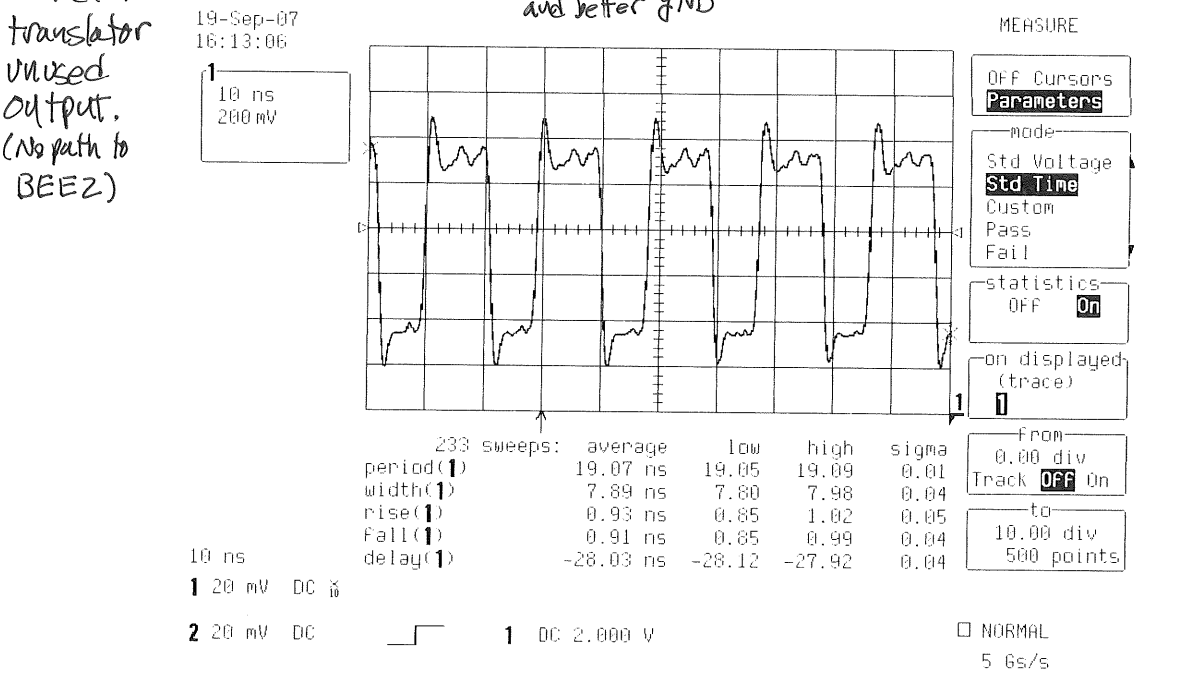
Nice sharp edges.

This output doesn't have 120 Ω pull down to gnd but its complimentary inverted output does

New 1M // 11pF scope probe "500MHz" and better GND

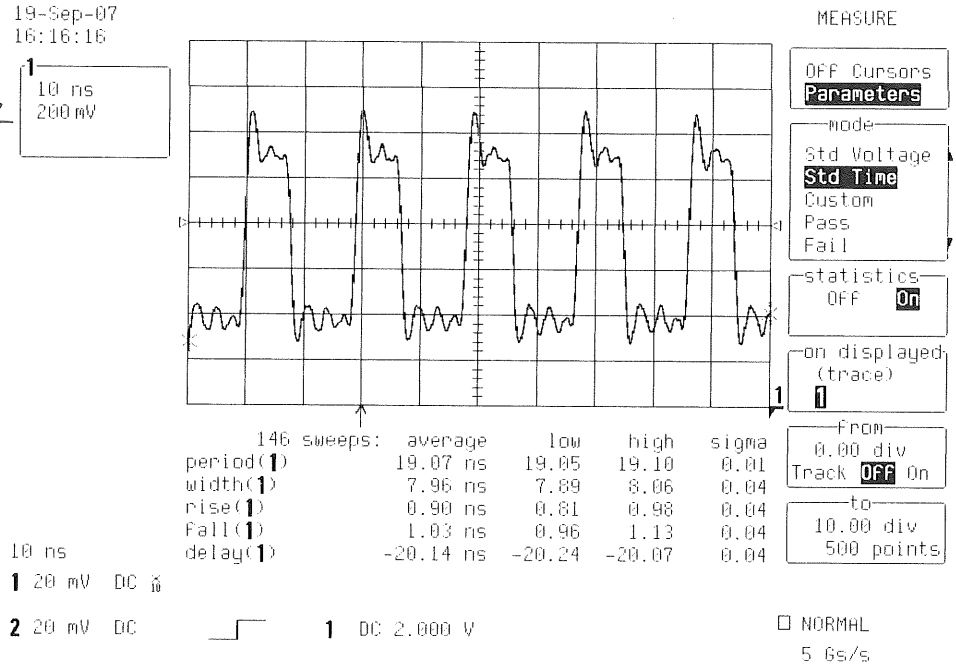
2a

Corrclk translator unused output. (No path to BEEZ)



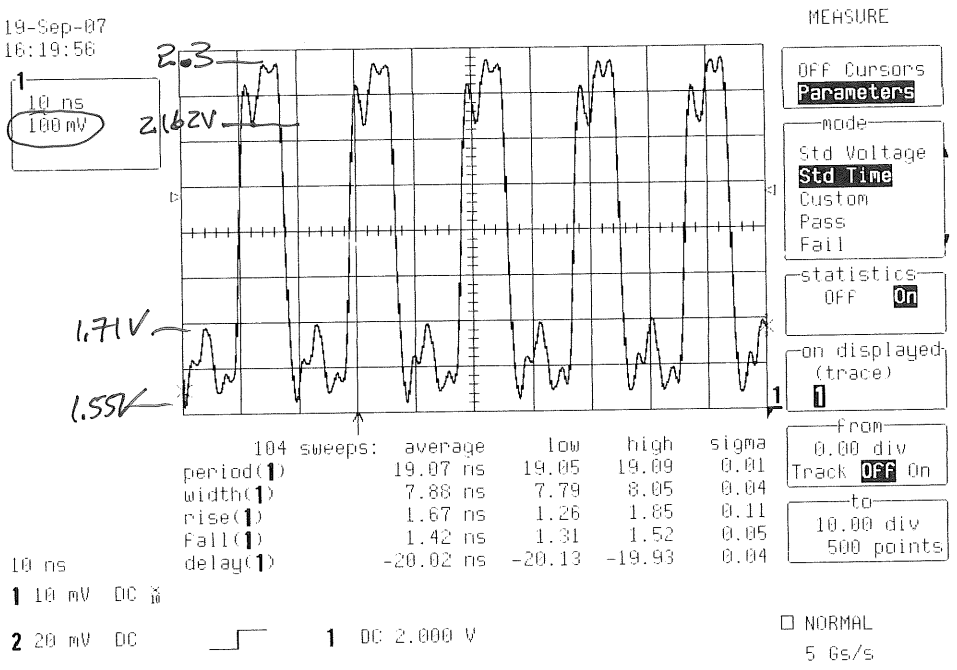
corr clk translator output used to drive BEEZ

better probe



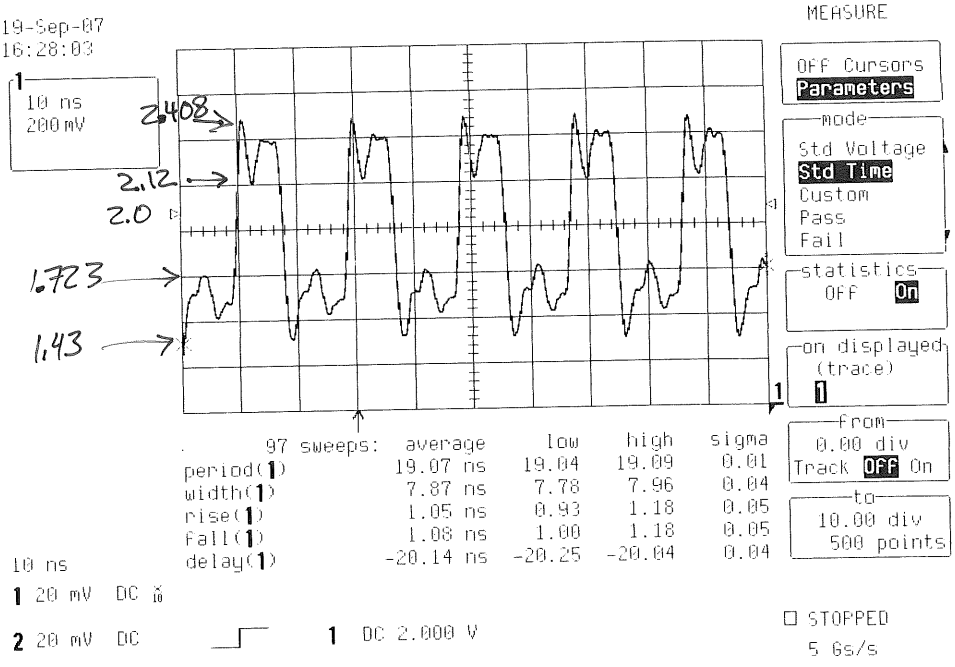
4a

BEE2
input
J117
better probe
with
LVPECL
termination
kludge



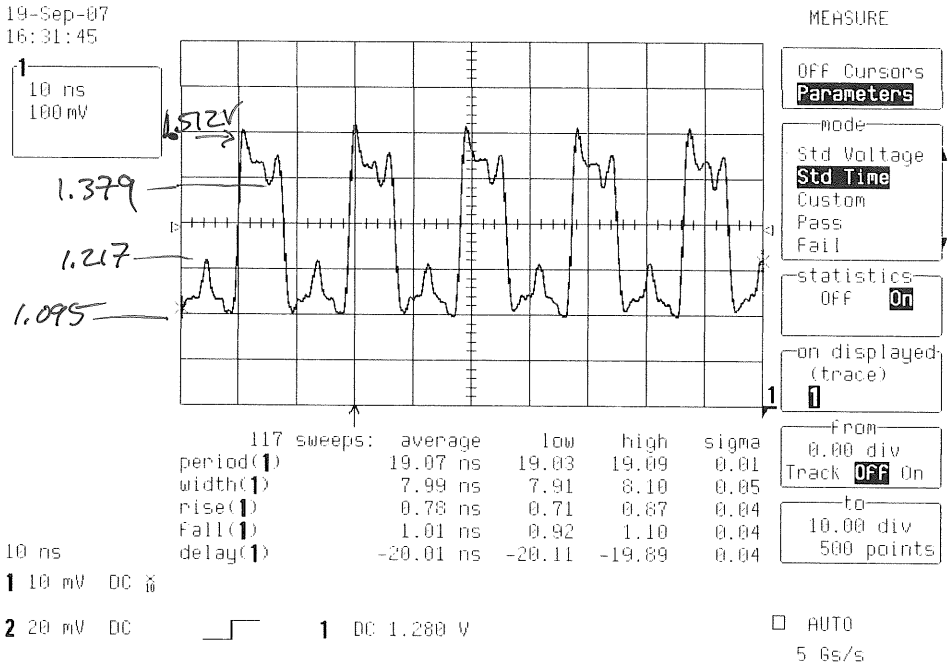
5a

U7.16
Betterprobe
input
to clock
driver



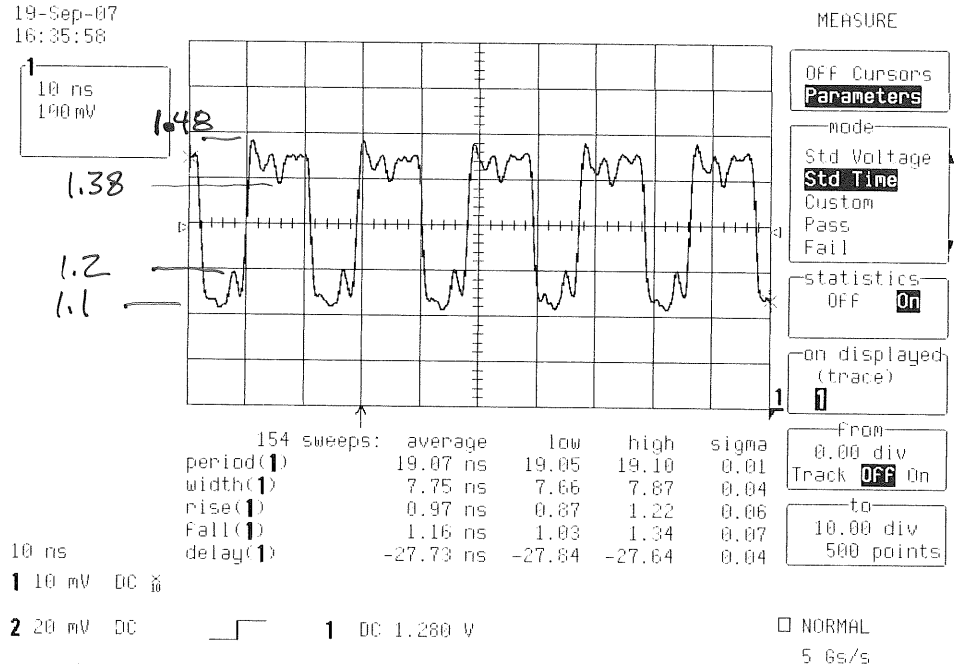
6a

U7.1
better probe
LVDS



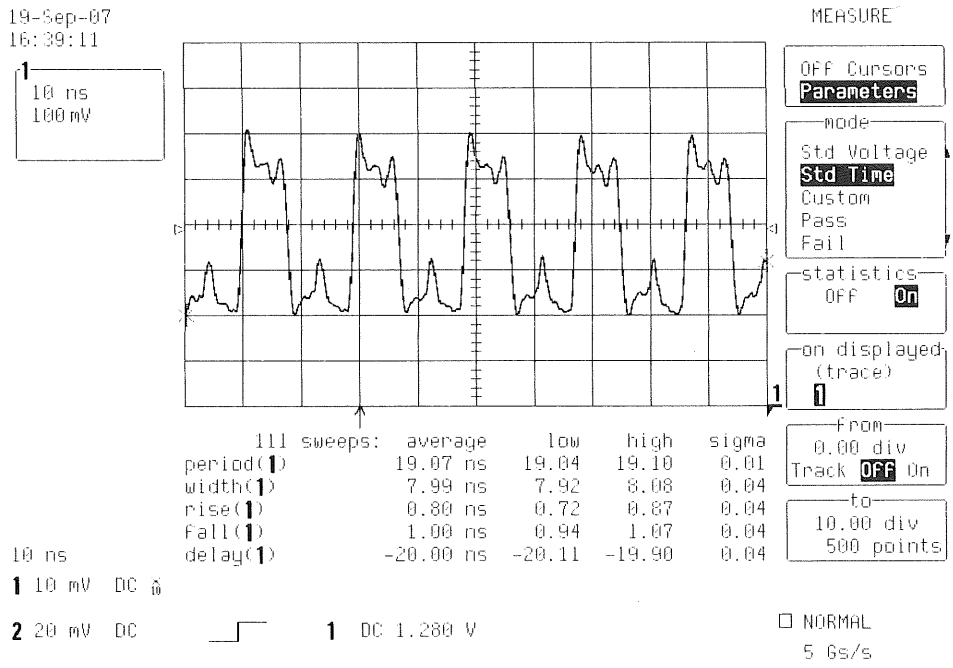
7a

U7.2
better probe
LVDS



U7.3
better probe

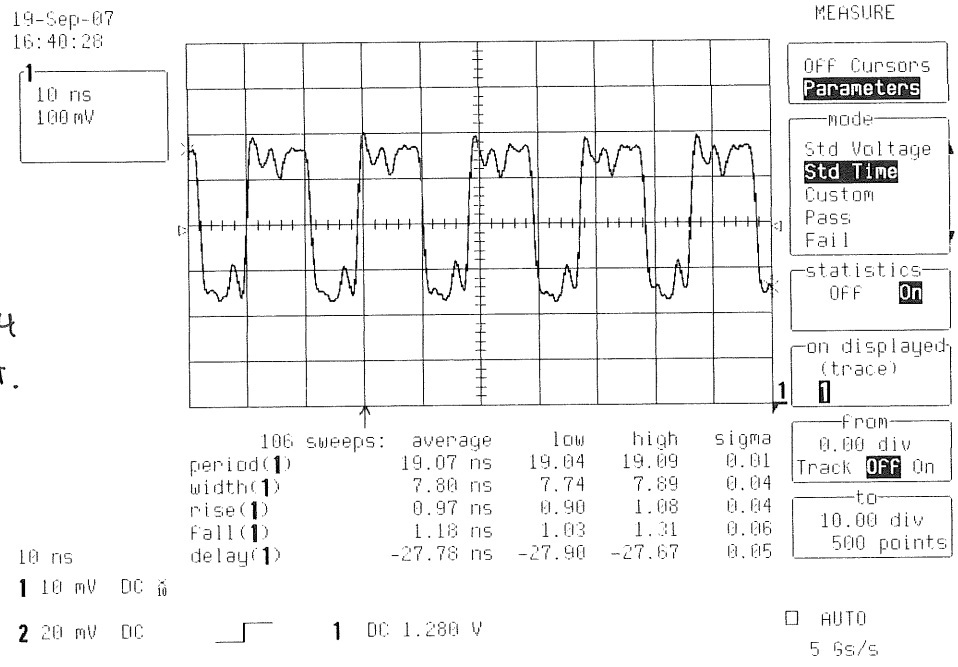
8a



9a

U7.4
better probe

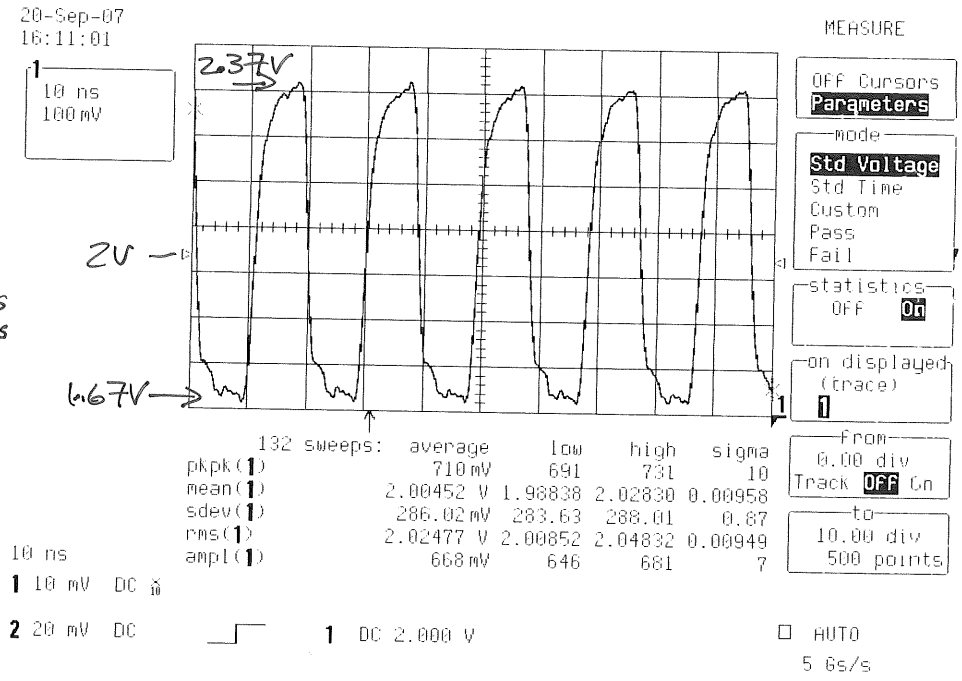
other
U7 outputs
match
U7.1 → U7.4
no need to plot.



OREN's Lab Setup

1D

U7.16
input



period = 19.07ns
width = 9.12ns
rise = 3.4ns
fall = 2.9ns

1Bob SMA0 → 24" about coax → DC Block BLK-89 → 10dB PAD → BIAS T (IF → long coax → BEEZ J117; RF → ZNBT-60-1W; DC ← 2V linear supply)

U7.1
output