Uses Xilinx Kintex XC7K160T-2FFG676

BOARDLAYOUT
Sheet 7

BOARDLAYOUT

BOARDLAYOUT also includes a list of design changes.

FPGA0
BANK 0
Sheet 11
FPGA_FCS
FPGA_FCS
CCLK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TCLK
FPGA_PROG_B
FPGA_DONE
QSPI_IC_CS_B
FLASH_D[3:0]

FPGAJTAG
Contains JTAG Connectors

FPGA14
Sheet 23
CCLK
QSPI_IC_CS_B
FPGA_PROG_B
FLASH_D[3:0]

QSPIFPGA
Contains SPI Flash for storing the personality

FPGA7
Sheet 12

FPGAPOWER
Hooking power to the FPGA

ADCREG
Sheet 5
SYNTH_PWR

ADC_ANALOG_REGULATORS

REG1
Sheet 6
PWRGD5V

FPGA_REGULATORS

Sheet 14
BANK 15
High Range
FPGA13
BANK 12 High Range
BANK 13 High Range
BANK 14 High Range
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TCLK
FPGA_FCS
FLASH_D[3:0]
SYNTH_PWR
PWRGD5V
FPGA_PROG_B
TX_DISABLE0
TX_DISABLE1
SCLK0P
SCLK0N
SCLK1P
SCLK1N
SCLK2P
SCLK2N
DONE33V
SCLK[2:0]
PMBUS_CLK
PMBUS_ALERT
PMBUS_CTRL
SM_FAN_PWM
PMBUS_DATA
SCLKP0
SCLKN0
SCLKP1
SCLKN1
SCLKP2
SCLKN2
SCLK[2:0]

FPGAZDOK
Contains ZDOK Connector, 1PPS Connector
Contains Clock Generator Synthesizer
Contains the Raspberry Pi Interface

POWER1
SM_FAN_PWM
PMBUS_CLK
PMBUS_ALERT
PMBUS_DATA
PMBUS_CTRL

Sheet 9

DIGITAL_POWER_SUPPLIES
Contains DC-DC Converters

BANK 16 High Range
BANK 115 GTX
BANK 116 GTX
FPGA116
Sheet 13
FPGA_DONE
TX_DISABLE0
TX_DISABLE1
DONE33V

FPGASFPP
Contains 2 SFP+ Connectors
Contains USB Interface
Contains Clocks and LEDs

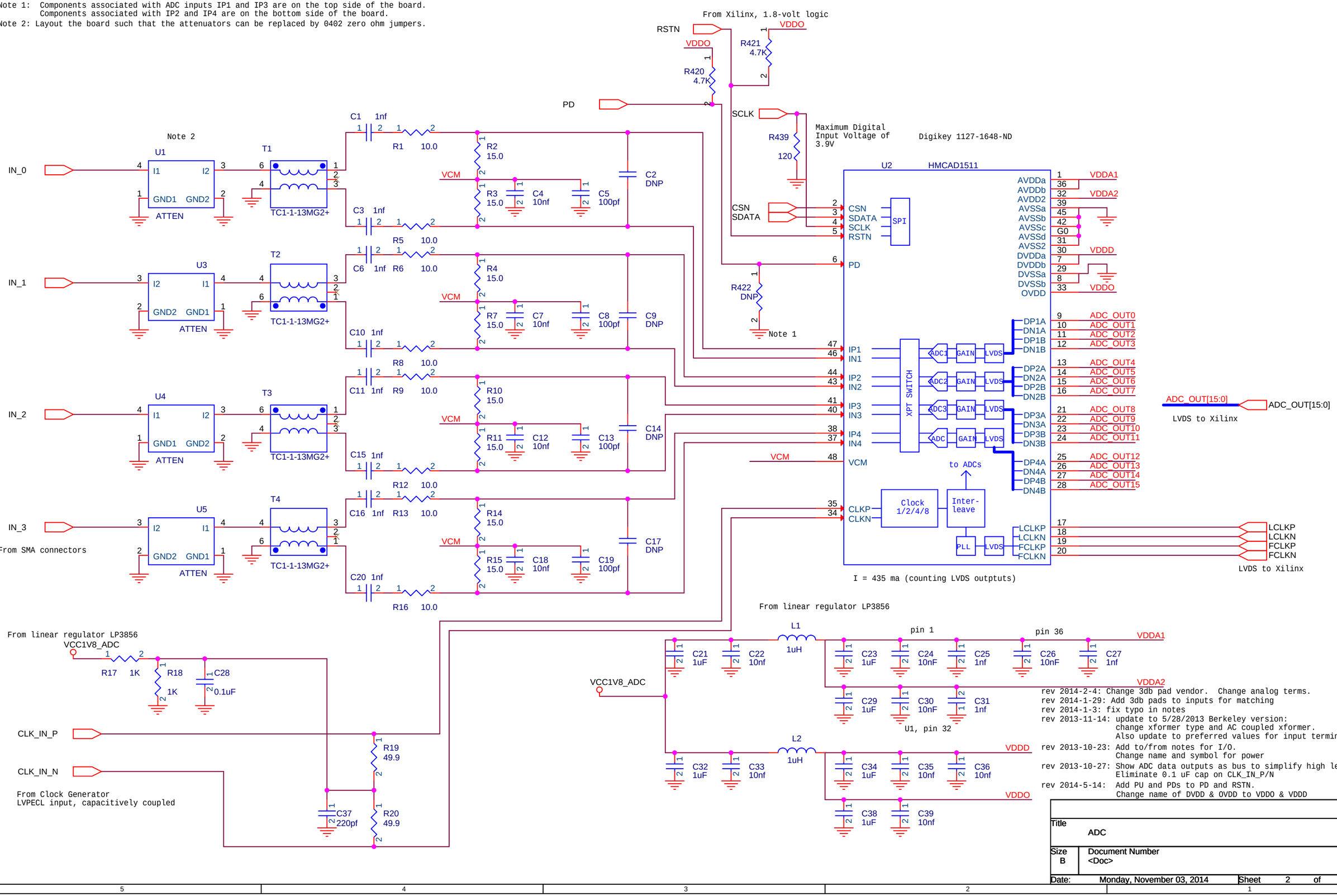
BANK 32 High Precision
BANK 33 High Precision
BANK 34 High Precision
FPGA32
Sheet 10
SCLK0P
SCLK0N
SCLK1P
SCLK1N
SCLK2P
SCLK2N
SCLK[2:0]
PMBUS_CLK
PMBUS_ALERT
PMBUS_DATA

Contains the 3 ADCs

FPGAADCS

Title: SMART NETWORK ADC PROCESSOR (SNAP) BOARD		
Size: A	Document Number: <Doc>	Rev: <RevCode>
Date: Monday, November 03, 2014	Sheet 1 of 27	

Note 1: Components associated with ADC inputs IP1 and IP3 are on the top side of the board.
Components associated with IP2 and IP4 are on the bottom side of the board.
Note 2: Layout the board such that the attenuators can be replaced by 0402 zero ohm jumpers.



rev 2014-2-4: Change 3db pad vendor. Change analog terms.
rev 2014-1-29: Add 3db pads to inputs for matching
rev 2014-1-3: fix typo in notes
rev 2013-11-14: update to 5/28/2013 Berkeley version:
change xformer type and AC coupled xformer.
Also update to preferred values for input terminations
rev 2013-10-23: Add to/from notes for I/O.
Change name and symbol for power
rev 2013-10-27: Show ADC data outputs as bus to simplify high level view.
Eliminate 0.1 uF cap on CLK_IN_P/N
rev 2014-5-14: Add PU and PDs to PD and RSTN.
Change name of DVDD & OVDD to VDDO & VDDD

Title: ADC		
Size: B	Document Number: <Doc>	Rev: A
Date: Monday, November 03, 2014	Sheet 2 of 27	

Note 1: Components associated with ADC inputs IP1 and IP3 are on the top side of the board.
Components associated with IP2 and IP4 are on the bottom side of the board.
Note 2: Layout the board such that the attenuators can be replaced by 0402 zero ohm jumpers.

From Xilinx, 1.8-volt logic

RSTN
VDDO
R424 4.7K
R423 4.7K
PD
SCLK
R440 120
Maximum Digital Input Voltage of 3.9V
Digikey 1127-1648-ND
CSN
SDATA
R425 DNP
Note 1

U7 HMCAD1511

SPI: CSN, SDATA, SCLK, RSTN
PD
XPT SWITCH: IP1/IN1, IP2/IN2, IP3/IN3, IP4/IN4, VCM
ADC1/ADC2/ADC3/ADC, GAIN, LVDS
Clock 1/2/4/8
Inter-leave
PLL, LVDS
CLKP, CLKN

AVDDa, AVDDb, AVDD2 → VDDA1, VDDA2
AVSSa, AVSSb, AVSSc, AVSSd, AVSS2, G0
DVDDa, DVDDb → VDDD
DVSSa, DVSSb, OVDD → VDDO

DP1A/DN1A/DP1B/DN1B → ADC_OUT0, ADC_OUT1, ADC_OUT2, ADC_OUT3
DP2A/DN2A/DP2B/DN2B → ADC_OUT4, ADC_OUT5, ADC_OUT6, ADC_OUT7
DP3A/DN3A/DP3B/DN3B → ADC_OUT8, ADC_OUT9, ADC_OUT10, ADC_OUT11
DP4A/DN4A/DP4B/DN4B → ADC_OUT12, ADC_OUT13, ADC_OUT14, ADC_OUT15

ADC_OUT[15:0] → ADC_OUT[15:0]
LVDS to Xilinx

LCLKP, LCLKN, FCLKP, FCLKN → LVDS to Xilinx

IN_0 / IN_1 / IN_2 / IN_3
U6 / U8 / U9 / U10
ATTEN
T5 / T6 / T7 / T8
TC1-1-13MG2+
From SMA connectors

C40 1nf, R21 10.0, C42 1nf, R25 10.0, C45 1nf, R26 10.0, C49 1nf, R28 10.0, C50 1nf, R29 10.0, C54 1nf, R32 10.0, C55 1nf, R33 10.0, C59 1nf, R36 10.0
R22 15.0, R23 15.0, R24 15.0, R27 15.0, R30 15.0, R31 15.0, R34 15.0, R35 15.0
VCM
C43 10nf, C46 10nf, C51 10nf, C57 10nf
C44 100pf, C47 100pf, C52 100pf, C58 100pf
C41 DNP, C48 DNP, C53 DNP, C56 DNP

I = 435 ma (counting LVDS outptuts)

From linear regulator LP3856
VCC1V8_ADC
R37 1K, R38 1K, C67 0.1uF

CLK_IN_P
CLK_IN_N
From Clock Generator
LVPECL input, capacitively coupled
R39 49.9, R40 49.9, C76 220pf

From linear regulator LP3856
L3 1uH, L4 1uH
C60 1uF, C61 10nf, C62 1uF, C63 10nF, C64 1nf, C65 10nF, C66 1nf
C68 1uF, C69 10nF, C70 1nf
C71 1uF, C72 10nf, C73 1uF, C74 10nf, C75 10nF
C77 1uF, C78 10nf
pin 1, pin 36
U1, pin 32

rev 2014-2-4: Change 3db pad vendor. Change analog terms.
rev 2014-1-29: Add 3db pads to inputs for matching
rev 2014-1-3: fix typo in notes
rev 2013-11-14: update to 5/28/2013 Berkeley version:
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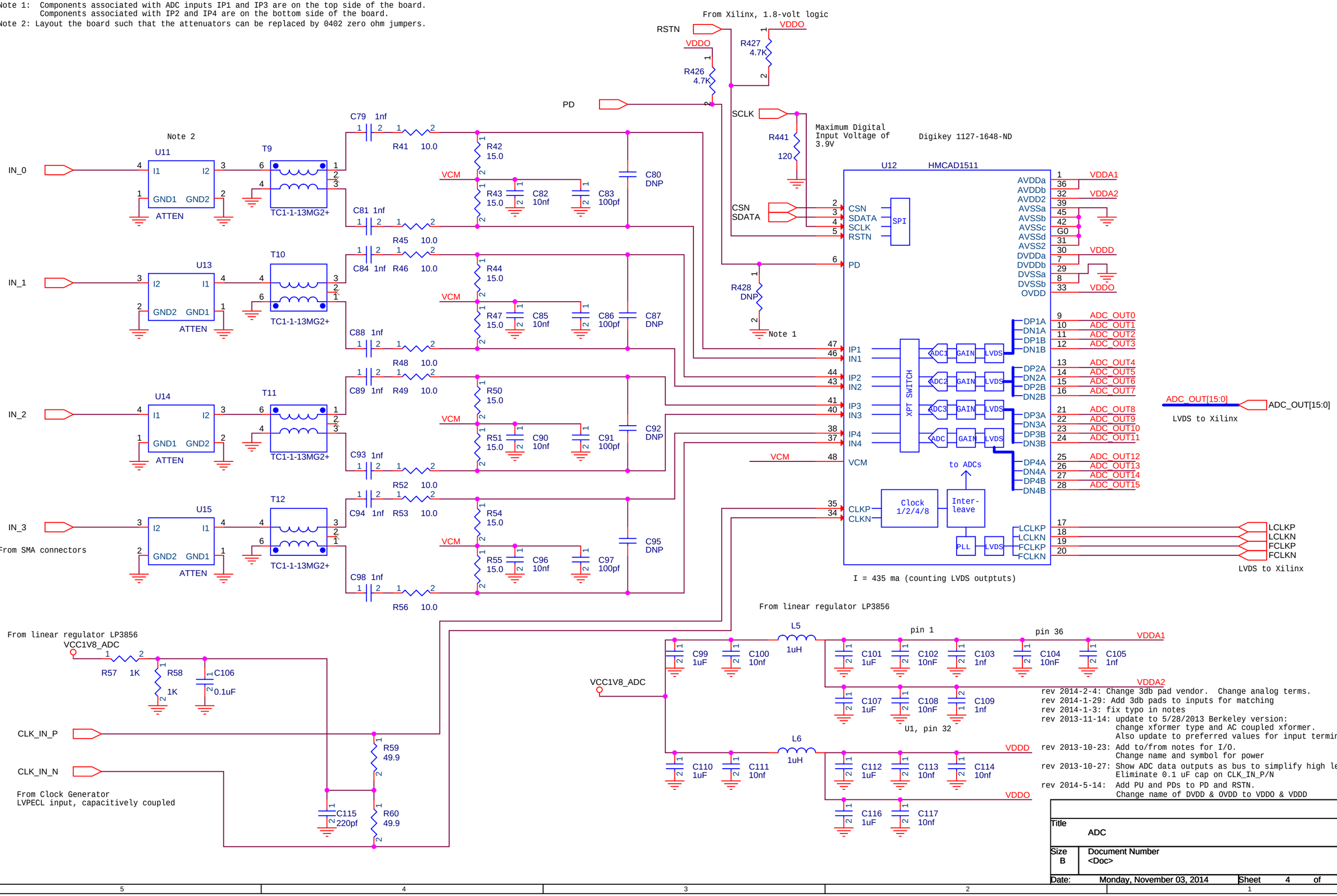
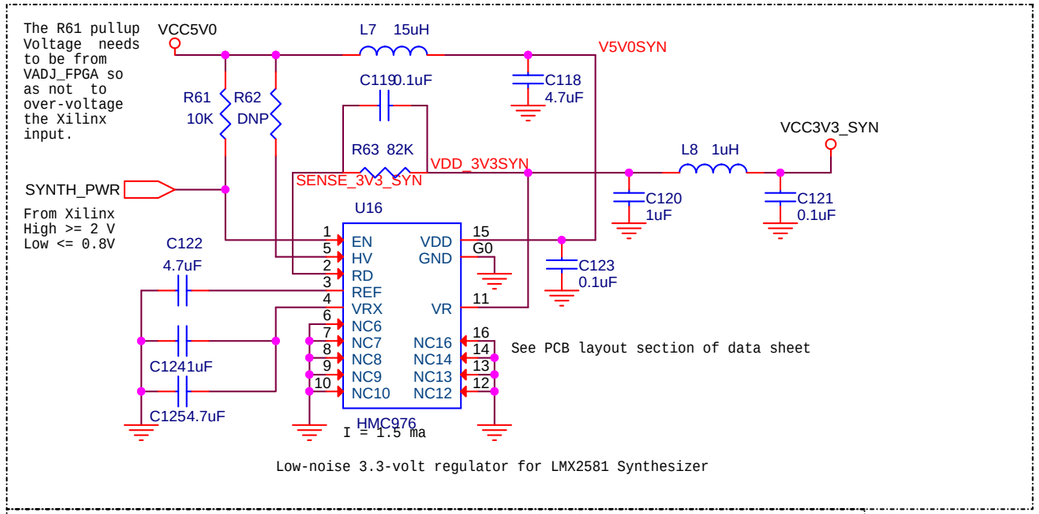
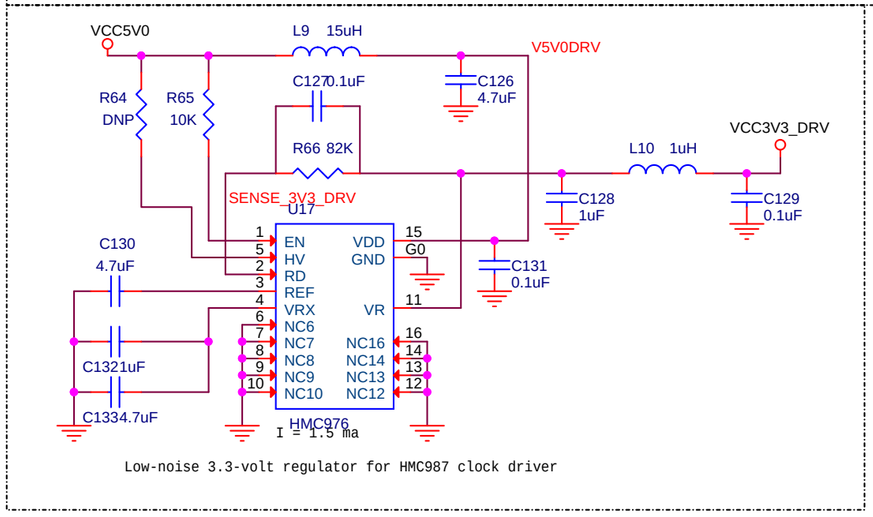
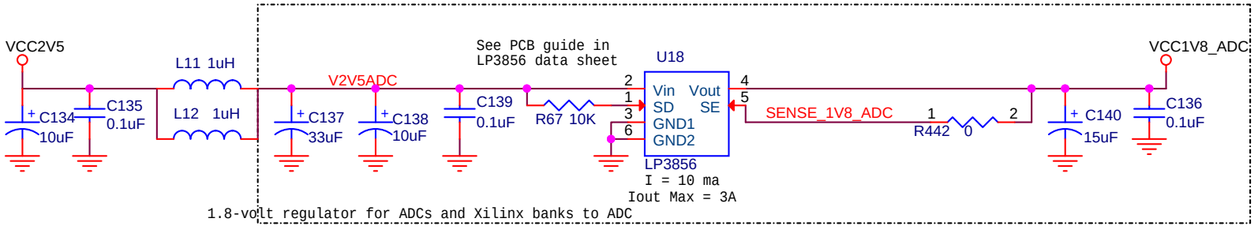
Title: ADC		
Size: B	Document Number: <Doc>	Rev: A
Date: Monday, November 03, 2014	Sheet 3 of 27	

Note 1: Components associated with ADC inputs IP1 and IP3 are on the top side of the board.
Components associated with IP2 and IP4 are on the bottom side of the board.
Note 2: Layout the board such that the attenuators can be replaced by 0402 zero ohm jumpers.



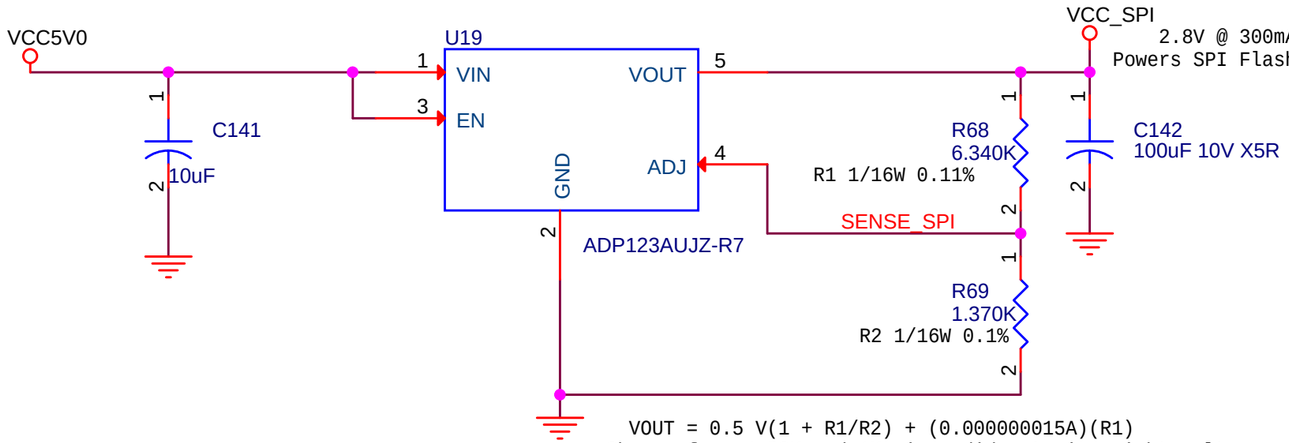






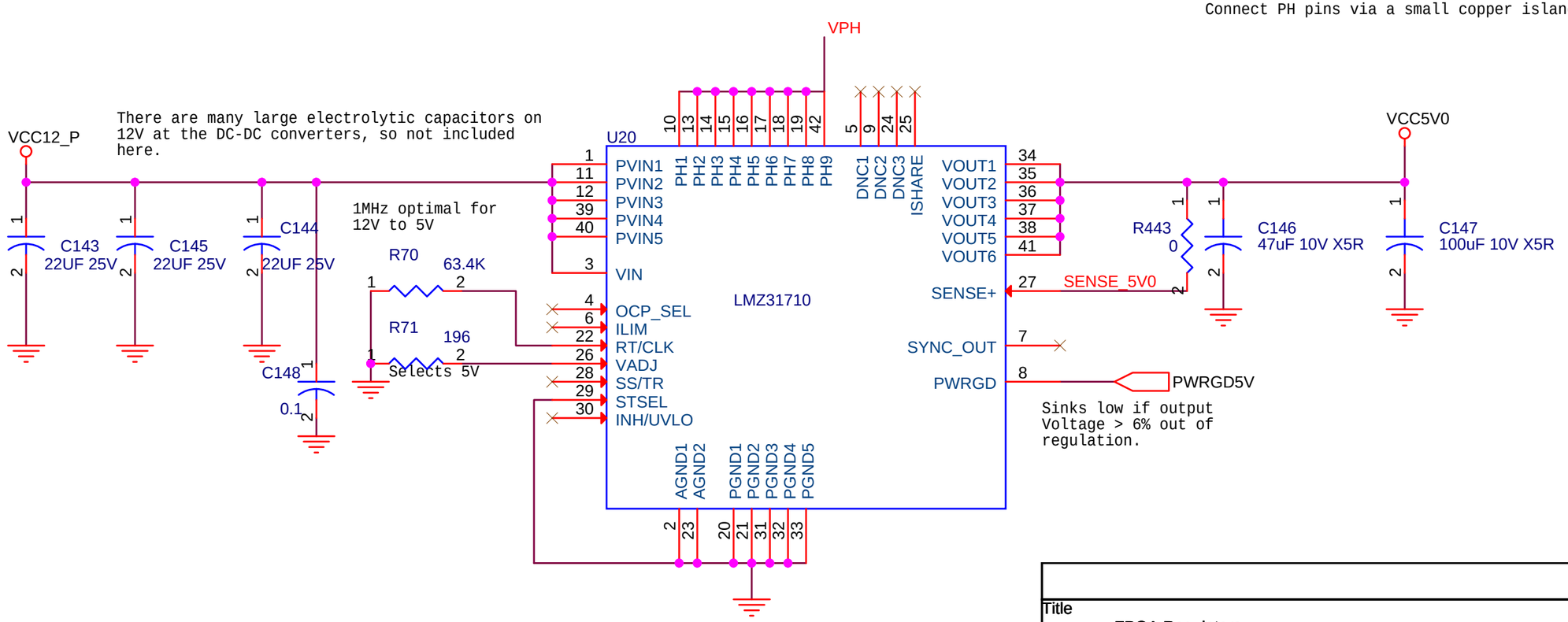
rev 2014-1-29: Add a pull-up to the synthesizer regulator.
rev 2014-1-3: change resistor value from 82K to 82.5K for HMC976s.
Change connection to HV input of both HMC976s from pull up common with the EN input to a separate DNP resistor.

Title: Analog Regulators		
Size: B	Document Number: <Doc>	Rev: -
Date: Monday, November 03, 2014	Sheet 5 of 27	



5V @ 10A Switching Power Supply
Powers Raspberry Pi, ADCs

Pins 41 and 42 are large pads in the center of the chip
Connect PH pins via a small copper island.



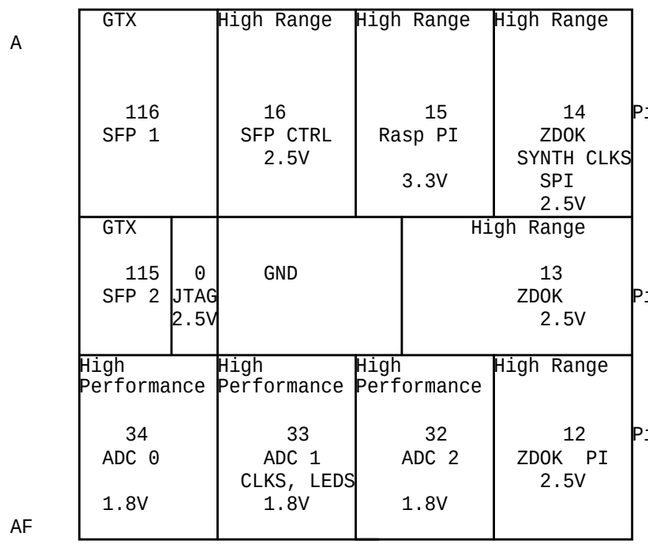
Title: FPGA Regulators		
Size: A	Document Number: <Doc>	Rev: -
Date: Monday, November 03, 2014	Sheet 6 of 27	

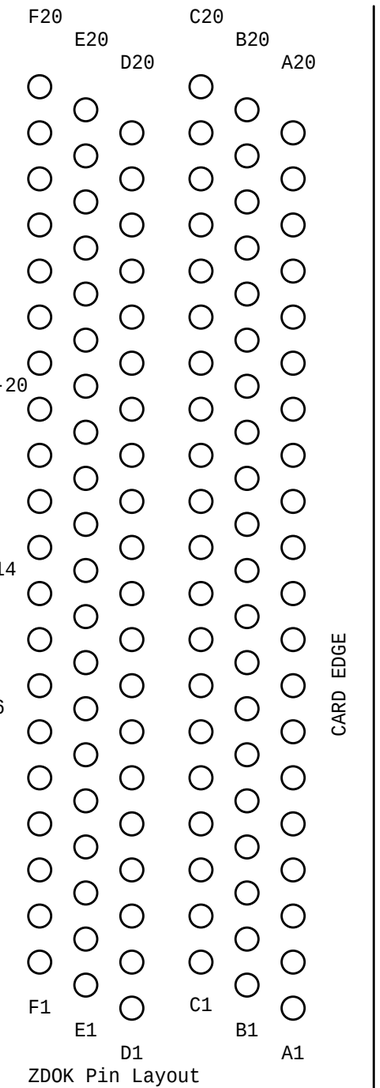
Changes for Second Version of the Board

Fix the footprint of the ZDOK connector so it doesn't have the offset pins.
Move J2, so it does not conflict with U24. Alternatively use a different connector, or reverse the wiring.
On the Xilinx silkscreen label pins from A1 to A26, not A1 to AF26.
Make the probe points on the back of the Xilinx not covered with laquer.
Change Voltage source of R61 from V5.0 to VADJ_FPGA to prevent an overvoltage to the Xilinx input.

TOP VIEW

After Changes



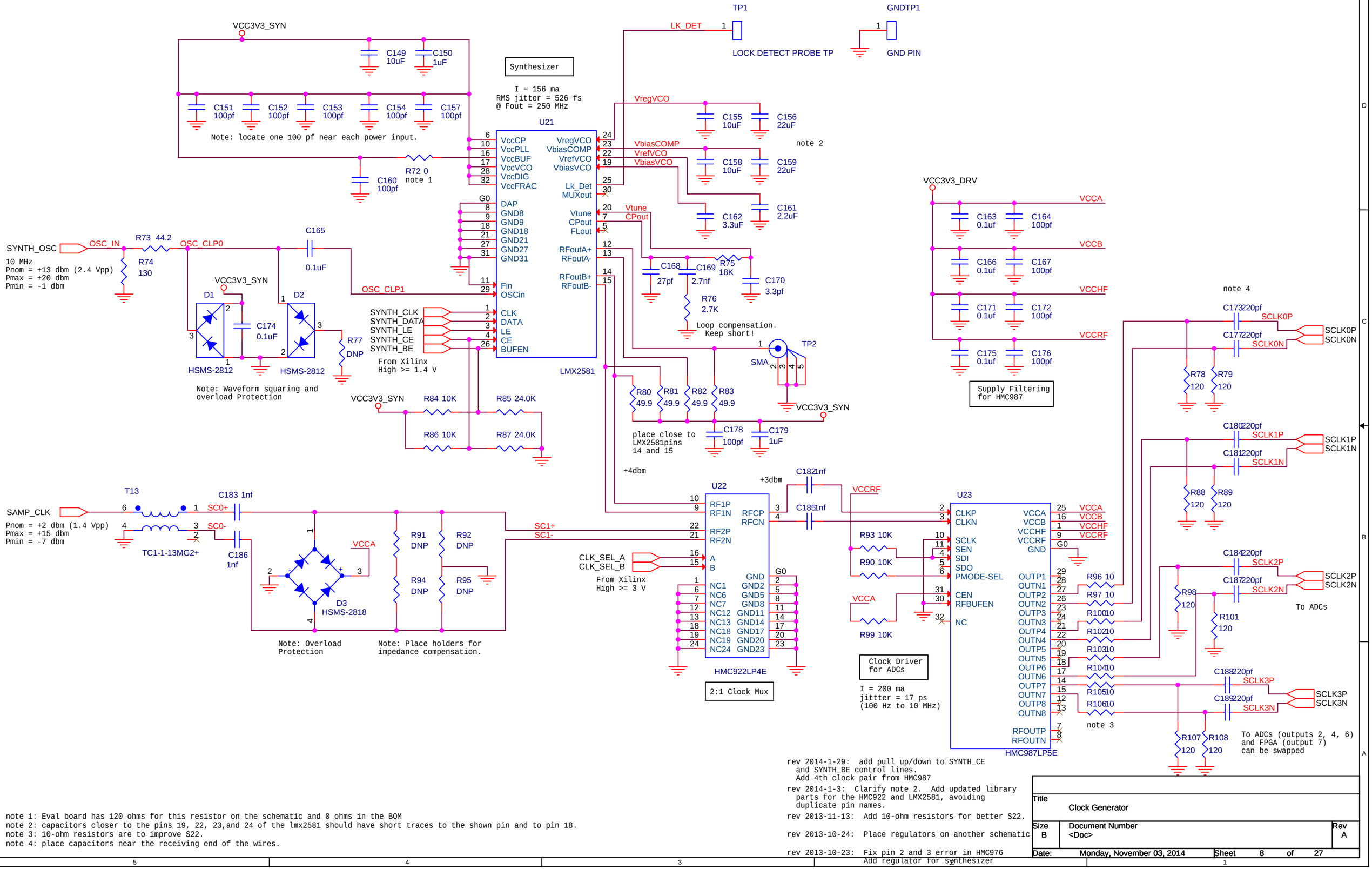


ZDOK Pin Layout

Changes

Change 33 to 1.8V and move ADC 1 to it.
Use only MRCC clocks for the ADCs
Move ZDOK to 16 to 14, SPI 14 to 15, and sfp ctrl to 15 to 16
Redistribute ZDOK pins.
Change ZDOK to 2.5V VCCO so can use LVDS-25 See UG471.
Change 100MHZ OSC to 200 MHZ. and eliminate termination resistor.
Replace 5V linear regulator with a DC-DC converter
Reduce number of TI Power Supply Controllers from 3 to 2
Remove C196 which wasn't connected to anything.
Add J9 as a test connector
Go to a single dual SFP+ Cage instead of two single cages.
Add a vertical USB J10 in parallel with horizontal USB J4
Change U43 from a 128 MByte to a 256 MByte Flash Memory.
Move the SPI pins to Bank 14 as on the Kintex Evaluation Board.
Hook up the FPGA_DONE and FPGA_PROG_B pins to the PI header thru level shifters
Add DNP bypass capacitors to allow for larger Xilinxs
Move PI signals to Bank 15 with a VCCO of 3.3V.
Move ZDOK clock lines to match the Roach II.
Change BOM to give options for 3 Xilinxs.
Add PU or PD to PD on the ADCs.
Add Heatsink to BOM
Add fan power receptacle with PWM
Arrange ADC Out pin parings so similar lengths.
Moved CLK_SEL_B and CLK_SEL_A to bank 15 which has the needed VCCO of 3.3V.
Install PD and DNP PU on PUDC_B pin.
Remove LK_DET TP3, since there were two test points.
Add net names V3V3SFPR, V3V3SFPT,V2V5ADC,V5V0DRV,V5V0SYN,V12PWRCTRL,V12D020W,V12D210W,V12D010W
Have ADC SCLK signals from 3.3V Voltage divider to terminate.
Move SYNTH_(CLK,DATA,LE,CE,BE) to 3.3V, then put series/parallel resistor on SYNTH_CLK.
Change Footprint of DNP resistors R114,R133,R135,R139 so they match the placed resistors.
Add zero Ohm resistors R442,R443 and make SENSE_... nets for sense lines.
Fix Pinout of U28,U46, & U47 so it matchs the BOM part number which is SN74AVC4T245RSVR
Fix typo to add VCC_3V3SYN to VCC3V3_SYN net.
Remove U27 and its resistors. Put in a 6pin vertical J3 and right angle jtag header J11. Move Xilinx Temperature to JP4.
Add ground test points GNDTP1-5.
Add a second ground pin to SMATP1 through 16.
Make Horizontal USB Connector J4 DNP so it won't short to the rail in a box. Also add a 0 Ohm DNP jumper.
 Deleted U25-E26 from net C20, and deleted U25-F25 from net C19.
To accomdate the new Pi B+, change PI2 from 26 to 40 pins & eliminate P8.

Title: BOARD LAYOUT		
Size: A	Document Number: <Doc>	Rev: <RevCode>
Date: Monday, November 03, 2014	Sheet 7 of 27	



note 1: Eval board has 120 ohms for this resistor on the schematic and 0 ohms in the BOM
note 2: capacitors closer to the pins 19, 22, 23,and 24 of the lmx2581 should have short traces to the shown pin and to pin 18.
note 3: 10-ohm resistors are to improve S22.
note 4: place capacitors near the receiving end of the wires.

rev 2014-1-29: add pull up/down to SYNTH_CE and SYNTH_BE control lines. Add 4th clock pair from HMC987

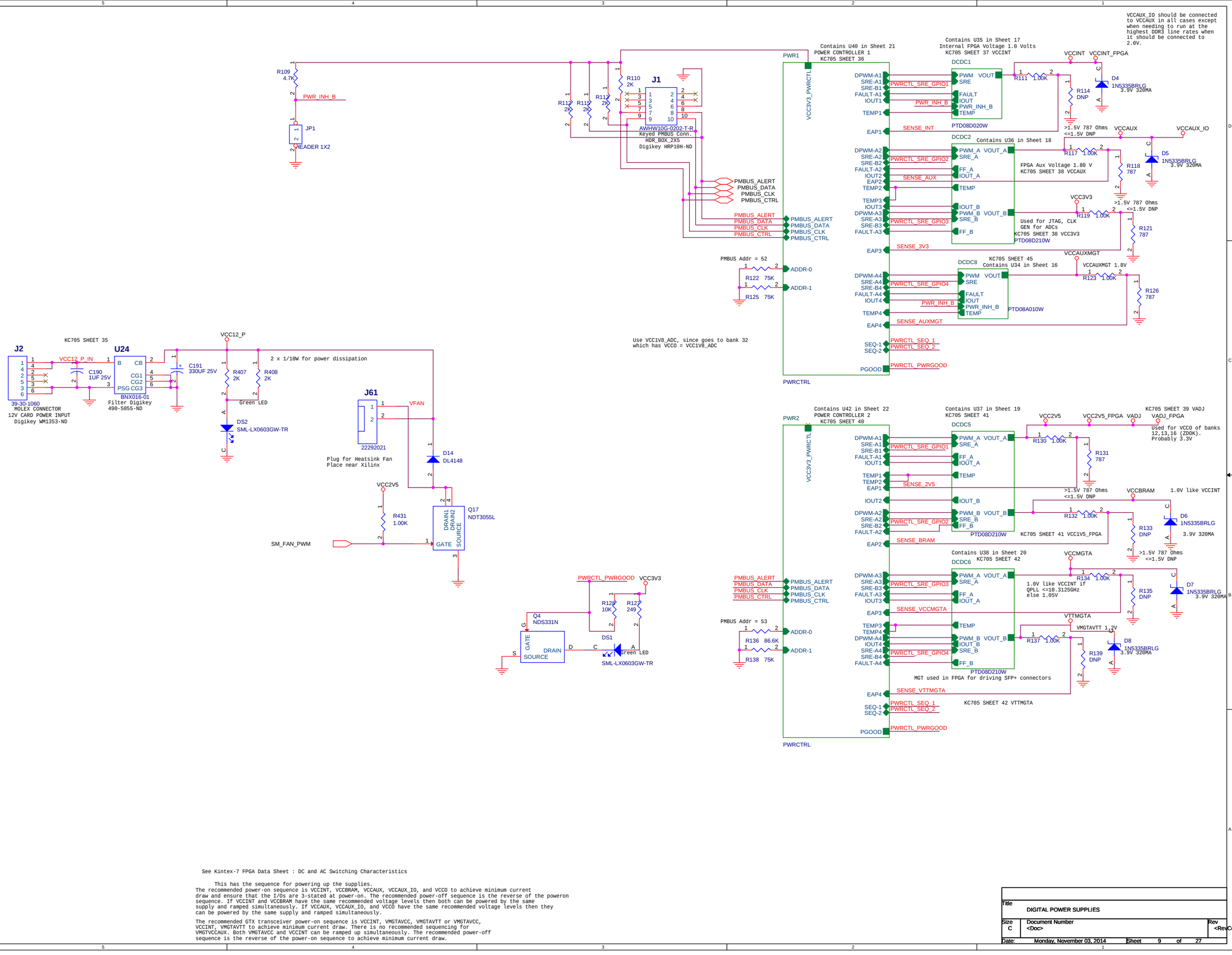
rev 2014-1-3: Clarify note 2. Add updated library parts for the HMC922 and LMX2581, avoiding duplicate pin names.

rev 2013-11-13: Add 10-ohm resistors for better S22.

rev 2013-10-24: Place regulators on another schematic

rev 2013-10-23: Fix pin 2 and 3 error in HMC976
Add regulator for synthesizer

Title: Clock Generator		
Size: B	Document Number: <Doc>	Rev: A
Date: Monday, November 03, 2014	Sheet 8 of 27	



See Kintex-7 FPGA Data Sheet : DC and AC Switching Characteristics

This has the sequence for powering up the supplies.
The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, VCCAUX_IO, and VCCO to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the poweron sequence. If VCCINT and VCCBRAM have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If VCCAUX, VCCAUX_IO, and VCCO have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

The recommended GTX transceiver power-on sequence is VCCINT, VMGTAVCC, VMGTAVTT or VMGTAVCC, VCCINT, VMGTAVTT to achieve minimum current draw. There is no recommended sequencing for VMGTVCCAUX. Both VMGTAVCC and VCCINT can be ramped up simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

Title: DIGITAL POWER SUPPLIES		
Size: C	Document Number: <Doc>	Rev: <RevCode>
Date: Monday, November 03, 2014	Sheet 9 of 27	

U25-7 High Performance

PMBUS_DATA_LS	V13	IO_0_VRN_32	IO_L9P_T1_DQS_32	Y15	
PMBUS_ALERT_LS	W13	IO_25_VRP_32	IO_L9N_T1_DQS_32	Y16	
	AB15	IO_L10N_T1_32	IO_L8P_T1_32	AC14	ADC2_OUT10
	AB14	IO_L10P_T1_32	IO_L8N_T1_32	AD14	ADC2_OUT11
	AA18	IO_L11N_T1_SRCC_32	IO_L7P_T1_32	AA14	ADC2_OUT8
PMBUS_CLK_LS	AA17	IO_L11P_T1_SRCC_32	IO_L7N_T1_32	AA15	ADC2_OUT9
LCLKN2	AC16	IO_L12N_T1_MRCC_32	IO_L6P_T0_32	AD16	
LCLKP2	AB16	IO_L12P_T1_MRCC_32	IO_L6N_T0_VREF_32	AE16	
FCLKN2	AD18	IO_L13N_T2_MRCC_32	IO_L5P_T0_32	AF19	ADC2_OUT6
FCLKP2	AC18	IO_L13P_T2_MRCC_32	IO_L5N_T0_32	AF20	ADC2_OUT7
	AC17	IO_L14N_T2_SRCC_32	IO_L4P_T0_32	AD15	ADC2_OUT2
	AB17	IO_L14P_T2_SRCC_32	IO_L4N_T0_32	AE15	ADC2_OUT3
	AE20	IO_L15N_T2_DQS_32	IO_L3P_T0_DQS_32	AE18	ADC2_OUT4
	AD20	IO_L15P_T2_DQS_32	IO_L3N_T0_DQS_32	AF18	ADC2_OUT5
ADC2_OUT15	AA20	IO_L16N_T2_32	IO_L2P_T0_32	AF14	ADC2_OUT0
ADC2_OUT14	AA19	IO_L16P_T2_32	IO_L2N_T0_32	AF15	ADC2_OUT1
	AD19	IO_L17N_T2_32	IO_L24P_T3_32	V14	CSN2
	AC19	IO_L17P_T2_32	IO_L24N_T3_32	W14	SDATA2
ADC2_OUT13	AB20	IO_L18N_T2_32	IO_L23P_T3_32	V18	
ADC2_OUT12	AB19	IO_L18P_T2_32	IO_L23N_T3_32	V19	RSTN2
	Y18	IO_L19N_T3_VREF_32	IO_L22P_T3_32	W15	PD2
	Y17	IO_L19P_T3_32	IO_L22N_T3_32	W16	
	AF17	IO_L1N_T0_32	IO_L21P_T3_DQS_32	W18	
	AE17	IO_L1P_T0_32	IO_L21N_T3_DQS_32	W19	
	V17	IO_L20N_T3_32	IO_L20P_T3_32	V16	

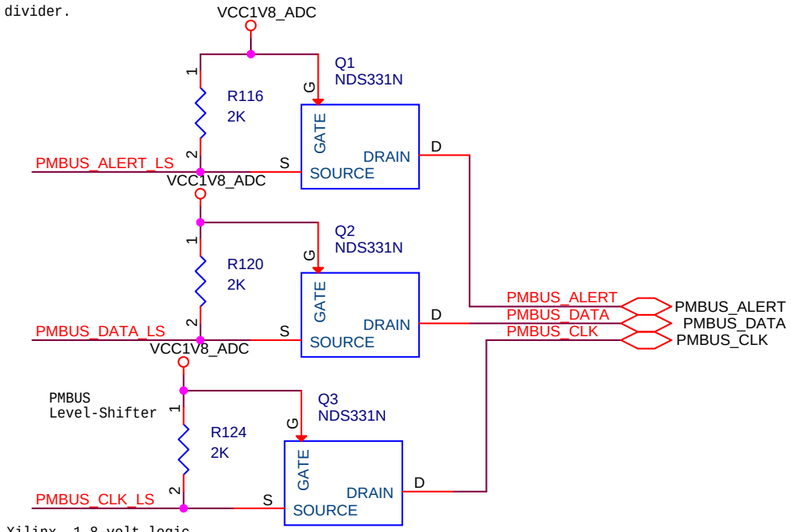
XC7K160T-FFG676

Used for DDR on sheet 3 of KC705
XC7K160T-2FFG676

Gets VCCO from VCCO1V8

ADC OUT PINS are placed so that pairs of differential pairs are close to each other for timing purposes.

From 3.3V with series/parallel divider.



U25-8 High Performance

U9		IO_0_VRN_33	IO_L9P_T1_DQS_33	AC8	ADC1_OUT14
V12		IO_25_VRP_33	IO_L9N_T1_DQS_33	AD8	ADC1_OUT15
AC7		IO_L10N_T1_33	IO_L8P_T1_33	AA8	ADC1_OUT12
AB7		IO_L10P_T1_33	IO_L8N_T1_33	AA7	ADC1_OUT13
AB9		IO_L11N_T1_SRCC_33	IO_L7P_T1_33	AE7	
AA9		IO_L11P_T1_SRCC_33	IO_L7N_T1_33	AF7	
AD9	LCLKN1	IO_L12N_T1_MRCC_33	IO_L6P_T0_33	V9	
AC9	LCLKP1	IO_L12P_T1_MRCC_33	IO_L6N_T0_VREF_33	W8	
AC11	FCLKN1	IO_L13N_T2_MRCC_33	IO_L5P_T0_33	Y11	ADC1_OUT6
AB11	FCLKP1	IO_L13P_T2_MRCC_33	IO_L5N_T0_33	Y10	ADC1_OUT7
AB10		IO_L14N_T2_SRCC_33	IO_L4P_T0_33	Y8	ADC1_OUT4
AA10		IO_L14P_T2_SRCC_33	IO_L4N_T0_33	Y7	ADC1_OUT5
AC12	ADC1_OUT9	IO_L15N_T2_DQS_33	IO_L3P_T0_DQS_33	W10	ADC1_OUT2
AB12	ADC1_OUT8	IO_L15P_T2_DQS_33	IO_L3N_T0_DQS_33	W9	ADC1_OUT3
AA12	ADC1_OUT11	IO_L16N_T2_33	IO_L2P_T0_33	V8	ADC1_OUT0
AA13	ADC1_OUT10	IO_L16P_T2_33	IO_L2N_T0_33	V7	ADC1_OUT1
AD13		IO_L17N_T2_33	IO_L24P_T3_33	AF10	CSN1
AC13		IO_L17P_T2_33	IO_L24N_T3_33	AF9	SDATA1
Y12		IO_L18N_T2_33	IO_L23P_T3_33	AE13	
Y13		IO_L18P_T2_33	IO_L23N_T3_33	AF13	RSTN1
AE11		IO_L19N_T3_VREF_33	IO_L22P_T3_33	AE8	PD1
AD11		IO_L19P_T3_33	IO_L22N_T3_33	AF8	
W11		IO_L1N_T0_33	IO_L21P_T3_DQS_33	AE12	
V11		IO_L1P_T0_33	IO_L21N_T3_DQS_33	AF12	
AE10		IO_L20N_T3_33	IO_L20P_T3_33	AD10	

XC7K160T-FFG676

See Sheet 7 of KC705

Gets VCCO from VCCO1V8

U25-9 High Performance

U4		IO_0_VRN_34	IO_L9P_T1_DQS_34	AB1	
T7		IO_25_VRP_34	IO_L9N_T1_DQS_34	AC1	
Y1		IO_L10N_T1_34	IO_L8P_T1_34	V2	ADC0_OUT0
W1		IO_L10P_T1_34	IO_L8N_T1_34	V1	ADC0_OUT1
AC2		IO_L11N_T1_SRCC_34	IO_L7P_T1_34	Y3	ADC0_OUT10
AB2		IO_L11P_T1_SRCC_34	IO_L7N_T1_34	Y2	ADC0_OUT11
AA2	LCLKN0	IO_L12N_T1_MRCC_34	IO_L6P_T0_34	V4	
AA3	LCLKP0	IO_L12P_T1_MRCC_34	IO_L6N_T0_VREF_34	W4	
AB4	FCLKN0	IO_L13N_T2_MRCC_34	IO_L5P_T0_34	U7	ADC0_OUT6
AA4	FCLKP0	IO_L13P_T2_MRCC_34	IO_L5N_T0_34	V6	ADC0_OUT7
AC3		IO_L14N_T2_SRCC_34	IO_L4P_T0_34	V3	ADC0_OUT8
AC4		IO_L14P_T2_SRCC_34	IO_L4N_T0_34	W3	ADC0_OUT9
AB5		IO_L15N_T2_DQS_34	IO_L3P_T0_DQS_34	W6	ADC0_OUT4
AA5		IO_L15P_T2_DQS_34	IO_L3N_T0_DQS_34	W5	ADC0_OUT5
AC6		IO_L16N_T2_34	IO_L2P_T0_34	U2	ADC0_OUT2
AB6		IO_L16P_T2_34	IO_L2N_T0_34	U1	ADC0_OUT3
Y5		IO_L17N_T2_34	IO_L24P_T3_34	AF3	CSN0
Y6		IO_L17P_T2_34	IO_L24N_T3_34	AF2	SDATA0
AD5	ADC0_OUT13	IO_L18N_T2_34	IO_L23P_T3_34	AE6	
AD6	ADC0_OUT12	IO_L18P_T2_34	IO_L23N_T3_34	AE5	RSTN0
AD3	ADC0_OUT15	IO_L19N_T3_VREF_34	IO_L22P_T3_34	AE3	PD0
AD4	ADC0_OUT14	IO_L19P_T3_34	IO_L22N_T3_34	AE2	
U5		IO_L1N_T0_34	IO_L21P_T3_DQS_34	AF5	
U6		IO_L1P_T0_34	IO_L21N_T3_DQS_34	AF4	
AE1		IO_L20N_T3_34	IO_L20P_T3_34	AD1	

XC7K160T-FFG676

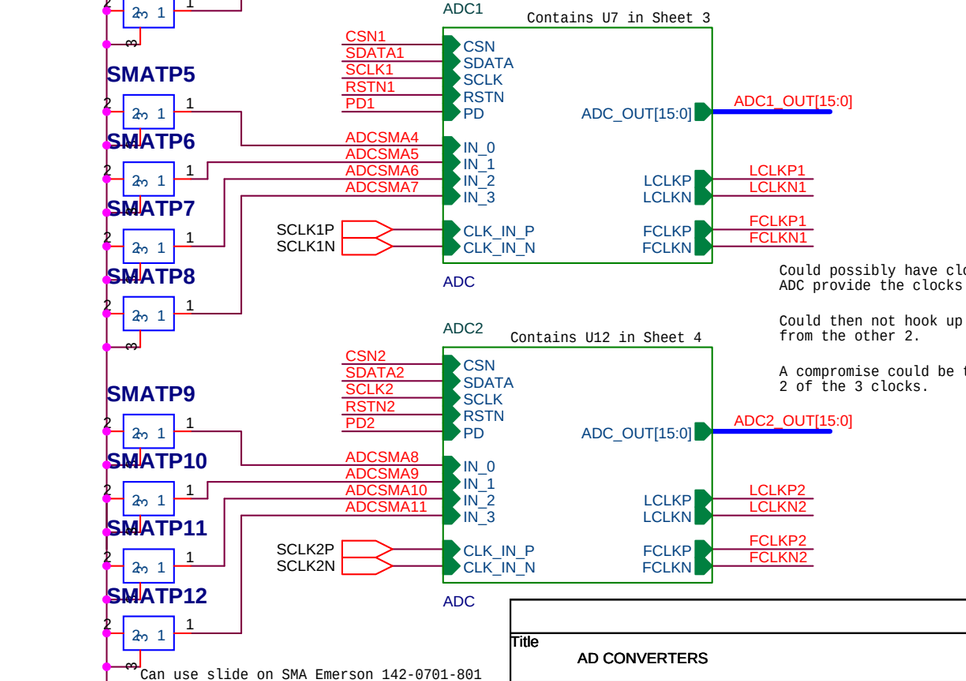
SRCC are single region clocks
MRCC are multi region clocks

See UG471 Series_Select IO for info on SERDES clocking.

See Sheet 8 of KC705

Gets VCCO from VCCO1V8

From Xilinx, 1.8-volt logic

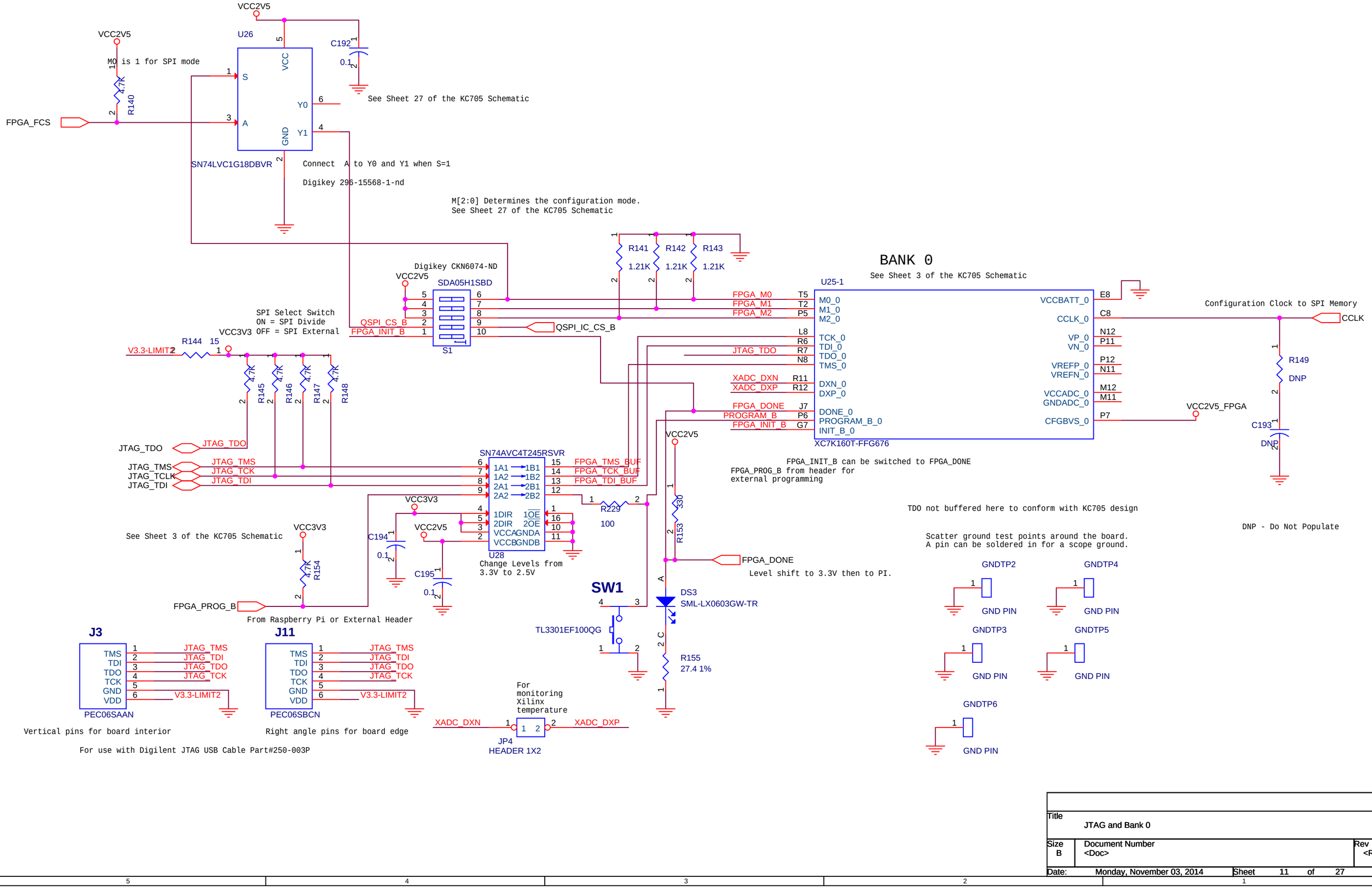


Could possibly have clocks from one ADC provide the clocks for all 3.

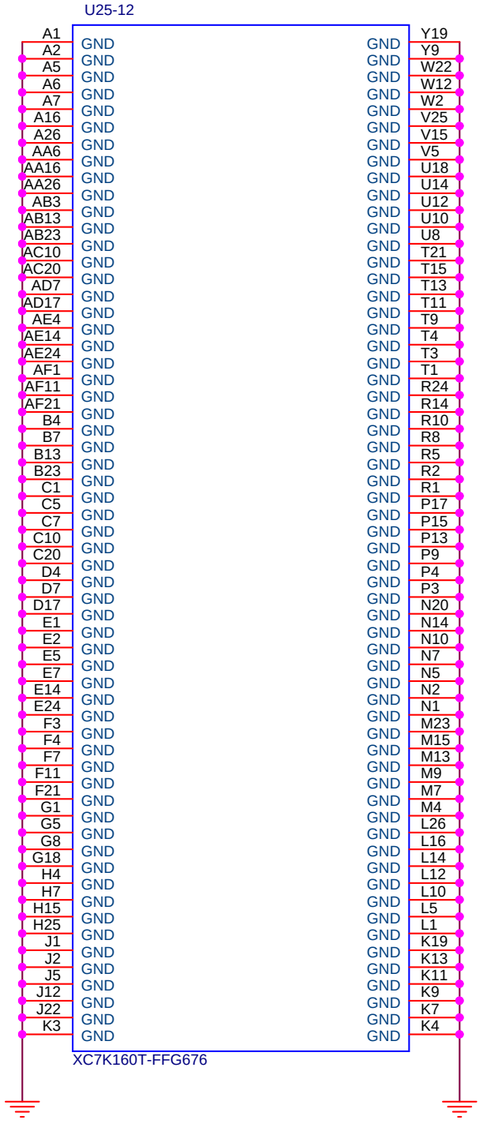
Could then not hook up the clocks from the other 2.

A compromise could be to hook up 2 of the 3 clocks.

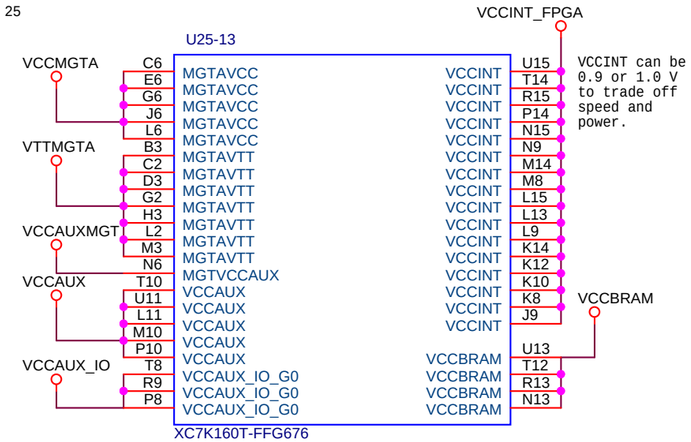
Title	AD CONVERTERS		
Size B	Document Number <Doc>		Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 10	of 27	



Title	JTAG and Bank 0	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 11 of 27	



See KC705 Sheet 25

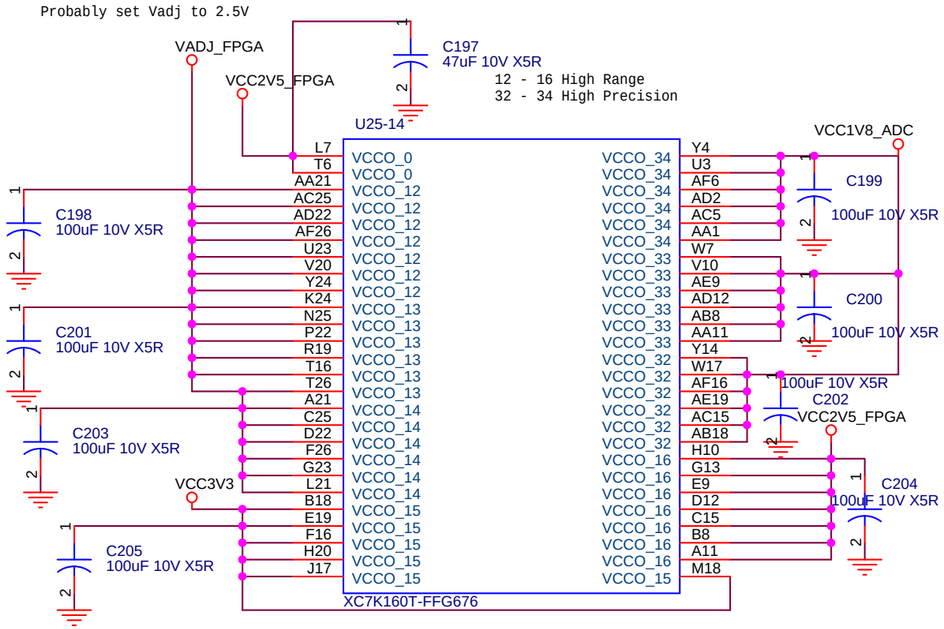


VCCINT_FPGA

VCCINT can be 0.9 or 1.0 V to trade off speed and power.

VCCBRAM

Probably set Vadj to 2.5V



See Sheet 12 of KC705

HR I/O Bank has 3.465 VCCO max
HP I/O Bank has 1.89 VCCO max

VCCINT_FPGA

VCCINT 4.7uF: 0 for 160T, 5 for 325T, 10 for 410T Xilinx

C403 DNP, C404 DNP, C405 DNP, C406 DNP, C407 DNP, C408 DNP, C409 DNP, C410 DNP, C411 DNP, C412 DNP

VCCBRAM 330 uF: have 0 for 160T, 0 for 325T, 1 for 410T Xilinx

VCCBRAM

C413 DNP

See the SNAP board design guide for a discussion of the Kintex Decoupling Capacitors.

VCCINT can be 0.9 or 1.0 V to trade off speed and power.

Per UG483, the xc7k160t ffg676requires the following bypass capacitors:
See UG483 for layout guidlines

VCCINT_FPGA

VCCINT 330 uF: have 2 for 160T, 3 for 325T, 5 for 410T Xilinx

C400 DNP, C401 DNP, C402 DNP, C206 330uF 2.5V, C207 330uF 2.5V

T520V337M2R5ATE025
Digikey 399-4105-1-ND

VCCBRAM 100 uF: have 1 for 160T, 2 for 325T, 0 for 410T Xilinx

VCCBRAM

C208 100uF 10V X5R DNP, C414

GRM32ER60J107ME20L

VCCBRAM

VCCBRAM 4.7 uF: have 3 for 160T, 5 for 325T, 9 for 410T Xilinx

C209 4.7uF, C210 4.7uF, C211 4.7uF, C415 DNP, C416 DNP, C417 DNP, C418 DNP, C419 DNP, C420 DNP

GRM155R60J475ME47D

VCCAUX

C212 47uF 10V X5R, C213 47uF 10V X5R

VCCAUX_IO

Per Group see UG471 and UG475

Bank 0

C214 47uF 10V X5R

GRM43ER61A476KE19L

Title	FPGA POWER	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 12 of 27	

Sheet 15
OSCILLATORS
SYSCLK_N
SYSCLK_P
ETHCLK_N
ETHCLK_P
OSCILLATORS

CLK200MHZ_N
CLK200MHZ_P
ETHCLK_N
ETHCLK_P

Sheet 26
SWITCHES
SW0
SW1
SW2
SW3
LED0
LED1
LED2
LED3
LED4
LED5
OUT1PPS
FPGA_DONE
DONE33V
SWITCHES

FPGA_DONE

U25-6
HIGH RANGE
XC7K160T-FFG676

USB_TX
USB_CTS
USB_RTS
USB_RX

DONE33V

VCCO is VCC2V5

TX_DISABLE0
TX_DISABLE1

SFP1
Contains P1 in Sheet 24
IIC_SCL_MAIN
IIC_SDA_MAIN
SFP_TX_DISABLE
SFP_RX_P
SFP_RX_N
SFP_TX_P
SFP_TX_N
SFPCONN

SFP2
Contains P2 in Sheet 25
SFPCONN

Leave Unused REFCLKs unconnected
GND
U25-11
See Sheet 9 of the KC705
MGTREFCLK0N_116
MGTREFCLK0P_116
MGTREFCLK1N_116
MGTREFCLK1P_116
MGTXRXN0_116
MGTXRXN1_116
MGTXRXN2_116
MGTXRXN3_116
MGTXRXP0_116
MGTXRXP1_116
MGTXTXP3_116
MGTXTXP2_116
MGTXTXP1_116
MGTXTXP0_116
MGTXTXN3_116
MGTXTXN2_116
MGTXTXN1_116
MGTXTXN0_116
MGTXRXP3_116
MGTXRXP2_116
XC7K160T-FFG676

See UG476 7 Series FPGAs GTX/GTH Tranceivers User Guide
1 GBE high speed traces require special layout care.
See UG483 - 7 Series FPGAs PCB Design and Pin Planning Guide
VCCMGTA
R156 100
U25-10
See Sheet 9 of the KC705
MGTAVTTRCAL_115
MGTREFCLK0N_115
MGTREFCLK0P_115
MGTREFCLK1N_115
MGTREFCLK1P_115
MGTRREF_115
MGTXRXN0_115
MGTXRXN1_115
MGTXRXN2_115
MGTXRXN3_115
MGTXRXP0_115
MGTXTXP3_115
MGTXTXP2_115
MGTXTXP1_115
MGTXTXP0_115
MGTXTXN3_115
MGTXTXN2_115
MGTXTXN1_115
MGTXTXN0_115
MGTXRXP3_115
MGTXRXP2_115
MGTXRXP1_115
XC7K160T-FFG676

USB_SHIELD
J10
CONN_USB_MINI_B-VERT
TE Connectivity 1734753-1
Digikey A107790-ND
R460 DNP
C215 DNP
C216 0.1
HZ0805E601R-10
Digikey 240-2399-2--ND
L13 FERRITE-600
USB_GND
X1
SP0503BAHTG
Transient Surpressor
Digikey F2715CT-ND
J4
DNP
Molex 548190589 (horizontal)
Digikey WM3895CT-ND
USB_D_P
USB_D_N
VCC2V5
C217 0.1
C218 1UF 25V
C219 0.1
R157 4.7K
VBUS_USB
L14
FERRITE-600
HZ0805E601R-10
Digikey 240-2399-2--ND
C220 0.1
C221 1UF 25V
VBUS
USB BUS POWERED
Digikey 336-1164-ND

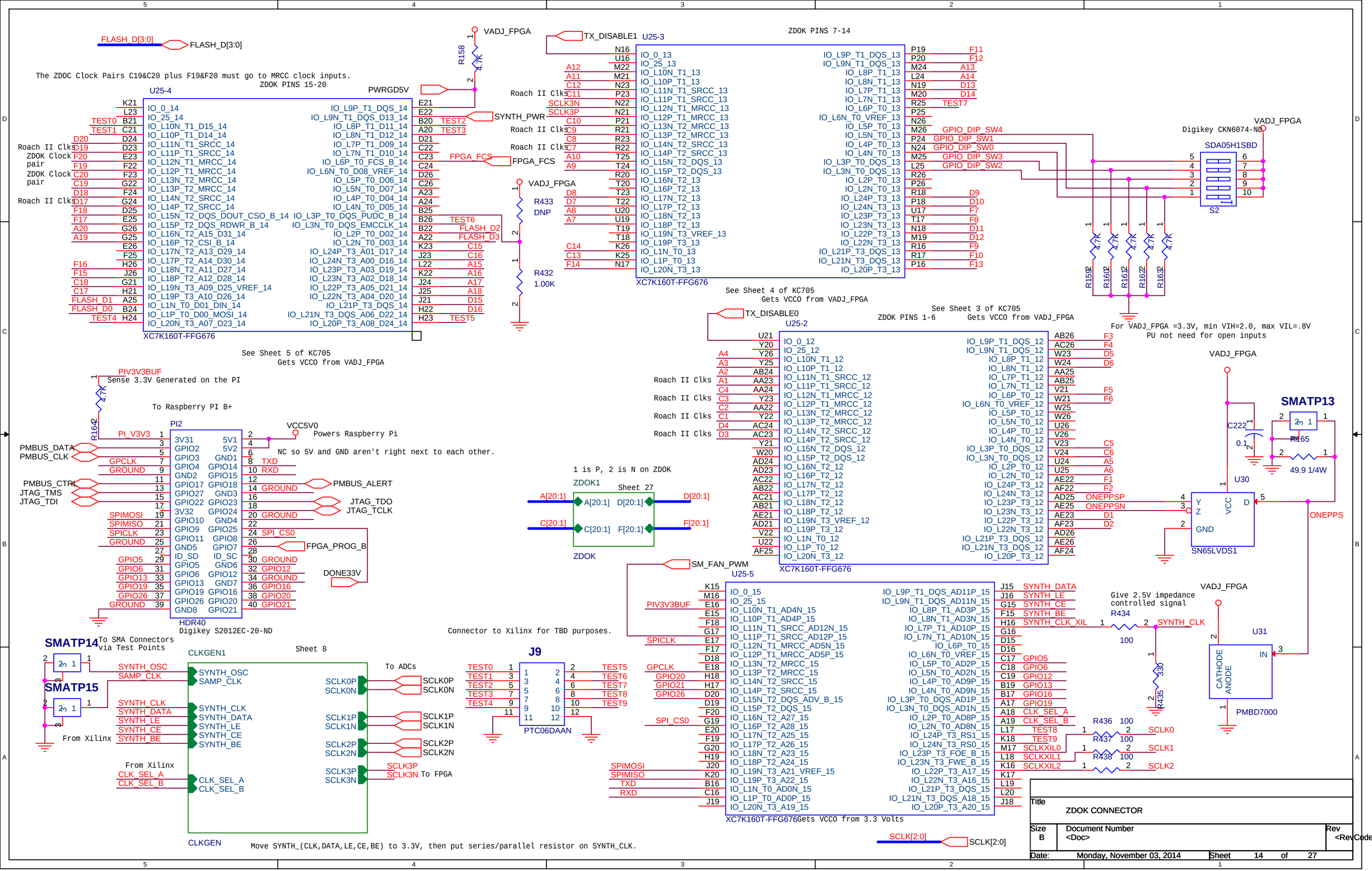
U29
CP2103-GM
CNR_GND
RI
GND
D+
D-
VIO
VDD
REGIN
VBUS
RST_B
NC1
SUSPEND_B
SUSPEND
NC2
NC3
CTR_GND
DCD
DTR
DSR
TXD
RXD
RTS
CTS
NC6
NC5
GPIO0
GPIO1
GPIO2
GPIO3
NC4

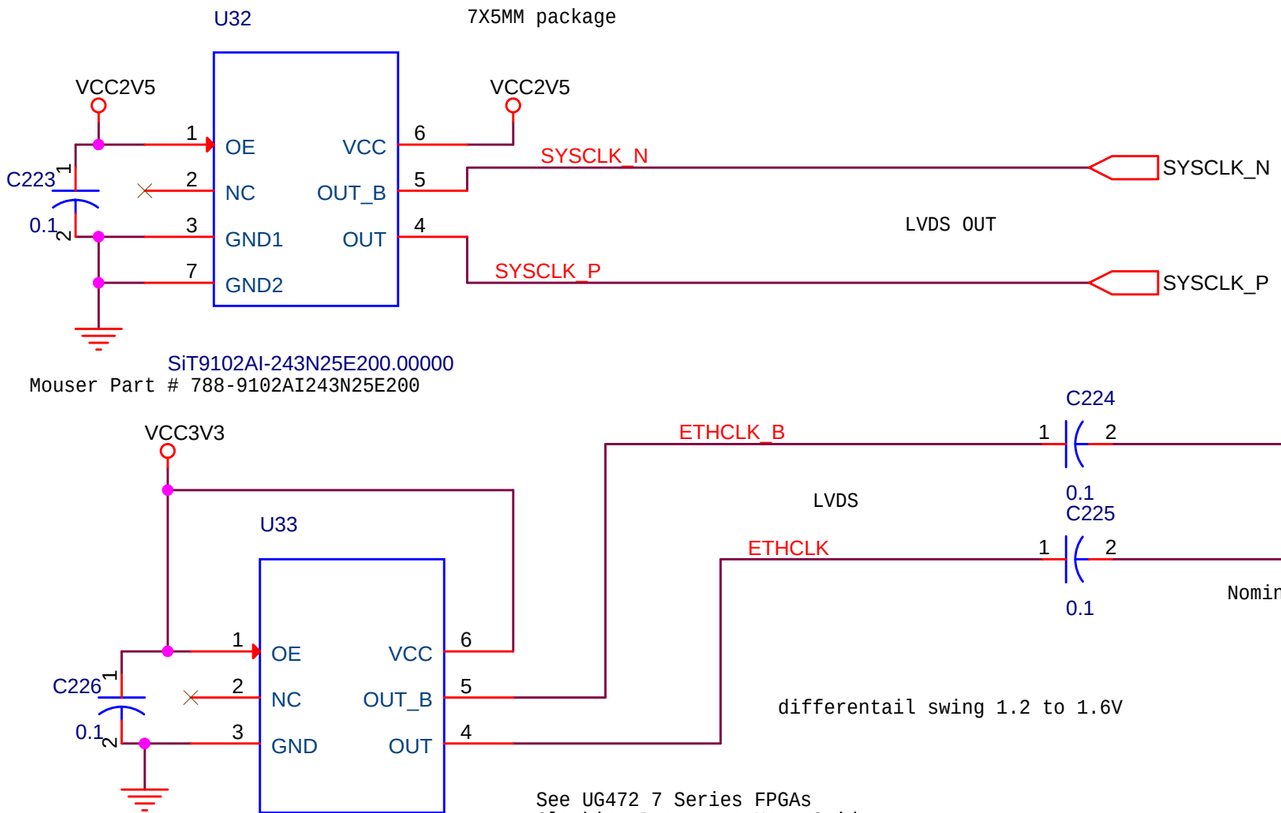
USB_TX
USB_RX
USB_RTS
USB_CTS
To Bank 15 above
See Sheet 27 of the KC705

If desired for a card cage J4, a right angle USB
can be installed in parallel.
If used, also install a zero Ohm resistor for 1206 R460

J4 is DNP if the card is in the box, since the shield pins
would short out to the ground rail.

Title	SFP+ Connector and Cage	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 13 of 27	


FLASH_D[3:0]
FLASH_D[3:0]
The ZDOC Clock Pairs C19&C20 plus F19&F20 must go to MRCC clock inputs.
ZDOK PINS 15-20
U25-4
PWRGD5V
R158
4.7K
VADJ_FPGA
SYNTH_PWR
FPGA_FCS
FPGA_FCS
R433
DNP
R432
1.00K
XC7K160T-FFG676
See Sheet 5 of KC705
Gets VCCO from VADJ_FPGA
TX_DISABLE1
U25-3
ZDOK PINS 7-14
XC7K160T-FFG676
See Sheet 4 of KC705
Gets VCCO from VADJ_FPGA
TX_DISABLE0
U25-2
See Sheet 3 of KC705
ZDOK PINS 1-6
Gets VCCO from VADJ_FPGA
XC7K160T-FFG676
Digikey CKN6074-ND
SDA05H1SBD
S2
R159
R160
R161
R162
R163
4.7K
For VADJ_FPGA =3.3V, min VIH=2.0, max VIL=.8V
PU not need for open inputs
PIV3V3BUF
Sense 3.3V Generated on the PI
R164
4.7K
To Raspberry PI B+
PI2
PI_V3V3
VCC5V0
Powers Raspberry Pi
NC so 5V and GND aren't right next to each other.
PMBUS_DATA
PMBUS_CLK
PMBUS_CTRL
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TCLK
PMBUS_ALERT
FPGA_PROG_B
DONE33V
HDR40
Digikey S2012EC-20-ND
1 is P, 2 is N on ZDOK
ZDOK1
Sheet 27
ZDOK
SM_FAN_PWM
U25-5
XC7K160T-FFG676Gets VCCO from 3.3 Volts
SMATP13
SMATP14
SMATP15
To SMA Connectors
via Test Points
From Xilinx
From Xilinx
CLKGEN1
Sheet 8
CLKGEN
To ADCs
To FPGA
Connector to Xilinx for TBD purposes.
J9
PTC06DAAN
Move SYNTH_(CLK,DATA,LE,CE,BE) to 3.3V, then put series/parallel resistor on SYNTH_CLK.
SCLK[2:0]
SCLK[2:0]
VADJ_FPGA
C222
0.1
R165
49.9 1/4W
U30
SN65LVDS1
ONEPPS
Give 2.5V impedance
controlled signal
R434
100
330
R435
U31
PMBD7000
R436
R437
R438
SCLK0
SCLK1
SCLK2
Title
ZDOK CONNECTOR
Size
B
Document Number
<Doc>
Rev
<RevCode
Date:
Monday, November 03, 2014
Sheet
14
of
27



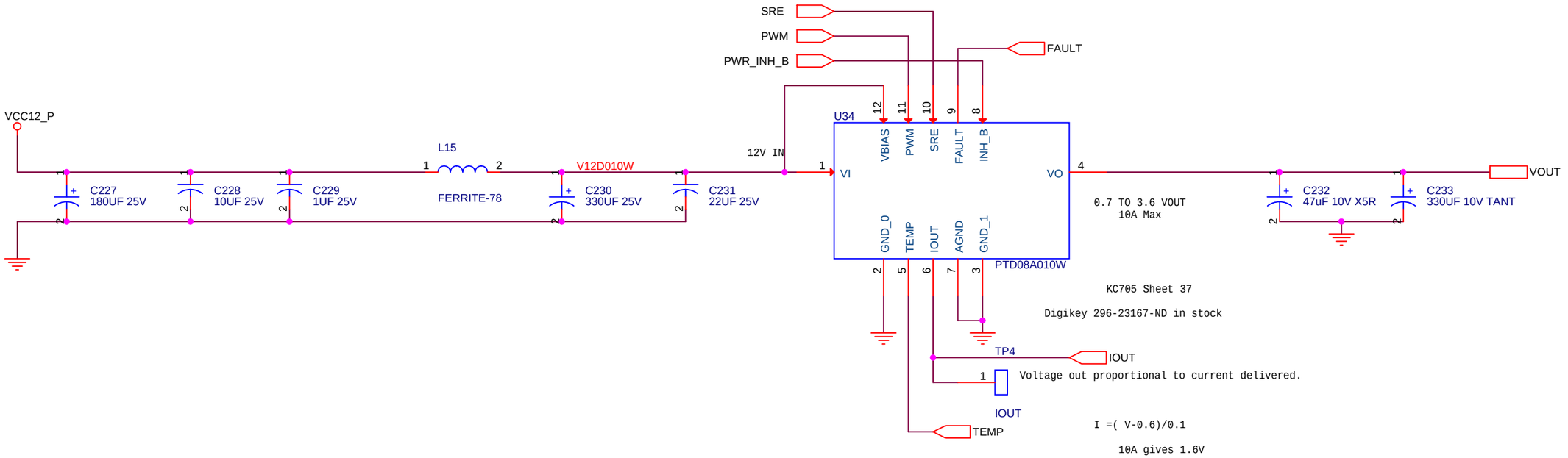
SiT9102AI-243N25E200.00000
Mouser Part # 788-9102AI243N25E200

See UG472 7 Series FPGAs
Clocking Resources User Guide

SiT9120AI-2D3-33E156.250000T
156.25 MHz 3.3V 50ppm
Mouser Part # 788-9120AI2D333E1562

Note these oscillators are different footprints, voltages, and outputs.

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 15 of 27	



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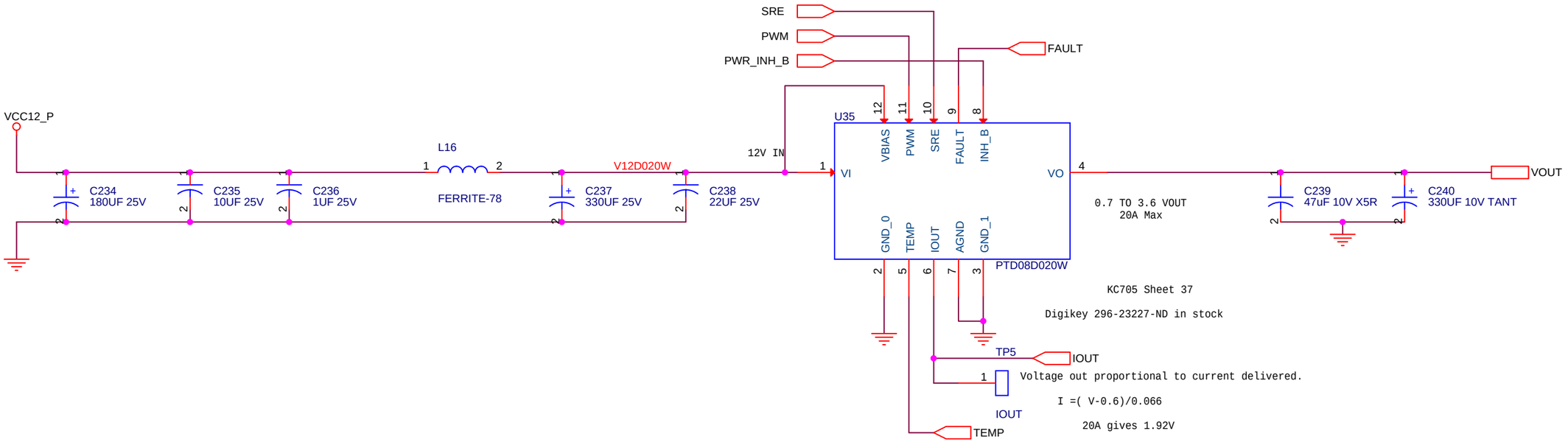
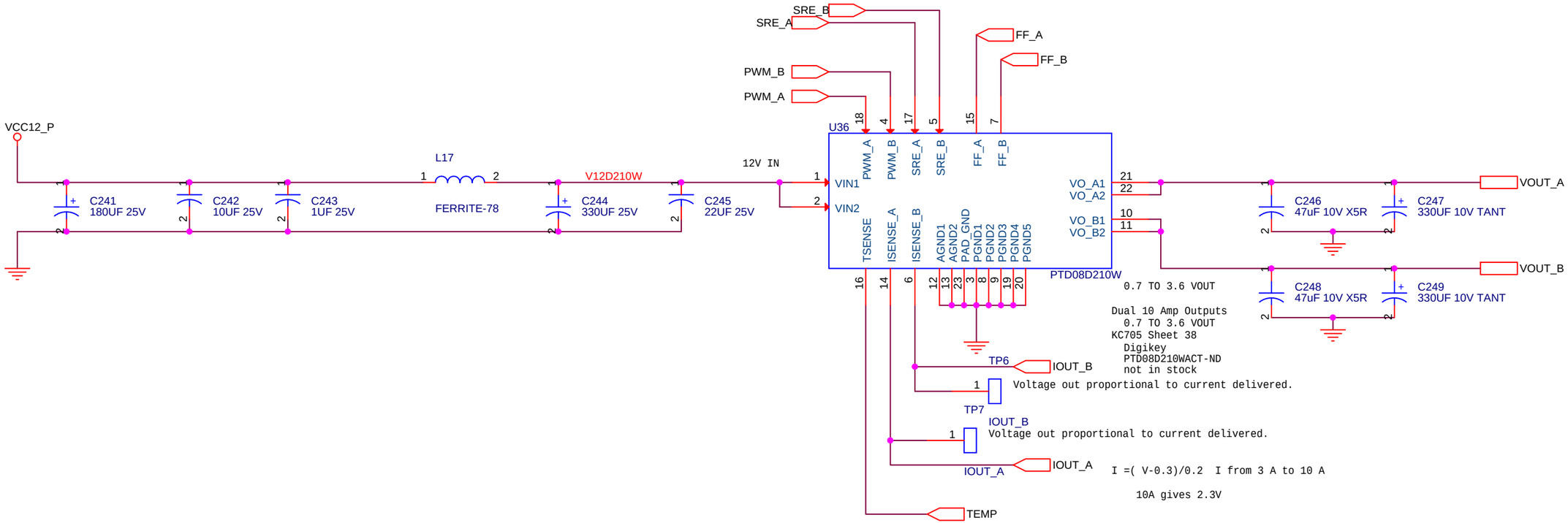
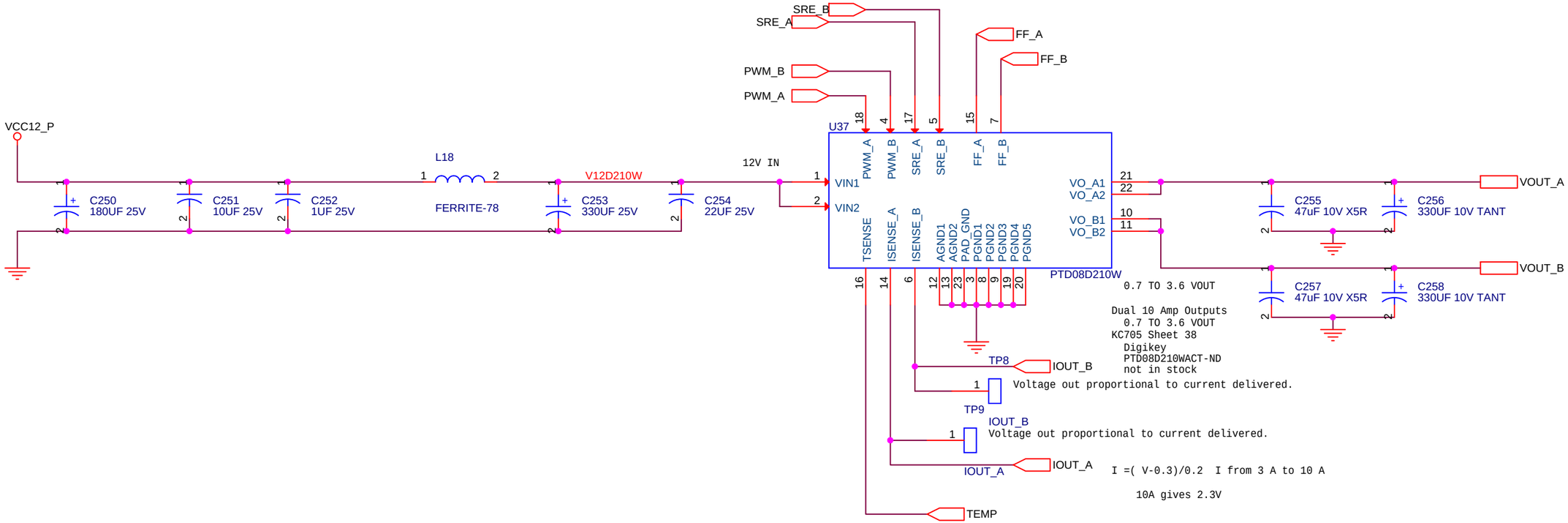
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 16 of 27	



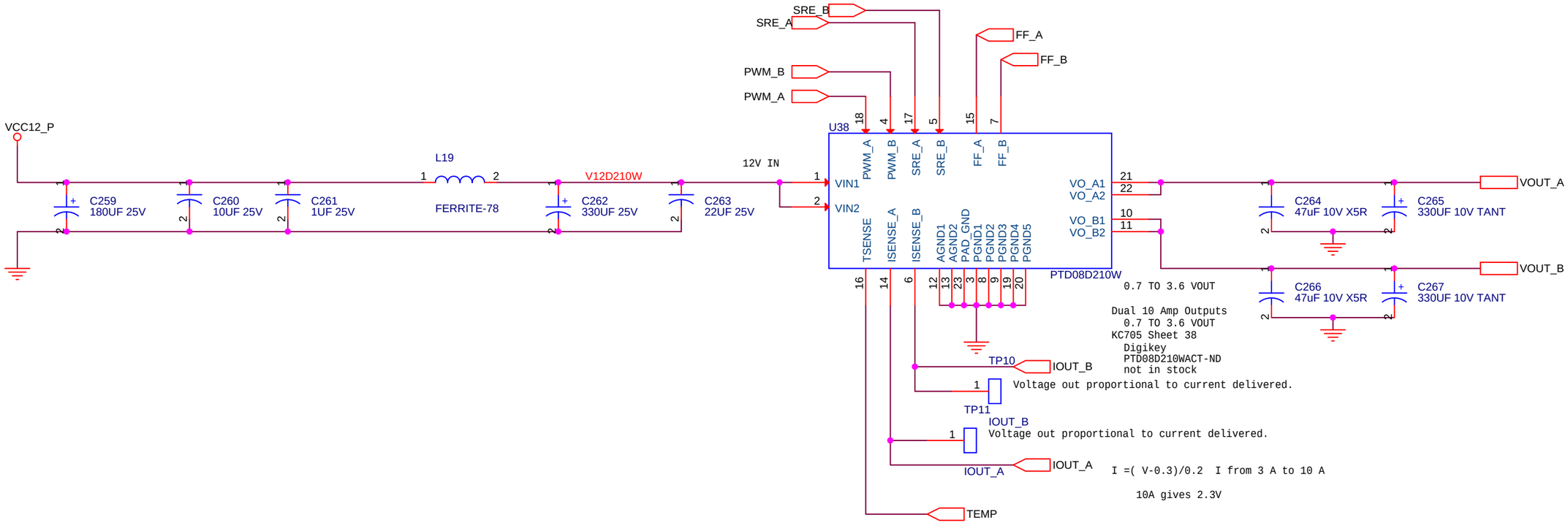
Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 17 of 27	



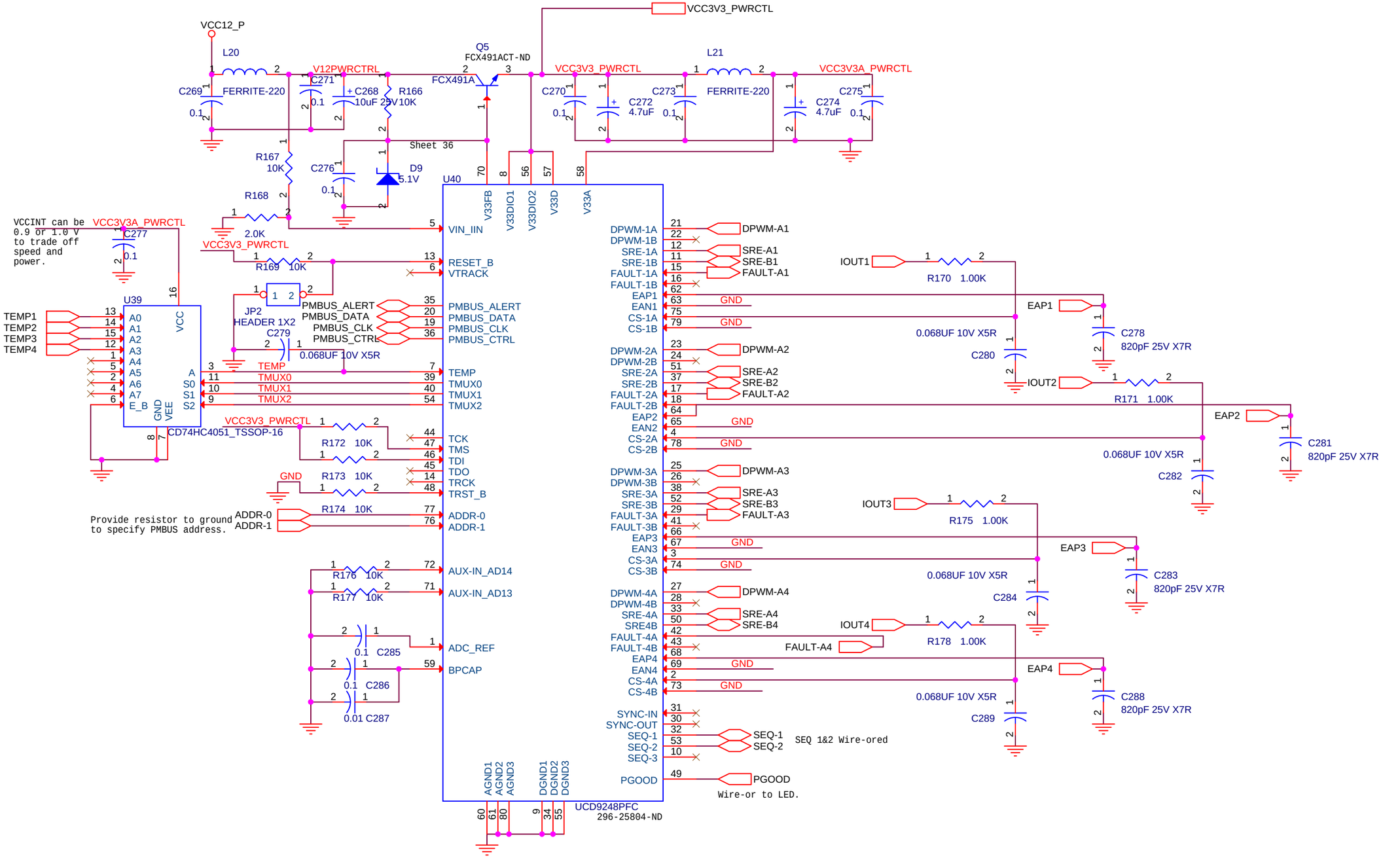
Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 18 of 27	



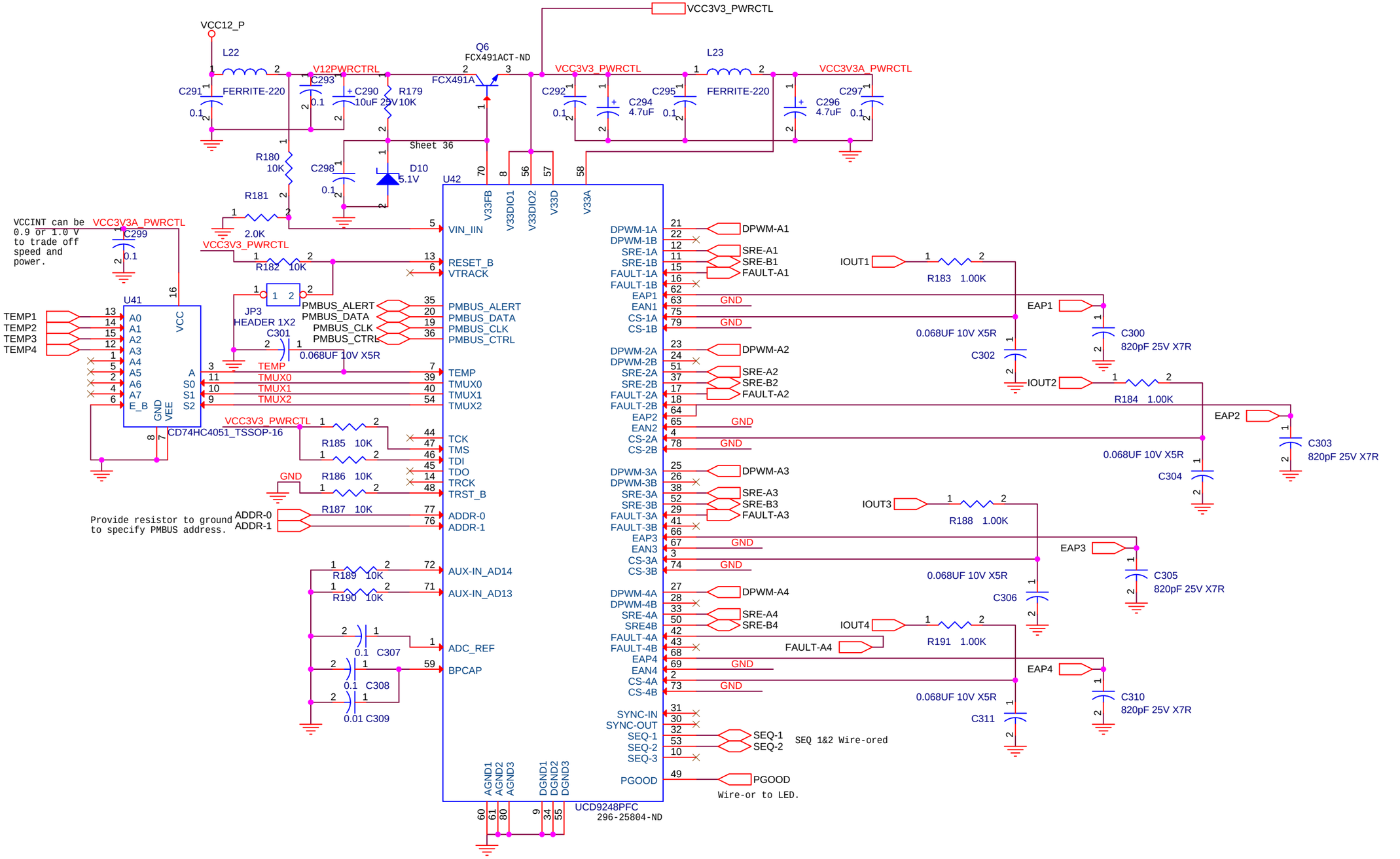
Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 19 of 27	



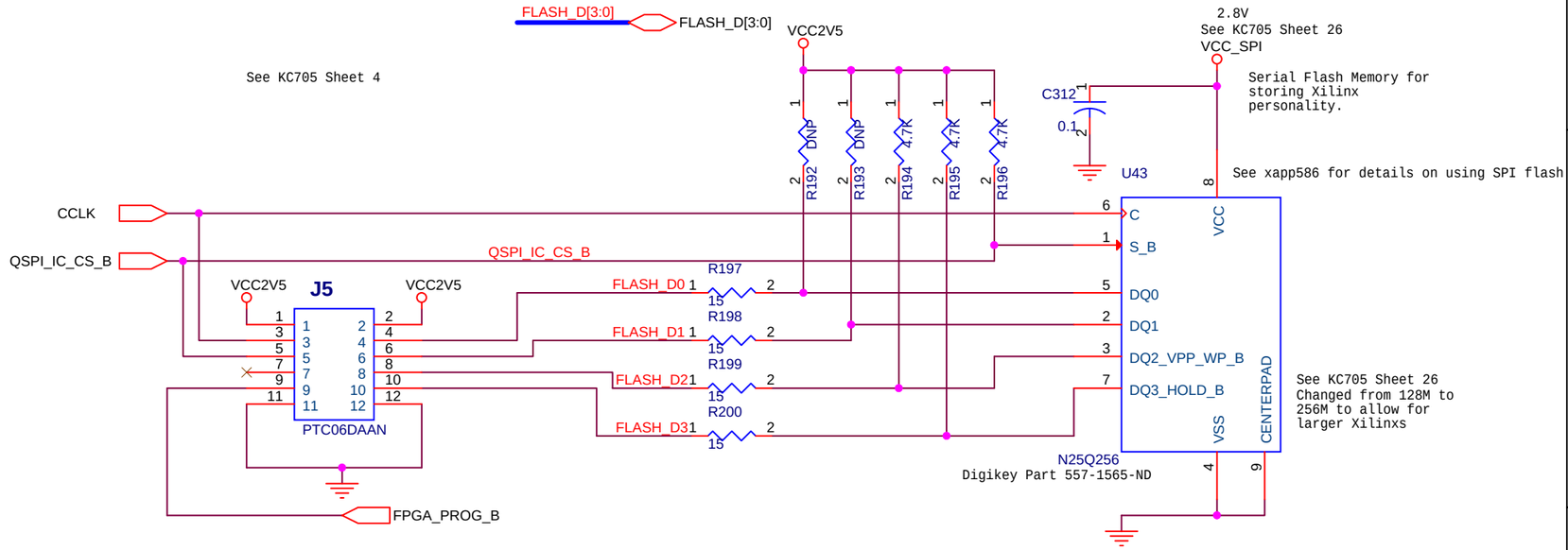
Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 20 of 27	



Title	DIGITAL PWM SYSTEM CONTROLLER	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 21 of 27	

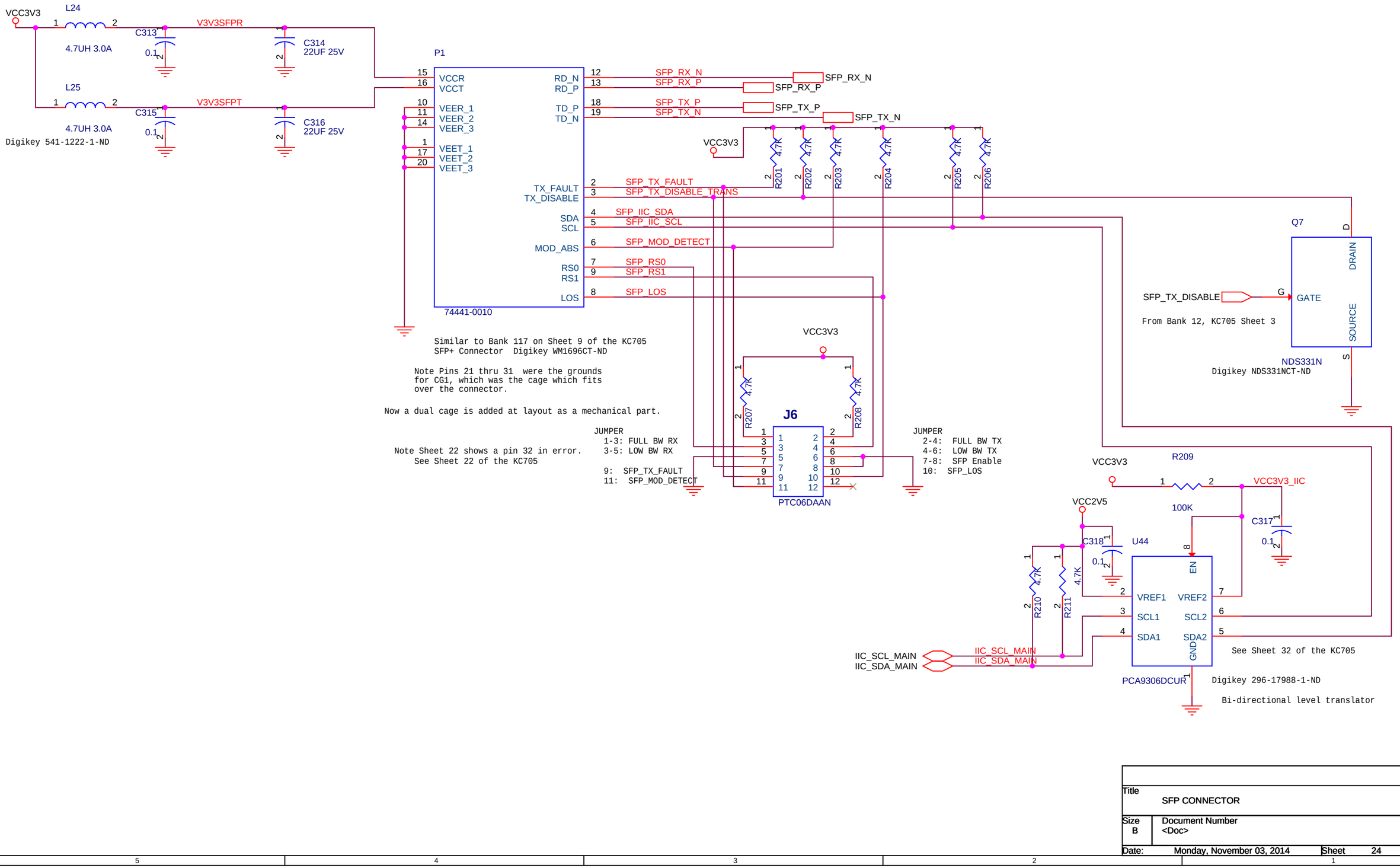


Title	DIGITAL PWM SYSTEM CONTROLLER	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 22 of 27	

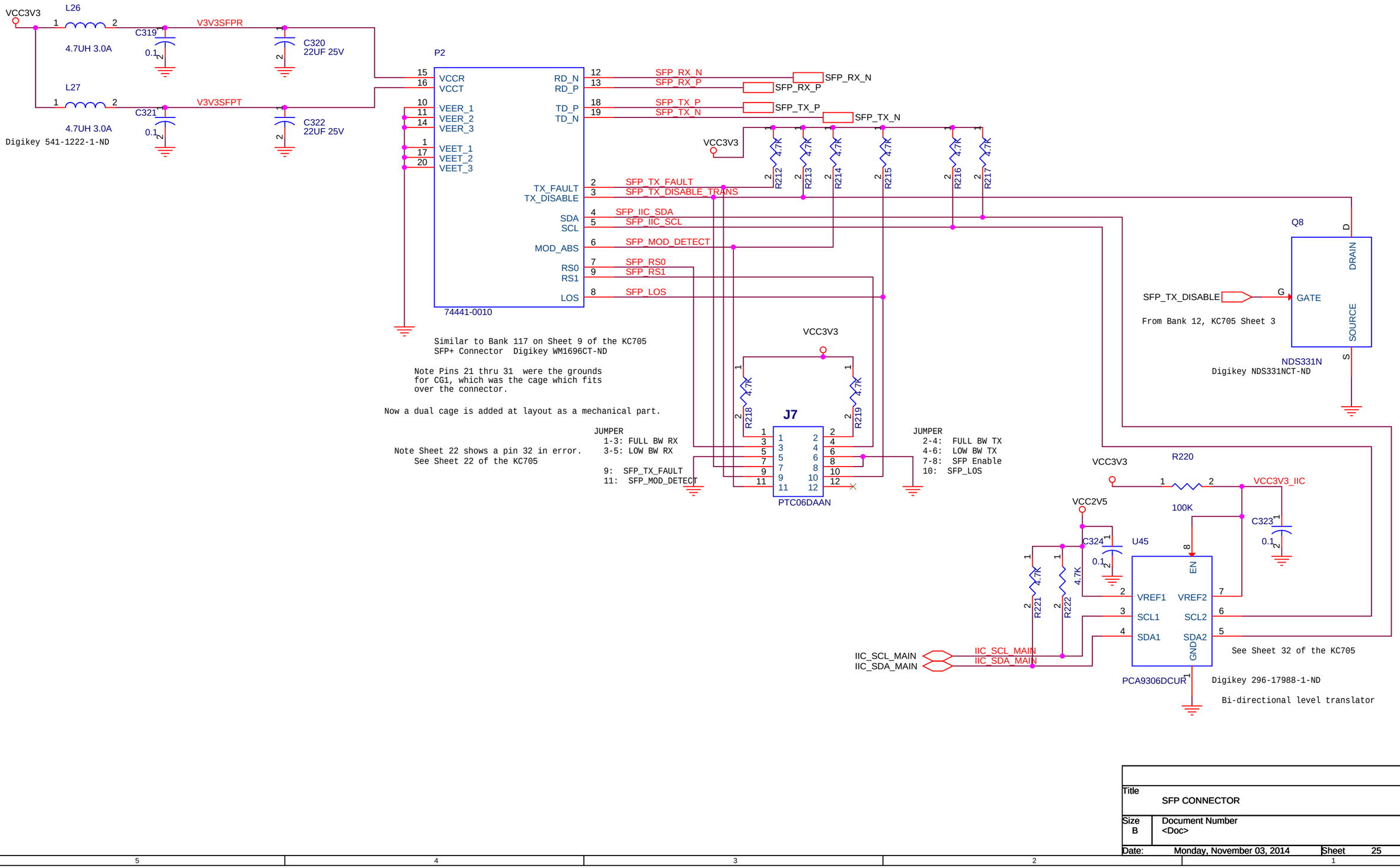


SPI EXTERNAL PROGRAMMING HEADER

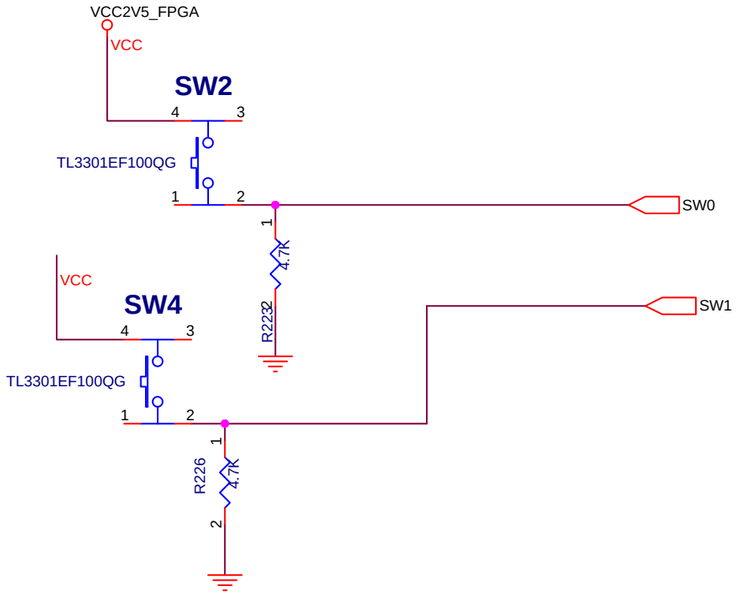
Title: FPGA QSPI		
Size: B	Document Number: <Doc>	Rev: <RevCode>
Date: Monday, November 03, 2014	Sheet 23 of 27	

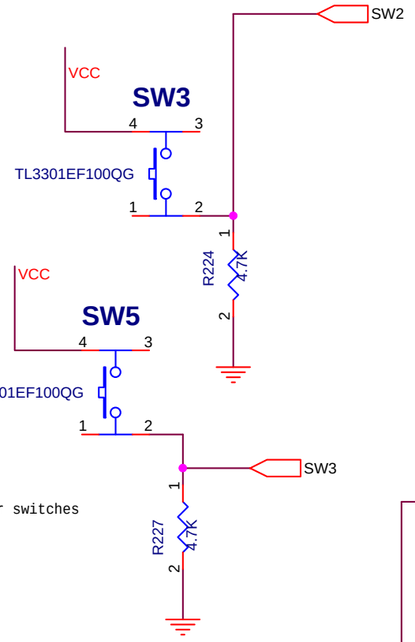


Title	SFP CONNECTOR	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 24 of 27	



Title	SFP CONNECTOR	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 25 of 27	





See Sheet 29 of KC705 for switches

Title	SWITCHES AND LEDS	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 03, 2014	Sheet 26 of 27	

ZDOK Connector 550-5 as on the Roach Board
Note this is the mirror image of the footprint on the ALMA Phasing Project ZDOK board.

Use 2.5V VCCO
1 is P, 2 is N on ZDOK

Digikey 6367550-5-ND

P3

ZDOK CONNECTOR 550-5

VCC5V0 VCC3V3 VCC2V5 VCCAUX

Supplies 1.8V

W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5

A[20:1]
D[20:1]
C[20:1]
F[20:1]

A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20

D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20

CLK0P_C19
CLK0N_C20

F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16 F17 F18 F19 F20

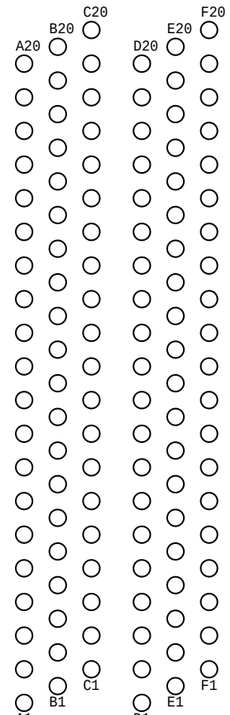
CLK1P_F19
CLK1N_F20

B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20

E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20

W1 X1 Y1 Z1 W6 X6 Y6 Z6

CARD EDGE



ZDOK Pin Layout

Title: ZDOK Connector		
Size: B	Document Number: <Doc>	Rev: <RevCode>
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