Single shielded enclosure

12 VDC

Regulators
(note 1)

DC
Filtered
Connector

Pwr Sup.
Controllers
(2)

DC to DC
Converters
(8)

Total of 12 analog inputs
(Design for > 500 MHz
bandwidth)

SMA
(note 6)

BALUN

Term &
Bias

ADC 0
HMCAD1511

IN_0

IN_1   DATA   8 LVDS Pairs

IN_2   Bit &
              Frame
IN_3   Clocks   2 LVDS Pairs

Note 2

FPGA_ADC_CTRL_0   CTRL

ADC_CLK_0   CLK

SMA

BALUN

Term &
Bias

ADC 1
HMCAD1511

IN_0

IN_1   DATA   8 LVDS Pairs

IN_2   Bit &
              Frame
IN_3   Clocks   2 LVDS Pairs

Note 2

FPGA_ADC_CTRL_1   CTRL

ADC_CLK_1   CLK

SMA

BALUN

Term &
Bias

ADC 2
HMCAD1511

IN_0

IN_1   DATA   8 LVDS Pairs

IN_2   Bit &
              Frame
IN_3   Clocks   2 LVDS Pairs

Note 2

FPGA_ADC_CTRL_2   CTRL

ADC_CLK_2   CLK

To FPGA
(sheet 2)
(Max data rate = 19 Gb/s)

SMA

PAD   BPF   Sine to
                          Square

Sample
Rate
Input

Clock
Select

Clock
Buf.

HMC987LP5E   HMC987LP5E

ADC_CLK_0

ADC_CLK_1

ADC_CLK_2

To
ADCs
Above
Via
coax

SMA

PAD   10 MHz   Sine to
             Filt.   Square

Synthesizer
LMX2851

OSC IN

RF_OUT_A

10 MHz
Input

FPGA_SYNTH_CTRL   CTRL

Note 1: Use switching regulators for digital components and linear regulators for ADCs and synthesizer.
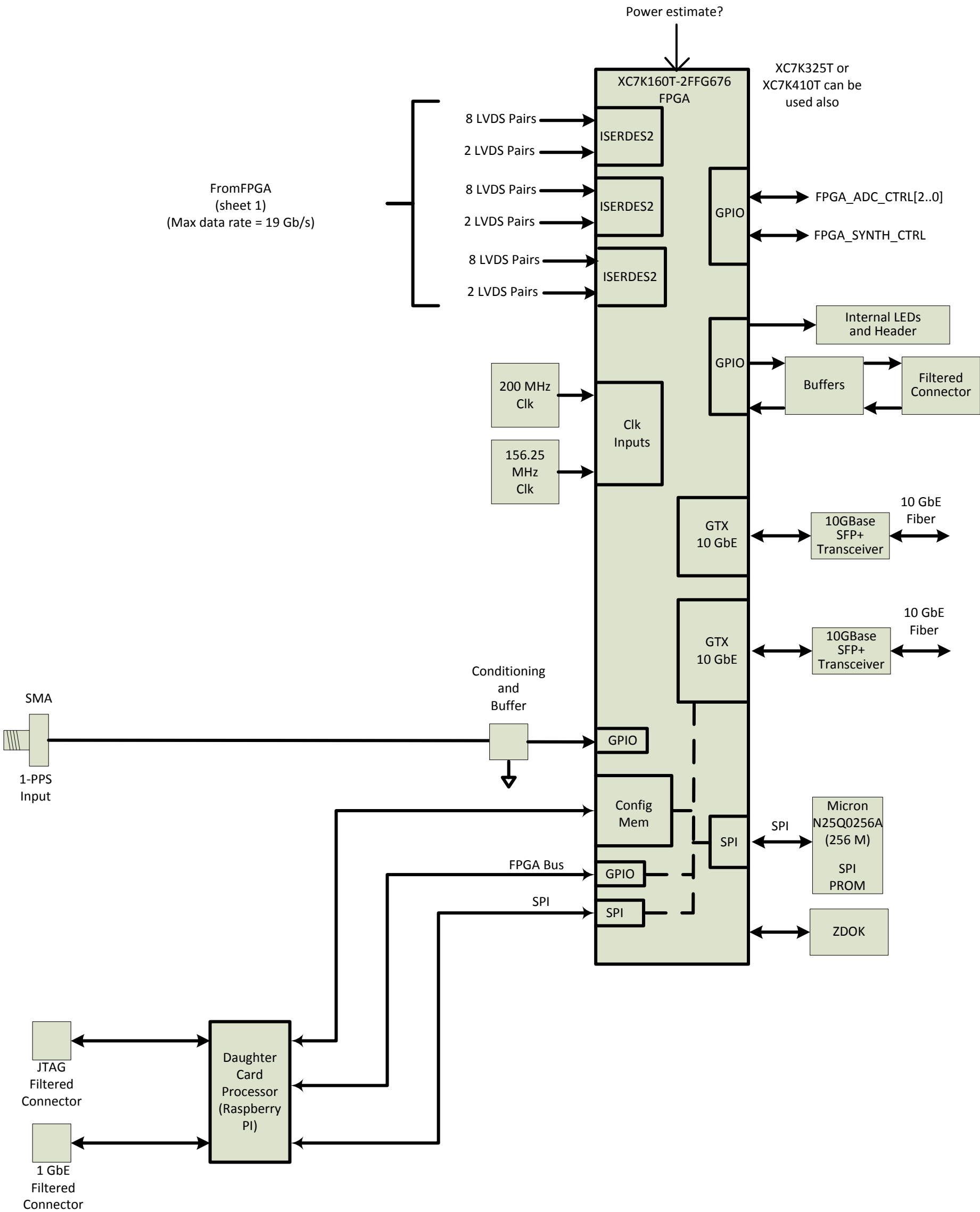Note 2: Keep the layout for the balun and termination similar to existing Berkeley design
Note 3: All components are enclosed in an shielded case. I/O is via shielded connector and the 10 GbE
        fiber is routed out of the case via "wave guide beyond cutoff.
Note 4: Clock logic for ADC is functional to 1 Gs/s.
Note 5: The LMX2581 (TI) was selected over HMC1034LP6GE (Hittite). LMX2581 (TI) has poorer, but adequate performance, and much better price.
Note 6: SMAs can be board or box mounted.

Power estimate?

XC7K160T-2FFG676
FPGA

XC7K325T or
XC7K410T can be
used also

8 LVDS Pairs → ISERDES2
2 LVDS Pairs →

FromFPGA
(sheet 1)
(Max data rate = 19 Gb/s)

8 LVDS Pairs → ISERDES2
2 LVDS Pairs →

8 LVDS Pairs → ISERDES2
2 LVDS Pairs →

GPIO ↔ FPGA_ADC_CTRL[2..0]
↔ FPGA_SYNTH_CTRL

GPIO → Internal LEDs and Header
→ Buffers ↔ Filtered Connector

200 MHz Clk →
156.25 MHz Clk →
Clk Inputs

GTX 10 GbE ↔ 10GBase SFP+ Transceiver ↔ 10 GbE Fiber

GTX 10 GbE ↔ 10GBase SFP+ Transceiver ↔ 10 GbE Fiber

SMA

Conditioning and Buffer

1-PPS Input

GPIO

Config Mem

SPI ↔ Micron N25Q0256A (256 M) SPI PROM

FPGA Bus → GPIO
SPI → SPI

↔ ZDOK

JTAG Filtered Connector ↔ Daughter Card Processor (Raspberry PI)

1 GbE Filtered Connector ↔

Power Requirements		
Component	**Volts**	**Milliamps**
HMCAD1511	1.8	400, per ADC
HMC987LP5E	3.3	100
FPGA		
10 GbE XCVRs		Depends on type
Processor		

DAB-HERALD Block Diagram
Revision 3
19 May 2014