Uses Xilinx Kintex XC7K160T-2FFG676

BOARDLAYOUT

Sheet 7

BOARDLAYOUT

BOARDLAYOUT also includes a list of design changes.

FPGA0

BANK 0 Sheet 11

FPGA_FCS

FPGA_FCS

CCLK

JTAG_TMS

JTAG_TDI

JTAG_TDO

JTAG_TCLK

FPGA_PROG_B

FPGA_DONE

QSPI_IC_CS_B

FLASH_D[3:0]

FPGAJTAG

Contains JTAG Connectors

FPGA14

Sheet 23

CCLK

QSPI_IC_CS_B

FPGA_PROG_B

FLASH_D[3:0]

QSPIFPGA

Contains SPI Flash for storing the personality

FPGA7

Sheet 12

FPGAPOWER

Hooking power to the FPGA

ADCREG

Sheet 5

SYNTH_PWR

ADC_ANALOG_REGULATORS

REG1

Sheet 6

PWRGD5V

FPGA_REGULATORS

Sheet 14 BANK 12 High Range

BANK 15 High Range FPGA13 BANK 13 High Range

BANK 14 High Range

JTAG_TMS

JTAG_TDI

JTAG_TDO

JTAG_TCLK

FPGA_PROG_B

TX_DISABLE0

TX_DISABLE1

SFP_STAT[5:0]

FPGA_FCS

FLASH_D[3:0]

SYNTH_PWR

PWRGD5V

SCLK0P

SCLK0N

SCLK1P

SCLK1N

SCLK2P

SCLK2N

DONE33V

SCLK[2:0]

PMBUS_CLK

PMBUS_ALERT

PMBUS_CTRL

SM_FAN_PWM

PMBUS_DATA

FPGAZDOK

Contains ZDOK Connector, 1PPS Connector

Contains Clock Generator Synthesizer

Contains the Raspberry Pi Interface

POWER1

SM_FAN_PWM

PMBUS_CLK

PMBUS_ALERT

PMBUS_DATA

PMBUS_CTRL

Sheet 9

DIGITAL_POWER_SUPPLIES

Contains DC-DC Converters

BANK 16 High Range

BANK 115 GTX

BANK 116 GTX

FPGA116

Sheet 13

FPGA_DONE

TX_DISABLE0

TX_DISABLE1

SFP_STAT[5:0]

DONE33V

SFP_STAT[5:0]

SCLKP0

SCLKN0

SCLKP1

SCLKN1

SCLKP2

SCLKN2

SCLK[2:0]

FPGASFPP

Contains 2 SFP+ Connectors

Contains USB Interface

Contains Clocks and LEDs

BANK 32 High Precision

BANK 33 High Precision

BANK 34 High Precision

FPGA32

Sheet 10

SCLK0P

SCLK0N

SCLK1P

SCLK1N

SCLK2P

SCLK2N

SCLK[2:0]

PMBUS_CLK

PMBUS_ALERT

PMBUS_DATA

Contains the 3 ADCs

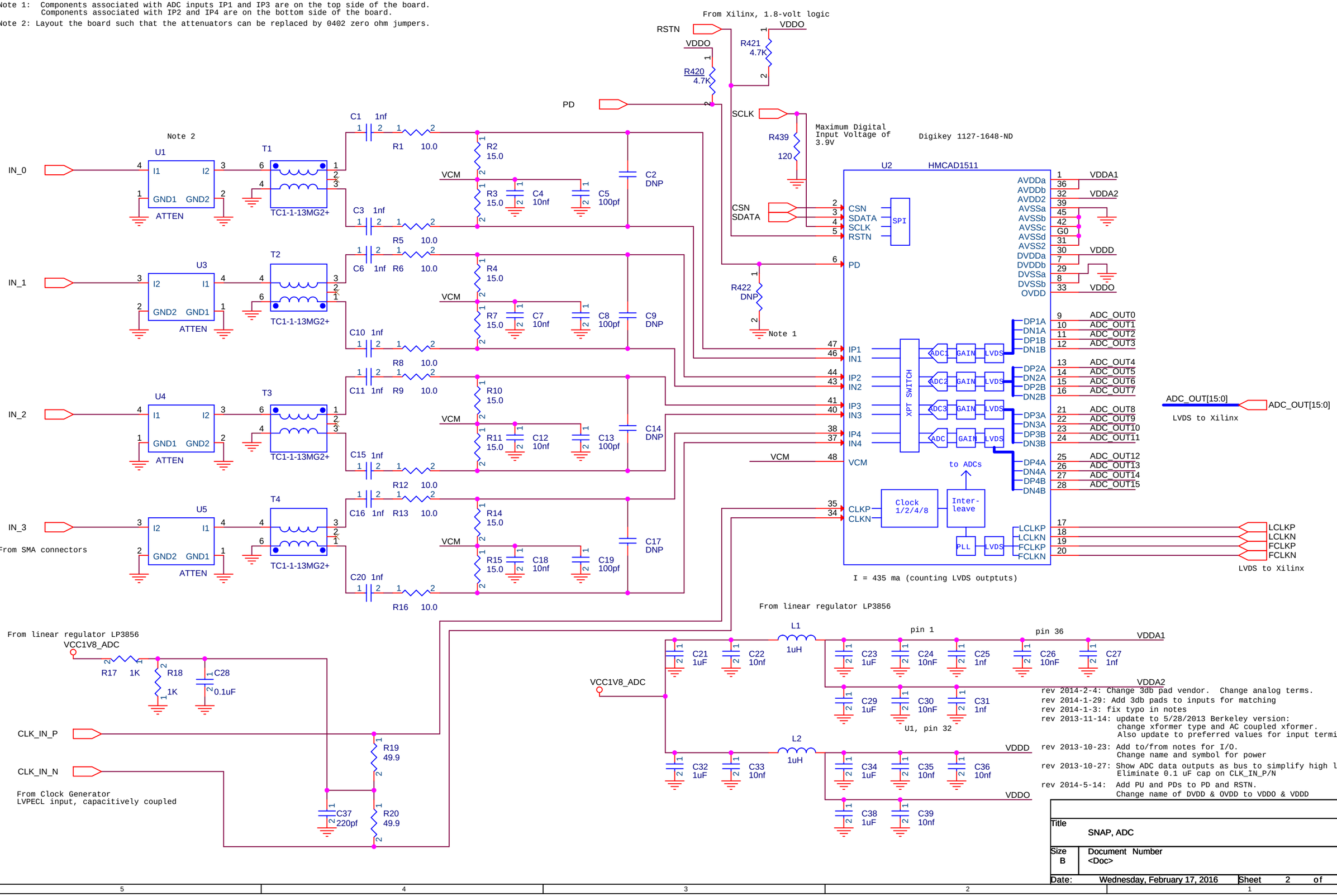
FPGAADCS

REV C CONTAINS CHANGES FOR THE SECOND VERSION OF THE BOARD.

Title: SMART NETWORK ADC PROCESSOR (SNAP) BOARD		
Size: A	Document Number: <Doc>	Rev: C
Date: Wednesday, February 17, 2016	Sheet 1 of 27	

Note 1: Components associated with ADC inputs IP1 and IP3 are on the top side of the board.
Components associated with IP2 and IP4 are on the bottom side of the board.

Note 2: Layout the board such that the attenuators can be replaced by 0402 zero ohm jumpers.

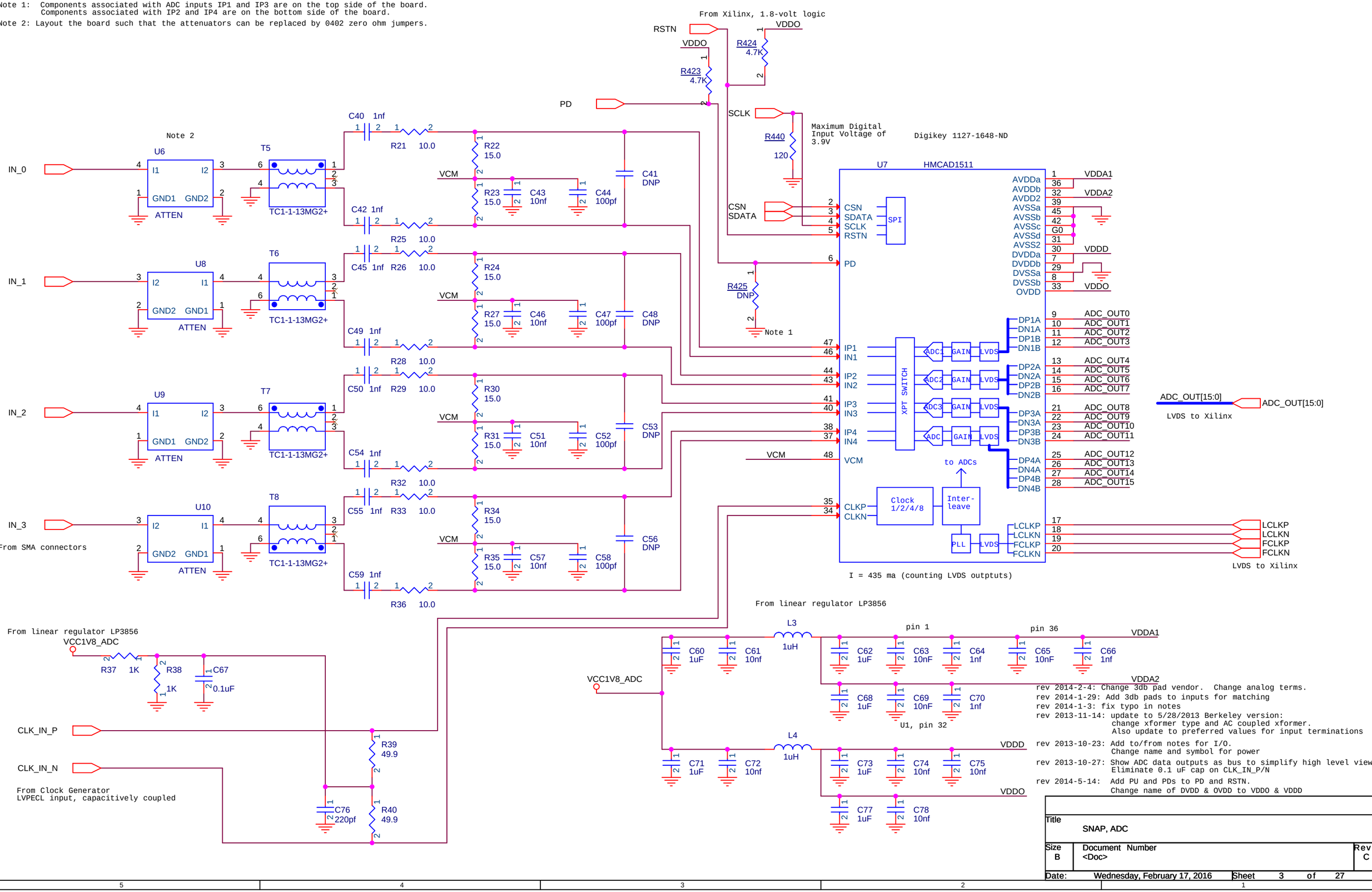


rev 2014-2-4: Change 3db pad vendor. Change analog terms.
rev 2014-1-29: Add 3db pads to inputs for matching
rev 2014-1-3: fix typo in notes
rev 2013-11-14: update to 5/28/2013 Berkeley version:
change xformer type and AC coupled xformer.
Also update to preferred values for input terminations
rev 2013-10-23: Add to/from notes for I/O.
Change name and symbol for power
rev 2013-10-27: Show ADC data outputs as bus to simplify high level view.
Eliminate 0.1 uF cap on CLK_IN_P/N
rev 2014-5-14: Add PU and PDs to PD and RSTN.
Change name of DVDD & OVDD to VDDO & VDDD

Title: SNAP, ADC		
Size: B	Document Number: <Doc>	Rev: C
Date: Wednesday, February 17, 2016	Sheet 2 of 27	

Note 1: Components associated with ADC inputs IP1 and IP3 are on the top side of the board.
Components associated with IP2 and IP4 are on the bottom side of the board.

Note 2: Layout the board such that the attenuators can be replaced by 0402 zero ohm jumpers.



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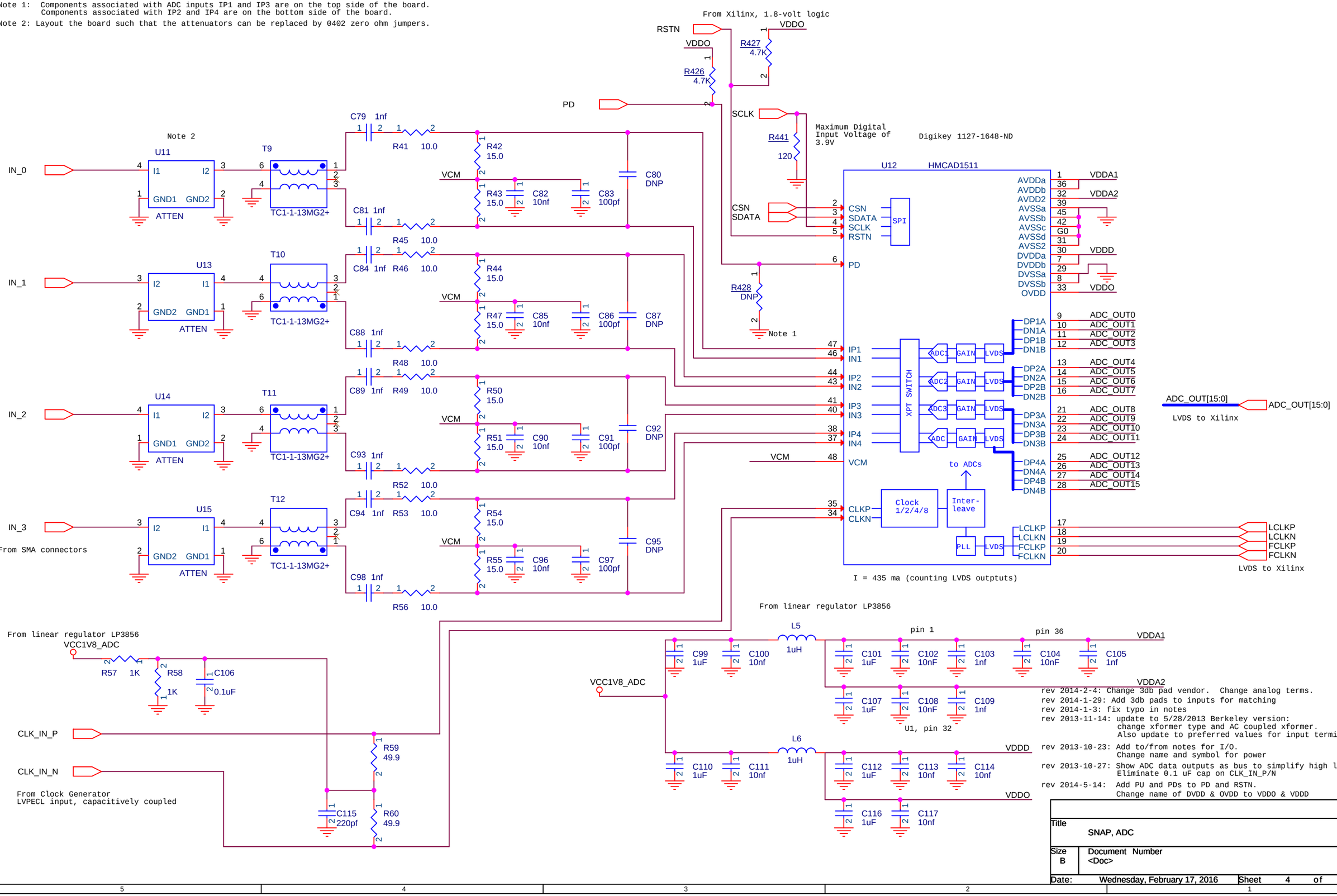

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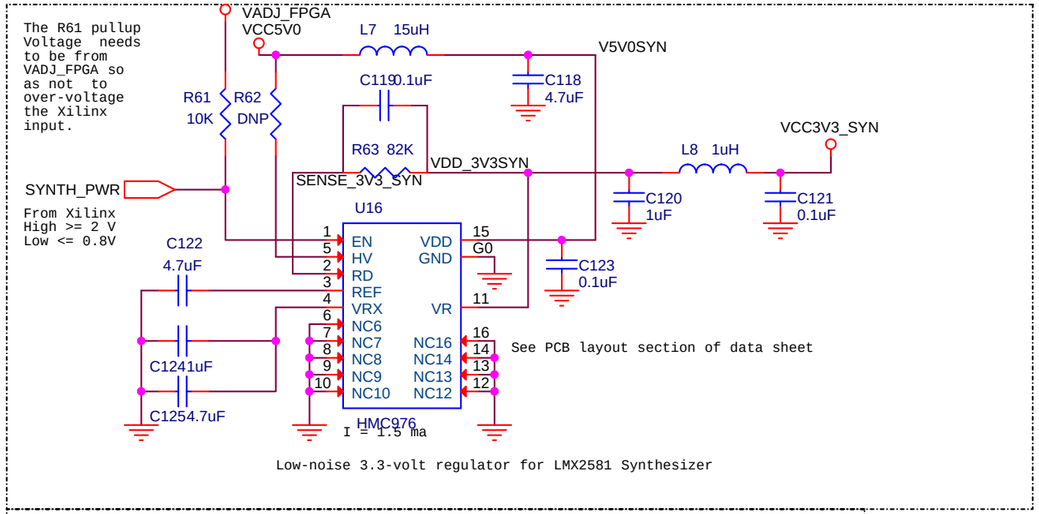
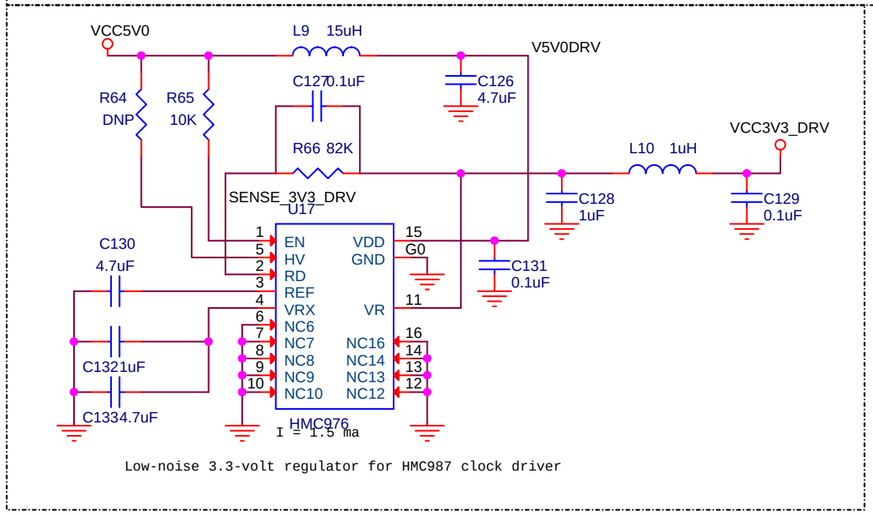
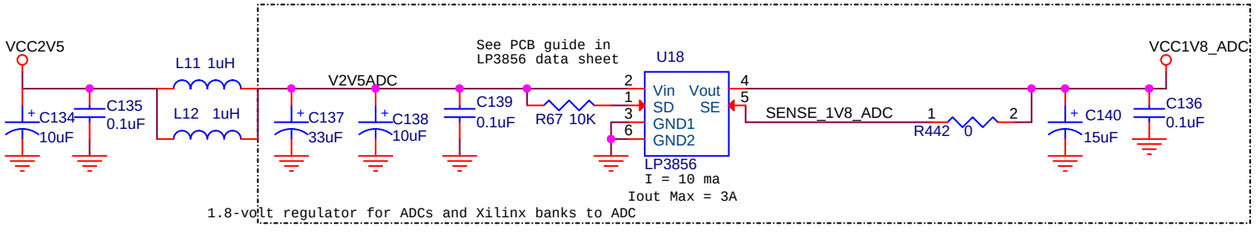
Title: SNAP, ADC		
Size: B	Document Number: <Doc>	Rev: C
Date: Wednesday, February 17, 2016	Sheet 4 of 27	







rev 2014-1-29: Add a pull-up to the synthesizer regulator.
rev 2014-1-3: change resistor value from 82K to 82.5K for HMC976s.
Change connection to HV input of both HMC976s from pull up common with the EN input to a separate DNP resistor.

Title: SNAP, Analog Regulators		
Size: B	Document Number: <Doc>	Rev: C
Date: Wednesday, February 17, 2016	Sheet 5 of 27	

VCC5V0

U19

VIN

EN

VOUT

ADJ

GND

ADP123AUJZ-R7

C141

10uF

VCC_SPI

2.8V @ 300mA

Powers SPI Flash that stores FPGA personality

See KC705 sheet 46 Linear Power Supplies

C142

100uF 10V X5R

R68

6.340K

R1 1/16W 0.11%

SENSE_SPI

R69

1.370K

R2 1/16W 0.1%

VOUT = 0.5 V(1 + R1/R2) + (0.000000015A)(R1)

Change from 4.53K and 1K since did not give right voltage.

VOUT = 2.8200V

5V @ 10A Switching Power Supply

Powers Raspberry Pi, ADCs

Pins 41 and 42 are large pads in the center of the chip

Connect PH pins via a small copper island.

VPH

There are many large electrolytic capacitors on 12V at the DC-DC converters, so not included here.

VCC12_P

U20

LMZ31710

PVIN1 PVIN2 PVIN3 PVIN4 PVIN5

VIN

OCP_SEL

ILIM

RT/CLK

VADJ

SS/TR

STSEL

INH/UVLO

PH1 PH2 PH3 PH4 PH5 PH6 PH7 PH8 PH9

DNC1 DNC2 DNC3 ISHARE

VOUT1 VOUT2 VOUT3 VOUT4 VOUT5 VOUT6

SENSE+

SYNC_OUT

PWRGD

AGND1 AGND2 PGND1 PGND2 PGND3 PGND4 PGND5

C143

22UF 25V

C145

22UF 25V

C144

22UF 25V

C148

0.1

1MHz optimal for 12V to 5V

R70

63.4K

R71

196

Selects 5V

R443

0

SENSE_5V0

C146

47uF 10V X5R

C147

100uF 10V X5R

VCC5V0

PWRGD5V

Sinks low if output Voltage > 6% out of regulation.

Title: SNAP, FPGA Regulators		
Size: A	Document Number: <Doc>	Rev: C
Date: Wednesday, February 17, 2016	Sheet 6 of 27	

Changes for Rev. C

NOT Done yet

See the Design Manual for a detailed explanation.

Done

Fix the footprint of the ZDOK connector so it doesn't have the offset pins.

On the Xilinx silkscreen label pins from A1 to A26, not A1 to AF26.

Make the probe points on the back of the Xilinx not covered with laquer.

Add RFI cage for SFP+ with 19 grounded connections

Add 22 2-56 mounting holes with electrical connections to ground

Move J2 (the 12V source), so it does not conflict with U24. Note that the wiring was reversed to do this.

Change Voltage source of R61 from V5.0 to VADJ_FPGA to prevent an overvoltage to the Xilinx input, SH 5

Change Voltage source of R431 from VCC2V5 to VCC3V3 to prevent an overvoltage to the Xilinx input, SH 9

Modify JTAG connectors J3 & J11 pinout to industry standard, SH 11. A

Add a 125 MHz oscillator for 1 GbE, SH 15

Move pin labels on the following resistor for clarity:
R17, R18, R37, R38, R57, R58

SYNTHMUXOUT added to connect U21 Synthesizer MUXOUT to Xilinx, SH 8.

Added connections of SFP status lines to Xilinx, SH 24, 25

Added connections for ADC, SH xx

Changes for Rev B (first manufacturing run)

Change 33 to 1.8V and move ADC 1 to it.

Use only MRCC clocks for the ADCs

Move ZDOK to 16 to 14, SPI 14 to 15, and sfp ctrl to 15 to 16

Redistribute ZDOK pins.

Change ZDOK to 2.5V VCCO so can use LVDS-25 See UG471.

Change 100MHZ OSC to 200 MHZ. and eliminate termination resistor.

Replace 5V linear regulator with a DC-DC converter

Reduce number of TI Power Supply Controllers from 3 to 2

Remove C196 which wasn't connected to anything.

Add J9 as a test connector

Go to a single dual SFP+ Cage instead of two single cages.

Add a vertical USB J10 in parallel with horizontal USB J4

Change U43 from a 128 MByte to a 256 MByte Flash Memory.

Move the SPI pins to Bank 14 as on the Kintex Evaluation Board.

Hook up the FPGA_DONE and FPGA_PROG_B pins to the PI header thru level shifters

Add DNP bypass capacitors to allow for larger Xilinxs

Move PI signals to Bank 15 with a VCCO of 3.3V.

Move ZDOK clock lines to match the Roach II.

Change BOM to give options for 3 Xilinxs.

Add PU or PD to PD on the ADCs.

Add Heatsink to BOM

Add fan power receptacle with PWM

Arrange ADC Out pin parings so similar lengths.

Moved CLK_SEL_B and CLK_SEL_A to bank 15 which has the needed VCCO of 3.3V.

Install PD and DNP PU on PUDC_B pin.

Remove LK_DET TP3, since there were two test points.

Add net names V3V3SFPR, V3V3SFPT,V2V5ADC,V5V0DRV,V5V0SYN,V12PWRCTRL,V12D020W,V12D210W,V12D010W

Have ADC SCLK signals from 3.3V Voltage divider to terminate.

Move SYNTH_(CLK,DATA,LE,CE,BE) to 3.3V, then put series/parallel resistor on SYNTH_CLK.

Change Footprint of DNP resistors R114,R133,R135,R139 so they match the placed resistors.

Add zero Ohm resistors R442,R443 and make SENSE_... nets for sense lines.

Fix Pinout of U28,U46, & U47 so it matchs the BOM part number which is SN74AVC4T245RSVR

Fix typo to add VCC_3V3SYN to VCC3V3_SYN net.

Remove U27 and its resistors. Put in a 6pin vertical J3 and right angle jtag header J11. Move Xilinx Temperature to JP4.

Add ground test points GNDTP1-5.

Add a second ground pin to SMATP1 through 16.

Make Horizontal USB Connector J4 DNP so it won't short to the rail in a box. Also add a 0 Ohm DNP jumper.
Deleted U25-E26 from net C20, and deleted U25-F25 from net C19.

To accomdate the new Pi B+, change PI2 from 26 to 40 pins & eliminate P8.

TOP VIEW
After Changes

1 26 AF

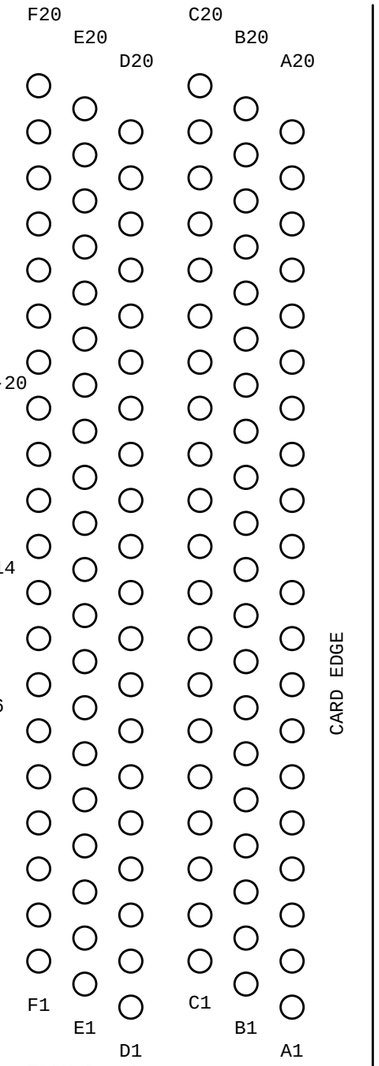
GTX 116 SFP 1		High Range 16 SFP CTRL 2.5V	High Range 15 Rasp PI 3.3V	High Range 14 ZDOK SYNTH CLKS SPI 2.5V
GTX 115 SFP 2	0 JTAG 2.5V	GND	High Range 13 ZDOK 2.5V	
High Performance 34 ADC 0 1.8V		High Performance 33 ADC 1 CLKS, LEDS 1.8V	High Performance 32 ADC 2 1.8V	High Range 12 ZDOK PI 2.5V

Pins 15-20

Pins 7-14

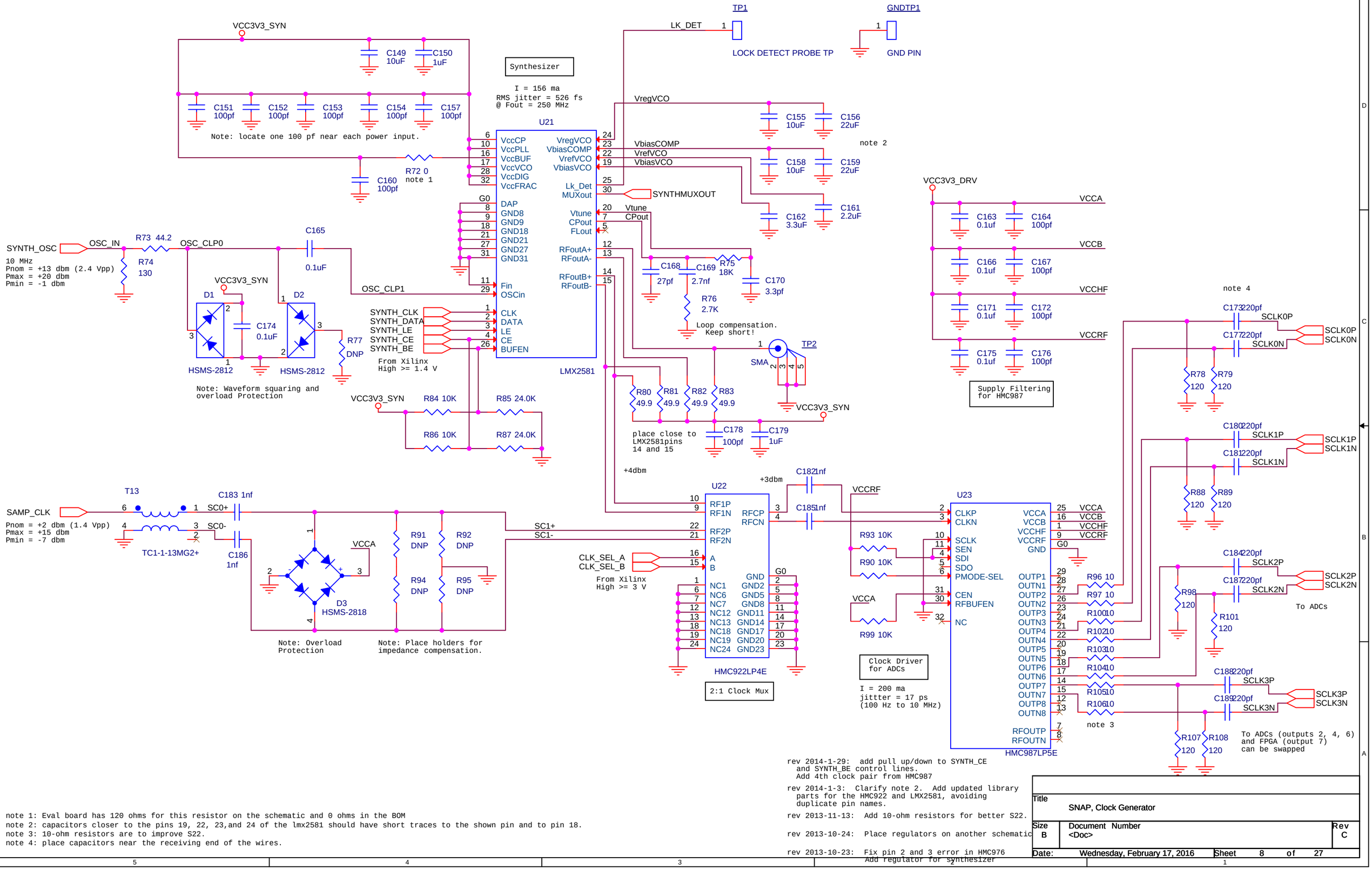
Pins 1-6

XILINX



ZDOK Pin Layout

Title: SNAP, BOARD LAYOUT and Change Log		
Size: A	Document Number: <Doc>	Rev: C
Date: Wednesday, February 17, 2016	Sheet 7 of 27	


Synthesizer
I = 156 ma
RMS jitter = 526 fs
@ Fout = 250 MHz
U21
LMX2581
VCC3V3_SYN
C149 10uF
C150 1uF
C151 100pf
C152 100pf
C153 100pf
C154 100pf
C157 100pf
Note: locate one 100 pf near each power input.
C160 100pf
R72 0
note 1
VccCP
VccPLL
VccBUF
VccVCO
VccDIG
VccFRAC
DAP
GND8
GND9
GND18
GND21
GND27
GND31
Fin
OSCin
VregVCO
VbiasCOMP
VrefVCO
VbiasVCO
Lk_Det
MUXout
Vtune
CPout
FLout
RFoutA+
RFoutA-
RFoutB+
RFoutB-
CLK
DATA
LE
CE
BUFEN
SYNTH_CLK
SYNTH_DATA
SYNTH_LE
SYNTH_CE
SYNTH_BE
From Xilinx
High >= 1.4 V
TP1
LK_DET
LOCK DETECT PROBE TP
GNDTP1
GND PIN
VregVCO
VbiasCOMP
VrefVCO
VbiasVCO
SYNTHMUXOUT
Vtune
CPout
C155 10uF
C156 22uF
C158 10uF
C159 22uF
C162 3.3uF
C161 2.2uF
note 2
C168 27pf
C169 2.7nf
R75 18K
R76 2.7K
C170 3.3pf
Loop compensation.
Keep short!
TP2
SMA
VCC3V3_SYN
SYNTH_OSC
10 MHz
Pnom = +13 dbm (2.4 Vpp)
Pmax = +20 dbm
Pmin = -1 dbm
OSC_IN
R73 44.2
R74 130
OSC_CLP0
C165 0.1uF
OSC_CLP1
D1
D2
HSMS-2812
HSMS-2812
C174 0.1uF
R77 DNP
Note: Waveform squaring and
overload Protection
R84 10K
R85 24.0K
R86 10K
R87 24.0K
R80 49.9
R81 49.9
R82 49.9
R83 49.9
place close to
LMX2581pins
14 and 15
C178 100pf
C179 1uF
+4dbm
C182 1nf
+3dbm
C185 1nf
VCCRF
VCC3V3_DRV
C163 0.1uf
C164 100pf
C166 0.1uf
C167 100pf
C171 0.1uf
C172 100pf
C175 0.1uf
C176 100pf
VCCA
VCCB
VCCHF
VCCRF
Supply Filtering
for HMC987
note 4
C173 220pf
C177 220pf
SCLK0P
SCLK0N
R78 120
R79 120
C180 220pf
C181 220pf
SCLK1P
SCLK1N
R88 120
R89 120
C184 220pf
C187 220pf
SCLK2P
SCLK2N
R98 120
R101 120
To ADCs
C188 220pf
C189 220pf
SCLK3P
SCLK3N
R107 120
R108 120
To ADCs (outputs 2, 4, 6)
and FPGA (output 7)
can be swapped
T13
SAMP_CLK
Pnom = +2 dbm (1.4 Vpp)
Pmax = +15 dbm
Pmin = -7 dbm
TC1-1-13MG2+
SC0+
SC0-
C183 1nf
C186 1nf
D3
HSMS-2818
VCCA
R91 DNP
R92 DNP
R94 DNP
R95 DNP
Note: Overload
Protection
Note: Place holders for
impedance compensation.
SC1+
SC1-
U22
HMC922LP4E
2:1 Clock Mux
CLK_SEL_A
CLK_SEL_B
From Xilinx
High >= 3 V
R93 10K
R90 10K
R99 10K
VCCRF
VCCA
U23
HMC987LP5E
Clock Driver
for ADCs
I = 200 ma
jittter = 17 ps
(100 Hz to 10 MHz)
R96 10
R97 10
R100 10
R102 10
R103 10
R104 10
R105 10
R106 10
note 3
rev 2014-1-29: add pull up/down to SYNTH_CE
and SYNTH_BE control lines.
Add 4th clock pair from HMC987
rev 2014-1-3: Clarify note 2. Add updated library
parts for the HMC922 and LMX2581, avoiding
duplicate pin names.
rev 2013-11-13: Add 10-ohm resistors for better S22.
rev 2013-10-24: Place regulators on another schematic
rev 2013-10-23: Fix pin 2 and 3 error in HMC976
Add regulator for synthesizer
note 1: Eval board has 120 ohms for this resistor on the schematic and 0 ohms in the BOM
note 2: capacitors closer to the pins 19, 22, 23,and 24 of the lmx2581 should have short traces to the shown pin and to pin 18.
note 3: 10-ohm resistors are to improve S22.
note 4: place capacitors near the receiving end of the wires.
Title
SNAP, Clock Generator
Size B
Document Number
<Doc>
Rev C
Date: Wednesday, February 17, 2016
Sheet 8 of 27

VCCAUX_IO should be connected to VCCAUX in all cases except when needing to run at the highest DDR3 line rates when it should be connected to 2.0V.

R109 4.7K — PWR_INH_B — JP1 HEADER 1X2

R110 2K, R111 2K, R112 2K, R113 2K

J1 — AWHW10G-0202-T-R Keyed PMBUS Conn. HDR_BOX_2X5 Digikey HRP10H-ND

PMBUS_ALERT, PMBUS_DATA, PMBUS_CLK, PMBUS_CTRL

PMBUS Addr = 52 — R122 75K — R125 75K — ADDR-0, ADDR-1

PWR1 — PWRCTL — VCC3V3_PWRCTL

Contains U40 in Sheet 21
POWER CONTROLLER 1
KC705 SHEET 36

DPWM-A1, SRE-A1, SRE-B1, FAULT-A1, IOUT1, TEMP1, EAP1
PWRCTL_SRE_GPIO1, PWR_INH_B, SENSE_INT

DCDC1 — PWM VOUT, SRE, FAULT, IOUT, PWR_INH_B, TEMP — PTD08D020W

Contains U35 in Sheet 17
Internal FPGA Voltage 1.0 Volts
KC705 SHEET 37 VCCINT

VCCINT — R111 1.00K — R114 DNP — >1.5V 787 Ohms <=1.5V DNP
VCCINT_FPGA — D4 1N5335BRLG 3.9V 320MA

DPWM-A2, SRE-A2, SRE-B2, FAULT-A2, IOUT2, EAP2, TEMP2
PWRCTL_SRE_GPIO2, SENSE_AUX

DCDC2 — PWM_A VOUT_A, SRE_A, FF_A, IOUT_A, TEMP — PTD08D210W

Contains U36 in Sheet 18

FPGA Aux Voltage 1.80 V
KC705 SHEET 38 VCCAUX

VCCAUX — R117 1.00K — R118 787 — >1.5V 787 Ohms <=1.5V DNP
VCCAUX_IO — D5 1N5335BRLG 3.9V 320MA

TEMP3, IOUT3, DPWM-A3, SRE-A3, SRE-B3, FAULT-A3, IOUT3, EAP3
PWRCTL_SRE_GPIO3, SENSE_3V3

IOUT_B, PWM_B VOUT_B, SRE_B, FF_B

Used for JTAG, CLK GEN for ADCs
KC705 SHEET 38 VCC3V3

VCC3V3 — R119 1.00K — R121 787 — >1.5V 787 Ohms <=1.5V DNP

VCCAUXMGT — R123 1.00K — R126 787 — VCCAUXMGT 1.8V

DCDC8 — PWM VOUT, SRE, FAULT, IOUT, PWR_INH_B, TEMP — PTD08A010W

KC705 SHEET 45
Contains U34 in Sheet 16

DPWM-A4, SRE-A4, SRE-B4, FAULT-A4, IOUT4, TEMP4, EAP4
PWRCTL_SRE_GPIO4, SENSE_AUXMGT

SEQ-1, SEQ-2 — PWRCTL_SEQ_1, PWRCTL_SEQ_2

PGOOD — PWRCTL_PWRGOOD

Use VCC1V8_ADC, since goes to bank 32 which has VCCO = VCC1V8_ADC

PWR2 — PWRCTL — VCC3V3_PWRCTL

Contains U42 in Sheet 22
POWER CONTROLLER 2
KC705 SHEET 40

DPWM-A1, SRE-A1, SRE-B1, FAULT-A1, IOUT1, TEMP1, TEMP2, EAP1
PWRCTL_SRE_GPIO1, SENSE_2V5

DCDC5 — PWM_A VOUT_A, SRE_A, FF_A, IOUT_A, TEMP — PTD08D210W

Contains U37 in Sheet 19
KC705 SHEET 41

VCC2V5 — R130 1.00K — R131 787 — >1.5V 787 Ohms <=1.5V DNP
VCC2V5_FPGA
VADJ — VADJ_FPGA — KC705 SHEET 39 VADJ
Used for VCCO of banks 12,13,16 (ZDOK). Probably 3.3V

IOUT2, DPWM-A2, SRE-A2, SRE-B2, FAULT-A2, EAP2
PWRCTL_SRE_GPIO2, SENSE_BRAM

IOUT_B, PWM_B VOUT_B, SRE_B, FF_B — PTD08D210W

KC705 SHEET 41 VCC1V5_FPGA

VCCBRAM — R132 1.00K — R133 DNP — >1.5V 787 Ohms <=1.5V DNP
1.0V like VCCINT — D6 1N5335BRLG 3.9V 320MA

Contains U38 in Sheet 20
KC705 SHEET 42

DCDC6 — PWM_A VOUT_A, SRE_A, FF_A, IOUT_A, TEMP — PTD08D210W

DPWM-A3, SRE-A3, SRE-B3, FAULT-A3, IOUT3, EAP3, TEMP3, TEMP4, DPWM-A4, IOUT4, SRE-A4, SRE-B4, FAULT-A4
PWRCTL_SRE_GPIO3, PWRCTL_SRE_GPIO4, SENSE_VCCMGTA, SENSE_VTTMGTA

VCCMGTA — R134 1.00K — R135 DNP — D7 1N5335BRLG 3.9V 320MA
1.0V like VCCINT if QPLL <=10.3125GHz else 1.05V

VTTMGTA — R137 1.00K — R139 DNP — D8 1N5335BRLG 3.9V 320MA — VMGTAVTT 1.2V
MGT used in FPGA for driving SFP+ connectors

KC705 SHEET 42 VTTMGTA

SEQ-1, SEQ-2 — PWRCTL_SEQ_1, PWRCTL_SEQ_2

PGOOD — PWRCTL_PWRGOOD

PMBUS_ALERT, PMBUS_DATA, PMBUS_CLK, PMBUS_CTRL

PMBUS Addr = 53 — R136 86.6K — R138 75K — ADDR-0, ADDR-1

J2 — 39-30-1060 MOLEX CONNECTOR 12V CARD POWER INPUT Digikey WM1353-ND

KC705 SHEET 35

VCC12_P_IN — C190 1UF 25V

U24 — BNX016-01 Filter Digikey 490-5055-ND

C191 330UF 25V

VCC12_P

R407 2K, R408 2K — 2 x 1/10W for power dissipation

DS2 SML-LX0603GW-TR — Green LED

J61 — 22292021 — Plug for Heatsink Fan Place near Xilinx — VFAN

D14 DL4148

Changed from VCC2V5 to VCC3V3 to match Xilinx in RevB

VCC3V3 — R431 1.00K — SM_FAN_PWM

Q17 NDT3055L — DRAIN1, DRAIN2, SOURCE, GATE

PWRCTL_PWRGOOD — VCC3V3

Q4 NDS331N — GATE, DRAIN, SOURCE

R128 10K, R127 249

DS1 SML-LX0603GW-TR — Green LED

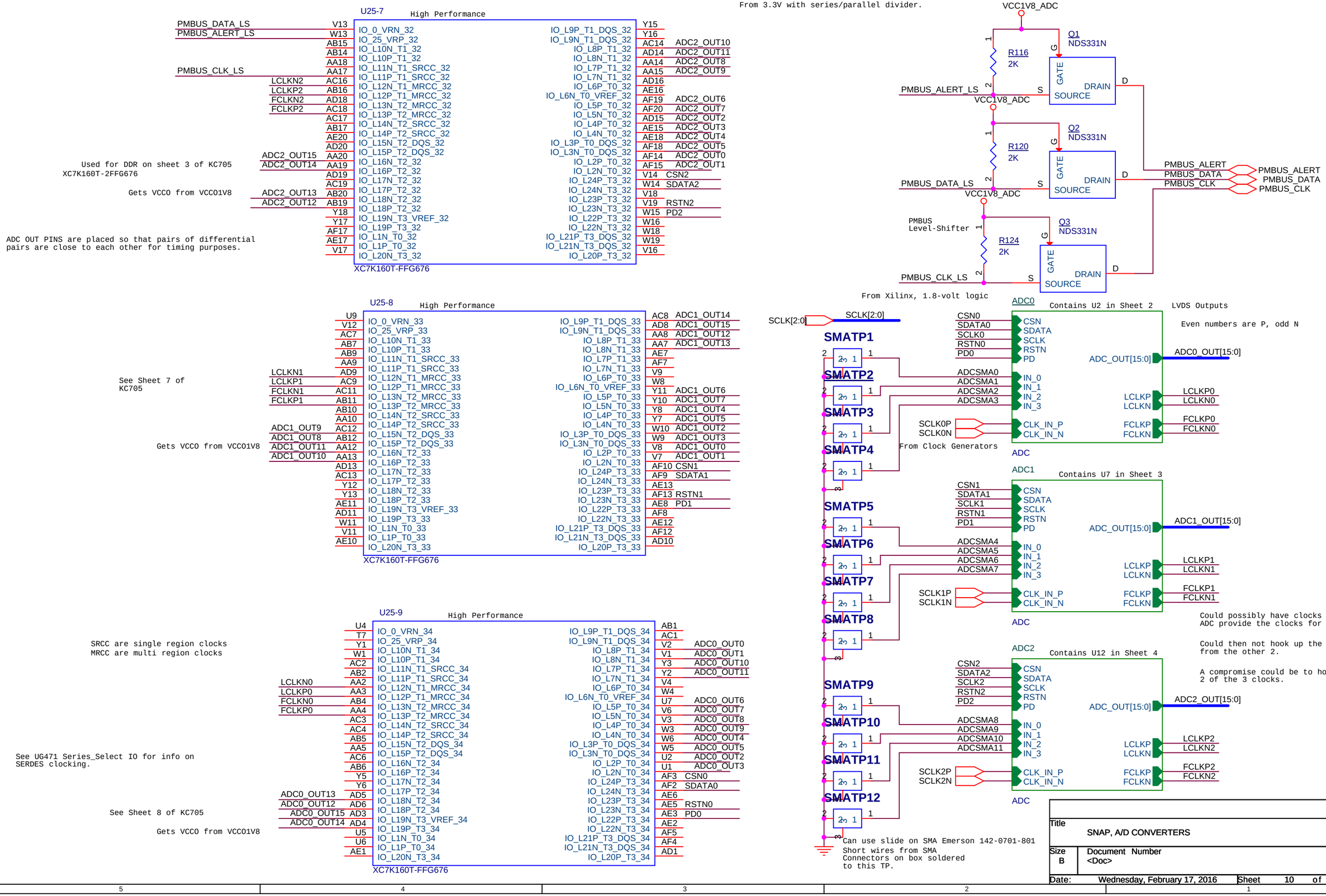
M1 2-56-MTG_HOLE, M2 2-56-MTG_HOLE, M3 2-56-MTG_HOLE, M4 2-56-MTG_HOLE, M5 2-56-MTG_HOLE, M6 2-56-MTG_HOLE, M7 2-56-MTG_HOLE, M8 2-56-MTG_HOLE, M9 2-56-MTG_HOLE, M10 2-56-MTG_HOLE, M11 2-56-MTG_HOLE, M12 2-56-MTG_HOLE, M13 2-56-MTG_HOLE, M14 2-56-MTG_HOLE, M15 2-56-MTG_HOLE, M16 2-56-MTG_HOLE, M17 2-56-MTG_HOLE, M18 2-56-MTG_HOLE, M19 2-56-MTG_HOLE, M20 2-56-MTG_HOLE, M21 2-56-MTG_HOLE, M22 2-56-MTG_HOLE

See Kintex-7 FPGA Data Sheet : DC and AC Switching Characteristics

This has the sequence for powering up the supplies.
The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, VCCAUX_IO, and VCCO to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the poweron sequence. If VCCINT and VCCBRAM have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If VCCAUX, VCCAUX_IO, and VCCO have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

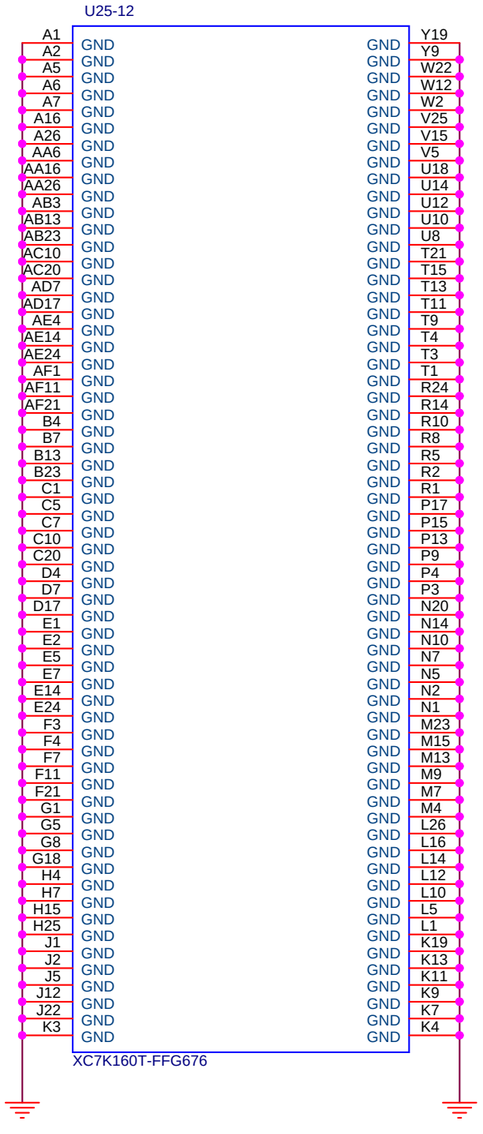
The recommended GTX transceiver power-on sequence is VCCINT, VMGTAVCC, VMGTAVTT or VMGTAVCC, VCCINT, VMGTAVTT to achieve minimum current draw. There is no recommended sequencing for VMGTVCCAUX. Both VMGTAVCC and VCCINT can be ramped up simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

Title	SNAP, DIGITAL POWER SUPPLIES	
Size C	Document Number <Doc>	Rev C
Date: Wednesday, February 17, 2016	Sheet 9 of 27	

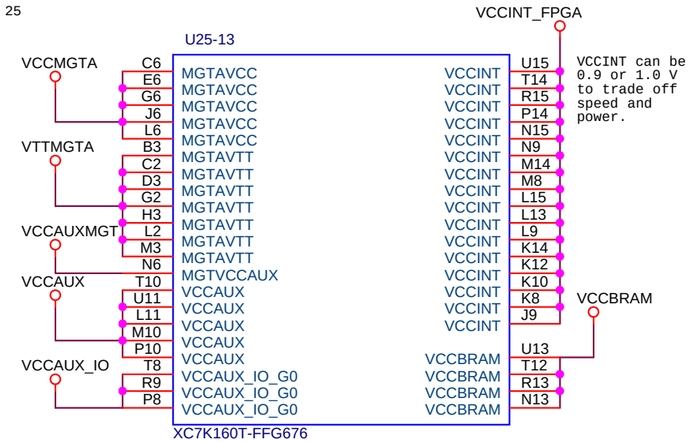

U25-7
High Performance
PMBUS_DATA_LS
PMBUS_ALERT_LS
PMBUS_CLK_LS
LCLKN2
LCLKP2
FCLKN2
FCLKP2
ADC2_OUT15
ADC2_OUT14
ADC2_OUT13
ADC2_OUT12
Used for DDR on sheet 3 of KC705
XC7K160T-2FFG676
Gets VCCO from VCCO1V8
ADC OUT PINS are placed so that pairs of differential pairs are close to each other for timing purposes.
XC7K160T-FFG676
From 3.3V with series/parallel divider.
VCC1V8_ADC
Q1
NDS331N
R116
2K
Q2
NDS331N
R120
2K
Q3
NDS331N
R124
2K
GATE
DRAIN
SOURCE
PMBUS_ALERT
PMBUS_DATA
PMBUS_CLK
PMBUS Level-Shifter
From Xilinx, 1.8-volt logic
U25-8
High Performance
See Sheet 7 of KC705
Gets VCCO from VCCO1V8
See Sheet 8 of KC705
XC7K160T-FFG676
U25-9
High Performance
SRCC are single region clocks
MRCC are multi region clocks
See UG471 Series_Select IO for info on SERDES clocking.
Gets VCCO from VCCO1V8
XC7K160T-FFG676
SCLK[2:0]
SMATP1
SMATP2
SMATP3
SMATP4
SMATP5
SMATP6
SMATP7
SMATP8
SMATP9
SMATP10
SMATP11
SMATP12
ADC0
Contains U2 in Sheet 2
LVDS Outputs
Even numbers are P, odd N
ADC0_OUT[15:0]
ADCSMA0
ADCSMA1
ADCSMA2
ADCSMA3
SCLK0P
SCLK0N
From Clock Generators
ADC
ADC1
Contains U7 in Sheet 3
ADC1_OUT[15:0]
ADCSMA4
ADCSMA5
ADCSMA6
ADCSMA7
SCLK1P
SCLK1N
ADC2
Contains U12 in Sheet 4
ADC2_OUT[15:0]
ADCSMA8
ADCSMA9
ADCSMA10
ADCSMA11
SCLK2P
SCLK2N
Could possibly have clocks from one ADC provide the clocks for all 3.
Could then not hook up the clocks from the other 2.
A compromise could be to hook up 2 of the 3 clocks.
Can use slide on SMA Emerson 142-0701-801
Short wires from SMA Connectors on box soldered to this TP.
Title
SNAP, A/D CONVERTERS
Size B
Document Number <Doc>
Rev C
Date: Wednesday, February 17, 2016
Sheet 10 of 27

VCC2V5
VCC2V5
M0 is 1 for SPI mode
U26
C192
0.1
See Sheet 27 of the KC705 Schematic
FPGA_FCS
SN74LVC1G18DBVR
Connect A to Y0 and Y1 when S=1
Digikey 296-15568-1-nd
M[2:0] Determines the configuration mode.
See Sheet 27 of the KC705 Schematic
VCCAUX
L30 BK1005HM601-T
L31 BK1005HM601-T
C603 470nf
C604 100nf
VCCADC
GNDADC
BANK 0
See Sheet 3 of the KC705 Schematic
U25-1
XC7K160T-FFG676
Digikey CKN6074-ND
SDA05H1SBD
S1
SPI Select Switch
ON = SPI Divide
OFF = SPI External
QSPI_CS_B
FPGA_INIT_B
QSPI_IC_CS_B
R141 1.21K
R142 1.21K
R143 1.21K
FPGA_M0
FPGA_M1
FPGA_M2
JTAG_TDO
XADC_DXN
XADC_DXP
FPGA_DONE
PROGRAM_B
FPGA_INIT_B
Configuration Clock to SPI Memory
CCLK
R149 DNP
C193 DNP
VCC2V5_FPGA
VCC3V3
V3.3-LIMIT2
R144
R145 4.7K
R146 4.7K
R147 4.7K
R148 4.7K
JTAG_TDO
JTAG_TMS
JTAG_TCK
JTAG_TDI
SN74AVC4T245RSVR
FPGA_TMS_BUF
FPGA_TCK_BUF
FPGA_TDI_BUF
R229 100
R153 330
FPGA_DONE
Level shift to 3.3V then to PI.
FPGA_INIT_B can be switched to FPGA_DONE
FPGA_PROG_B from header for
external programming
TDO not buffered here to conform with KC705 design
DNP - Do Not Populate
Scatter ground test points around the board.
A pin can be soldered in for a scope ground.
See Sheet 3 of the KC705 Schematic
R154 4.7K
FPGA_PROG_B
From Raspberry Pi or External Header
C194 0.1
C195 0.1
U28
Change Levels from
3.3V to 2.5V
SW1
TL3301EF100QG
DS3
SML-LX0603GW-TR
R155 27.4 1%
For
monitoring
Xilinx
temperature
JP4
HEADER 1X2
GNDTP2
GNDTP3
GNDTP4
GNDTP5
GNDTP6
GND PIN
J3
J11
Molex 87831-1420
Molex 87833-1420
Vertical pins for board interior Digikey WM17469-ND
Right angle pins for board edge Digikey WM18863-ND
For use with Digilent JTAG USB Cable Part#250-003P
J3 & J11 changed to industry standard format connectors for Rev B

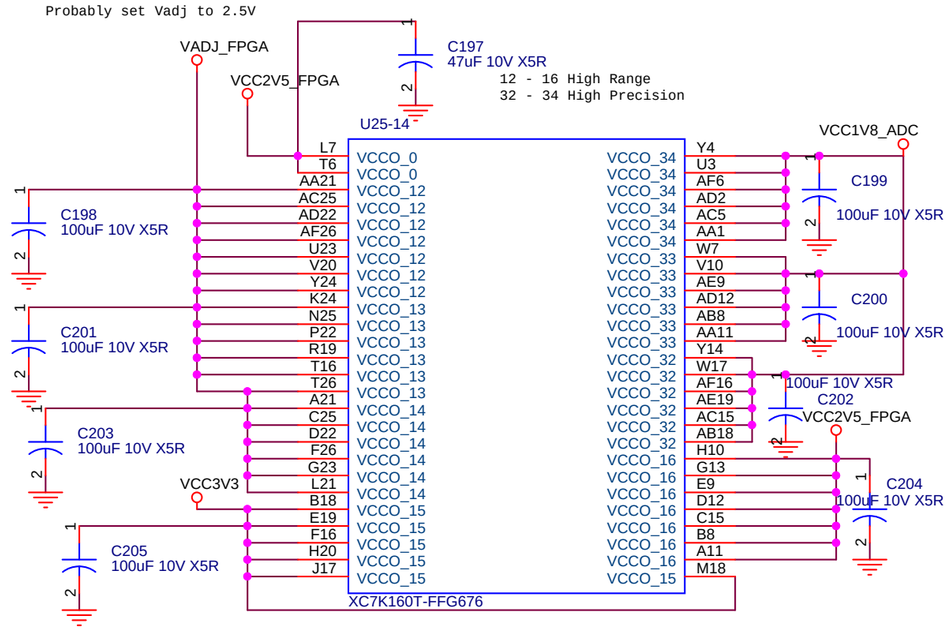
Title	SNAP, JTAG and Bank 0	
Size B	Document Number <Doc>	Rev C
Date: Thursday, February 18, 2016	Sheet 11 of 27	



See KC705 Sheet 25



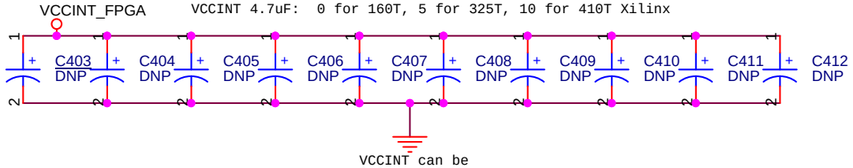
Probably set Vadj to 2.5V



See Sheet 12 of KC705

HR I/O Bank has 3.465 VCCO max
HP I/O Bank has 1.89 VCCO max

VCCBRAM 330 uF: have 0 for 160T, 0 for 325T, 1 for 410T Xilinx

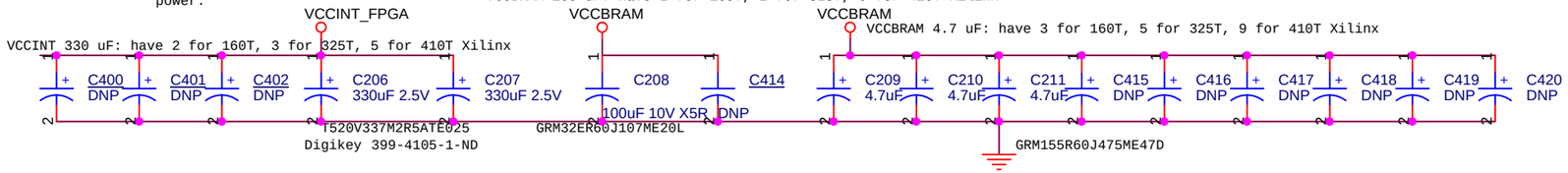


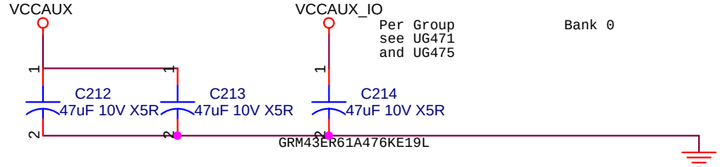
See the SNAP board design guide for a discussion of the Kintex Decoupling Capacitors.

VCCINT can be 0.9 or 1.0 V to trade off speed and power.

Per UG483, the xc7k160t ffg676requires the following bypass capacitors:
See UG483 for layout guidlines

VCCBRAM 100 uF: have 1 for 160T, 2 for 325T, 0 for 410T Xilinx





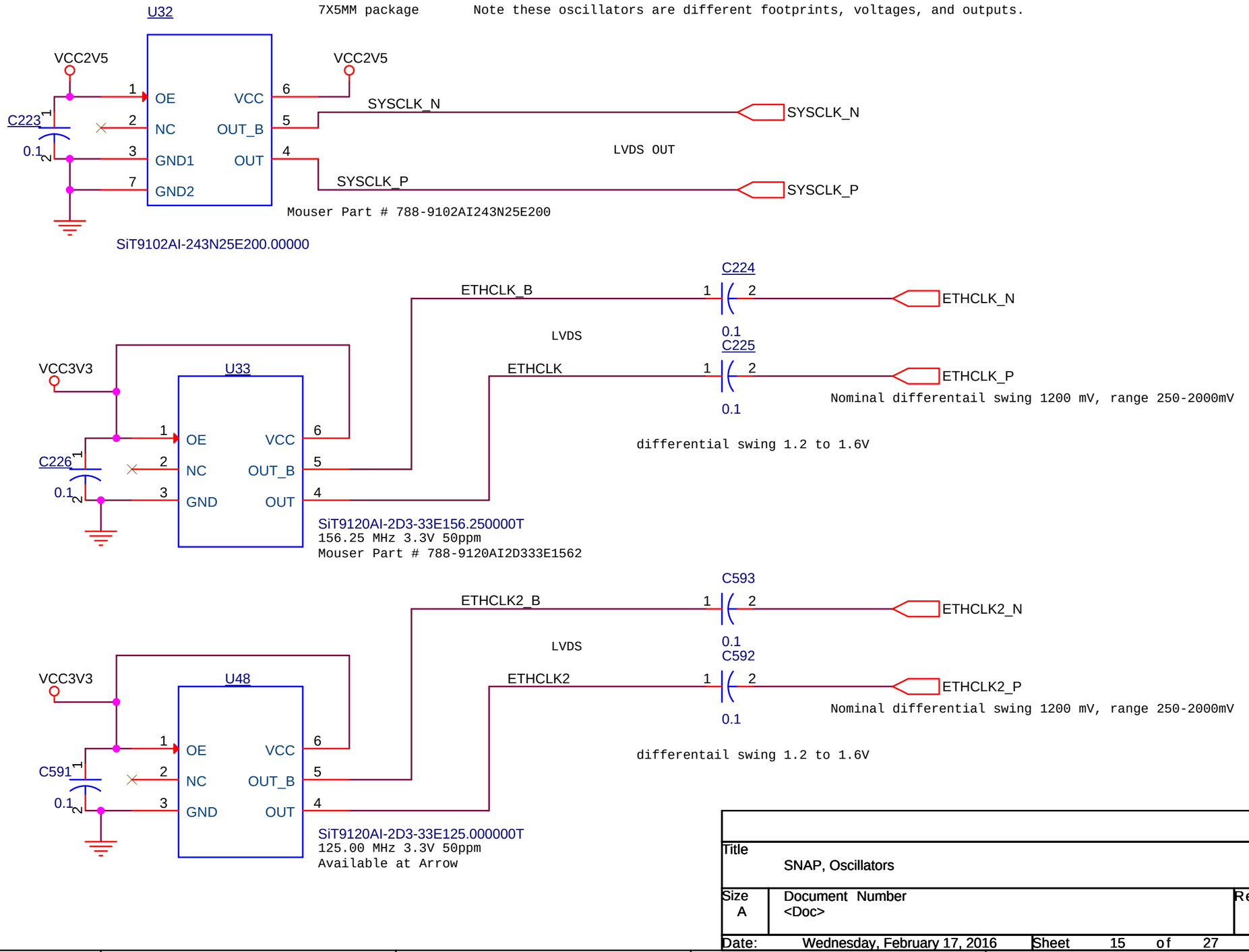
Title: SNAP, FPGA POWER		
Size: B	Document Number: <Doc>	Rev: C
Date: Wednesday, February 17, 2016	Sheet 12 of 27	

Sheet 15
OSCILLATORS
SYSCLK_N
SYSCLK_P
ETHCLK_N
ETHCLK_P
ETHCLK2_N
ETHCLK2_P
OSCILLATORS
CLK200MHZ_N
CLK200MHZ_P
ETHCLK_N
ETHCLK_P
ETHCLK2_N
ETHCLK2_P
USB_TX
USB_CTS
U25-6
HIGH RANGE
VCCO is VCC2V5
J8 IO_0_16
J14 IO_25_16
B9 IO_L10N_T1_16
C9 IO_L10P_T1_16
F10 IO_L11N_T1_SRCC_16
G11 IO_L11P_T1_SRCC_16
D10 IO_L12N_T1_MRCC_16
E10 IO_L12P_T1_MRCC_16
C11 IO_L13N_T2_MRCC_16
C12 IO_L13P_T2_MRCC_16
D11 IO_L14N_T2_SRCC_16
E11 IO_L14P_T2_SRCC_16
F13 IO_L15N_T2_DQS_16
F14 IO_L15P_T2_DQS_16
F12 IO_L16N_T2_16
G12 IO_L16P_T2_16
D13 IO_L17N_T2_16
D14 IO_L17P_T2_16
E12 IO_L18N_T2_16
E13 IO_L18P_T2_16
C13 IO_L19N_T3_VREF_16
C14 IO_L19P_T3_16
H8 IO_L1N_T0_16
H9 IO_L1P_T0_16
B11 IO_L20N_T3_16
IO_L9P_T1_DQS_16 A9
IO_L9N_T1_DQS_16 A8
IO_L8P_T1_16 D9
IO_L8N_T1_16 D8
IO_L7P_T1_16 F9
IO_L7N_T1_16 F8
IO_L6P_T0_16 H12
IO_L6N_T0_VREF_16 H11
IO_L5P_T0_16 H14
IO_L5N_T0_16 G14
IO_L4P_T0_16 J11
IO_L4N_T0_16 J10
IO_L3P_T0_DQS_16 J13 USB_RTS
IO_L3N_T0_DQS_16 H13 USB_RX
IO_L2P_T0_16 G10
IO_L2N_T0_16 G9
IO_L24P_T3_16 A13
IO_L24N_T3_16 A12
IO_L23P_T3_16 B15
IO_L23N_T3_16 A15
IO_L22P_T3_16 B10
IO_L22N_T3_16 A10
IO_L21P_T3_DQS_16 B14
IO_L21N_T3_DQS_16 A14
IO_L20P_T3_16 B12
XC7K160T-FFG676
DONE33V
TX_DISABLE0
TX_DISABLE1
SFP1
Contains P1 in Sheet 24
IIC_SCL_MAIN
IIC_SDA_MAIN
SFP_TX_DISABLE
SFP_RX_P
SFP_RX_N
SFP_TX_P
SFP_TX_N
SFP_TXF
SFP_MD
SFP_LOS
SFP1_TXF
SFP1_MD
SFP1_LOS
SFPCONN
SFP2
Contains P2 in Sheet 25
SFP2_TXF
SFP2_MD
SFP2_LOS
Sheet 26
SWITCHES
SW0
SW1
SW2
SW3
LED0
LED1
LED2
LED3
LED4
LED5
OUT1PPS
DONE33V
FPGA_DONE
SWITCHES
Leave Unused REFCLKs unconnected
GND
U25-11
See Sheet 9 of the KC705
D5 MGTREFCLK0N_116
D6 MGTREFCLK0P_116
F5 MGTREFCLK1N_116
F6 MGTREFCLK1P_116
G3 MGTRXRXN0_116
E3 MGTRXRXN1_116
C3 MGTRXRXN2_116
B5 MGTRXRXN3_116
G4 MGTRXRXP0_116
E4 MGTRXRXP1_116
MGTXTXP3_116 A4
MGTXTXP2_116 B2
MGTXTXP1_116 D2
MGTXTXP0_116 F2
MGTXTXN3_116 A3
MGTXTXN2_116 B1
MGTXTXN1_116 D1
MGTXTXN0_116 F1
MGTXRXP3_116 B6
MGTXRXP2_116 C4
GND
GND
XC7K160T-FFG676
See UG476 7 Series FPGAs GTX/GTH Tranceivers User Guide
10 GBE high speed traces require special layout care.
See UG483 - 7 Series FPGAs PCB Design and Pin Planning Guide
VCCMGTA
R156 100
ETHCLK2_N
ETHCLK2_P
ETHCLK_N
ETHCLK_P
U25-10
See Sheet 9 of the KC705
M5 MGTAVTTRCAL_115
H5 MGTREFCLK0N_115
H6 MGTREFCLK0P_115
K5 MGTREFCLK1N_115
K6 MGTREFCLK1P_115
M6 MGTRREF_115
R3 MGTRXRXN0_115
N3 MGTRXRXN1_115
L3 MGTRXRXN2_115
J3 MGTRXRXN3_115
R4 MGTRXRXP0_115
MGTXTXP3_115 H2
MGTXTXP2_115 K2
MGTXTXP1_115 M2
MGTXTXP0_115 P2
MGTXTXN3_115 H1
MGTXTXN2_115 K1
MGTXTXN1_115 M1
MGTXTXN0_115 P1
MGTXRXP3_115 J4
MGTXRXP2_115 L4
MGTXRXP1_115 N4
GND
GND
GND
XC7K160T-FFG676
USB_SHIELD
J10
CONN_USB_MINI_B-VERT
TE Connectivity 1734753-1
Digikey A107790-ND
SHLD1
SHLD2
SHLD3
GND
ID
D_P
D_N
VBUS
R460 DNP
C215 DNP
C216 0.1
HZ0805E601R-10
Digikey 240-2399-2--ND
L13 FERRITE-600
USB_GND
X1
CATH3
ANODES
CATH2
CATH1
SP0503BAHTG
Transient Surpressor
Digikey F2715CT-ND
SFPCONN
J4
SHLD9
DNP
Molex 548190589 (horizontal)
Digikey WM3895CT-ND
USB_D_P
USB_D_N
VCC2V5
C217 0.1
C218 1UF 25V
C219 0.1
4.7K R157
VBUS_USB
L14
FERRITE-600
HZ0805E601R-10
Digikey 240-2399-2--ND
C220 0.1
C221 1UF 25V
VBUS
U29
CP2103-GM
CNR_GND
RI
GND
D+
D-
VIO
VDD
REGIN
DCD
DTR
DSR
TXD
RXD
RTS
CTS
NC6
NC5
GPIO0
GPIO1
GPIO2
GPIO3
NC4
VBUS
RST_B
NC1
SUSPEND_B
SUSPEND
NC2
NC3
CTR_GND
USB BUS POWERED
Digikey 336-1164-ND
To Bank 15 above
USB_TX
USB_RX
USB_RTS
USB_CTS
See Sheet 27 of the KC705
Group SFP status signals
for convnience in ascending
to next level of hierarchy
SFP_STAT[5:0]
SFP1_TXF SFP_STAT0
SFP1_MD SFP_STAT1
SFP1_LOS SFP_STAT2
SFP2_TXF SFP_STAT3
SFP2_MD SFP_STAT4
SFP2_LOS SFP_STAT5
M23
G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 G11 G12 G13 G14 G15 G16 G17 G18 G19
SFP_CAGE
If desired for a card cage J4, a right angle USB
can be installed in parallel.
If used, also install a zero Ohm resistor for 1206 R460
J4 is DNP if the card is in the box, since the shield pins
would short out to the ground rail.
Title
SNAP, SFP+ Connector and Cage
Size B
Document Number
<Doc>
Rev C
Date: Wednesday, February 17, 2016
Sheet 13 of 27

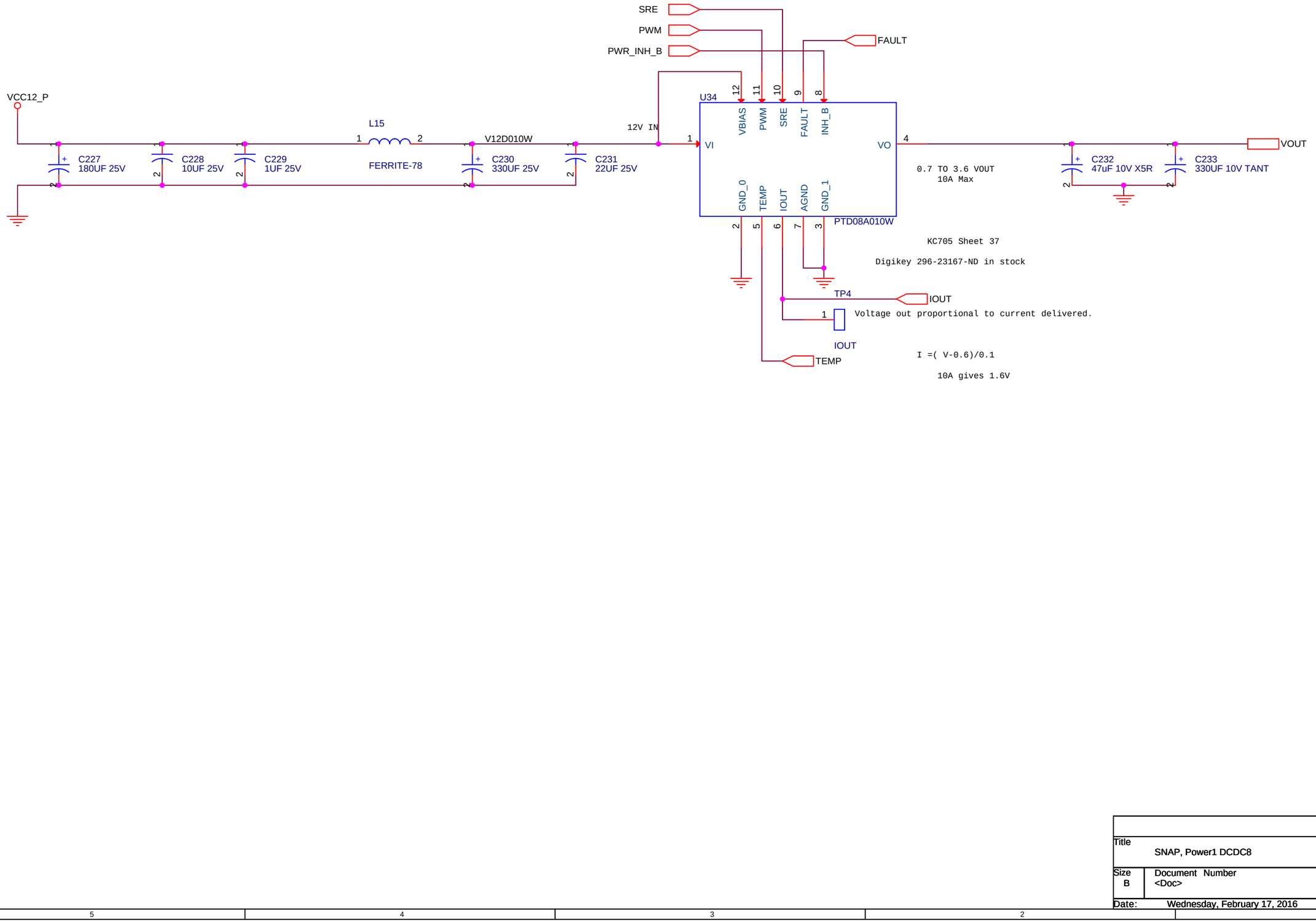
FLASH_D[3:0]
FLASH_D[3:0]
SFP_STAT[5:0]
SFP_STAT[5:0]
The ZDOC Clock Pairs C19&C20 plus F19&F20 must go to MRCC clock inputs.
ZDOK PINS 15-20
U25-4
PWRGD5V
VADJ_FPGA
R158
4.7K
SYNTH_PWR
TEST2
TEST3
FPGA_FCS
FPGA_FCS
SFP_STAT2
SFP_STAT3
SFP_STAT0
SFP_STAT1
TEST6
FLASH_D2
FLASH_D3
R433
DNP
R432
1.00K
XC7K160T-FFG676
Roach II Clks
ZDOK Clock pair
ZDOK Clock pair
Roach II Clks
Roach II Clks
TX_DISABLE1
U25-3
Roach II Clks
Roach II Clks
Roach II Clks
Roach II Clks
ZDOK PINS 7-14
XC7K160T-FFG676
GPIO_DIP_SW4
GPIO_DIP_SW1
GPIO_DIP_SW0
GPIO_DIP_SW3
GPIO_DIP_SW2
VADJ_FPGA
Digikey CKN6074-ND
SDA05H1SBD
S2
R1592
R1602
R1612
R1622
R1632
4.7K
For VADJ_FPGA =3.3V, min VIH=2.0, max VIL=.8V
PU not need for open inputs
See Sheet 5 of KC705
Gets VCCO from VADJ_FPGA
See Sheet 4 of KC705
Gets VCCO from VADJ_FPGA
See Sheet 3 of KC705
ZDOK PINS 1-6
Gets VCCO from VADJ_FPGA
TX_DISABLE0
U25-2
XC7K160T-FFG676
VADJ_FPGA
SMATP13
C222
0.1
R165
49.9 1/4W
U30
SN65LVDS1
ONEPPS
ONEPPSP
ONEPPSN
PIV3V3BUF
Sense 3.3V Generated on the PI
R1642
4.7K
To Raspberry PI B+
PI2
PI_V3V3
VCC5V0
Powers Raspberry Pi
NC so 5V and GND aren't right next to each other.
PMBUS_DATA
PMBUS_CLK
PMBUS_CTRL
JTAG_TMS
JTAG_TDI
PMBUS_ALERT
JTAG_TDO
JTAG_TCLK
FPGA_PROG_B
DONE33V
SPIMOSI
SPIMISO
SPICLK
HDR40
Digikey S2012EC-20-ND
1 is P, 2 is N on ZDOK
ZDOK1
Sheet 27
ZDOK
SM_FAN_PWM
U25-5
XC7K160T-FFG676
Gets VCCO from 3.3 Volts
SYNTH_DATA
SYNTH_LE
SYNTH_CE
SYNTH_BE
SYNTH_CLK_XIL
SYNTH_CLK
Give 2.5V impedance controlled signal
R434
100
330
R435
VADJ_FPGA
U31
CATHODE
ANODE
IN
PMBD7000
R436
R437
R438
SCLK0
SCLK1
SCLK2
SMATP14
To SMA Connectors via Test Points
SMATP15
From Xilinx
SYNTH_OSC
SAMP_CLK
CLKGEN1
Sheet 8
To ADCs
SCLK0P
SCLK0N
SCLK1P
SCLK1N
SCLK2P
SCLK2N
SCLK3P
SCLK3N
To FPGA
From Xilinx
CLK_SEL_A
CLK_SEL_B
SYNTHMUXOUT
SYNTHMUXOUT added for Rev C
CLKGEN
Connector to Xilinx for TBD purposes.
J9
PTC06DAAN
Move SYNTH_(CLK,DATA,LE,CE,BE) to 3.3V, then put series/parallel resistor on SYNTH_CLK.
SCLK[2:0]
SCLK[2:0]

Title: SNAP, ZDOK CONNECTOR
Size: B
Document Number: <Doc>
Rev: C
Date: Wednesday, February 17, 2016
Sheet 14 of 27

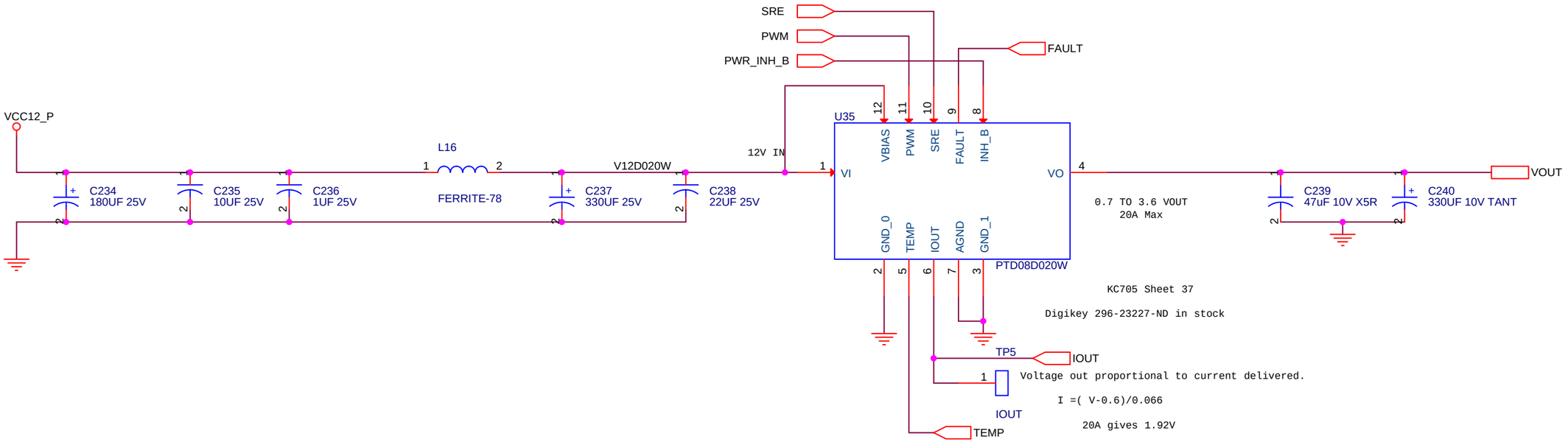
See UG472 7 Series FPGAs
Clocking Resources User Guide



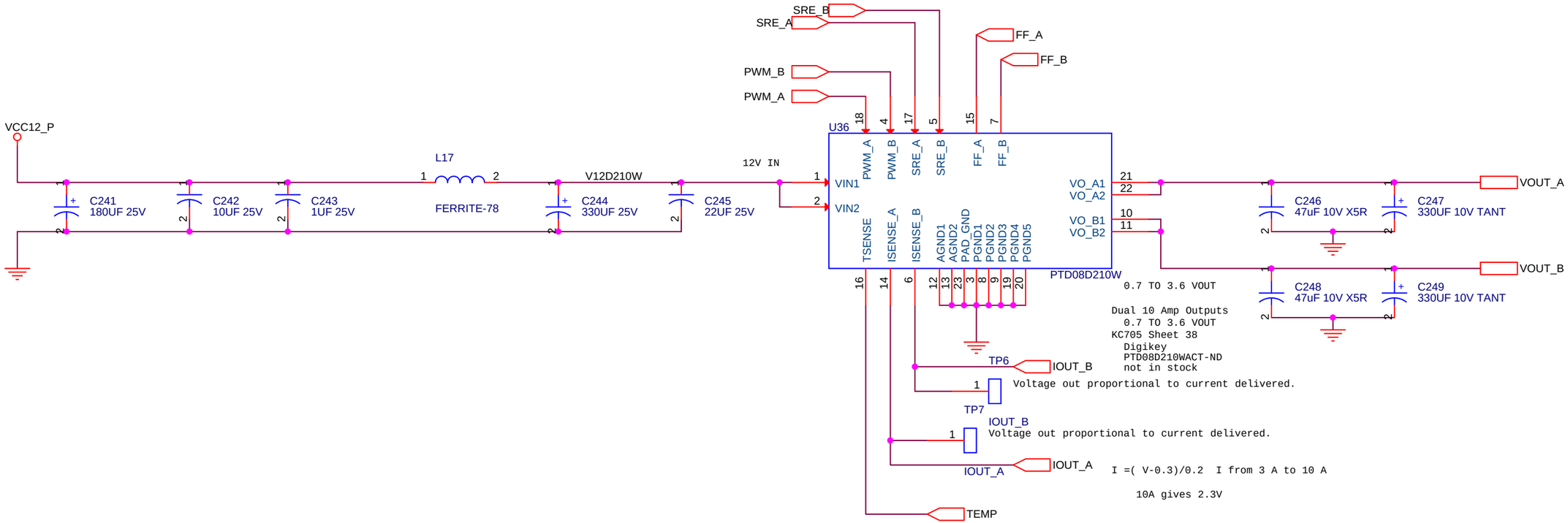
Title: SNAP, Oscillators		
Size: A	Document Number: <Doc>	Rev: C
Date: Wednesday, February 17, 2016	Sheet 15 of 27	



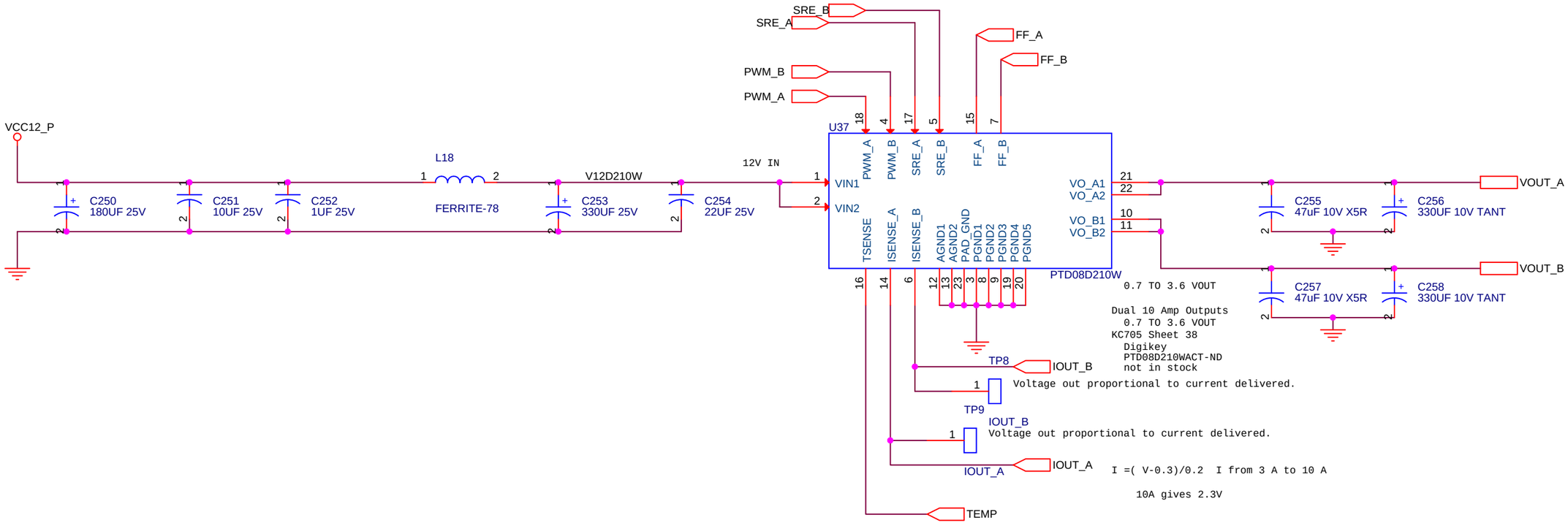
Title	SNAP, Power1 DCDC8	
Size B	Document Number <Doc>	Rev C
Date: Wednesday, February 17, 2016	Sheet 16 of 27	



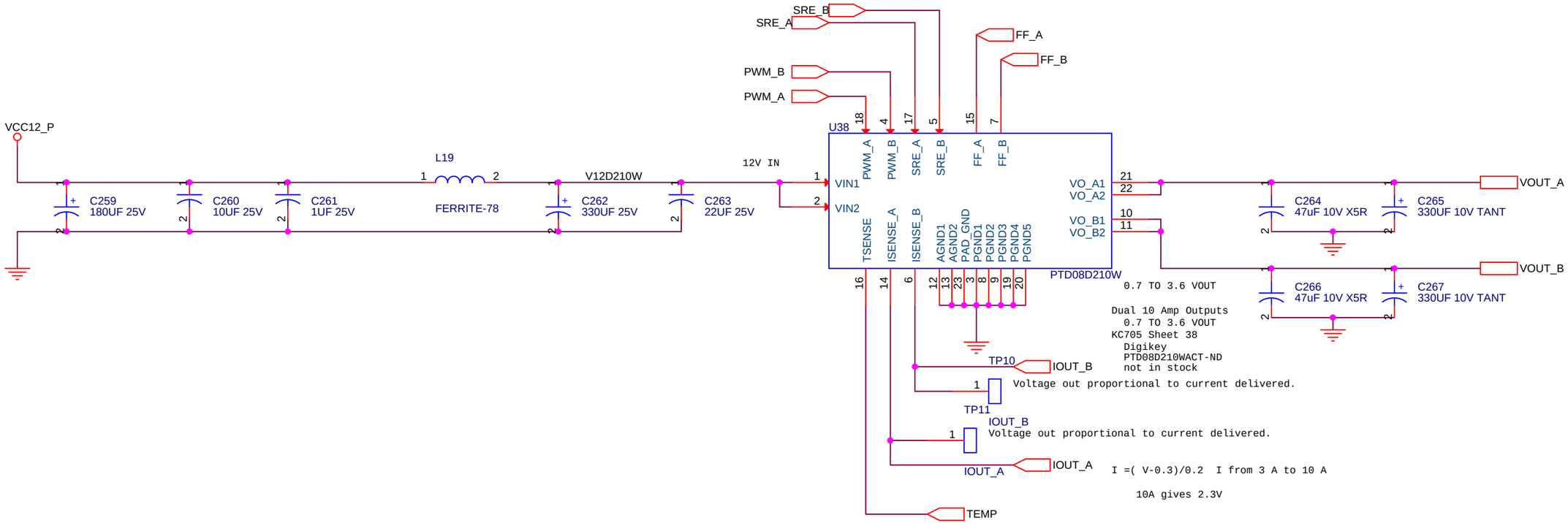
Title	SNAP, Power1 DCDC1	
Size B	Document Number <Doc>	Rev C
Date: Wednesday, February 17, 2016	Sheet 17 of 27	



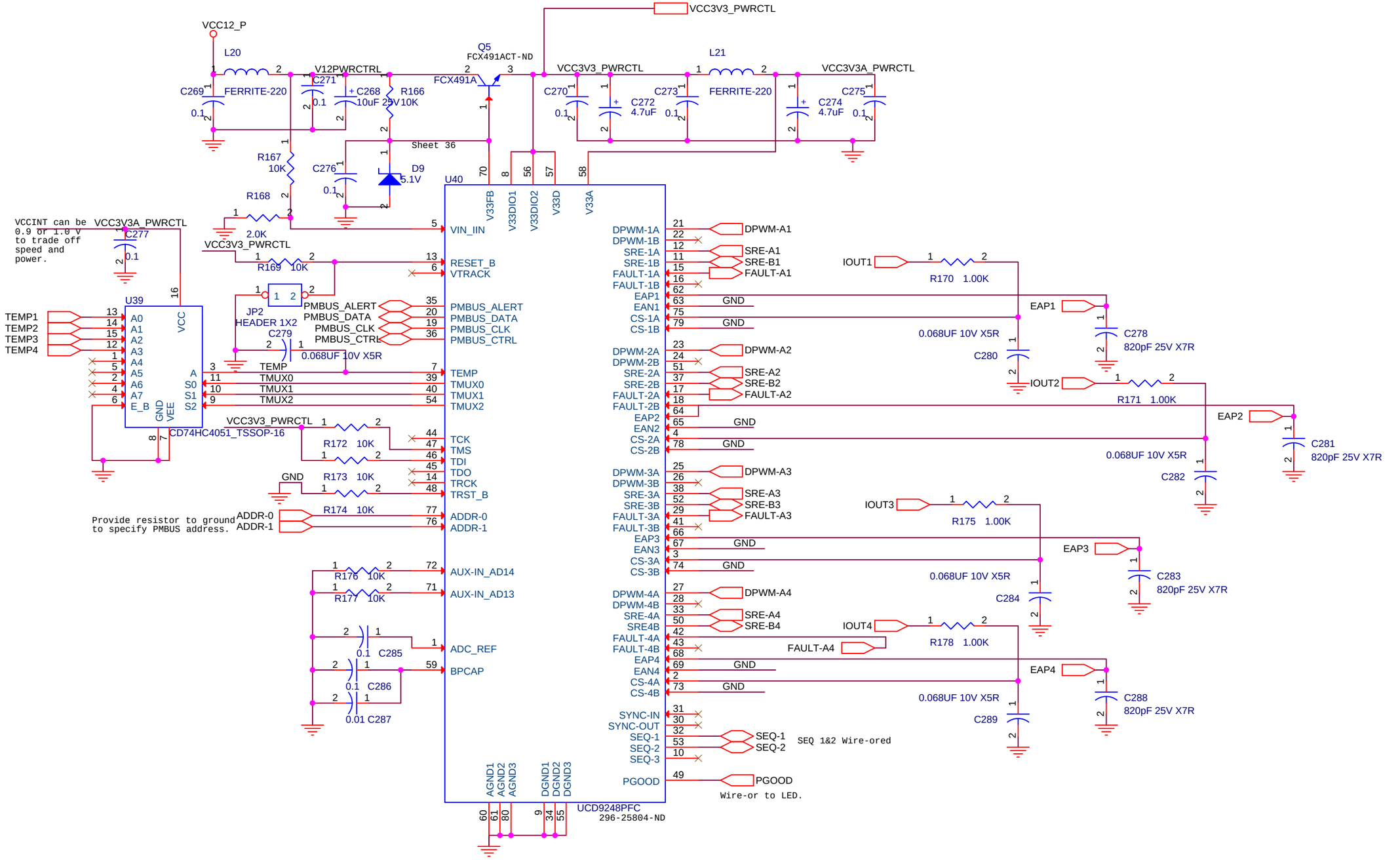
Title	SNAP, Power1, DCDCx	
Size B	Document Number <Doc>	Rev C
Date: Wednesday, February 17, 2016	Sheet 18 of 27	



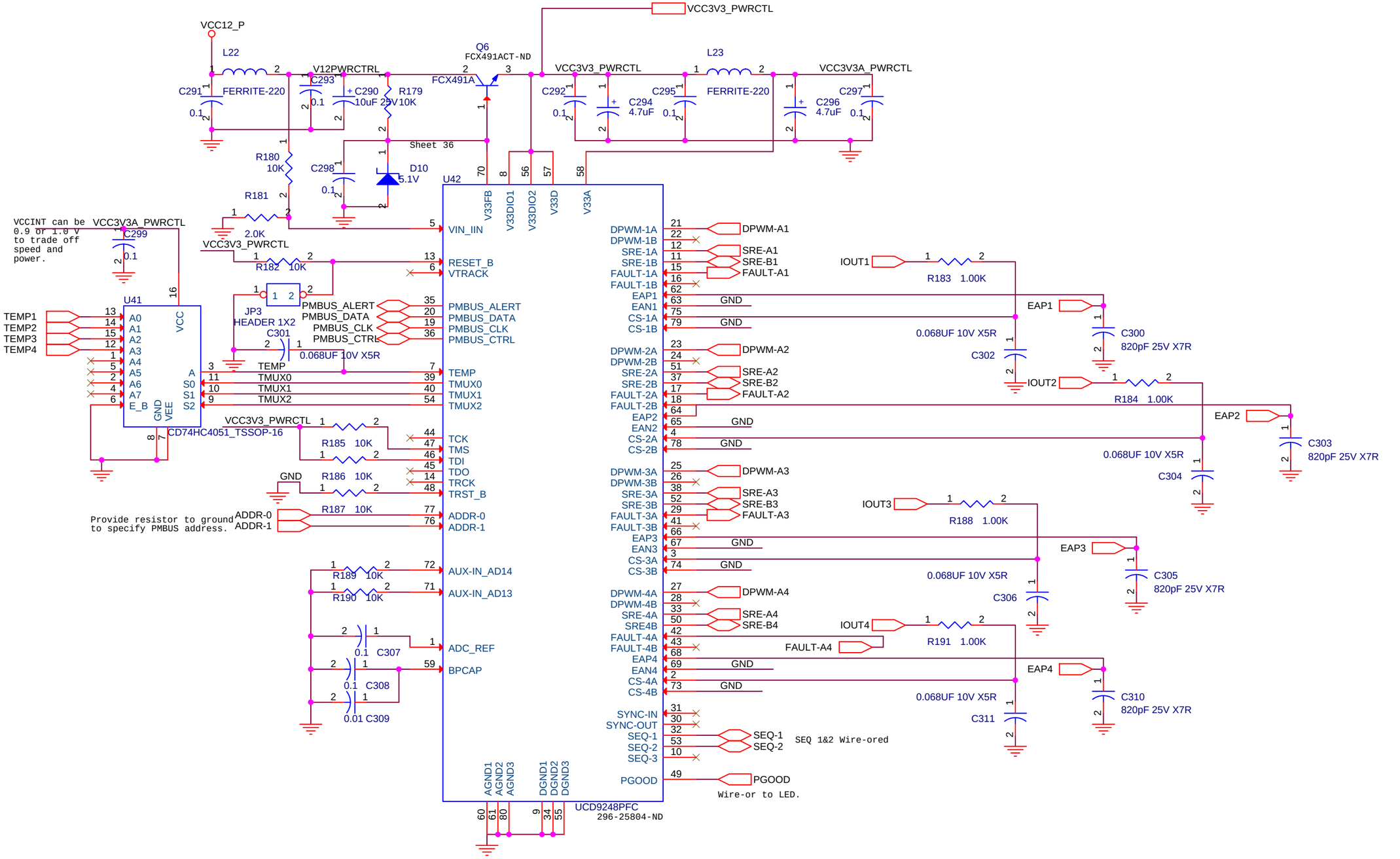
Title	SNAP, Power1, DCDCx	
Size B	Document Number <Doc>	Rev C
Date: Wednesday, February 17, 2016	Sheet 19 of 27	



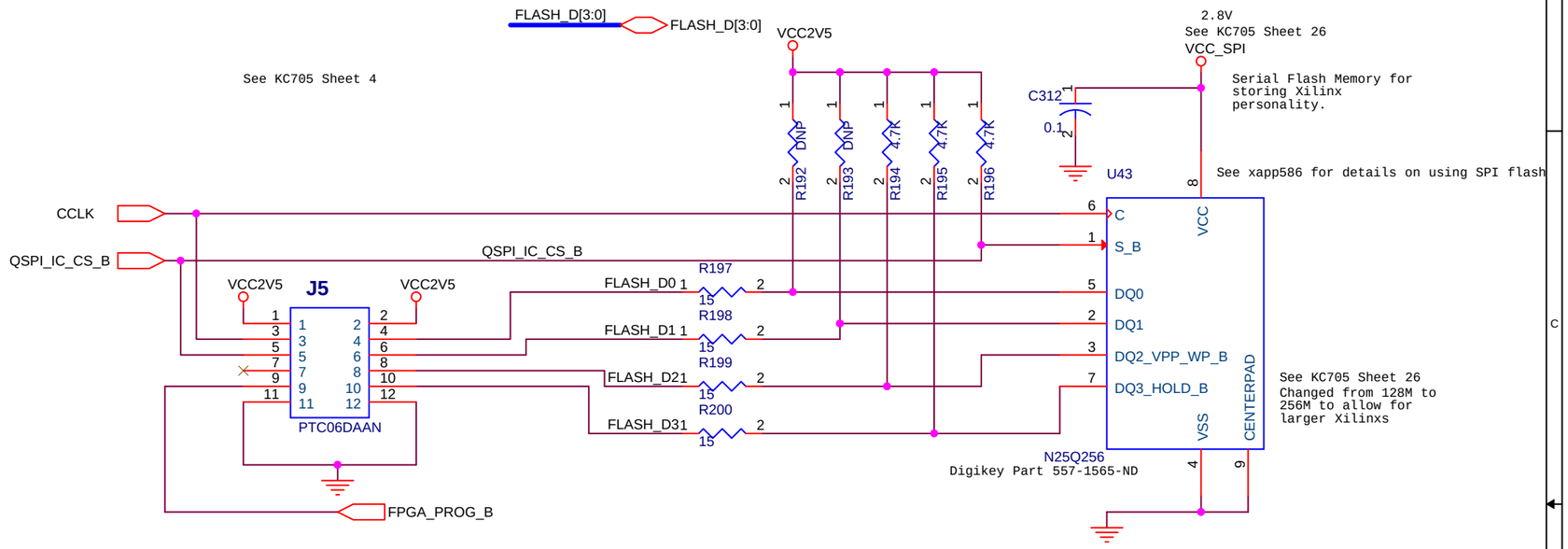
Title	SNAP, Power1, DCDCx	
Size B	Document Number <Doc>	Rev C
Date: Wednesday, February 17, 2016	Sheet 20 of 27	



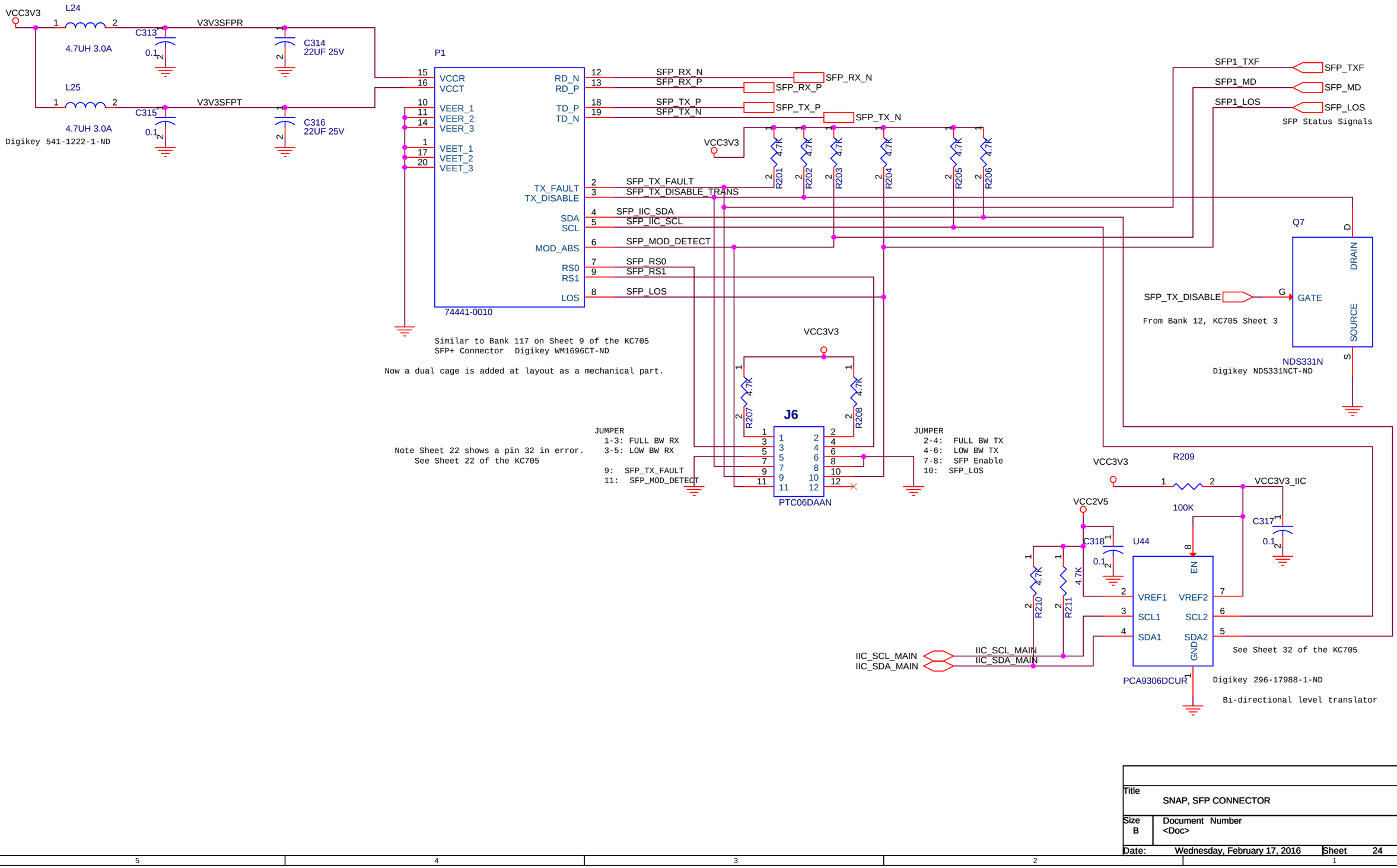
Title	SNAP, DIGITAL PWM SYSTEM CONTROLLER	
Size B	Document Number <Doc>	Rev C
Date: Wednesday, February 17, 2016	Sheet 21 of 27	



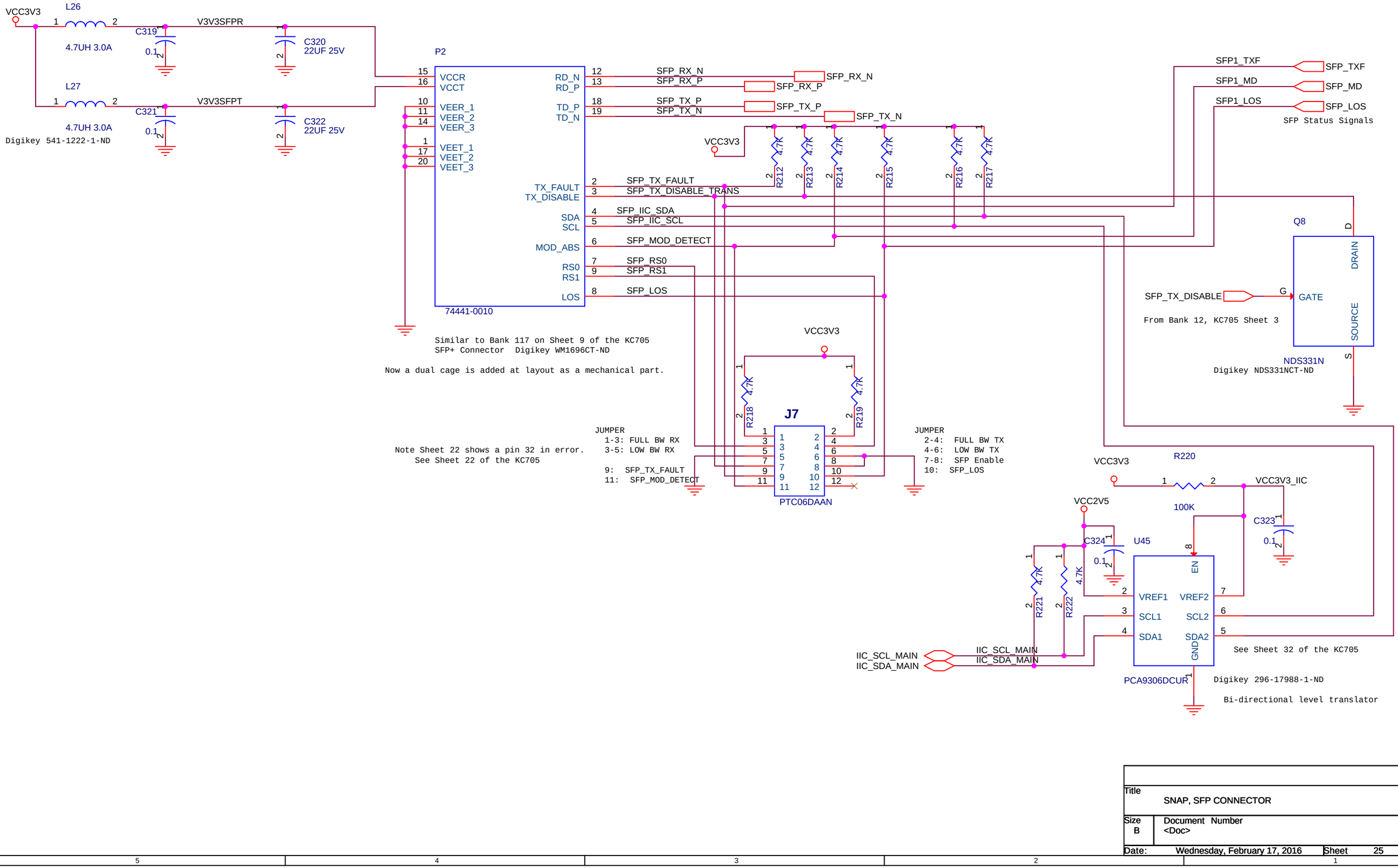
Title	SNAP, DIGITAL PWM SYSTEM CONTROLLER	
Size B	Document Number <Doc>	Rev C
Date: Wednesday, February 17, 2016	Sheet 22 of 27	



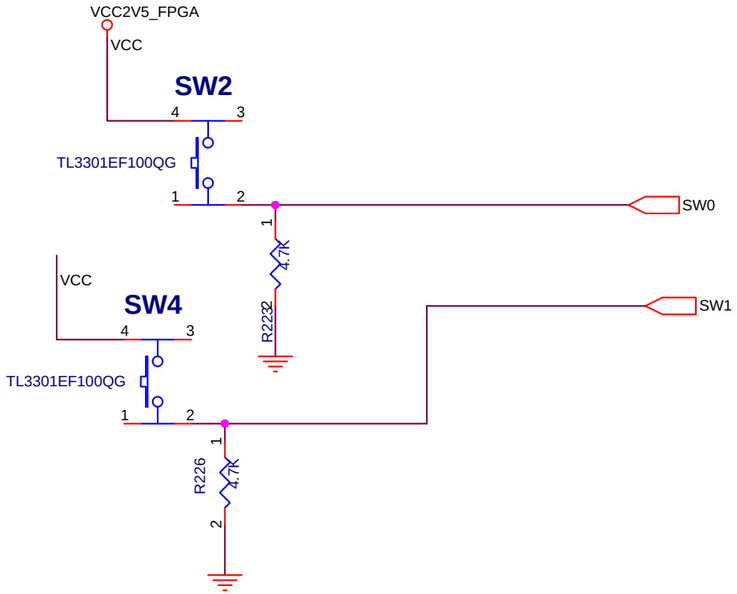
Title	SNAP, FPGA QSPI	
Size B	Document Number <Doc>	Rev C
Date: Wednesday, February 17, 2016	Sheet 23 of 27	

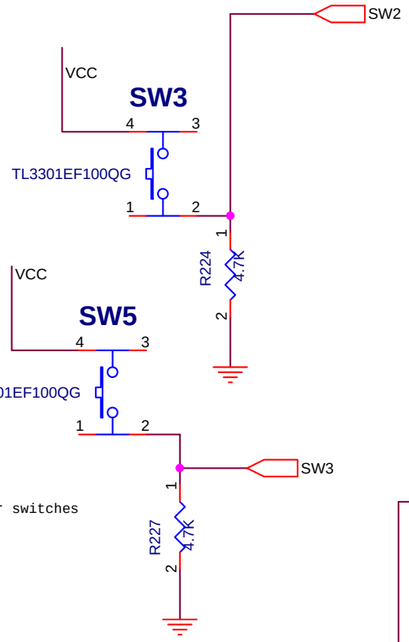


Title	SNAP, SFP CONNECTOR	
Size B	Document Number <Doc>	Rev C
Date: Wednesday, February 17, 2016	Sheet 24 of 27	



Title	SNAP, SFP CONNECTOR	
Size B	Document Number <Doc>	Rev C
Date: Wednesday, February 17, 2016	Sheet 25 of 27	





See Sheet 29 of KC705 for switches

Title	SNAP, SWITCHES AND LEDS	
Size B	Document Number <Doc>	Rev C
Date: Wednesday, February 17, 2016	Sheet 26 of 27	

ZDOK Connector 550-5 as on the Roach Board
Note this is the mirror image of the footprint on the ALMA Phasing Project ZDOK board.

Use 2.5V VCCO
1 is P, 2 is N on ZDOK

Digikey 6367550-5-ND

P3

ZDOK CONNECTOR 550-5

VCC5V0 VCC3V3 VCC2V5 VCCAUX

Supplies 1.8V

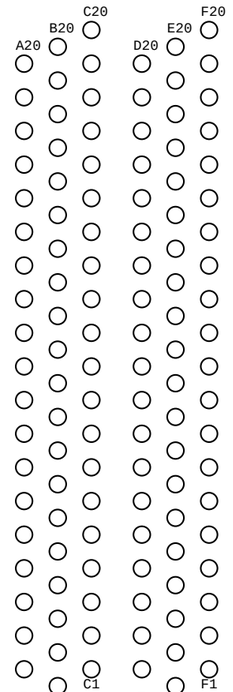
W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5

A[20:1]
D[20:1]
C[20:1]
F[20:1]

CLK0P_C19
CLK0N_C20
CLK1P_F19
CLK1N_F20

W1 X1 Y1 Z1 W6 X6 Y6 Z6

CARD EDGE



ZDOK Pin Layout

Title	SNAP, ZDOK Connector
Size B	Document Number <Doc>
Rev C	
Date: Wednesday, February 17, 2016	Sheet 27 of 27