IBOB Block Diagram

```
┌──────────────┐        ┌──────────────┐
│ 2x diff. clock│       │ 2x diff. clock│
└──────────────┘        └──────────────┘
```

| 40 pair diff. I/O (ZDOK) | 40 pair diff. I/O (ZDOK) | 40 pair diff. I/O (MDR) |

| RS232 | | 80x GPIO |

Xilinx Virtex II Pro 2VP50 FPGA

| 10/100 Ethernet | | 10 Gbps I/O (CX4) |

| Diff. Clock I/O (SMA) | | 10 Gbps I/O (CX4) |

| Configuration PROM | 36x512k SRAM | 36x512k SRAM |