Uses Xilinx Kintex XC7K160T-2FFG676

FPGA0
BANK 0
FPGA_FCS
CCLK
QSPI_IC_CS_B
FPGA_PROB_B

FPGAJTAG
Contains JTAG Connectors

FPGA14
BANK 14 High Range
CCLK
FPGA_FCS
QSPI_IC_CS_B
FPGA_PROB_B

QSPIFPGA
Contains SPI Flash for storing the personality

FPGA33
BANK 33 High Precision

FPGACLKS
Contains Clocks and LEDs

FPGA7

FPGAPOWER
Hooking power to the FPGA

FPGA13
BANK 12 High Range
BANK 13 High Range
BANK 16 High Range
TX_DISABLE0
TX_DISABLE1
SCLK0P
SCLK0N
SCLK1P
SCLK1N
SCLK2P
SCLK2N

FPGAZDOK
Contains ZDOK Connector
Contains the Raspberry Pi Interface
Contains Clock Generator Synthesizer

FPGA116
BANK 15 High Range
BANK 115 GTX
BANK 116 GTX
TX_DISABLE0
TX_DISABLE1

FPGASFPP
Contains 2 SFP+ Connectors
Contains USB Interface

FPGA32
BANK 32 High Precision
BANK 34 High Precision
SCLK0P
SCLK0N
SCLK1P
SCLK1N
SCLK2P
SCLK2N
PMBUS_DATA_LS
PMBUS_CLK_LS
PMBUS_ALERT_LS
Contains the 3 ADCs

FPGAADCS

REG1

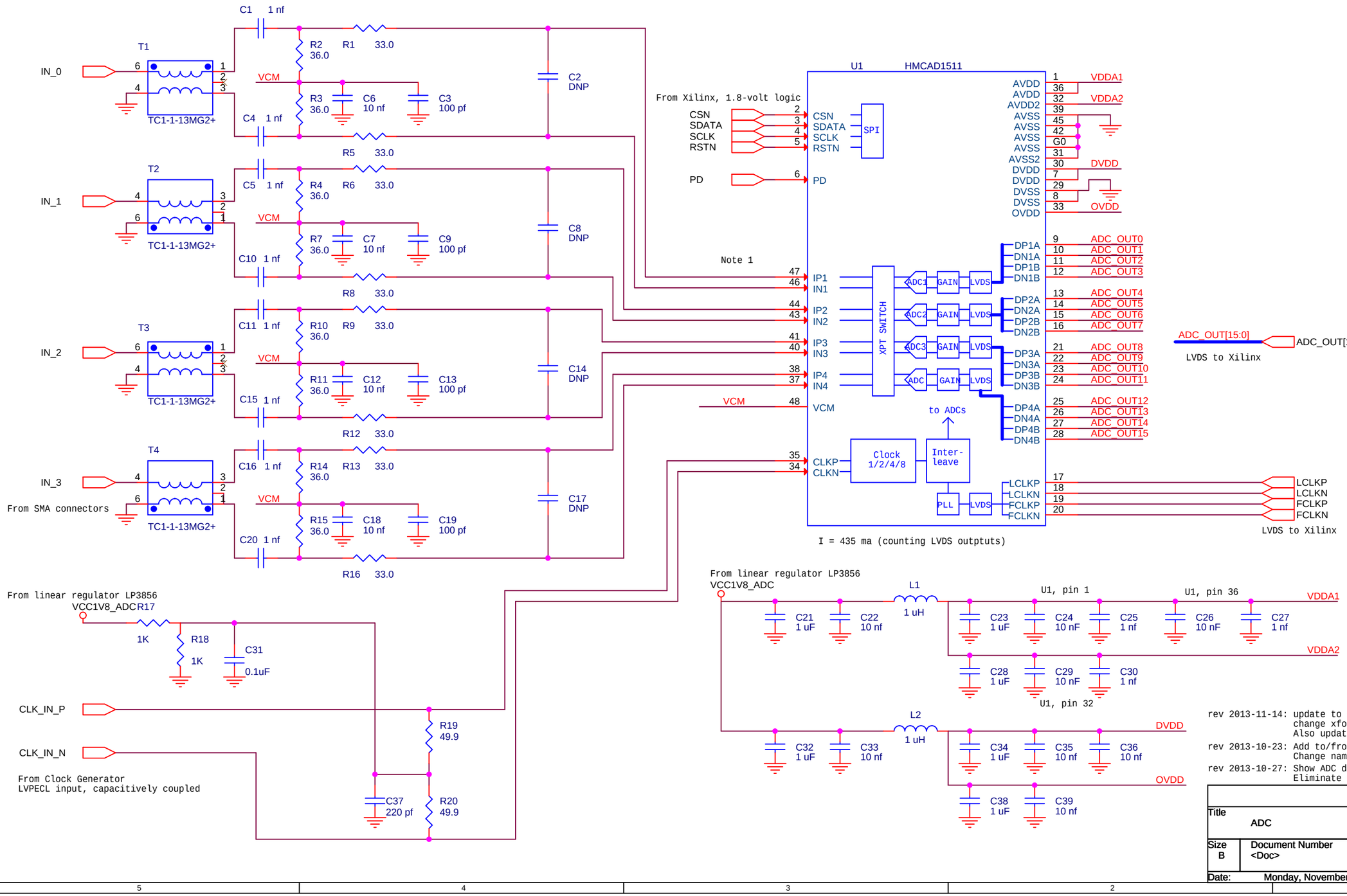
ANALOG_REGULATOR
Contains DC-DC Converters

POWER1
PMBUS_DATA_LS
PMBUS_CLK_LS
PMBUS_ALERT_LS

DIGITAL_POWER_SUPPLIES

Title	SMART NETWORK ADC PROCESSOR (SNAP) BOARD	
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 1 of 27	

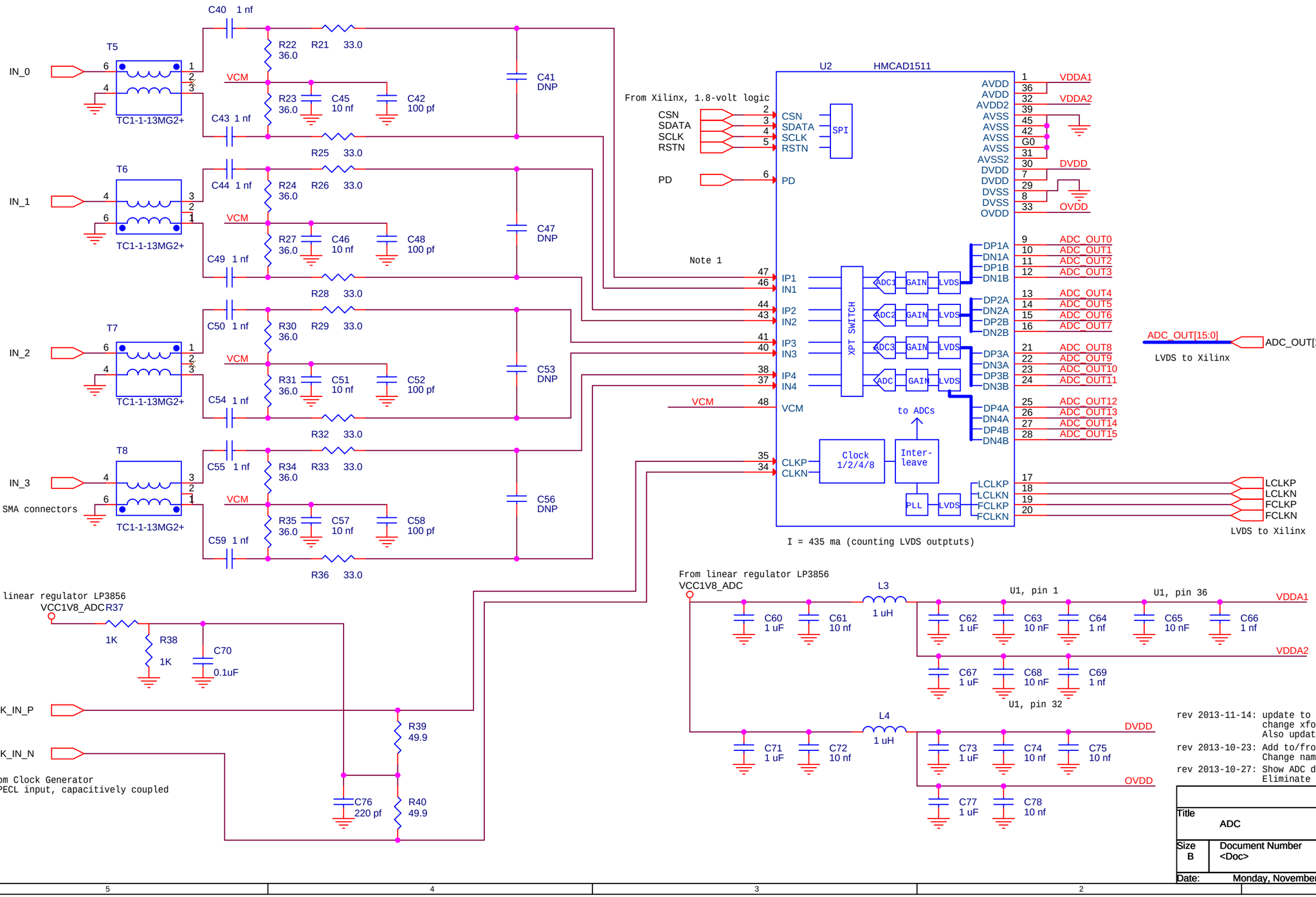
Note 1: Components associated with ADC inputs IP1 and IP3 are on the top side of the board.
Components associated with IP2 adn IP4 are on the bottom side of the board.



rev 2013-11-14: update to 5/28/2013 Berkeley version:
change xformer type and AC coupled xformer.
Also update to preferred values for input terminations
rev 2013-10-23: Add to/from notes for I/O.
Change name and symbol for power
rev 2013-10-27: Show ADC data outputs as bus to simplify high level view.
Eliminate 0.1 uF cap on CLK_IN_P/N

Title: ADC		
Size: B	Document Number: <Doc>	Rev: A
Date: Monday, November 25, 2013	Sheet 2 of 27	

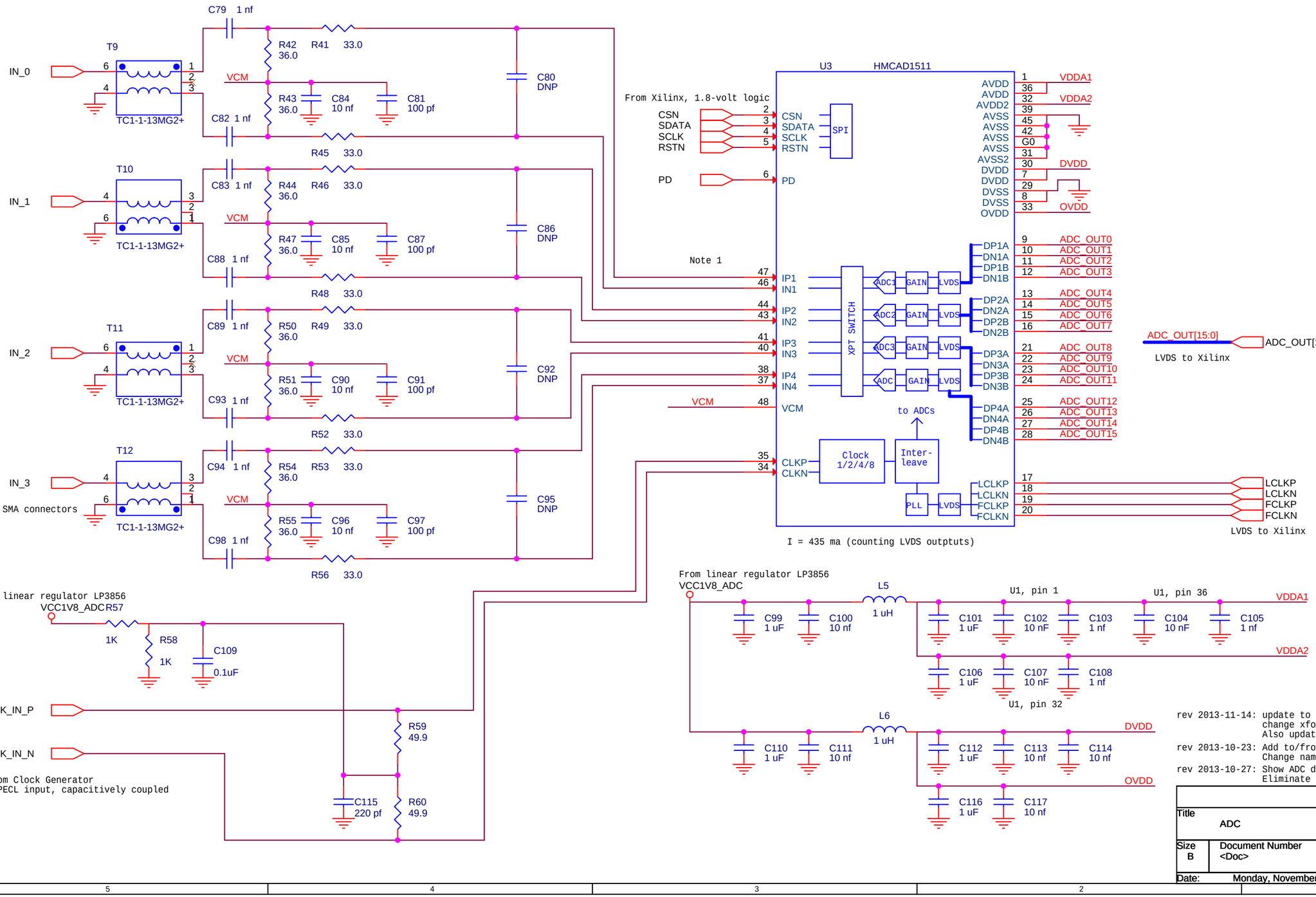
Note 1: Components associated with ADC inputs IP1 and IP3 are on the top side of the board.
Components associated with IP2 adn IP4 are on the bottom side of the board.



rev 2013-11-14: update to 5/28/2013 Berkeley version:
change xformer type and AC coupled xformer.
Also update to preferred values for input terminations
rev 2013-10-23: Add to/from notes for I/O.
Change name and symbol for power
rev 2013-10-27: Show ADC data outputs as bus to simplify high level view.
Eliminate 0.1 uF cap on CLK_IN_P/N

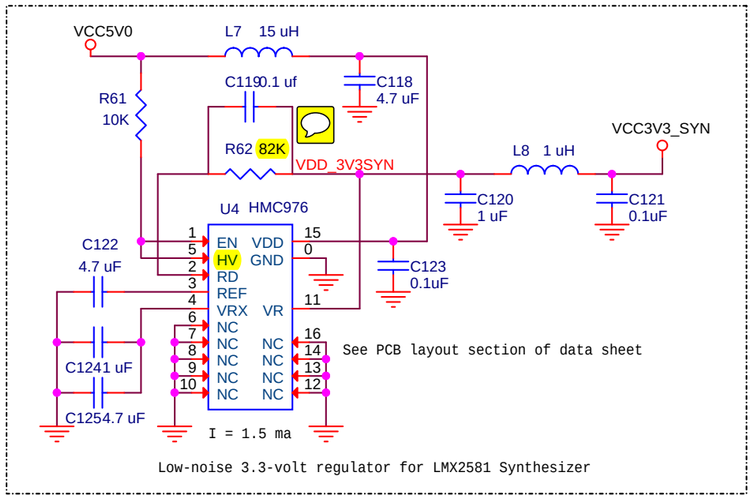
Title: ADC		
Size: B	Document Number: <Doc>	Rev: A
Date: Monday, November 25, 2013	Sheet 3 of 27	

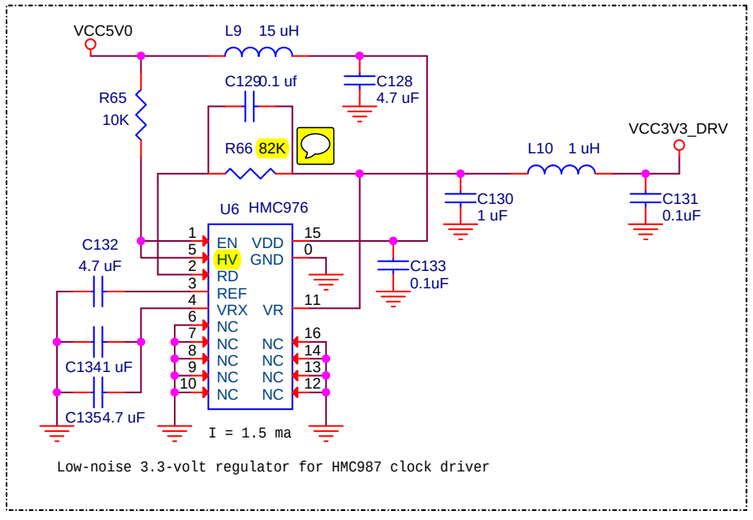
Note 1: Components associated with ADC inputs IP1 and IP3 are on the top side of the board.
Components associated with IP2 adn IP4 are on the bottom side of the board.

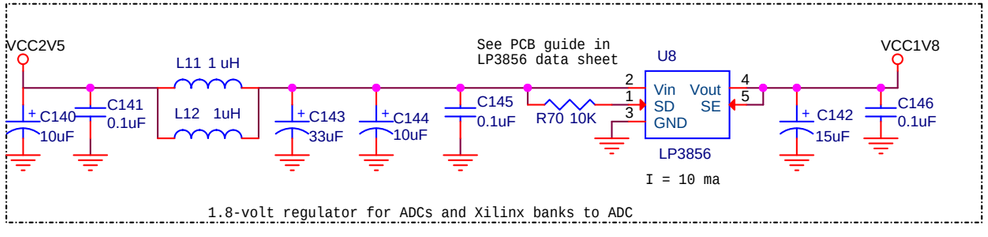


rev 2013-11-14: update to 5/28/2013 Berkeley version:
change xformer type and AC coupled xformer.
Also update to preferred values for input terminations
rev 2013-10-23: Add to/from notes for I/O.
Change name and symbol for power
rev 2013-10-27: Show ADC data outputs as bus to simplify high level view.
Eliminate 0.1 uF cap on CLK_IN_P/N

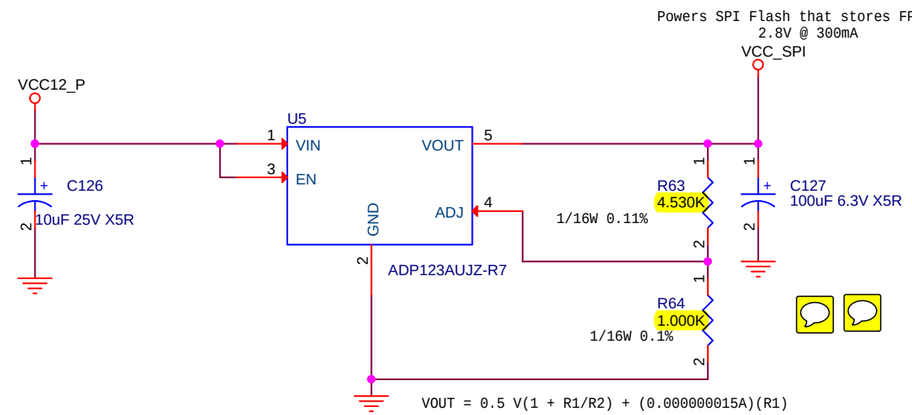
Title: ADC		
Size: B	Document Number: <Doc>	Rev: A
Date: Monday, November 25, 2013	Sheet 4 of 27	

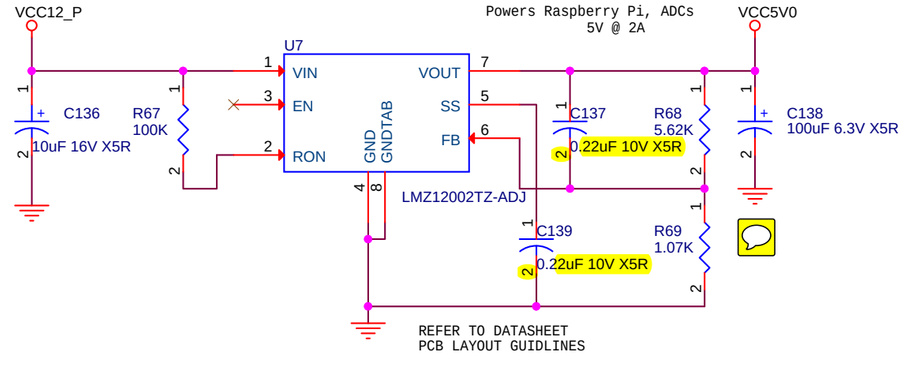






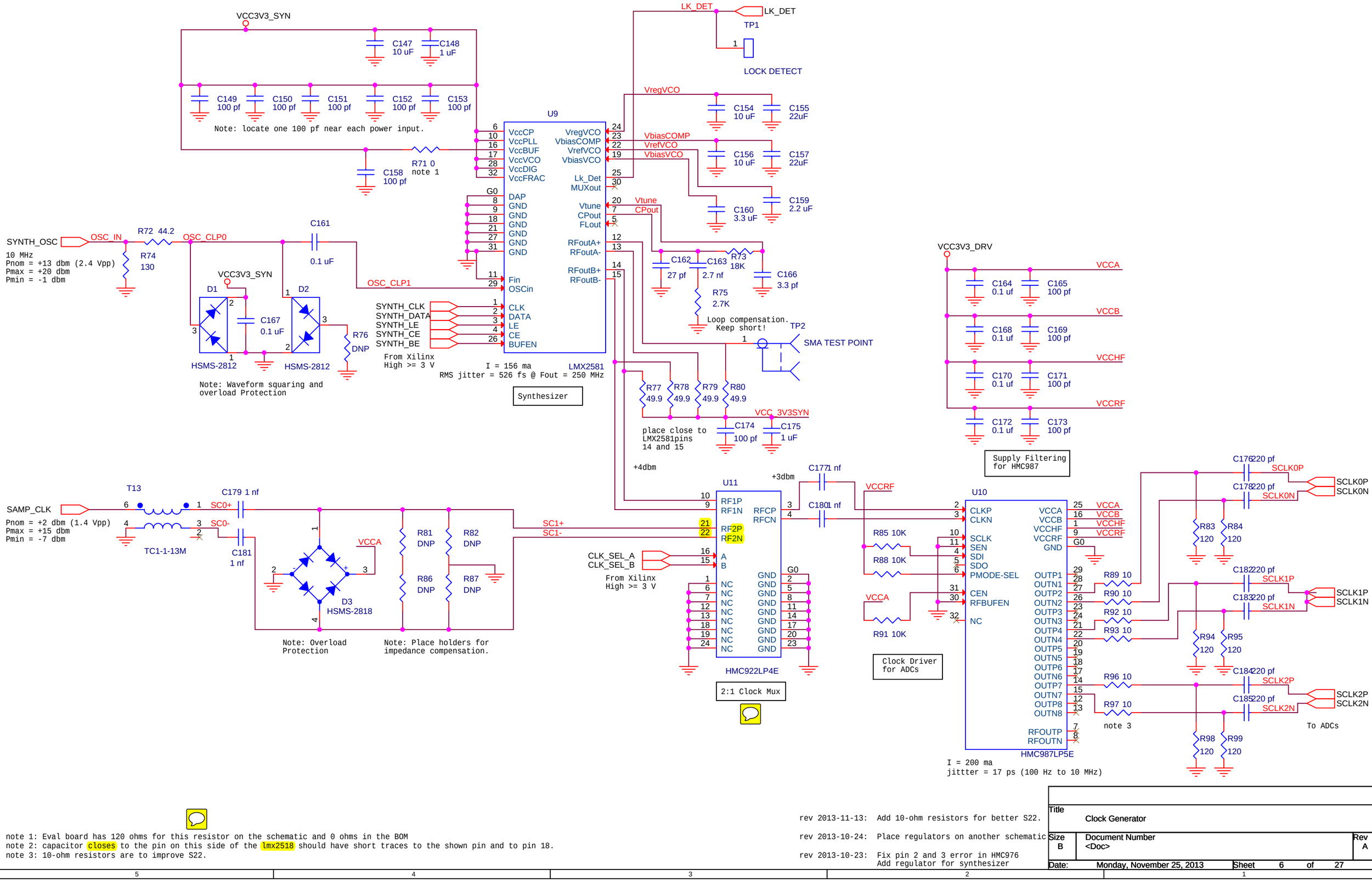
See KC705 sheet 46 Linear Power Supplies





Made by Rich Lacasse for the ADC voltages

Title: Analog Regulators		
Size: B	Document Number: <Doc>	Rev: -
Date: Monday, November 25, 2013	Sheet 5 of 27	



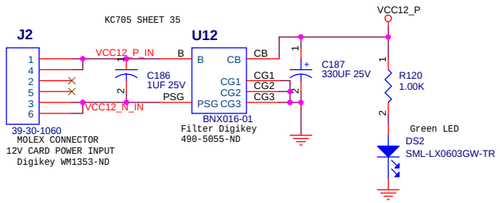
note 1: Eval board has 120 ohms for this resistor on the schematic and 0 ohms in the BOM
note 2: capacitor closes to the pin on this side of the lmx2518 should have short traces to the shown pin and to pin 18.
note 3: 10-ohm resistors are to improve S22.

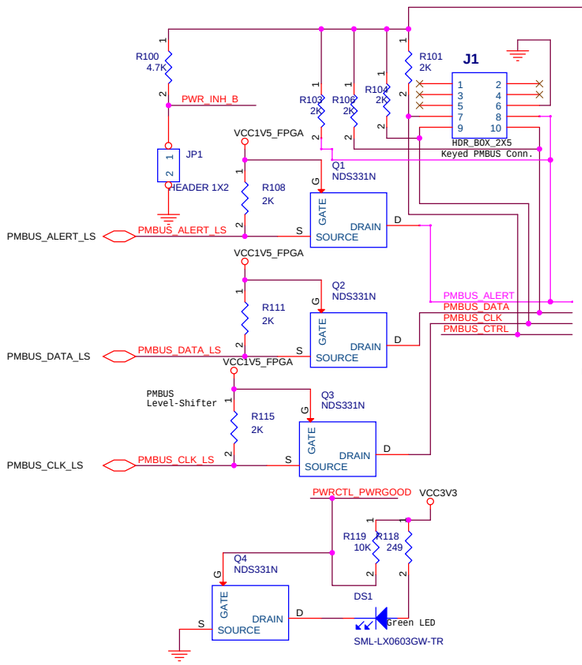
rev 2013-11-13: Add 10-ohm resistors for better S22.

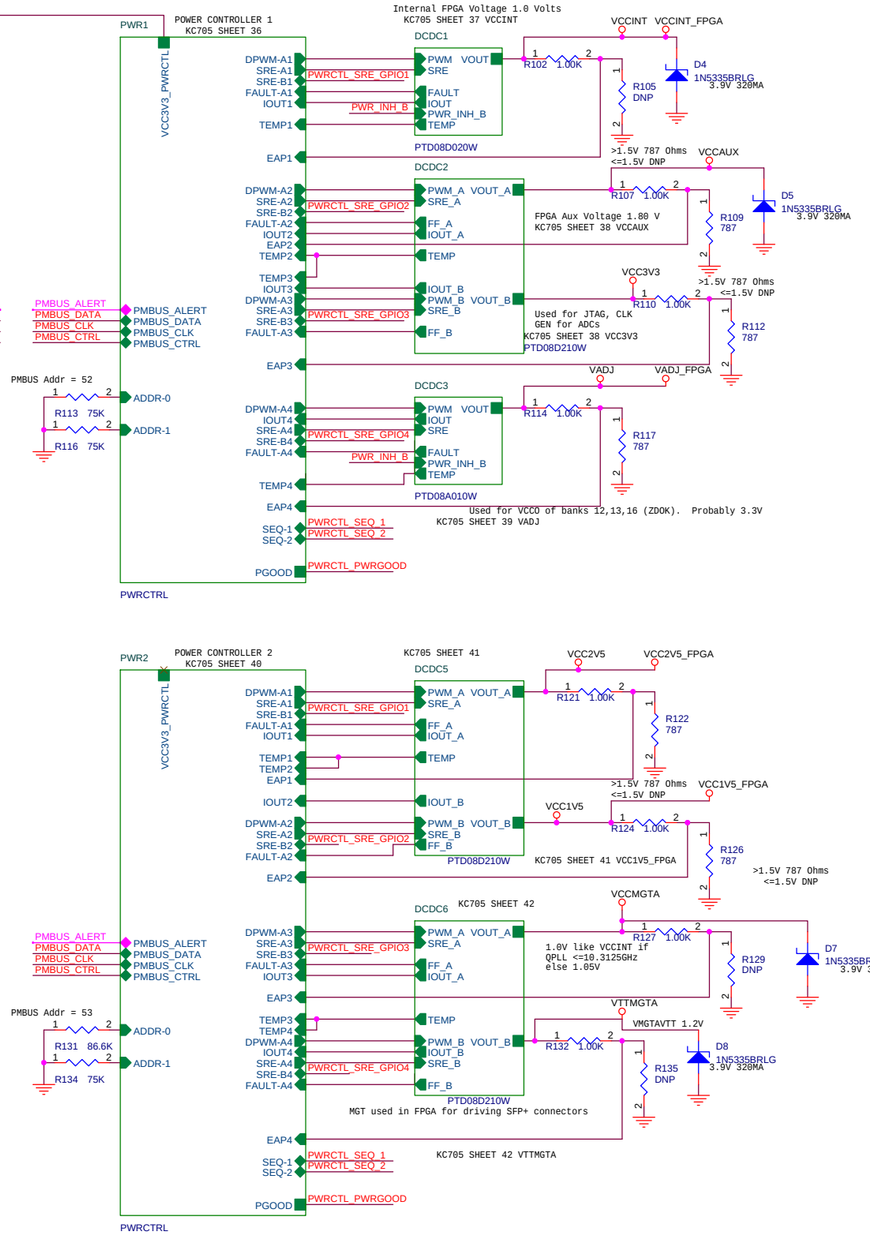
rev 2013-10-24: Place regulators on another schematic

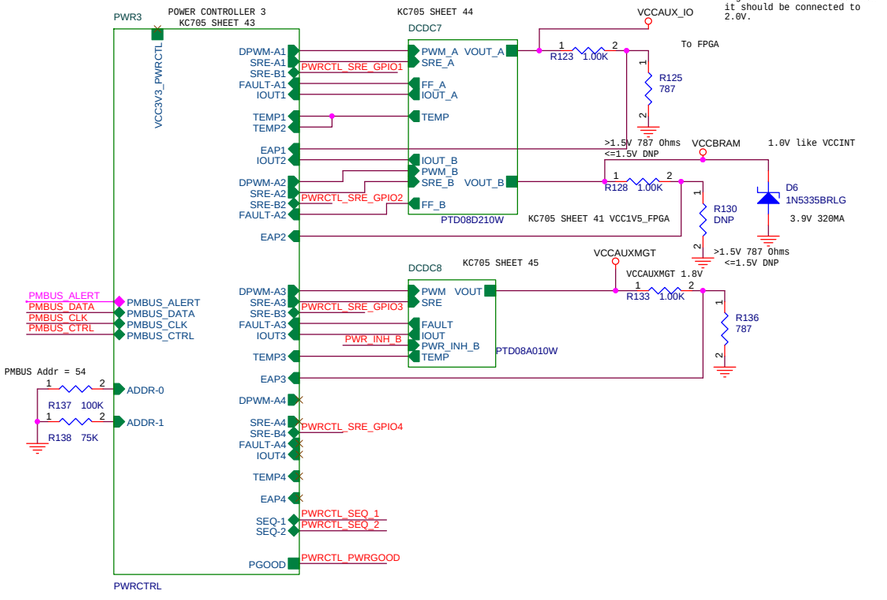
rev 2013-10-23: Fix pin 2 and 3 error in HMC976
Add regulator for synthesizer

Title	Clock Generator	
Size B	Document Number <Doc>	Rev A
Date: Monday, November 25, 2013	Sheet 6 of 27	









VCCAUX_IO should be connected to VCCAUX in all cases except when needing to run at the highest DDR3 line rates when it should be connected to 2.0V.

See Kintex-7 FPGA Data Sheet : DC and AC Switching Characteristics

This has the sequence for powering up the supplies.
The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, VCCAUX_IO, and VCCO to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the poweron sequence. If VCCINT and VCCBRAM have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If VCCAUX, VCCAUX_IO, and VCCO have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

The recommended GTX transceiver power-on sequence is VCCINT, VMGTAVCC, VMGTAVTT or VMGTAVCC, VCCINT, VMGTAVTT to achieve minimum current draw. There is no recommended sequencing for VMGTVCCAUX. Both VMGTAVCC and VCCINT can be ramped up simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

Title	DIGITAL POWER SUPPLIES		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 7	of 27	

SRCC are single region clocks
MRCC are multi region clocks

U13-9

	U4	IO_0_VRN_34	IO_L9P_T1_DQS_34	AB1	ADC0_OUT14
	T7	IO_25_VRP_34	IO_L9N_T1_DQS_34	AC1	ADC0_OUT15
ADC1_OUT1	Y1	IO_L10N_T1_34	IO_L8P_T1_34	V2	ADC0_OUT12
ADC1_OUT0	W1	IO_L10P_T1_34	IO_L8N_T1_34	V1	ADC0_OUT13
LCLKP0	AC2	IO_L11N_T1_SRCC_34	IO_L7P_T1_34	Y3	ADC0_OUT10
LCLKN0	AB2	IO_L11P_T1_SRCC_34	IO_L7N_T1_34	Y2	ADC0_OUT11
LCLKP1	AA2	IO_L12N_T1_MRCC_34	IO_L6P_T0_34	V4	ADC0_OUT8
LCLKN1	AA3	IO_L12P_T1_MRCC_34	IO_L6N_T0_VREF_34	W4	ADC0_OUT9
FCLKP1	AB4	IO_L13N_T2_MRCC_34	IO_L5P_T0_34	U7	ADC0_OUT6
FCLKN1	AA4	IO_L13P_T2_MRCC_34	IO_L5N_T0_34	V6	ADC0_OUT7
FCLKP0	AC3	IO_L14N_T2_SRCC_34	IO_L4P_T0_34	V3	ADC0_OUT4
FCLKN0	AC4	IO_L14P_T2_SRCC_34	IO_L4N_T0_34	W3	ADC0_OUT5
ADC1_OUT3	AB5	IO_L15N_T2_DQS_34	IO_L3P_T0_DQS_34	W6	ADC0_OUT2
ADC1_OUT2	AA5	IO_L15P_T2_DQS_34	IO_L3N_T0_DQS_34	W5	ADC0_OUT3
ADC1_OUT5	AC6	IO_L16N_T2_34	IO_L2P_T0_34	U2	ADC0_OUT0
ADC1_OUT4	AB6	IO_L16P_T2_34	IO_L2N_T0_34	U1	ADC0_OUT1
ADC1_OUT7	Y5	IO_L17N_T2_34	IO_L24P_T3_34	AF3	CSN0
ADC1_OUT6	Y6	IO_L17P_T2_34	IO_L24N_T3_34	AF2	SDATA0
ADC1_OUT9	AD5	IO_L18N_T2_34	IO_L23P_T3_34	AE6	SCLK0
ADC1_OUT8	AD6	IO_L18P_T2_34	IO_L23N_T3_34	AE5	RSTN0
ADC1_OUT11	AD3	IO_L19N_T3_VREF_34	IO_L22P_T3_34	AE3	PD0
ADC1_OUT10	AD4	IO_L19P_T3_34	IO_L22N_T3_34	AE2	
	U5	IO_L1N_T0_34	IO_L21P_T3_DQS_34	AF5	ADC1_OUT14
	U6	IO_L1P_T0_34	IO_L21N_T3_DQS_34	AF4	ADC1_OUT15
ADC1_OUT13	AE1	IO_L20N_T3_34	IO_L20P_T3_34	AD1	ADC1_OUT12

XC7K160T-FFG676

See UG471 Series_Select IO for info on SERDES clocking.

See Sheet 8 of KC705
Gets VCCO from VCCO1V8

High Precision

U13-7

PMBUS_DATA_LS	V13	IO_0_VRN_32	IO_L9P_T1_DQS_32	Y15	ADC2_OUT14
PMBUS_ALERT_LS	W13	IO_25_VRP_32	IO_L9N_T1_DQS_32	Y16	ADC2_OUT15
	AB15	IO_L10N_T1_32	IO_L8P_T1_32	AC14	ADC2_OUT12
	AB14	IO_L10P_T1_32	IO_L8N_T1_32	AD14	ADC2_OUT13
LCLKP2	AA18	IO_L11N_T1_SRCC_32	IO_L7P_T1_32	AA14	ADC2_OUT10
LCLKN2	AA17	IO_L11P_T1_SRCC_32	IO_L7N_T1_32	AA15	ADC2_OUT11
PMBUS_CLK_LS	AC16	IO_L12N_T1_MRCC_32	IO_L6P_T0_32	AD16	ADC2_OUT8
	AB16	IO_L12P_T1_MRCC_32	IO_L6N_T0_VREF_32	AE16	ADC2_OUT9
	AD18	IO_L13N_T2_MRCC_32	IO_L5P_T0_32	AF19	ADC2_OUT6
	AC18	IO_L13P_T2_MRCC_32	IO_L5N_T0_32	AF20	ADC2_OUT7
FCLKP2	AC17	IO_L14N_T2_SRCC_32	IO_L4P_T0_32	AD15	ADC2_OUT4
FCLKN2	AB17	IO_L14P_T2_SRCC_32	IO_L4N_T0_32	AE15	ADC2_OUT5
	AE20	IO_L15N_T2_DQS_32	IO_L3P_T0_DQS_32	AE18	ADC2_OUT2
	AD20	IO_L15P_T2_DQS_32	IO_L3N_T0_DQS_32	AF18	ADC2_OUT3
	AA20	IO_L16N_T2_32	IO_L2P_T0_32	AF14	ADC2_OUT0
	AA19	IO_L16P_T2_32	IO_L2N_T0_32	AF15	ADC2_OUT1
	AD19	IO_L17N_T2_32	IO_L24P_T3_32	V14	CSN2
	AC19	IO_L17P_T2_32	IO_L24N_T3_32	W14	SDATA2
	AB20	IO_L18N_T2_32	IO_L23P_T3_32	V18	SCLK2
	AB19	IO_L18P_T2_32	IO_L23N_T3_32	V19	RSTN2
	Y18	IO_L19N_T3_VREF_32	IO_L22P_T3_32	W15	PD2
	Y17	IO_L19P_T3_32	IO_L22N_T3_32	W16	CSN1
	AF17	IO_L1N_T0_32	IO_L21P_T3_DQS_32	W18	SDATA1
	AE17	IO_L1P_T0_32	IO_L21N_T3_DQS_32	W19	SCLK1
PD1	V17	IO_L20N_T3_32	IO_L20P_T3_32	V16	RSTN1

XC7K160T-FFG676

Used for DDR on sheet 3 of KC705
XC7K160T-2FFG676

Gets VCCO from VCCO1V8

LVDS Outputs

SMATP1 2 1
SMATP2 2 1
SMATP3 2 1
SMATP4 2 1
SMATP5 2 1
SMATP6 2 1
SMATP7 2 1
SMATP8 2 1
SMATP9 2 1
SMATP10 2 1
SMATP11 2 1
SMATP12 2 1

From Clock Generators

ADC0

CSN0	CSN	ADC_OUT[15:0]	ADC0_OUT[15:0]
SDATA0	SDATA		
SCLK0	SCLK		
RSTN0	RSTN		
PD0	PD		
ADCSMA0	IN_0	LCLKP	LCLKP0
ADCSMA1	IN_1	LCLKN	LCLKN0
ADCSMA2	IN_2	FCLKP	FCLKP0
ADCSMA3	IN_3	FCLKN	FCLKN0
SCLK0P	CLK_IN_P		
SCLK0N	CLK_IN_N		

ADC

ADC1

CSN1	CSN	ADC_OUT[15:0]	ADC1_OUT[15:0]
SDATA1	SDATA		
SCLK1	SCLK		
RSTN1	RSTN		
PD1	PD		
ADCSMA4	IN_0	LCLKP	LCLKP1
ADCSMA5	IN_1	LCLKN	LCLKN1
ADCSMA6	IN_2	FCLKP	FCLKP1
ADCSMA7	IN_3	FCLKN	FCLKN1
SCLK1P	CLK_IN_P		
SCLK1N	CLK_IN_N		

ADC

ADC2

CSN2	CSN	ADC_OUT[15:0]	ADC2_OUT[15:0]
SDATA2	SDATA		
SCLK2	SCLK		
RSTN2	RSTN		
PD2	PD		
ADCSMA8	IN_0	LCLKP	LCLKP2
ADCSMA9	IN_1	LCLKN	LCLKN2
ADCSMA10	IN_2	FCLKP	FCLKP2
ADCSMA11	IN_3	FCLKN	FCLKN2
SCLK2P	CLK_IN_P		
SCLK2N	CLK_IN_N		

ADC

Even numbers are P, odd N

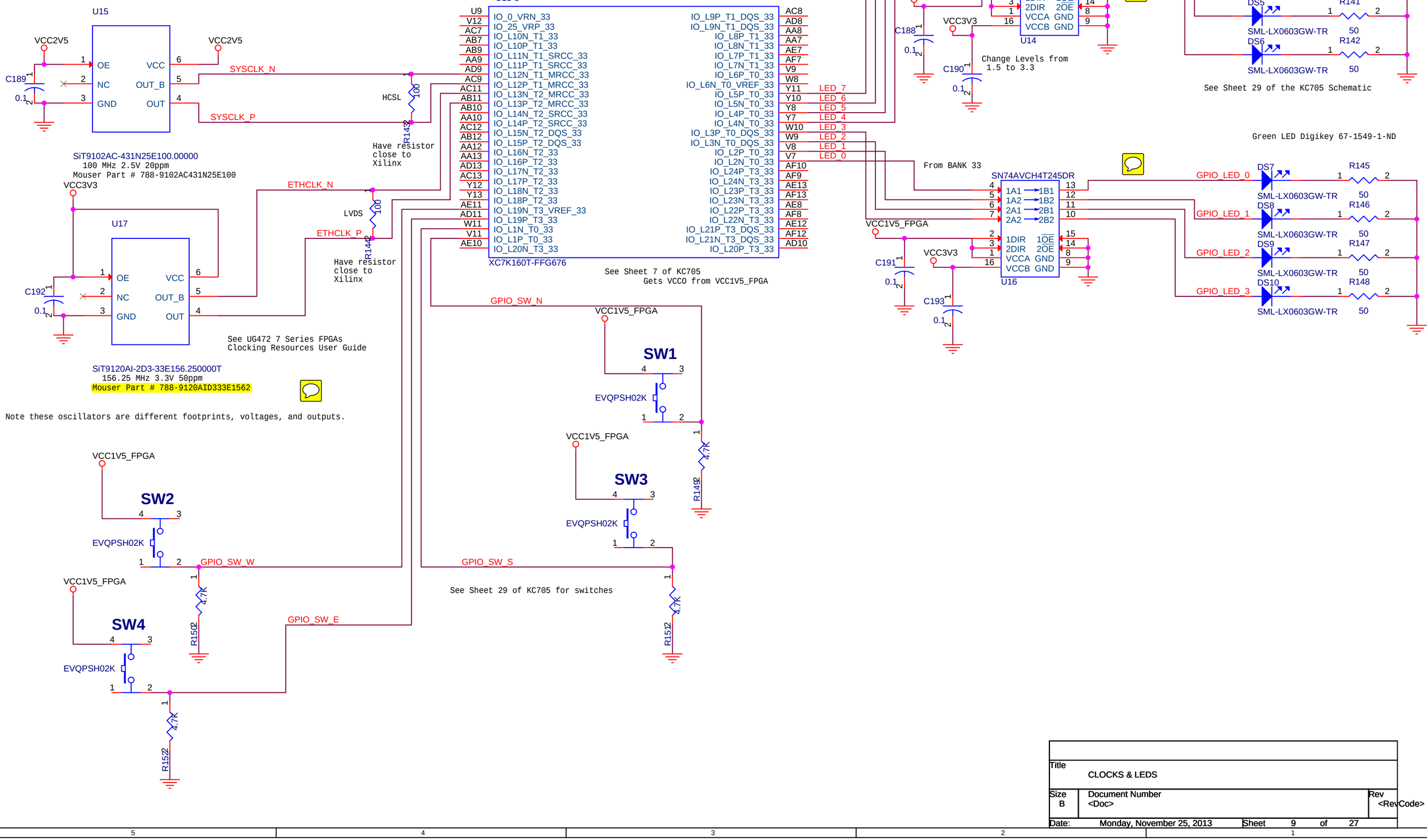
Could possibly have clocks from one ADC provide the clocks for all 3.

Could then not hook up the clocks from the other 2.

A compromise could be to hook up 2 of the 3 clocks.

Short wires from SMA Connectors on box soldered to this TP.

Title	AD CONVERTERS	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 8 of 27	



Title	CLOCKS & LEDS		
Size B	Document Number <Doc>		Rev <RevCode>
Date: Monday, November 25, 2013		Sheet 9 of 27	

VCC2V5

VCC2V5

M0 is 1 for SPI mode

U18

C194

0.1

See Sheet 27 of the KC705 Schematic

R153 4.7K

FPGA_FCS

SN74LVC1G18DBVR

Connect A to Y0 and Y1 when S=1

Digikey 296-15568-1-nd

M[2:0] Determines the configuration mode.
See Sheet 27 of the KC705 Schematic

R154 1.21K R155 1.21K R156 1.21K R157 1.21K R158 1.21K

Digikey CKN6074-ND

VCC2V5

SDA05H1SBD

SPI Select Switch
ON = SPI Devide
OFF = SPI External

VCC3V3

QSPI_CS_B

FPGA_INIT_B

QSPI_IC_CS_B

S1

R159 33

V3.3-LIMIT2

J3

PTC06DAAN

JTAG_TDO

R161 15

R162 15

R163 15

U19

DIGILENT_USB_JTAG

VCC3V3

SN74AVCH4T245DR

JTAG_TMS
JTAG_TCK
JTAG_TDI

FPGA_TMS_BUF
FPGA_TCK_BUF
FPGA_TDI_BUF

VCC3V3

VCC2V5

C196 0.1

C197 0.1

U20

Change Levels from
3.3V to 2.5V

See Sheet 3 of the KC705 Schematic

BANK 0

See Sheet 3 of the KC705 Schematic

U13-1

XC7K160T-FFG676

FPGA_M0
FPGA_M1
FPGA_M2

JTAG_TDO

FPGA_DONE

FPGA_INIT_B

VCC2V5

FPGA_INIT_B can be switched to FPGA_DONE

FPGA_PROG_B

TDO not buffered here to conform with KC705 design

R164 330

R165 4.7K

SW5

EVQPSH02K

DS11

SML-LX0603GW-TR

R166

27.4 1%

Configuration Clock to SPI Memory

CCLK

R160

DNP

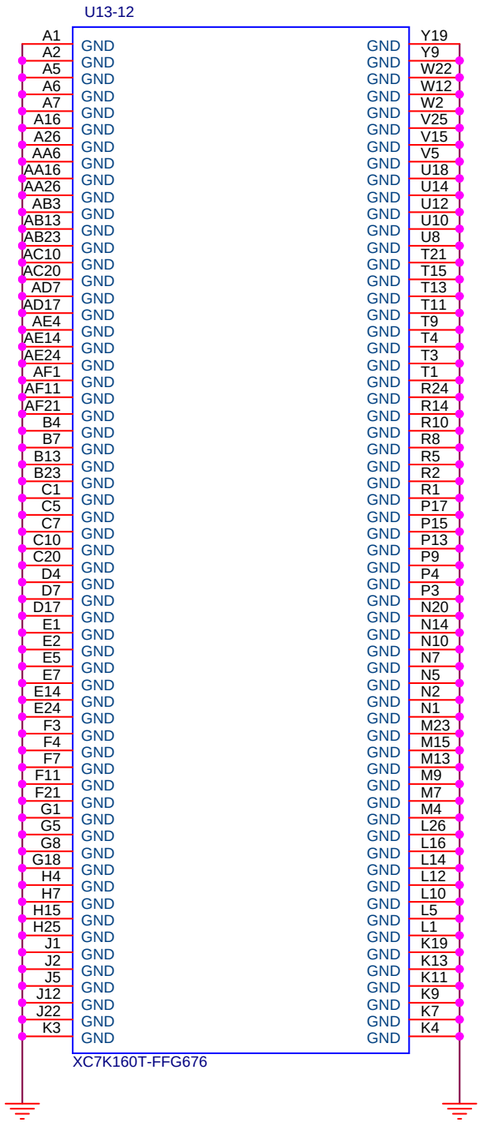
VCC2V5_FPGA

C195

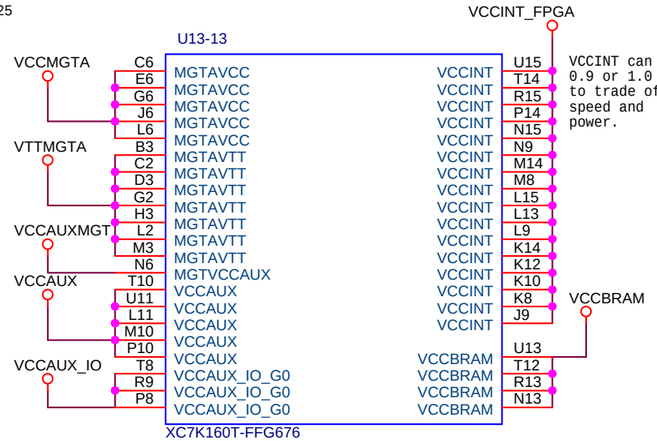
DNP

DNP - Do Not Populate

Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 10 of 27	

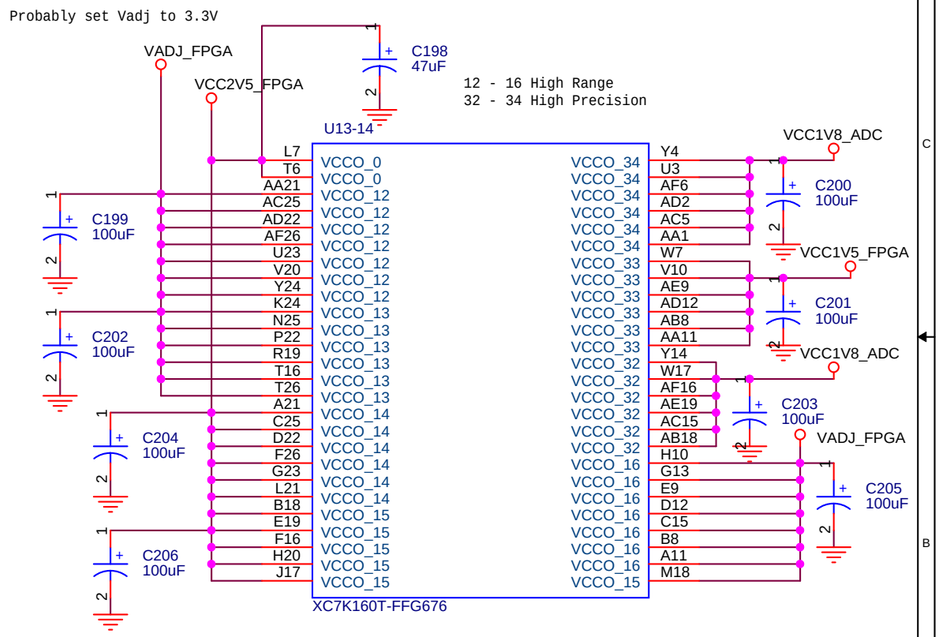


See KC705 Sheet 25



VCCINT can be 0.9 or 1.0 V to trade off speed and power.

Probably set Vadj to 3.3V

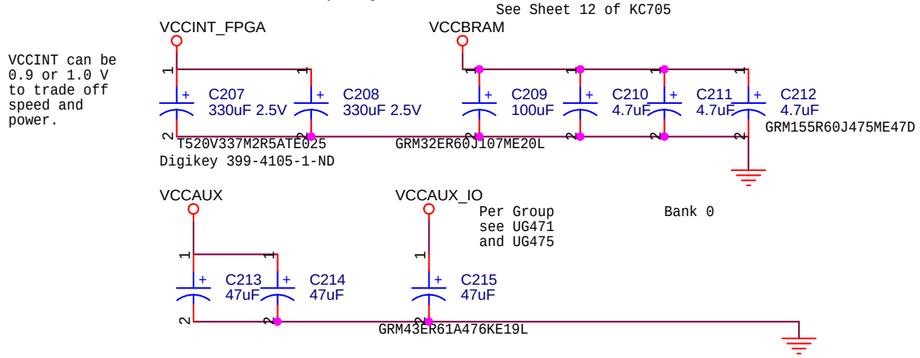


12 - 16 High Range
32 - 34 High Precision

HR I/O Bank has 3.465 VCCO max
HP I/O Bank has 1.89 VCCO max

Per UG483, the xc7k160t ffg676requires the following bypass capacitors:
See UG483 for layout guidlines

See Sheet 12 of KC705



VCCINT can be 0.9 or 1.0 V to trade off speed and power.

Per Group see UG471 and UG475

Bank 0

Title: FPGA POWER		
Size: B	Document Number: <Doc>	Rev: <RevCode>
Date: Monday, November 25, 2013	Sheet 11 of 27	

U13-5

XC7K160T-FFG676

USB_TX	K15	IO_0_15	IO_L9P_T1_DQS_AD11P_15	J15	
	M16	IO_25_15	IO_L9N_T1_DQS_AD11N_15	J16	
	E16	IO_L10N_T1_AD4N_15	IO_L8P_T1_AD3P_15	G15	
	E15	IO_L10P_T1_AD4P_15	IO_L8N_T1_AD3N_15	F15	
USB_CTS	F18	IO_L11N_T1_SRCC_AD12N_15	IO_L7P_T1_AD10P_15	H16	
	G17	IO_L11P_T1_SRCC_AD12P_15	IO_L7N_T1_AD10N_15	G16	
	E17	IO_L12N_T1_MRCC_AD5N_15	IO_L6P_T0_15	D15	
	F17	IO_L12P_T1_MRCC_AD5P_15	IO_L6N_T0_VREF_15	D16	
	D18	IO_L13N_T2_MRCC_15	IO_L5P_T0_AD2P_15	C17	
	E18	IO_L13P_T2_MRCC_15	IO_L5N_T0_AD2N_15	C18	
	H18	IO_L14N_T2_SRCC_15	IO_L4P_T0_AD9P_15	C19	
	H17	IO_L14P_T2_SRCC_15	IO_L4N_T0_AD9N_15	B19	
	D20	IO_L15N_T2_DQS_ADV_B_15	IO_L3P_T0_DQS_AD1P_15	B17	USB_RTS
	D19	IO_L15P_T2_DQS_15	IO_L3N_T0_DQS_AD1N_15	A17	USB_RX
	F20	IO_L16N_T2_A27_15	IO_L2P_T0_AD8P_15	A18	
	G19	IO_L16P_T2_A28_15	IO_L2N_T0_AD8N_15	A19	
	E20	IO_L17N_T2_A25_15	IO_L24P_T3_RS1_15	L17	
	F19	IO_L17P_T2_A26_15	IO_L24N_T3_RS0_15	K18	
	G20	IO_L18N_T2_A23_15	IO_L23P_T3_FOE_B_15	M17	
	H19	IO_L18P_T2_A24_15	IO_L23N_T3_FWE_B_15	L18	
	J20	IO_L19N_T3_A21_VREF_15	IO_L22P_T3_A17_15	K16	
	K20	IO_L19P_T3_A22_15	IO_L22N_T3_A16_15	K17	
	B16	IO_L1N_T0_AD0N_15	IO_L21P_T3_DQS_15	L19	
	C16	IO_L1P_T0_AD0P_15	IO_L21N_T3_DQS_A18_15	L20	
	J19	IO_L20N_T3_A19_15	IO_L20P_T3_A20_15	J18	

TX_DISABLE0

SFP1

IIC_SCL_MAIN		SFP_RX_N	
IIC_SDA_MAIN		SFP_RX_P	
		SFP_TX_P	
SFP_TX_DISABLE		SFP_TX_N	

SFPCONN

U13-11

See Sheet 9 of the KC705

XC7K160T-FFG676

D5	MGTREFCLK0N_116	MGTXTXP3_116	A4
D6	MGTREFCLK0P_116	MGTXTXP2_116	B2
F5	MGTREFCLK1N_116	MGTXTXP1_116	D2
F6	MGTREFCLK1P_116	MGTXTXP0_116	F2
G3	MGTXRXN0_116	MGTXTXN3_116	A3
E3	MGTXRXN1_116	MGTXTXN2_116	B1
C3	MGTXRXN2_116	MGTXTXN1_116	D1
B5	MGTXRXN3_116	MGTXTXN0_116	F1
G4	MGTXRXP0_116	MGTXRXP3_116	B6
E4	MGTXRXP1_116	MGTXRXP2_116	C4

TX_DISABLE1

SFP2

IIC_SCL_MAIN		SFP_RX_N	
IIC_SDA_MAIN		SFP_RX_P	
		SFP_TX_P	
SFP_TX_DISABLE		SFP_TX_N	

SFPCONN

U13-10

See Sheet 9 of the KC705

XC7K160T-FFG676

M5	MGTAVTTRCAL_115	MGTXTXP3_115	H2
H5	MGTREFCLK0N_115	MGTXTXP2_115	K2
H6	MGTREFCLK0P_115	MGTXTXP1_115	M2
K5	MGTREFCLK1N_115	MGTXTXP0_115	P2
K6	MGTREFCLK1P_115	MGTXTXN3_115	H1
M6	MGTRREF_115	MGTXTXN2_115	K1
R3	MGTXRXN0_115	MGTXTXN1_115	M1
N3	MGTXRXN1_115	MGTXTXN0_115	P1
L3	MGTXRXN2_115	MGTXRXP3_115	J4
J3	MGTXRXN3_115	MGTXRXP2_115	L4
R4	MGTXRXP0_115	MGTXRXP1_115	N4

USB_SHIELD

J4

CONN_USB_MINI_B_TH
MOLEX 0548190589
Digikey WM3895CT-ND

6	SHLD1	GND	5
7	SHLD2	ID	4
8	SHLD3	D_P	3
9	SHLD9	D_N	2
		VBUS	1

C216 DNP

C217 0.1

USB_GND

L13 FERRITE-600
HZ0805E601R-10
Digikey 240-2399-2--ND

X1

SP0503BAHTG
Transient Surpressor
Digikey F2715CT-ND

1	ANODES	CATH3	4
2	CATH1	CATH2	3

USB_D_P

USB_D_N

VCC2V5

C218 0.1

C219 1UF 25V

C220 0.1

R167 4.7K

VBUS_USB

L14 FERRITE-600
HZ0805E601R-10
Digikey 240-2399-2--ND

C221 0.1

C222 1UF 25V

VBUS

USB BUS POWERED
Digikey 336-1164-ND

U21

CP2103-GM

1	RI	CNR_GND	
2	GND		
3	D+		
4	D-		
5	VIO		
6	VDD		
7	REGIN		
8	VBUS		
9	RST_B		
10	NC1		
11	SUSPEND_B		
12	SUSPEND		
13	NC2		
14	NC3		
15	NC4		
16	GPIO3		
17	GPIO2		
18	GPIO1		
19	GPIO0		
20	NC5		
21	NC6		
22	CTS		
23	RTS		
24	RXD		
25	TXD		
26	DSR		
27	DTR		
28	DCD		
29			
30	CTR_GND		

USB_TX

USB_RX

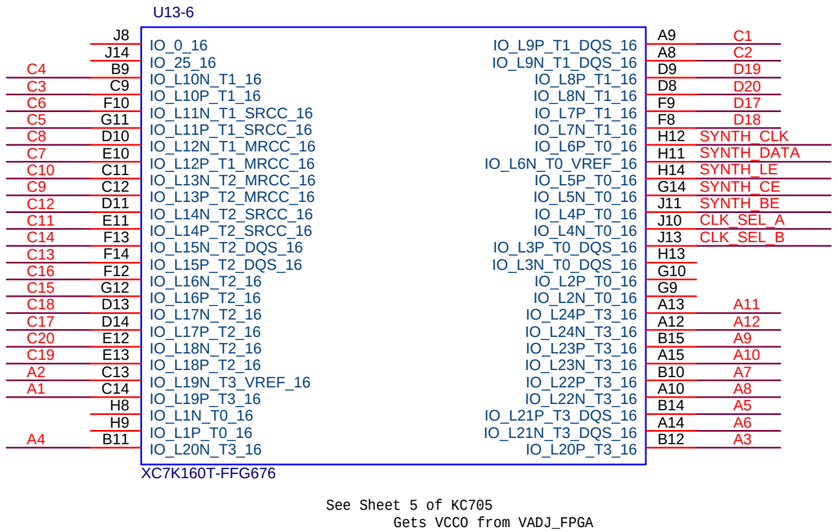
USB_RTS

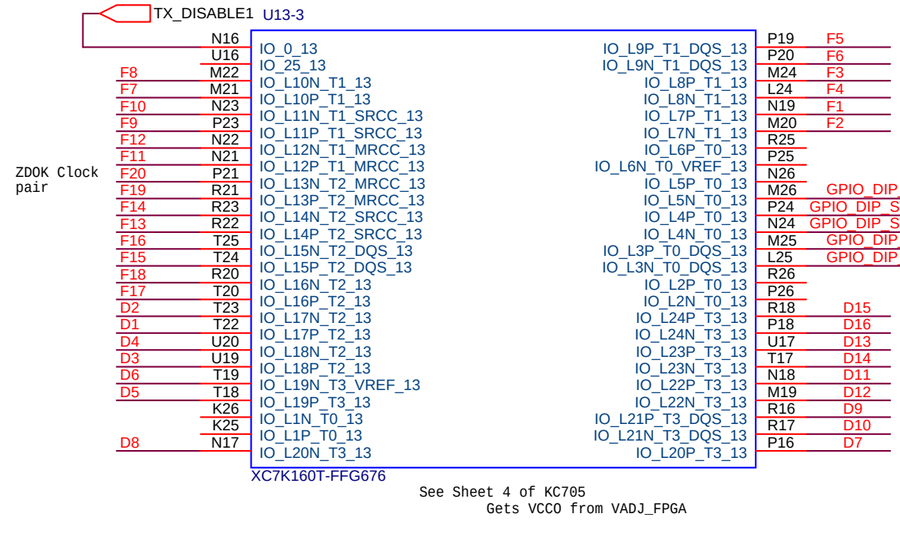
USB_CTS

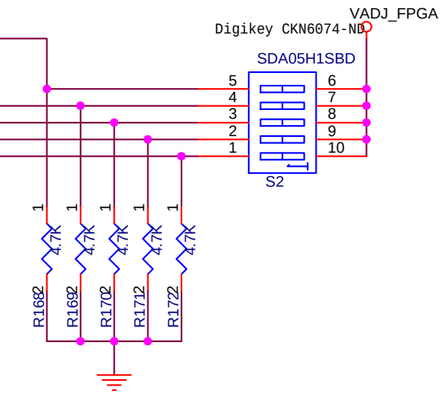
To Bank 15 above

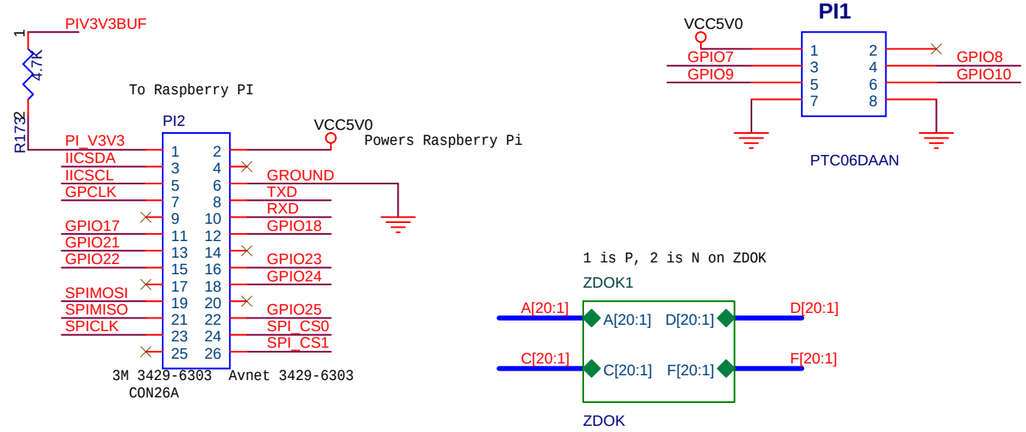
See Sheet 27 of the KC705

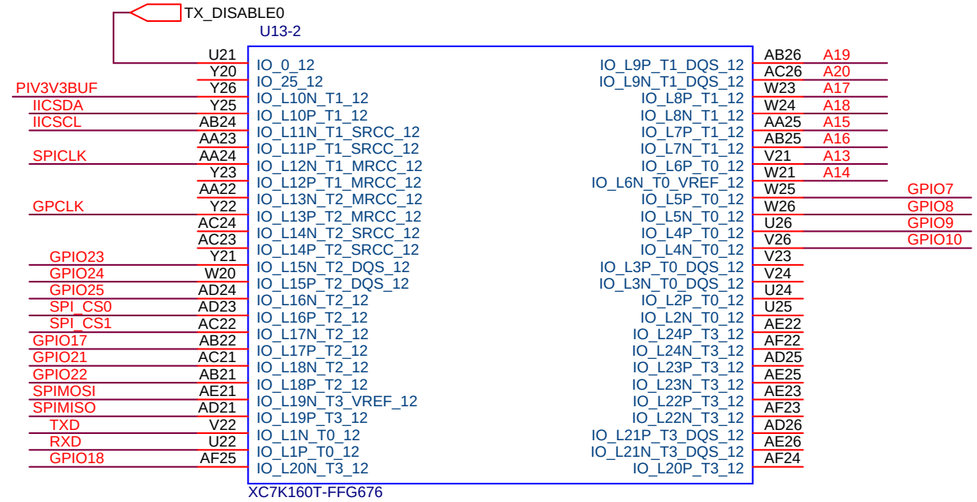
Title	SFP+ Connector and Cage		
Size B	Document Number <Doc>		Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 12 of 27		

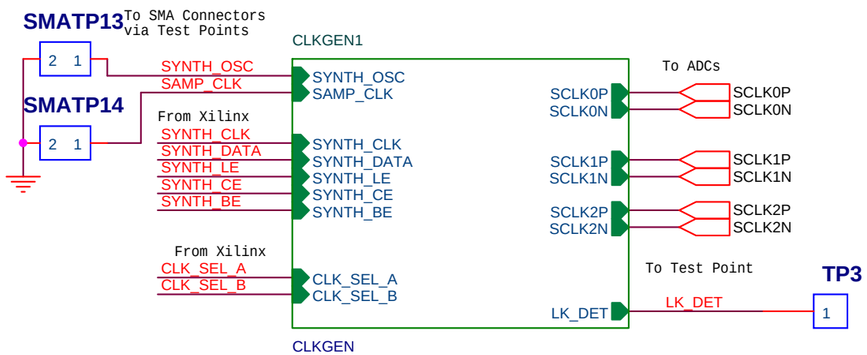








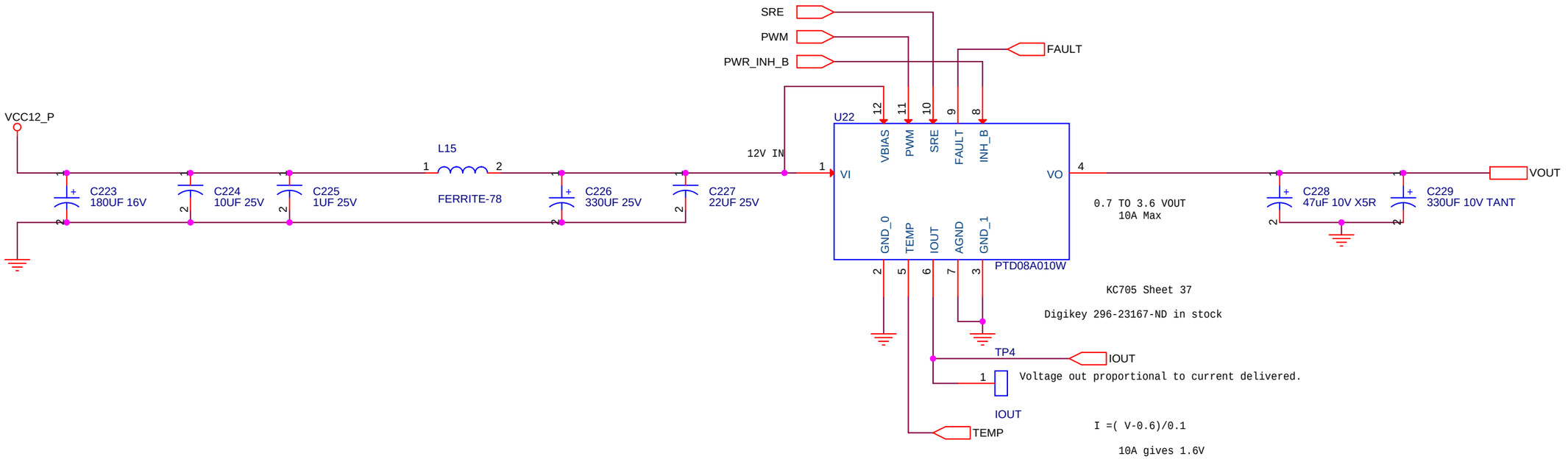




Title: ZDOK CONNECTOR

Size: B | Document Number: <Doc> | Rev: <RevCode>

Date: Monday, November 25, 2013 | Sheet 13 of 27



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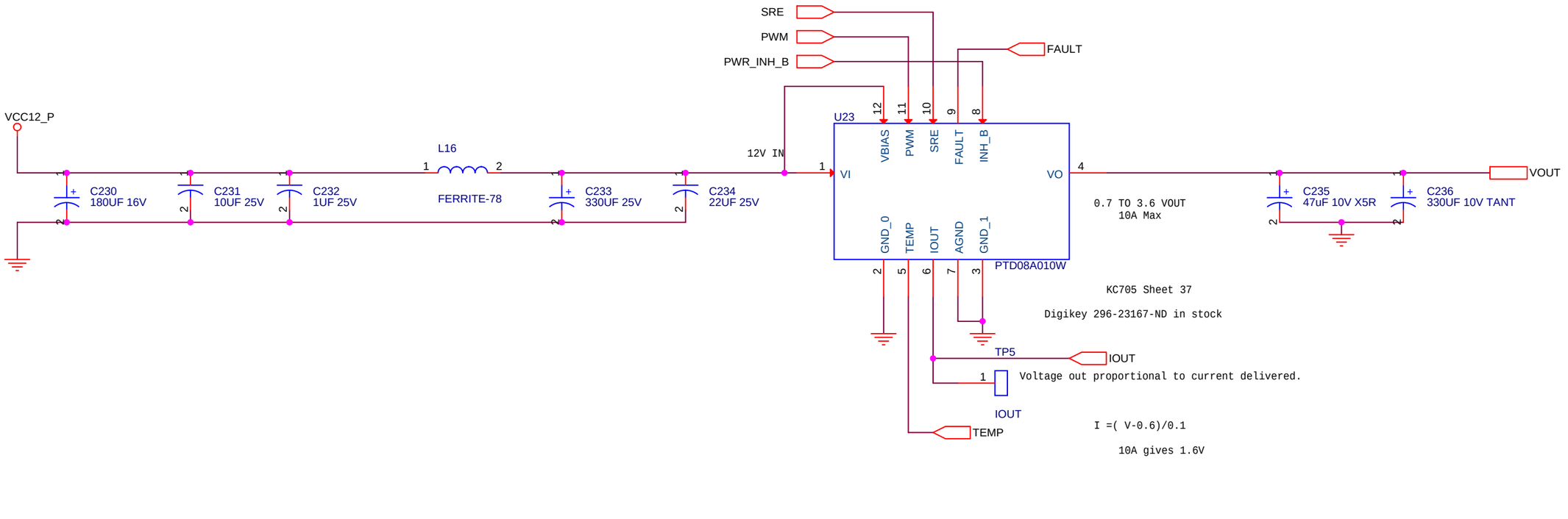
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 14 of 27	



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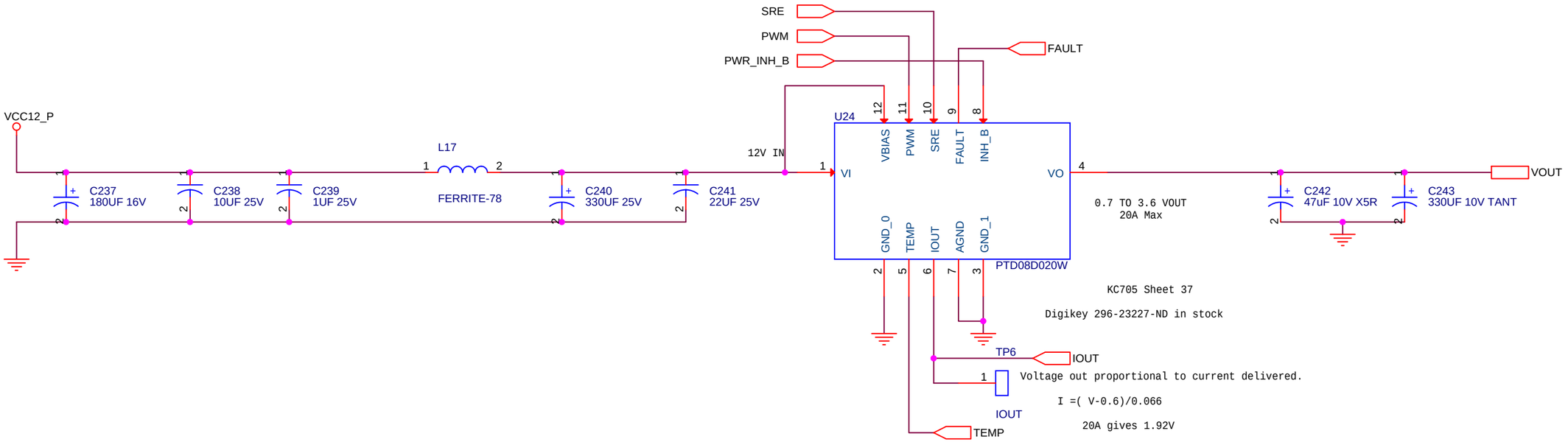
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 15 of 27	



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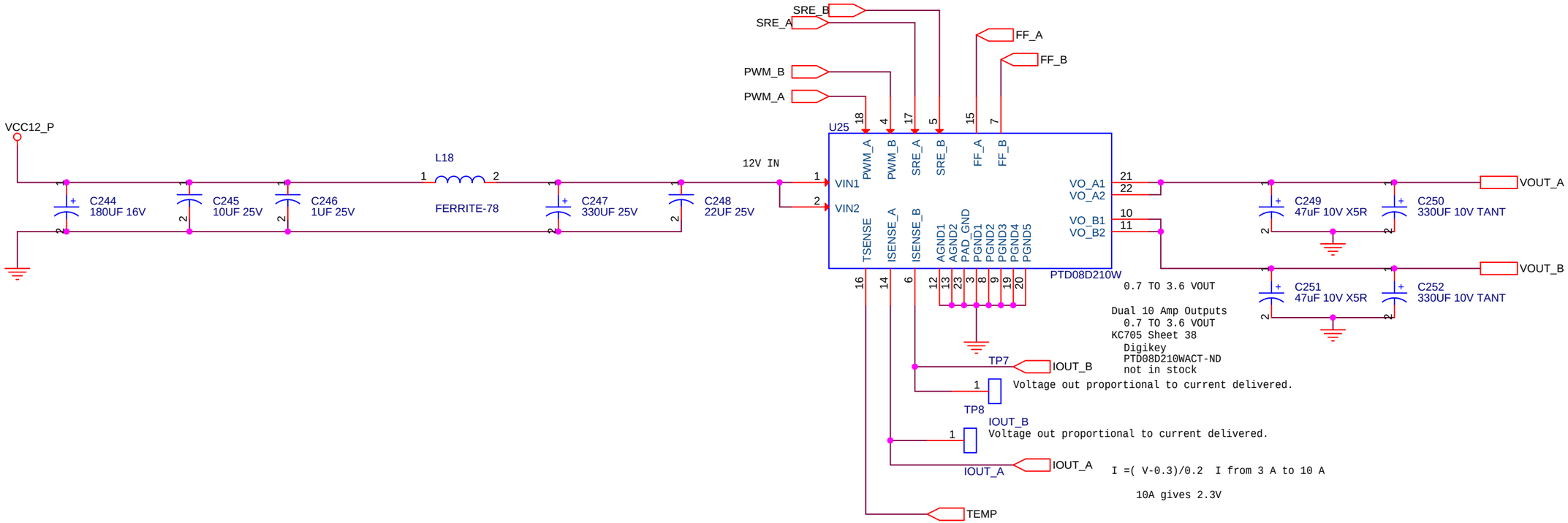
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 16 of 27	



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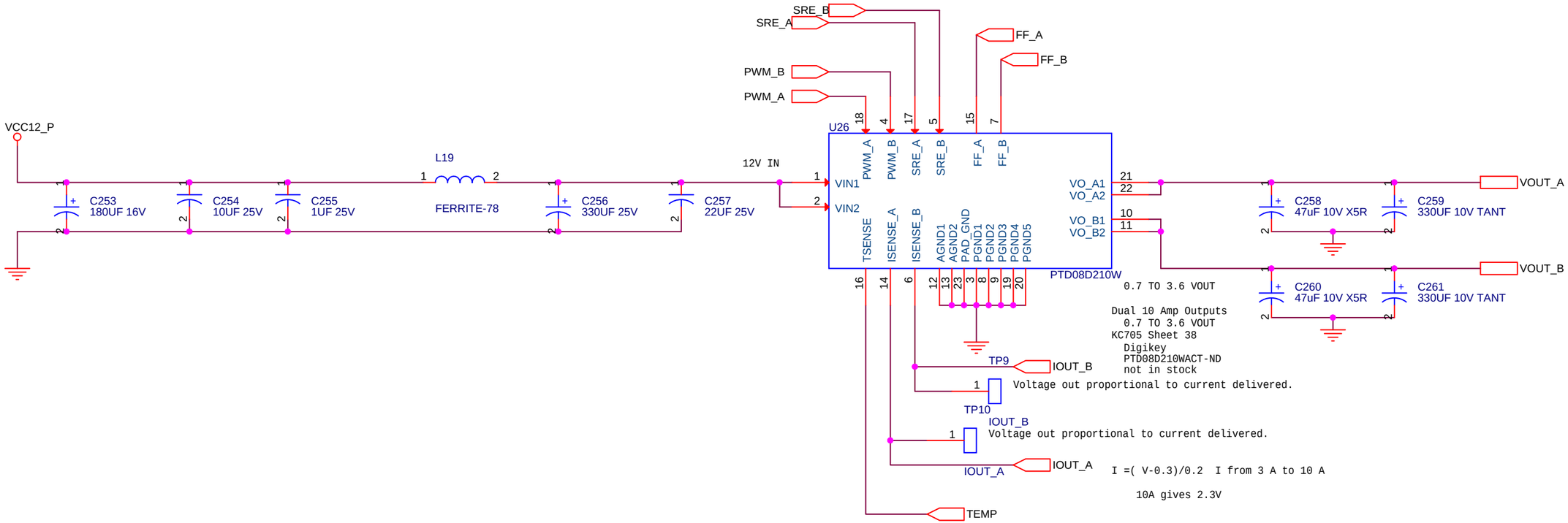
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 17 of 27	



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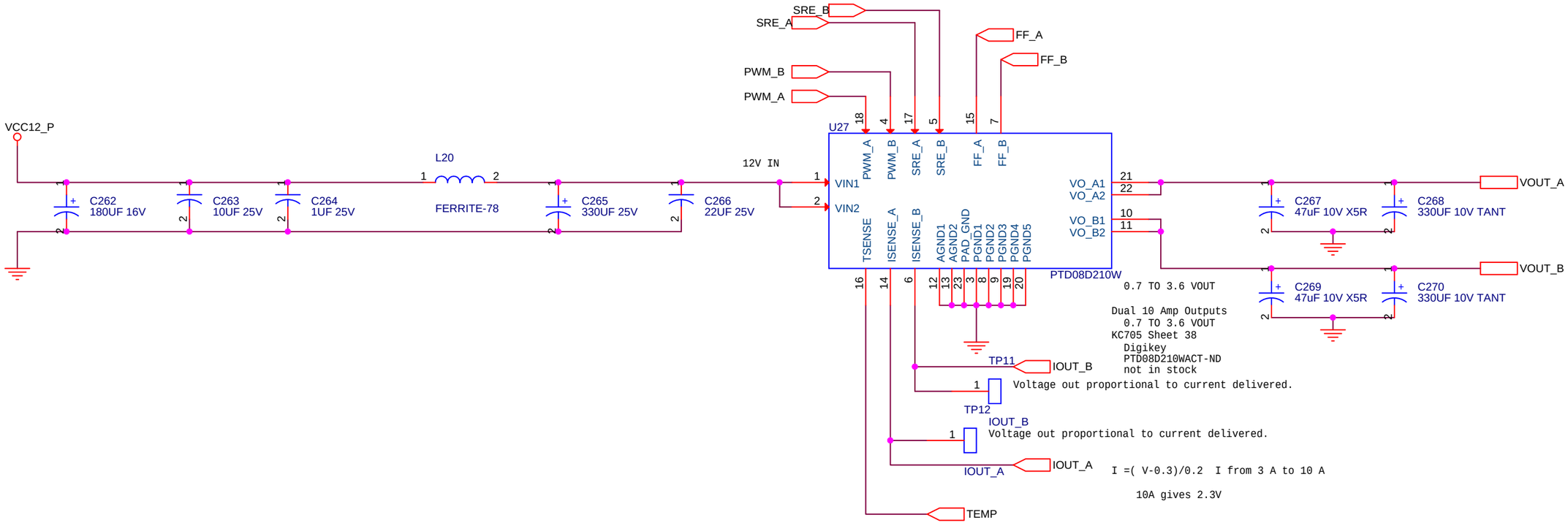
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 18 of 27	



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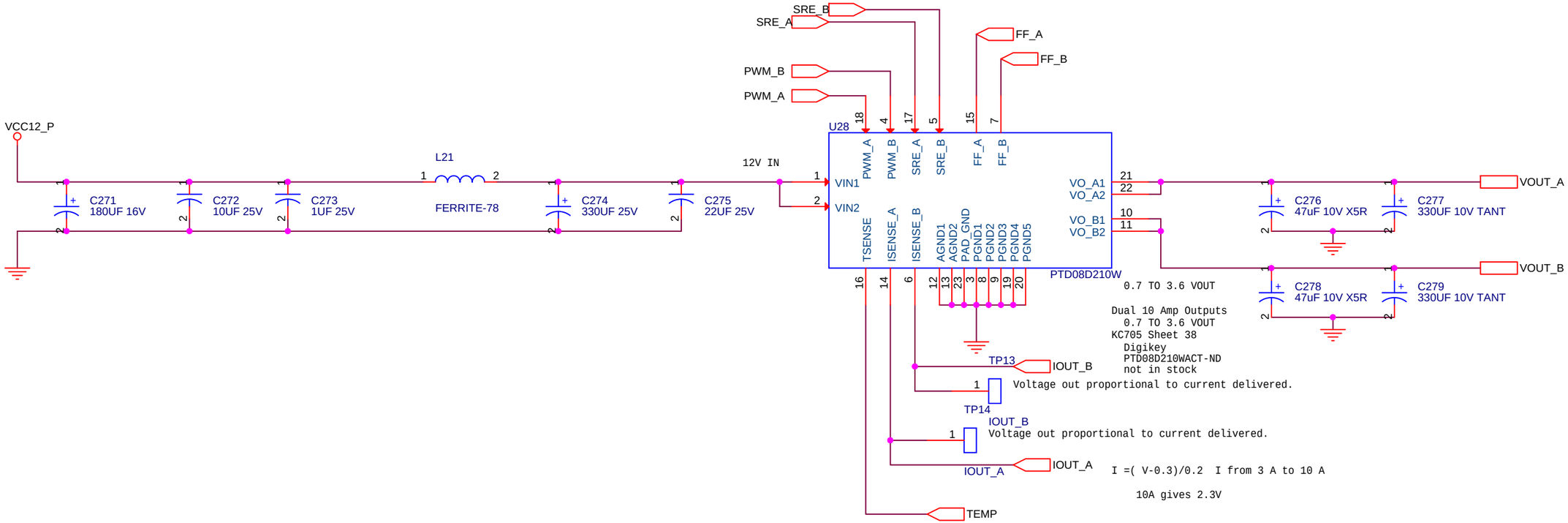
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 19 of 27	



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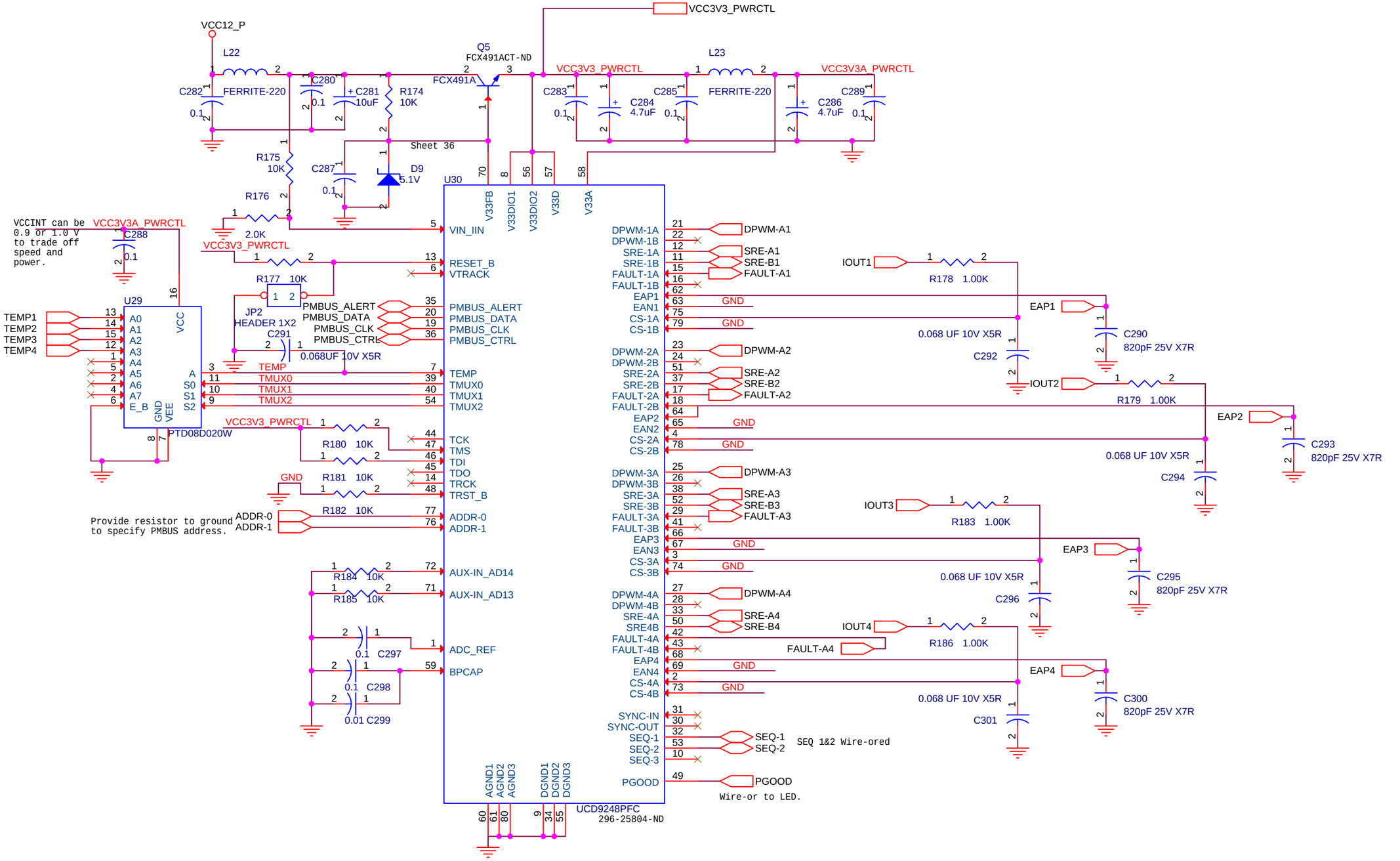
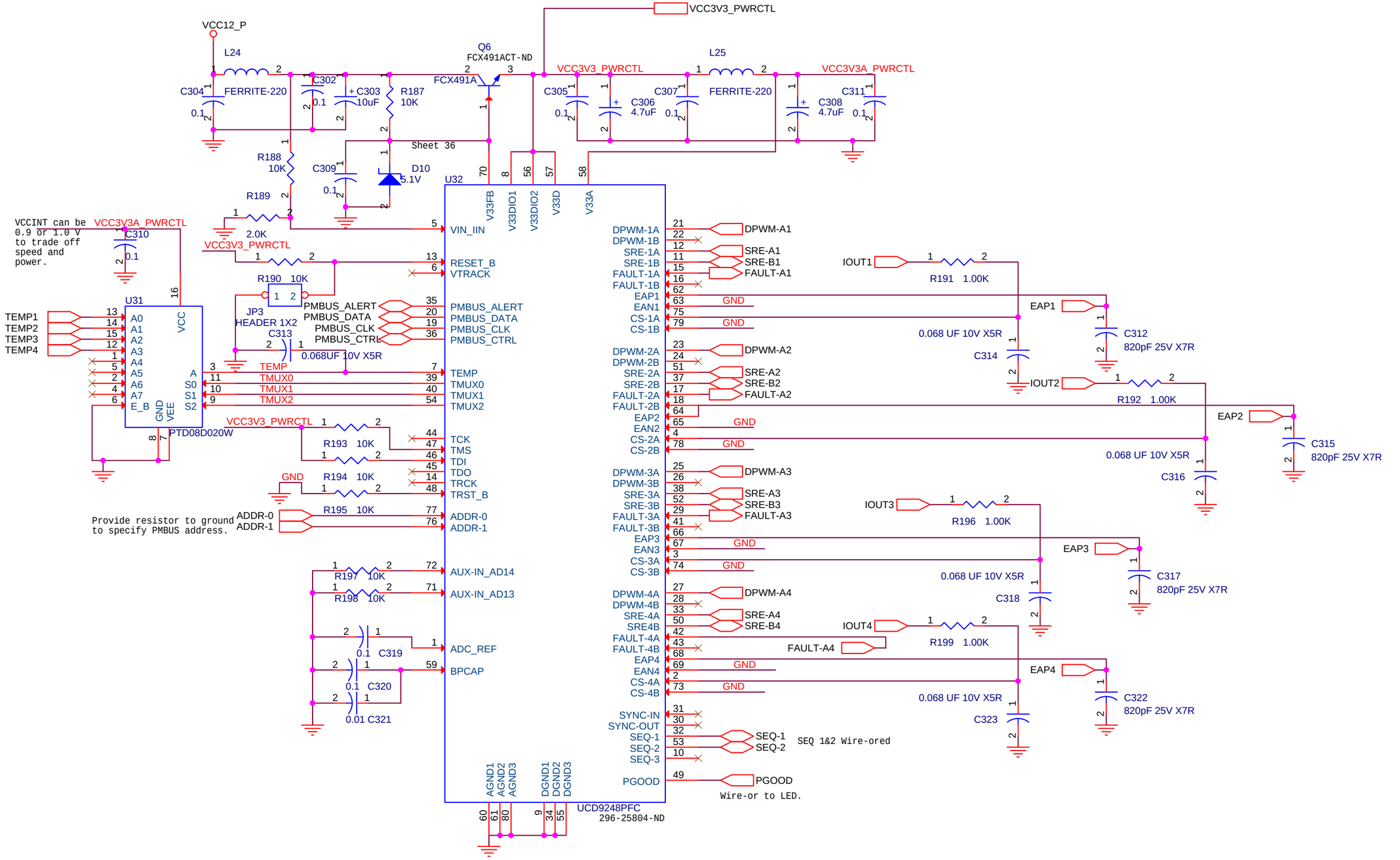
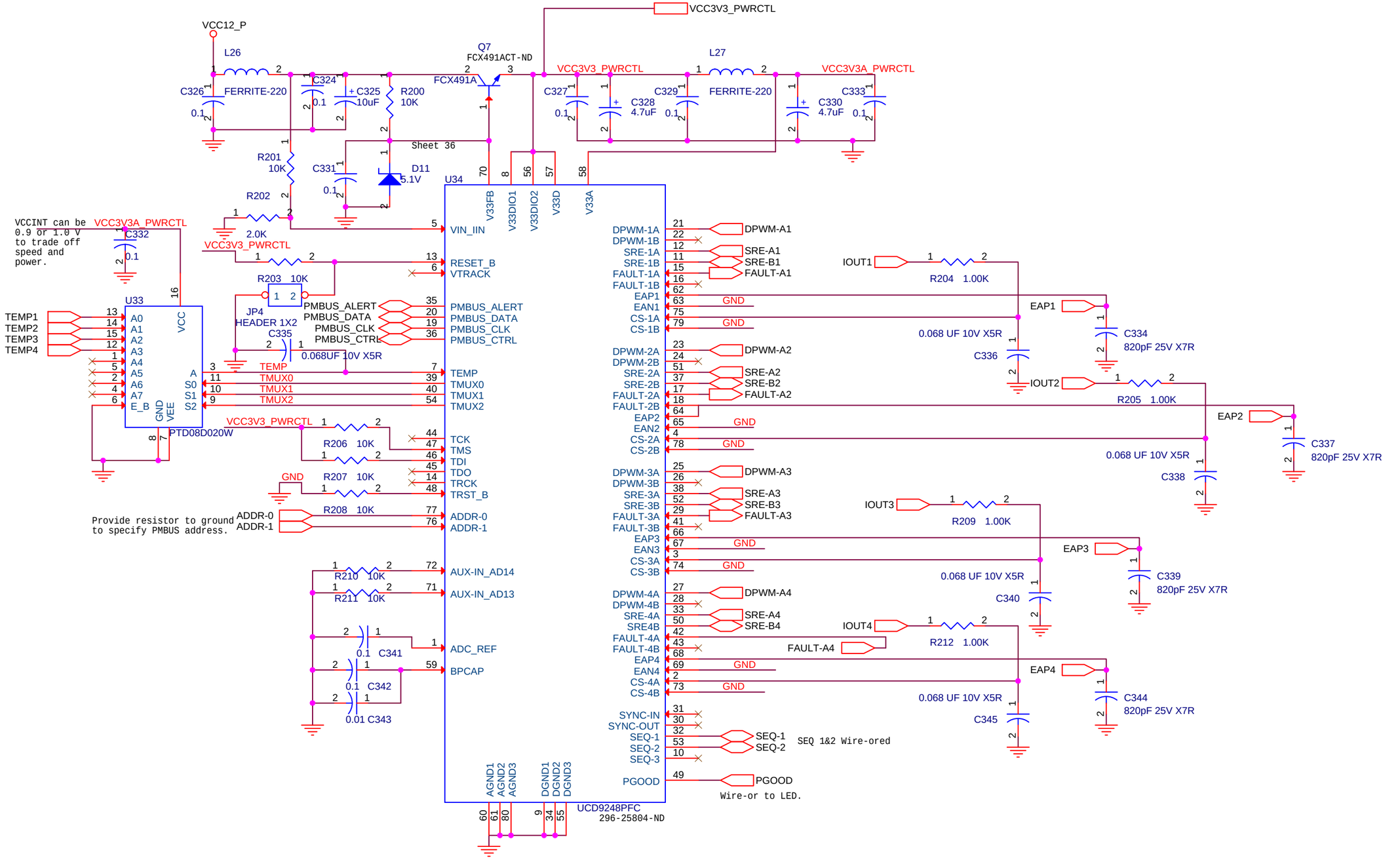
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 20 of 27	



Title	DIGITAL PWM SYSTEM CONTROLLER	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 21 of 27	



Title	DIGITAL PWM SYSTEM CONTROLLER	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 22 of 27	



Title	DIGITAL PWM SYSTEM CONTROLLER	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 23 of 27	

See KC705 Sheet 4

U13-4

K21	IO_0_14	IO_L9P_T1_DQS_14	E21
L23	IO_25_14	IO_L9N_T1_DQS_D13_14	E22
B21	IO_L10N_T1_D15_14	IO_L8P_T1_D11_14	B20
C21	IO_L10P_T1_D14_14	IO_L8N_T1_D12_14	A20
D24	IO_L11N_T1_SRCC_14	IO_L7P_T1_D09_14	D21
D23	IO_L11P_T1_SRCC_14	IO_L7N_T1_D10_14	C22
E23	IO_L12N_T1_MRCC_14	IO_L6P_T0_FCS_B_14	C23
F22	IO_L12P_T1_MRCC_14	IO_L6N_T0_D08_VREF_14	C24
F23	IO_L13N_T2_MRCC_14	IO_L5P_T0_D06_14	D26
G22	IO_L13P_T2_MRCC_14	IO_L5N_T0_D07_14	C26
F24	IO_L14N_T2_SRCC_14	IO_L4P_T0_D04_14	A23
G24	IO_L14P_T2_SRCC_14	IO_L4N_T0_D05_14	A24
D25	IO_L15N_T2_DQS_DOUT_CSO_B_14	IO_L3P_T0_DQS_PUDC_B_14	B25
E25	IO_L15P_T2_DQS_RDWR_B_14	IO_L3N_T0_DQS_EMCCLK_14	B26
G26	IO_L16N_T2_A15_D31_14	IO_L2P_T0_D02_14	B22
G25	IO_L16P_T2_CSI_B_14	IO_L2N_T0_D03_14	A22
E26	IO_L17N_T2_A13_D29_14	IO_L24P_T3_A01_D17_14	K23
F25	IO_L17P_T2_A14_D30_14	IO_L24N_T3_A00_D16_14	J23
H26	IO_L18N_T2_A11_D27_14	IO_L23P_T3_A03_D19_14	L22
J26	IO_L18P_T2_A12_D28_14	IO_L23N_T3_A02_D18_14	K22
G21	IO_L19N_T3_A09_D25_VREF_14	IO_L22P_T3_A05_D21_14	J24
H21	IO_L19P_T3_A10_D26_14	IO_L22N_T3_A04_D20_14	J25
A25	IO_L1N_T0_D01_DIN_14	IO_L21P_T3_DQS_14	J21
B24	IO_L1P_T0_D00_MOSI_14	IO_L21N_T3_DQS_A06_D22_14	H22
H24	IO_L20N_T3_A07_D23_14	IO_L20P_T3_A08_D24_14	H23

XC7K160T-FFG676

FLASH_D1
FLASH_D0
FPGA_FCS
FLASH_D2
FLASH_D3

FPGA_FCS

CCLK
QSPI_IC_CS_B
FPGA_PROG_B

VCC2V5 J5 VCC2V5

1	2
3	4
5	6
7	8
9	10
11	12

PTC06DAAN

SPI EXTERNAL PROGRAMMING HEADER

VCC2V5

R213 DNP
R214 DNP
R215 4.7K
R216 4.7K
R217 4.7K

FLASH_D0 R218 15
FLASH_D1 R219 15
FLASH_D21 R220 15
FLASH_D31 R221 15

QSPI_IC_CS_B

2.8V
See KC705 Sheet 26
VCC_SPI

C346 0.1

Serial Flash Memory for storing Xilinx personality.

U35

See xapp586 for details on using SPI flash

6	C
1	S_B
5	DQ0
2	DQ1
3	DQ2_VPP_WP_B
7	DQ3_HOLD_B
8	VCC
4	VSS

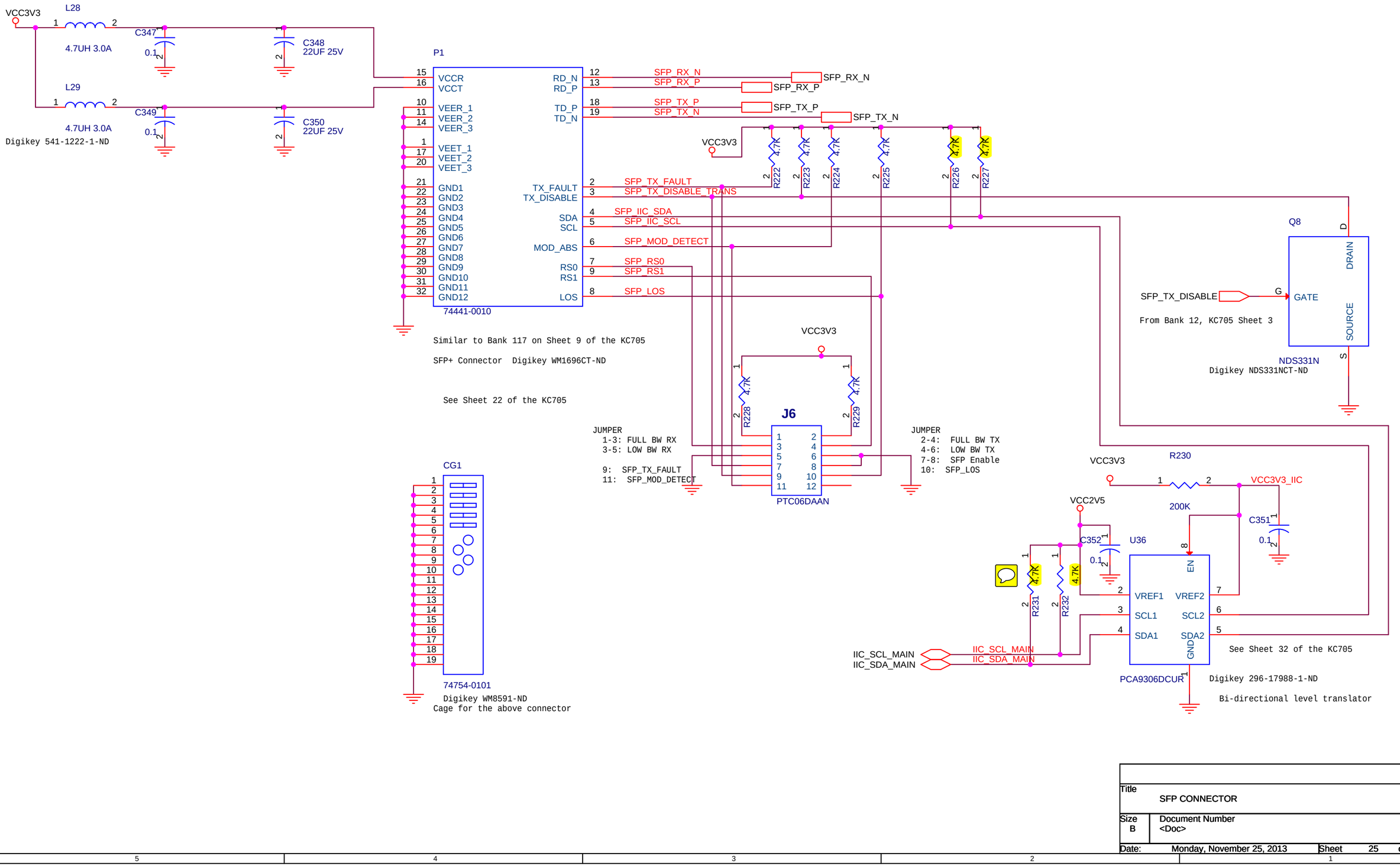
N25Q128

See KC705 Sheet 26

Digikey Part 557-1562-ND

128 Mb even though our Xilinx only needs 64Mb.

Title	FPGA QSPI	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 24 of 27	



Title	SFP CONNECTOR	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 25 of 27	

VCC3V3

L30

4.7UH 3.0A

L31

4.7UH 3.0A

Digikey 541-1222-1-ND

C353 0.1

C354 22UF 25V

C355 0.1

C356 22UF 25V

P2

15	VCCR	RD_N	12
16	VCCT	RD_P	13
10	VEER_1	TD_P	18
11	VEER_2	TD_N	19
14	VEER_3		
1	VEET_1		
17	VEET_2		
20	VEET_3		
21	GND1	TX_FAULT	2
22	GND2	TX_DISABLE	3
23	GND3		
24	GND4	SDA	4
25	GND5	SCL	5
26	GND6		
27	GND7	MOD_ABS	6
28	GND8		
29	GND9	RS0	7
30	GND10	RS1	9
31	GND11		
32	GND12	LOS	8

74441-0010

SFP_RX_N — SFP_RX_N

SFP_RX_P — SFP_RX_P

SFP_TX_P — SFP_TX_P

SFP_TX_N — SFP_TX_N

VCC3V3

R233 4.7K

R234 4.7K

R235 4.7K

R236 4.7K

R237 4.7K

R238 4.7K

SFP_TX_FAULT

SFP_TX_DISABLE_TRANS

SFP_IIC_SDA

SFP_IIC_SCL

SFP_MOD_DETECT

SFP_RS0

SFP_RS1

SFP_LOS

Similar to Bank 117 on Sheet 9 of the KC705

SFP+ Connector Digikey WM1696CT-ND

See Sheet 22 of the KC705

Q9

SFP_TX_DISABLE — G — GATE

D — DRAIN

S — SOURCE

From Bank 12, KC705 Sheet 3

NDS331N

Digikey NDS331NCT-ND

VCC3V3

R239 4.7K

R240 4.7K

J7

1	2
3	4
5	6
7	8
9	10
11	12

PTC06DAAN

JUMPER
1-3: FULL BW RX
3-5: LOW BW RX

9: SFP_TX_FAULT
11: SFP_MOD_DETECT

JUMPER
2-4: FULL BW TX
4-6: LOW BW TX
7-8: SFP Enable
10: SFP_LOS

CG2

74754-0101

Digikey WM8591-ND
Cage for the above connector

VCC3V3

R241 200K

VCC3V3_IIC

VCC2V5

C358 0.1

C357 0.1

U37

		EN	8
2	VREF1	VREF2	7
3	SCL1	SCL2	6
4	SDA1	SDA2	5
		GND	

PCA9306DCUR

Digikey 296-17988-1-ND

Bi-directional level translator

R242 4.7K

R243 4.7K

IIC_SCL_MAIN

IIC_SDA_MAIN

IIC_SCL_MAIN

IIC_SDA_MAIN

See Sheet 32 of the KC705

Title	SFP CONNECTOR	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 25, 2013	Sheet 26 of 27	

ZDOK Connector 550-5 as on the Roach Board
Note this is the mirror image of the
footprint on the ZDOK board.

Use 2.5V VCCO
1 is P, 2 is N on ZDOK

Digikey 6367550-5-ND

P3

ZDOK CONNECTOR 550-5

VCC5V0 VCC3V3 VCC2V5 VCCAUX

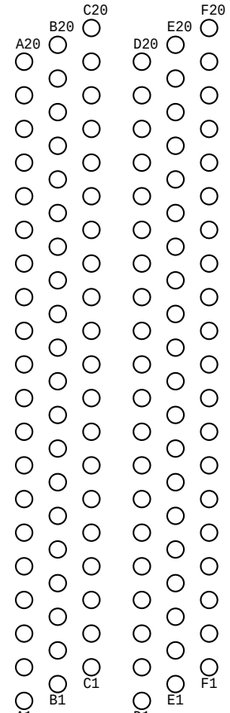
Supplies 1.8V

W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5

A[20:1] D[20:1] C[20:1] F[20:1]

CLK1P_F19
CLK1N_F20

W1 X1 Y1 Z1 W6 X6 Y6 Z6



ZDOK Pin Layout

Title	ZDOK Connector
Size B	Document Number <Doc>
Rev	<RevCode>
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