IBOB Test Procedure (last rev. 2007/06/11, HC, SM)

1. Visually inspect PC board for assembly issues.
    1. Check orientations of all of polarized capacitors.
    2. Check Pin 1 orientations of all active devices.
    3. Check that voltage regulators have correct placement.
    4. Check solder and for any visible shorts.
2. Record FPGA datecode.
3. Install Headers.
    1. Set GPIO I/O bank voltage selection at J4 to 2.5V.
    2. XAUI reference clock selection headers: use 125.00MHz (see Figure 1); J11/J12 and J13/J14 are horizontal mirror images.

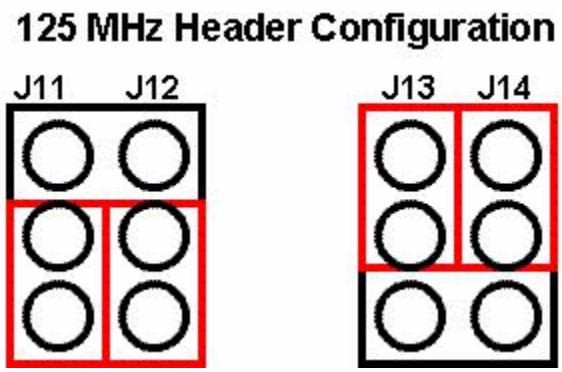

Figure 1: Orientation of J11/J12, J13/J14 header installation for 125MHz XAUI reference clock.

4. Check for cross-rail shorts by probing inter-plane impedances using DMM; GND at J19 is convenient for probe; P4, P5, P6–pin 4 is output of PT regulators. See Figures 2, 3, and 4.

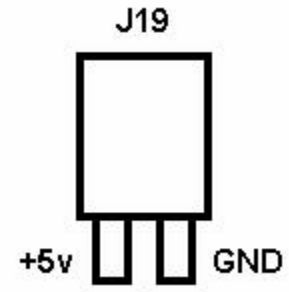

Figure 2: Main power connector J19 pinout.

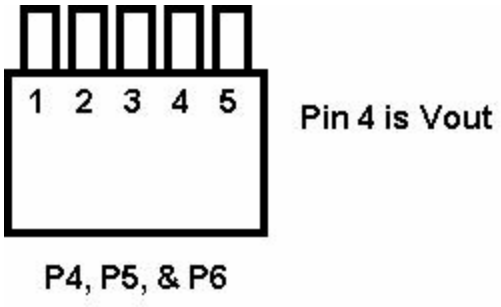

Figure 3: DC/DC switching regulator P4/P5/P6 pinout.

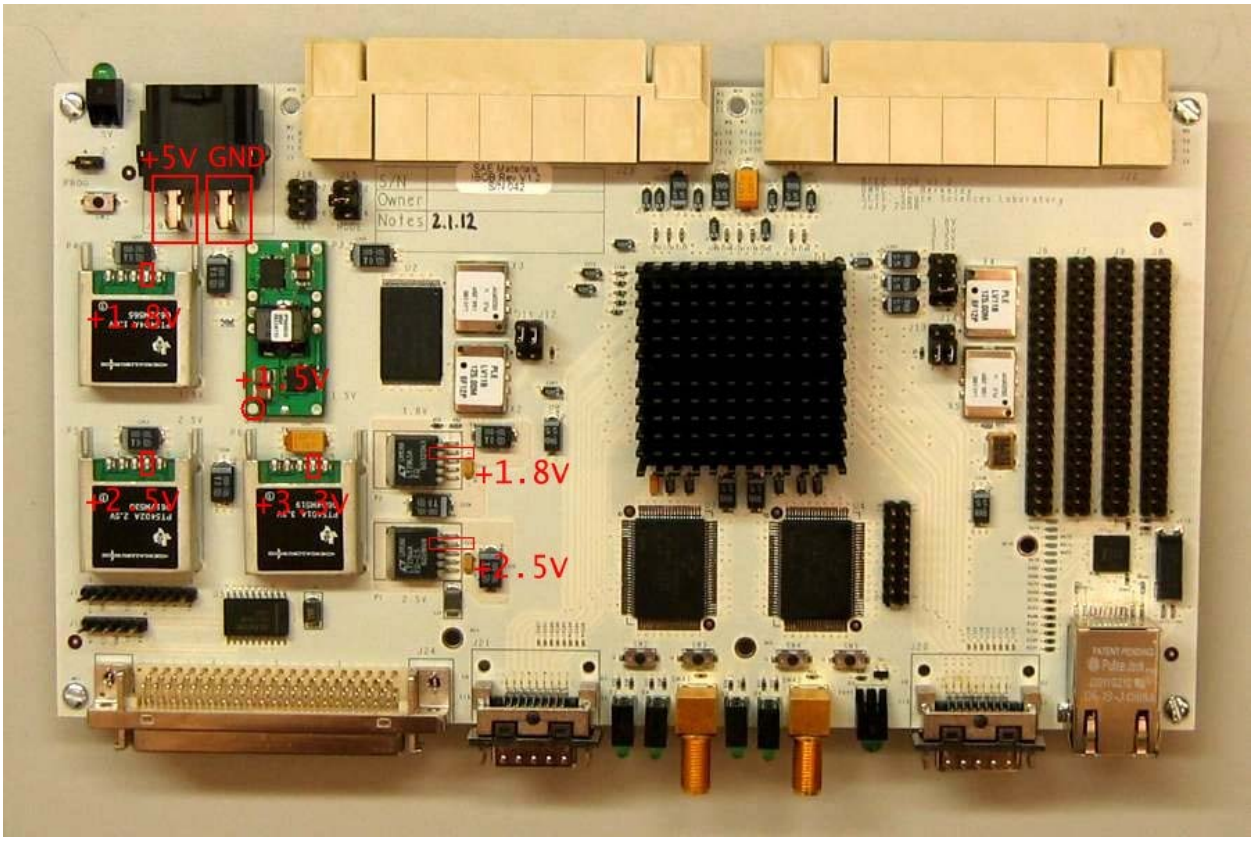

Figure 4: Voltage probe points.

Typical cross-rail resistances:

	GND	5V	1.5V	1.8V	2.5V	3.3V	A2.5V	A1.8V
GND	x	15kOhm	20Ohm	20kOhm	4.5kOhm	1.5kOhm	3kOhm	1.5kOhm
5V	x	x	20kOhm	60kOhm	15kOhm	20 kOhm	100kOhm	50kOhm
1.5V	x	x	x	20kOhm	4.5kOhm	1.5kOhm	450Ohm	1.5kOhm
1.8V	x	x	x	x	20kOhm	4.5kOhm	6kOhm	4.5kOhm
2.5V	x	x	x	x	x	5kOhm	650Ohm	3MOhm
3.3V	x	x	x	x	x	x	4.5kOhm	3kOhm
A2.5V	x	x	x	x	x	x	x	450Ohm
A1.8V	x	x	x	x	x	x	x	x

5. Set up the voltage source.
    1. Limit the current to 1A; the idle current of the boards with no fans or attachments should be ~0.3A.
6. Board power-up check.
    1. Turn on board; loss of magic smoke?
    2. Check voltage levels @ regulators, and caps C252 (1.5V), C247 (2.5V), C240 (1.8V), and C241 (2.5V).
7. Install heatsink.
    1. Turn power supply off.
    2. Clean surface of FPGA package with rubbing alcohol.
    3. Attach heatsink–it has double sticky side tape. Primary “channel” or “trough” on heatsink should be parallel to length of board (Figure 5).

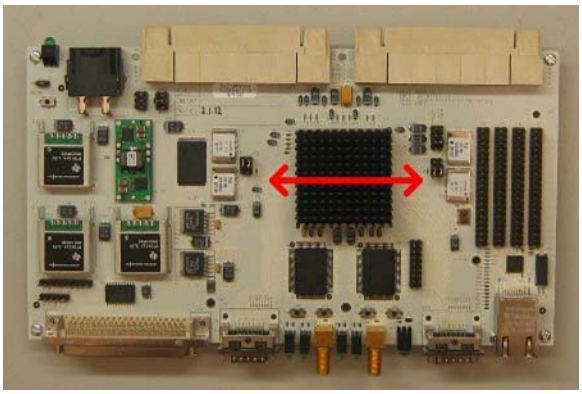

Figure 5: IBOB heatsink alignment.

8. Attach cables
    1. Connect 3-meter XAUI cable between XAUI ports J20 and J21.
    2. Connect CAT5 cable with custom loopback (labeled loop) to RJ45 port J115.
    3. Attach Xilinx Parallel IV download cable to J17. Match VREF pin from download pod to VCC pin on IBOB J17.

4. Attach serial cable from serial terminal host to J18; RXs should provide cable orientation (marked side is RX).

9. Turn on main power supply. Increase current limit to ~3A.
10. Run the test suite
    1. Connect to the IBOB's serial interface using a serial terminal emulator. If using a Linux machine, **minicom** is suggested. On a Windows machine, two options are available: **HyperTerminal** or **CRT**. The serial terminal settings needed are:
        - *Protocol*: Serial
        - *Port*: COM1 (varies based on host computer and setup)
        - *Baud*: 115200
        - *Databits*: 8
        - *Parity*: None
        - *Stop Bits*: 1
        - *Flow Control*: none
    2. Program the FPGA with the test suite bitstream
        - Run **iMPACT**
        - Click *Cancel* when asked to create a new project.
        - Select the *Boundary-Scan* mode tab. Right-click and select *Initialize Chain* or type **CTRL-I**. 2 devices should be detected in the boundary scan chain: an *xcf32p* (PROM) and an *xc2vp50* (FPGA).
        - When asked to assign a new .MCS configuration file for the PROM, click *Cancel* or *Bypass*.
        - When asked to assign a new .BIT configuration file for the FPGA, select the test suite bitfile.
        - Download the bistream to the FPGA:
            1. Right click on Xilinx chip *XC2VP50*
            2. Click *Program*
            3. Make sure *Pulse Prog* is selected
            4. Click *OK*
        - When completed successfully, *Done* LED D2 lights.
        - Current draw should be ~1.8A.
    3. Serial terminal should display *IBOB%* prompt
11. Run the test suite testers in the serial console to test SRAM, Ethernet, XAUI functionality
    1. *?* gives list of available commands
    2. Test the Ethernet
        - Run **testmac**
        - If *No packet received* something is wrong with Ethernet. When the Ethernet works, you will see a test packet sent and received.
    3. Test the SRAM using **sramreset** and **sramrefresh**
        - **sramreset 0** tests the SRAM using a sequential addressing pattern and an LFSR pseudo-random number data pattern.
        - **sramreset 1** tests the SRAM using a sequential addressing pattern and an all-zeros data pattern.
        - **sramreset 2** tests the SRAM using a sequential addressing pattern and an all-ones data pattern.

- **sramrefresh** refreshes the status displays of how many write/readback passes have been completed and the error count.

4. Test the XAUI connection running with 125.00MHz reference clock (8Gb/s)
    - Run **xauireset 0 xff**
    - Refclk display is hardcoded at 156.00 MHz, so ignore. Make sure you see "*0*'s" and not "*Link Down*" or "*No Link*"
    - Run **xauirefresh** repeatedly to refresh the test status display.
    - Check to see the link doesn't drop and that it can achieve an error rate of better than 10^-13.
5. Test the XAUI connection running with 156.25MHz reference clock (10Gb/s)
    - Turn off board
    - Change headers for 156.25MHz XAUI reference clock (Figure 6)
    - Turn board on and reprogram test suite, rerun XAUI test as above.

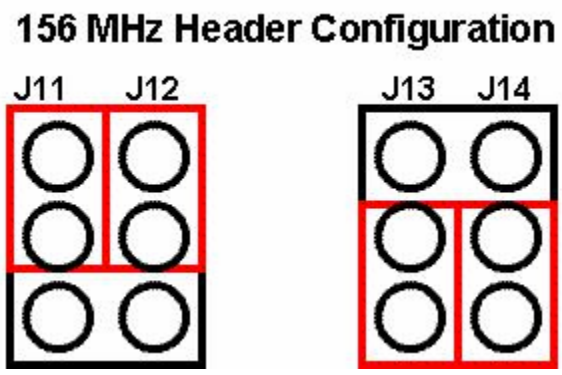

Figure 6: Orientation of J11/J12, J13/J14 header installation for 156.25MHz XAUI reference clock.

12. Test Z-DOK connectors
    1. There are two ways to test the Z-DOKs:
    2. Run ADC capture scope; tests both Z-DOKs
    3. Run the pocket spectrometer; tests 1 Z-DOK (J22)
        - Installing a heatsink fan or some other form of active cooling is recommended.
        - Attach iADC Atmel AT84AD001B dual 1-Gsps ADC board to Z-DOK J22
        - Connect 500MHz@0dBm RF signal to ADC *clk_i* SMA input
        - Connect test signal (CW tone < -15dBm or noise through VLF-220MHz filter) to ADC *I+* SMA input
        - Idle (unprogrammed) current draw with ADC attached should be ~0.8A.
        - Program the FPGA with pocketspec bitstream
        - Pocketspec current draw should be ~3.4A.
        - Run **pocketplot** backend software on Linux host machine to see spectra