Smart Network ADC Processor (SNAP)
Design Manual

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Change Record

Version	Date	Affected Section(s)	Reason/Initiation/Remarks
A	2013-8-5	All	Initial version
A01	2013-8-28	Several	Add clk gen partial schematic and ADC schematic. Add some discussion on the ADC and clk gen.
A02	2013-9-13	Several	Add info on Xilinx, synthesizer
A03	2013-11-12	Several	Add info on analog regulators
A04	2013-12-03	Several	Merge versions A02 and A03. Change project name from HERALD to SNAP

1. Contents

2. Description

2.1 Purpose

The purpose of this document is to describe the design and operation of Data Acquisition Board for the Smart Network ADC Processor (SNAP) project.

2.2 Scope

This document serves as the repository for documenting design-related decisions as well as for providing an overview of the design.

2.3 Related Documents and Drawings

2.4 References

2.5 Abbreviations and Acronyms

2.6 Glossary

2.7 Related Interface Control Drawings

3. Overview

3.1 Data Acquisition Board function

The SNAP Data Acquisition Board includes many features that make it a stand-alone data acquisition system. Please reference the block diagram on the last two pages of Appendix 1. The SNAP includes 12 analog inputs, provisions for an internal or external sampling clock, an FPGA primarily to format the data, a microprocessor for control and two SFP+ connectors for transmitting the formatted data.

3.2 Design Methodology

The prototype board will be stand alone. It will not be packaged in the box.

a) Features already designed or easily implemented will be included to allow an easy transition to a box for subsequent versions.

b) Extensive additional effort relating to the board going in the box can be put off for the next

version.

c) Include on the board holes for standoffs so the board can sit on those standoffs on the bench.

d) Include the slide on SMA connectors, soldered to the board.

e) Include a heatsink for the Kintex Chip.

4. Detailed Design Description

4.1 ADC design

4.1.1 Analog Input

The analog inputs are a copy of the Berkeley rev 2 design. Inputs are transformer coupled to turn the 50-ohm single-ended inputs into differential inputs that the ADC expects. Two 36.0-ohm resistors form the termination for the input. The common mode offset from the ADC is used to bias the center-point of the resistor terminations to set the DC bias of the input at optimum for the chip. The 33.0 ohm resistors are recommended by Hittite to limit the "kickback" from the ADC into the analog input lines. The capacitors in parallel with the input are included for possible matching. The values used are based on tests by Matt Dexter to achieve the best S11 at the input. For the record, a summary of Matt's measurements are the following:

Rterm ohm	Rseries ohm	Cshunt pF	S11	rms change for CW from 101 to 401 MHz
36	33	none	-17 to -21	0 to -5.9 dB
36	22	none	-19 to -18	0 to -5.0 dB
36	10	none	-14 to -15	0 to -3.8 dB
36	0	none	-17 to -12	0 to -3.9 dB

Clearly, these values can be adjusted to optimize the inputs for other applications.

4.1.2 ADC IC

The HMCAD1511 is selected. This is the same ADC that is used in the Berkeley rev 2 design.

4.1.3 Supply Voltages and Decoupling

For ADC decoupling, the eval board recommends 10nf as close as possible to each power pin and 1 uF where it will fit. They have a total of 4 1uF and 6 10 nF for the total of 6 power pins. The Berkeley has 4 of the 1 uF and 6 10 nf as well. The Berkeley design also includes an inductor for the analog but none for the digital power for each ADC. The inductor is preceded by another set of 10 nf + 1 uF. Since our design will include many noisy components, add a second inductor and 10 nf + 1 uF for the digital power as well. Further, Werthimer recommends an additional 1 nf in parallel with the 10 nf associated with the analog supplies to the ADC. This provides lower impedance decoupling in the critical 60 to 250 MHz range.

Per Matt Dexter, all grounds are connected together on the Berkeley rev 2 board. This was a decision made at a higher level. We may want to consider adding a zero-ohm jumper to the design to force the ground planes to connect in one place. This is worth discussing. If we decide to do this, the schematic will need to be revised to incorporate two ground symbols, digital and analog. We can also use judicious layout to control where the ground currents flow and avoid picking up digital hash in the analog part of the circuit.

4.2 Clock

4.2.1 Clock Driver

The quality of the input clock is extremely important for high-speed, high-resolution ADCs. The contribution to SNR from clock jitter with a full scale signal at a given frequency is shown in equation 1.

$SNR_{jitter} = 20 \bullet \log (2 \bullet \pi \bullet f_{IN} \bullet \epsilon t)$

Where f_{IN} is the signal frequency and ϵt is the total rms jitter measured in seconds. The total jitter includes all jitter sources including the clock generation circuitry, clock distribution and internal ADC circuitry. (from HMCAD1511 data sheet, p. 28).

The Hittite ADC eval board provides several options for its clock. These are not particularly applicable in our case since we have 3 ADCs on our board.

The Berkeley 4-ADC board uses a Hittite HMC987LP5E for clock distribution to its 4 ADCs. This seems like a good option for us. The chip is designed for low jitter clock distribution. Also, unused outputs can be powered down, so there is no power penalty.

The clock input has built-in terminations. Several impedance configurations can be programmed via the SDI interface. The outputs of the 987 are LVPECL. Power is nominally 3.3V and Hittite recommends its own HMC976LP3E regulator to provide power because it has good noise properties (low noise density and high PSRR).

The clock driver output swing is nominally 800 mv with 120 ohm per leg DC termination and 50-ohm AC-coupled load (so 1600 mv differential swing). This is the configuration on the Berkeley ADC board. Further, the data sheet for the 987 claims that a 200 ohm DC load results in no degradation and that a 10-ohm series resistor improves S22. So we can design our circuit to have the 200-ohm and 10 ohm resistors and easily revert to the Berkeley configuration if necessary.

As a check, the ADC chip says it accepts LVDS and LVPECL inputs. It also says that a differential sine wave clock should have an impedance of at least 1500 mv. So we should be in good shape with the existing configuration so long as line losses don't attenuate the signal too much.

Another chip that has been considered is the OnSemi NB7L585. It includes more functionality than the HMC987LP5E: it has a 2:1 mux in front of the clock tree. Using this chip would save a chip in the design since we need a 2:1 mux in front of the clock distributor. However, the chip has a considerably higher phase noise spec and using it would make it tough to meet our total jitter specification of 1 pico-second. A comparison between the two chips is shown below:

Spec	**OnSemi NB7L585**	**HMC987LP5E**
Vin range (differential)	100 - 1200 mv	NS
Vin range (single ended)	0.2 - 1.2 Vpp	0.2 - 2 Vpp
Built-in term	Yes	Yes
Phase Noise		
Fin = 1 GHz, offset = 10 KHz	-135 dbc	NS
offset = 100 KHz	-137 dbc	NS
offset = 1 MHz	-149 dbc	NS
offset = 10 MHz	-150 dbc	NS
offset = 20 MHz	-150 dbc	NS
offset = 40 MHz	-151 dbc	NS
Fin = 622.08 MHz, offset = 100 Hz		-147 dbc
Integrated Phase jitter 12KHz - 20 MHz, fin = 1 GHz	36 fs rms	
Integrated Phase jitter 12KHz - 20 MHz, fin = 622.08Hz	NS	8 fs rms
Integrated Phase jitter 12KHz - 20 MHz, fin = 1750Hz	NS	3 fs rms
Integrated Phase jitter 4MHz - 80 MHz, fin = 1750Hz	NS	6 fs
Output random jitter, Fin < 5 GHz	0.8 ps max	ns
Output swing	1.7 Vpp differential	1.6 Vpp differential
Output rise/fall times	25 - 85 ps	65 ps typ

Output skew	20 ps max	3.1 ps max
Fmax	5 GHz, min	5 GHz, 3db BW
Power supply voltage	2.5 or 3.3 V	3.3 V
Power supply rejection		
AM	NS	7 db
FM	NS	.8 ps/V
Pin programmable	Yes	Yes
price, 1	10.73	16.19
price, 1000	7.71	10.34

Table 4-1. Comparison of two clock driver chips.

Given the above choice, we need to select a 2:1 mux. A survey of available suitable chips resulted in the conclusion that the Hittite HMC922LP4E was the best choice. It has a far better phase noise specification than the rest of the chips surveyed. This is likely because it consists of solid state switches and not amplifiers.

4.3 Synthesizer Design

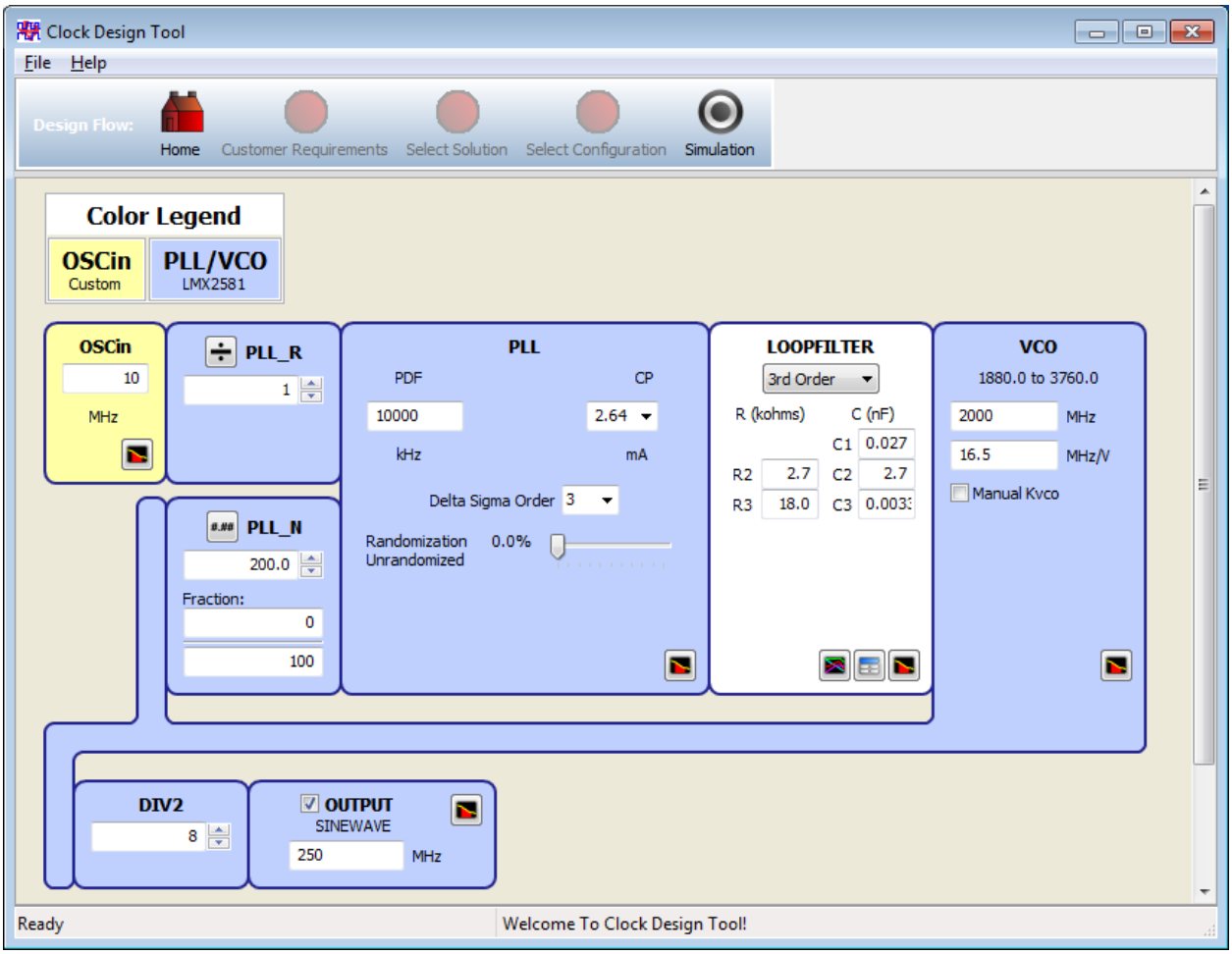
Per telecom discussions we decided to use the Texas Instruments LMX2879 over the Hittite HMC1034 even though the Hittite part had better phase noise. It was found that the TI part would meet the goals of the project. A comparison of the two synthesizer chips is shown below:

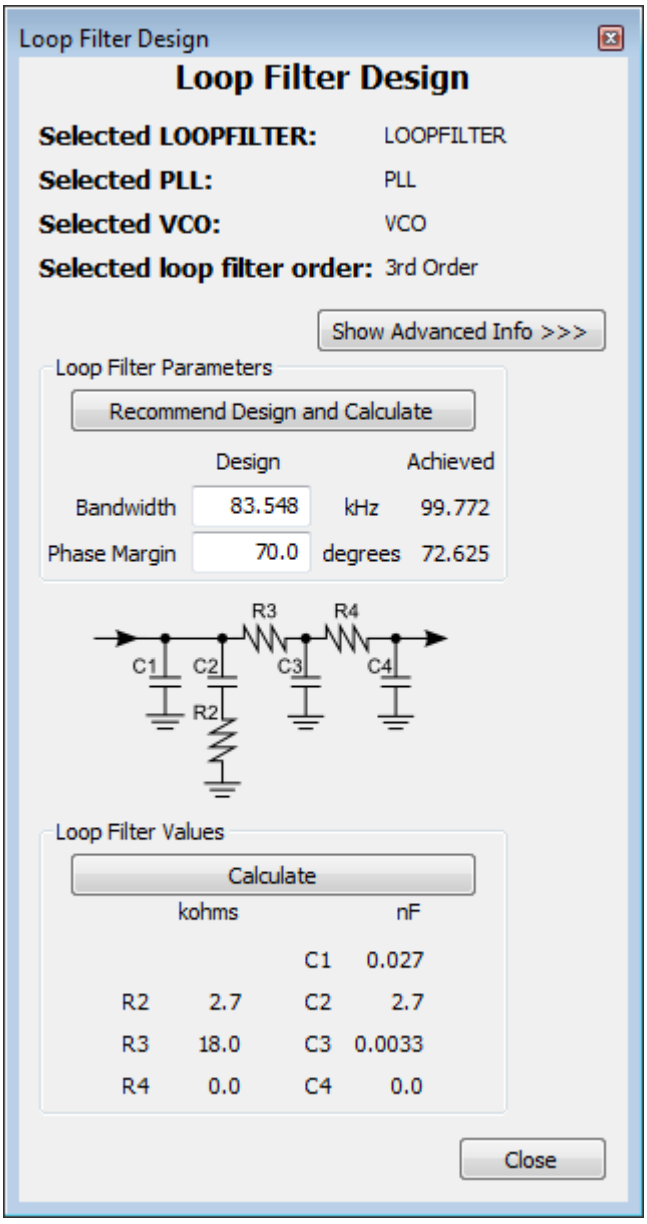
	HMC1034LP6GE	**LMX2581SQ**
Support	Rapid direct response	Only support is TI forum
Price, single	$44.90	$14.30
Price, 500	$31.27	$8.35
Icc, 3.3 V	52 ma	178 ma
ICC, 5V	228 ma	not req'd
Power	1.3116	0.5874

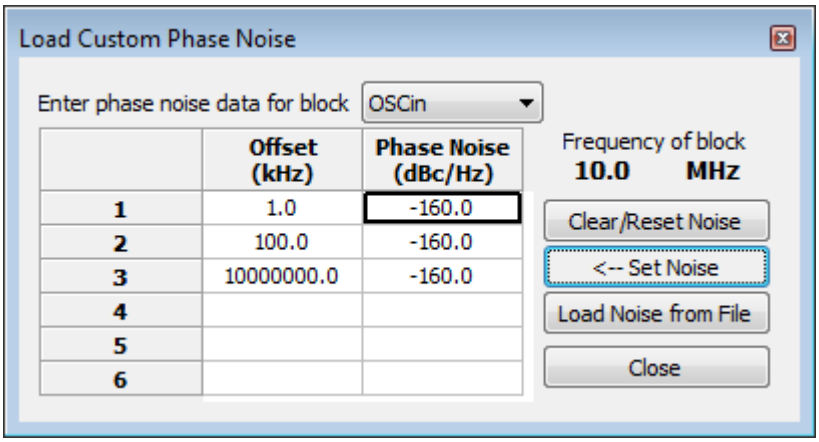
Input Osc Freq. Range	.008 to 350 MHz	5 to 250 MHz
Output Freq.	125 to 3000 MHz	50 to 3760 MHz
Phase noise, offset 10 KHz	-115 dBc/Hz	-84.8 dBc/Hz
Phase noise, offset 1 MHz, f = 2 Ghz	-130 dBc/Hz	-136.7 dBc/Hz
Noise floor	-227 dBc/Hz	-229 dBc/Hz
Phase jitter (.012 to 20 MHz)	78 to 118 fs	not specified
Output Power max	0 to 3.3V diff swing	11 dbm (2.26 Vpp)
Control Interface	serial	serial

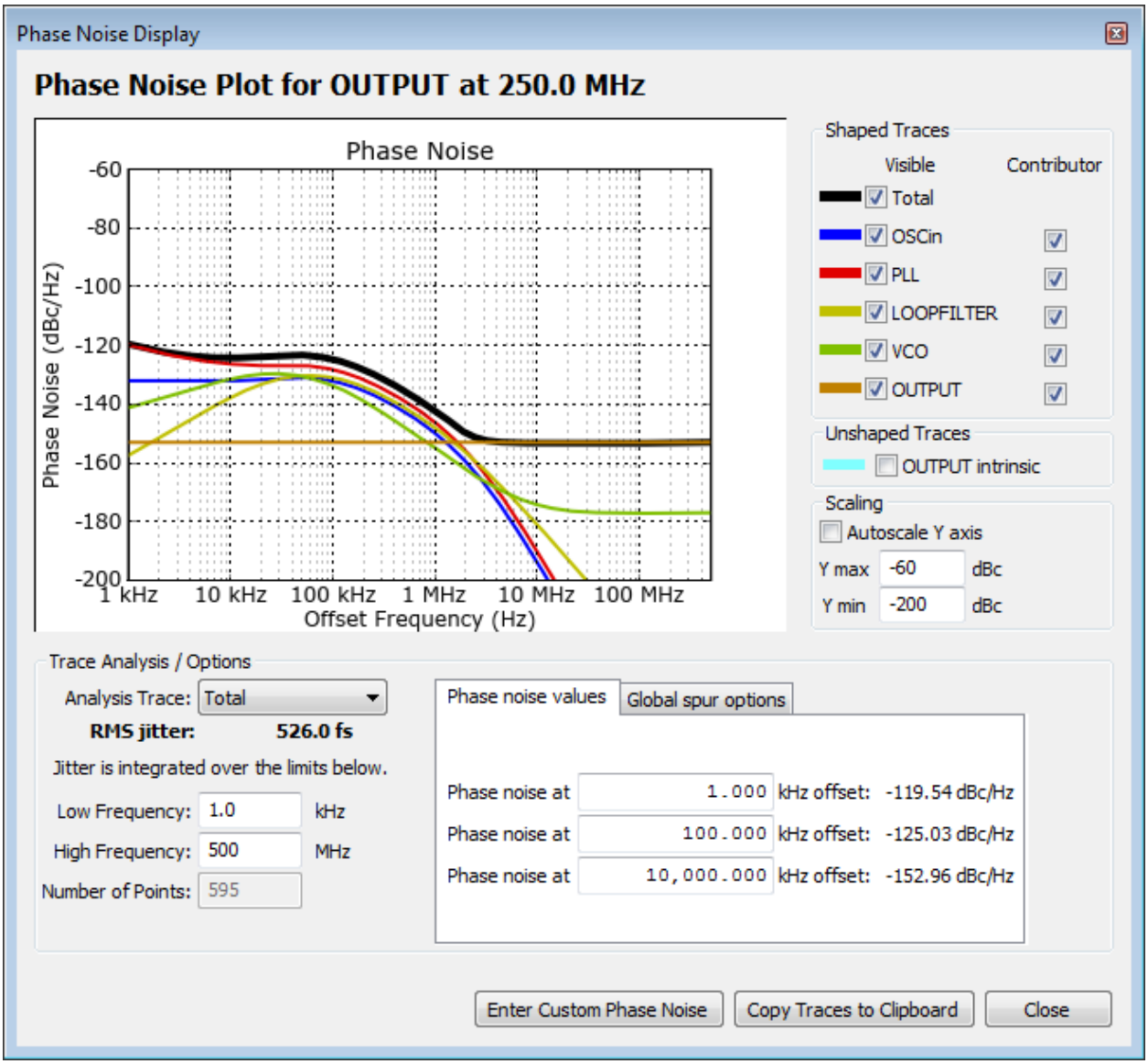
Table 4-2. Comparison of TI and Hittie synthesizer chips.

Use the TI-supplied synthesizer Clock Design Tool CAD package for detailed design. Assume we have a 10 MHz input. The following design provides 250 MHz:


Clock Design Tool
File Help
Design Flow:
Home
Customer Requirements
Select Solution
Select Configuration
Simulation
Color Legend
OSCin
Custom
PLL/VCO
LMX2581
OSCin
10
MHz
PLL_R
1
PLL_N
200.0
Fraction:
0
100
PLL
PDF
10000
kHz
CP
2.64
mA
Delta Sigma Order
3
Randomization
Unrandomized
0.0%
LOOPFILTER
3rd Order
R (kohms)
C (nF)
C1
0.027
R2
2.7
C2
2.7
R3
18.0
C3
0.003
VCO
1880.0 to 3760.0
2000
MHz
16.5
MHz/V
Manual Kvco
DIV2
8
OUTPUT
SINEWAVE
250
MHz
Ready
Welcome To Clock Design Tool!

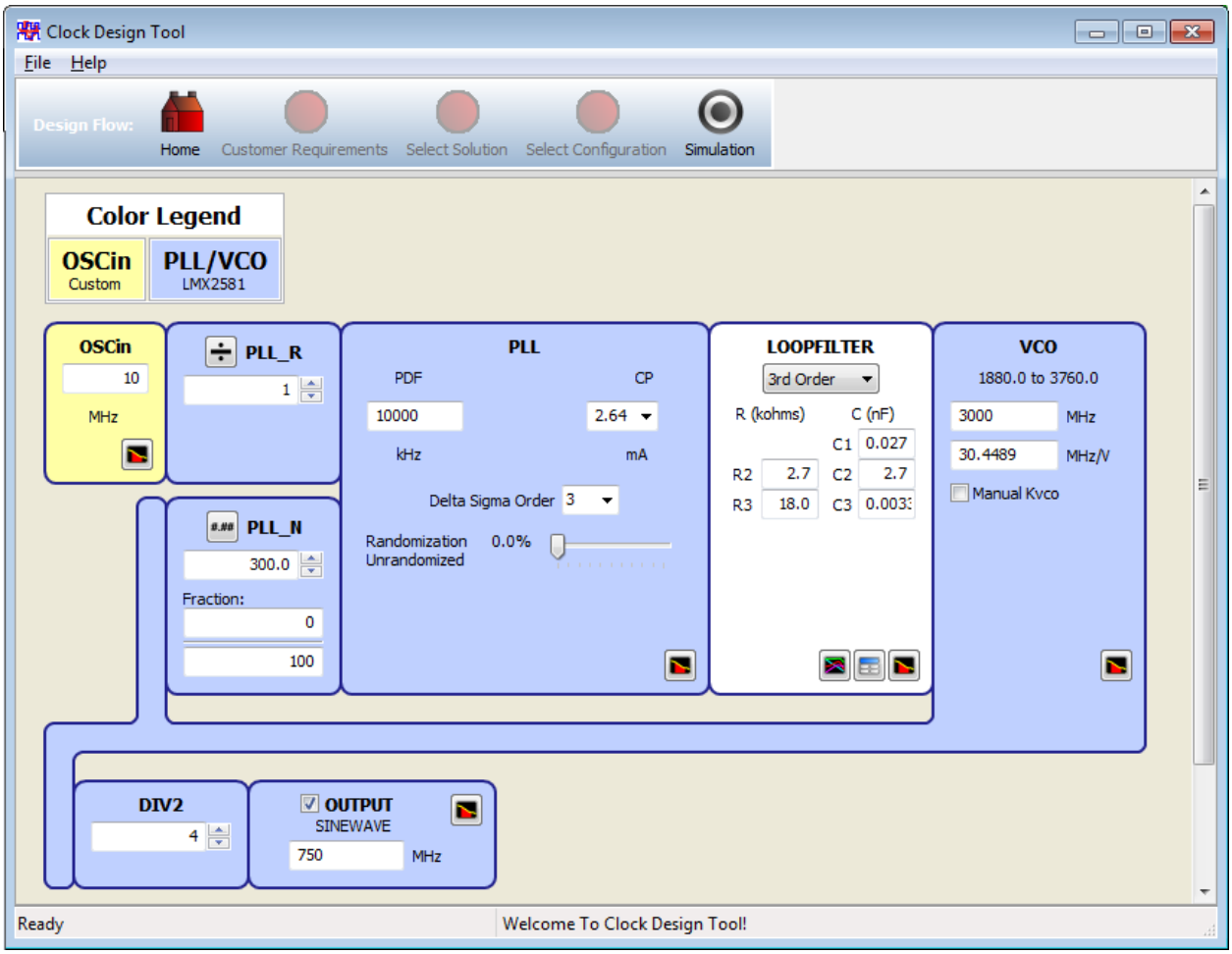

Loop Filter Design
Loop Filter Design
Selected LOOPFILTER: LOOPFILTER
Selected PLL: PLL
Selected VCO: VCO
Selected loop filter order: 3rd Order
Show Advanced Info >>>
Loop Filter Parameters
Recommend Design and Calculate
Design
Achieved
Bandwidth 83.548 kHz 99.772
Phase Margin 70.0 degrees 72.625
R3
R4
C1
C2
C3
C4
R2
Loop Filter Values
Calculate
kohms
nF
C1 0.027
R2 2.7
C2 2.7
R3 18.0
C3 0.0033
R4 0.0
C4 0.0
Close

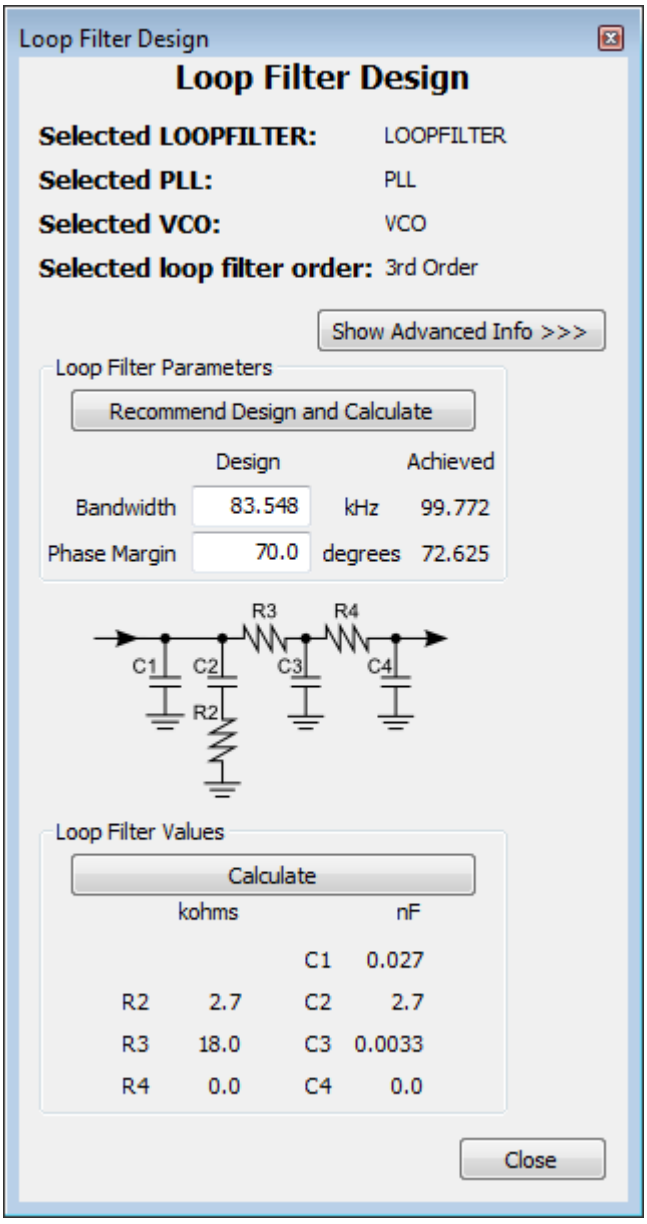

Load Custom Phase Noise
Enter phase noise data for block
OSCin
Offset (kHz)
Phase Noise (dBc/Hz)
1
1.0
-160.0
2
100.0
-160.0
3
10000000.0
-160.0
4
5
6
Frequency of block
10.0 MHz
Clear/Reset Noise
<-- Set Noise
Load Noise from File
Close

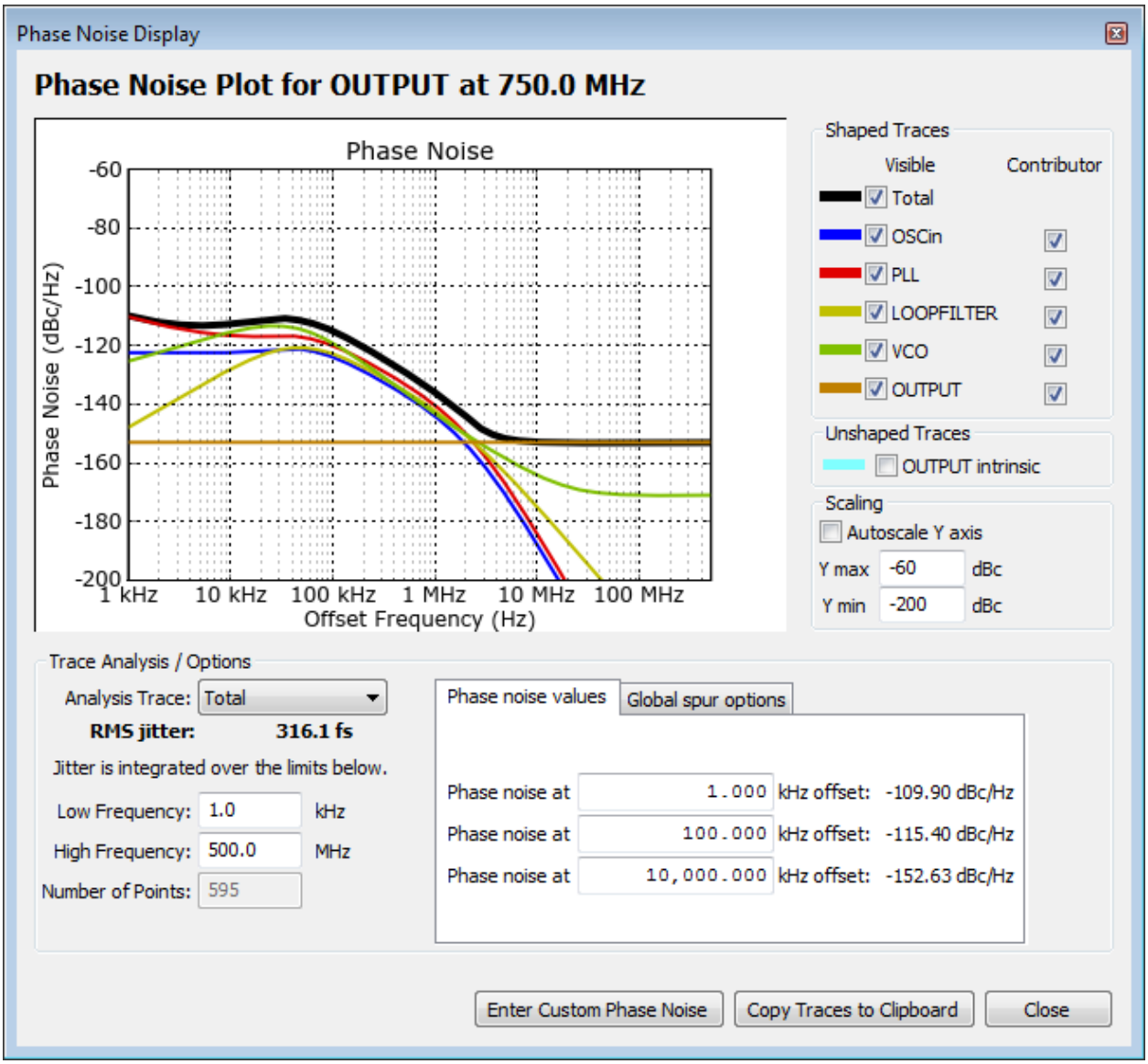


So we meet the jitter spec by a factor of two at 250 MHz. This assumes a low phase noise 10 MHz reference as shown above.

The following design provides a 750 MHz output:


Clock Design Tool
File Help
Design Flow:
Home
Customer Requirements
Select Solution
Select Configuration
Simulation
Color Legend
OSCin
Custom
PLL/VCO
LMX2581
OSCin
10
MHz
PLL_R
1
PLL_N
300.0
Fraction:
0
100
PLL
PDF
10000
kHz
CP
2.64
mA
Delta Sigma Order
3
Randomization
Unrandomized
0.0%
LOOPFILTER
3rd Order
R (kohms)
C (nF)
C1
0.027
R2
2.7
C2
2.7
R3
18.0
C3
0.003
VCO
1880.0 to 3760.0
3000
MHz
30.4489
MHz/V
Manual Kvco
DIV2
4
OUTPUT
SINEWAVE
750
MHz
Ready
Welcome To Clock Design Tool!


Loop Filter Design
Loop Filter Design
Selected LOOPFILTER: LOOPFILTER
Selected PLL: PLL
Selected VCO: VCO
Selected loop filter order: 3rd Order
Show Advanced Info >>>
Loop Filter Parameters
Recommend Design and Calculate
Design
Achieved
Bandwidth
83.548
kHz
99.772
Phase Margin
70.0
degrees
72.625
R3
R4
C1
C2
C3
C4
R2
Loop Filter Values
Calculate
kohms
nF
C1 0.027
R2 2.7
C2 2.7
R3 18.0
C3 0.0033
R4 0.0
C4 0.0
Close



For this frequency, we have an even more comfortable margin for jitter.

One down-side of this chip is that it has 16 32-bit registers that need to be programmed. We can provide an electrical interface to the FPGA. We can worry about the programming later.

The synthesizer has a very restrictive specification for the oscillator input: ≤ 1.8 volts with VCC applied and ≤ 1.0 volts with power off. The Shottky diode arrays D2 and D3 are used to provide the required limits. With power on, we should see about 0.8 volts positive due to D3 and -0.4 volts

negative due to D2. With power off, VCC_3V3_SYN = 0 and D2 limits the swing to ± 0.4 volts. If the asymmetry turns out to be a problem, zero ohms can be installed at R41. The synthesizer prefers a high-slew-rate square-wave to a sine-wave, so there may be a trade-off between over-driving the input and having a good S11.

An SMA test point is associated with the synthesizer to allow for the measurement of phase noise.

4.4 FPGA Design

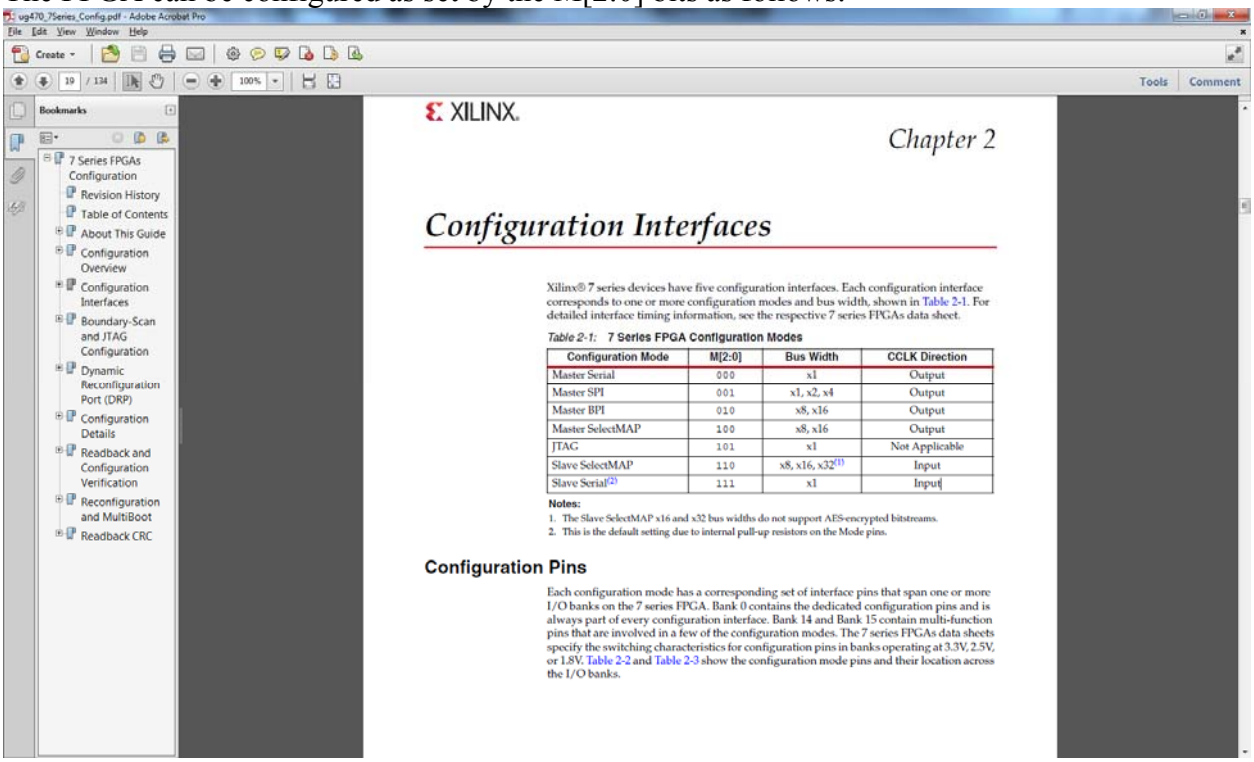
4.4.1 FPGA Design Based on Kintex Evaluation Board

The FPGA design is based on the KC705 Kintex Evaluation Board we have purchased.
Note the Evaluation Board uses the larger XC7K325TFFG900 Kintex 7 chip than the XC7K1605-FFG676 which we use in our design. These chips have different pinouts.

4.4.2 Orcad Xilinx Schematic Symbol

The library symbol for the FPGA was purchased for $14 from the site:
http://www.schematicsymbol.com/Xilinx_Kintex-7.htm

FPGA Configuration
The FPGA can be configured as set by the M[2:0] bits as follows:



4.4.3 JTAG Interface to the FPGA

The JTAG interface is via Xilinx Bank 0. A JTAG header and also a USB JTAG connection are provided for downloading the Xilinx personality. The evaluation board has the JTAG going to a possible Mezzanine card. For simplicity I eliminated that option. I use a 4 bit level shifter instead of a 2 bit and a 1 bit, since we have already used the 4 bit chip on the PIC. I don't buffer the TDO since the KC705 did not buffer the TDO.

4.4.4 Done and Init

Also via Bank 0 is the FPGA_DONE line. This indicates when the Xilinx personality has been successfully downloaded.

Also via Bank 0 is the FPGA_INIT_B line. This can be activated by a push button. Alternately a switch is in place that connects to the FPGA_DONE line. This will automatically initialize the FPGA whenever the personality is not loaded.

4.4.5 SPI Loading of the FPGA

Decided to use the N25Q128 as in the evaluation board. This is the 128 M RAM rather than the 64 M Ram we specified because the 64 M RAM is not available in small quantities. See xap586 for details on using the SPI Flash for configuration.

4.4.6 SFP+ Cage

A Hierarchal block is included for providing each SFP+ interface. The connectors go directly to Bank 115 and 116 which provide the MGT high speed interfaces. The SFP+ connector cage is a separate component that has its pins soldered to ground. IIC interface is provided via connections to Bank 15.

An IIC mux/translator PCA9548ARGER was eliminated since we don't have multiple IIC component and its spec said "not recommended for new designs". Instead a single channel PCA9306 translator was used to provide the 3.3V to 2.5V bidirectional translation.

4.4.7 Clocks

Two off the shelf from Mouser Clock Oscillators were chosen for the 100 MHz and 156.25 MHz clocks. The 100 MHz uses 2.5V, is 20 ppm, outputs HCSL. The 156.25 MHz uses 3.3V, is 50 ppm, and outputs LVDS. The two oscillators could be special ordered with more similar specs. These each go into MRCC (Multi Regional) Clock inputs of the Xilinx.

4.4.8 LED's

Four LED's were added to bank 33 as on the KC705. Rather than scatter the remaining 4 LEDs onto different Banks, I put them on bank 33 as well, in place of some LCD display signals.

4.4.9 ZDOK Connector

A ZDOK Connector is added to include 40 LVDS pairs. The thought is to allow existing cards that plug into a Roach Board to plug into this card as well. The VCCO output goes to VADJ_FPGA which may be adjustable if implemented that way.

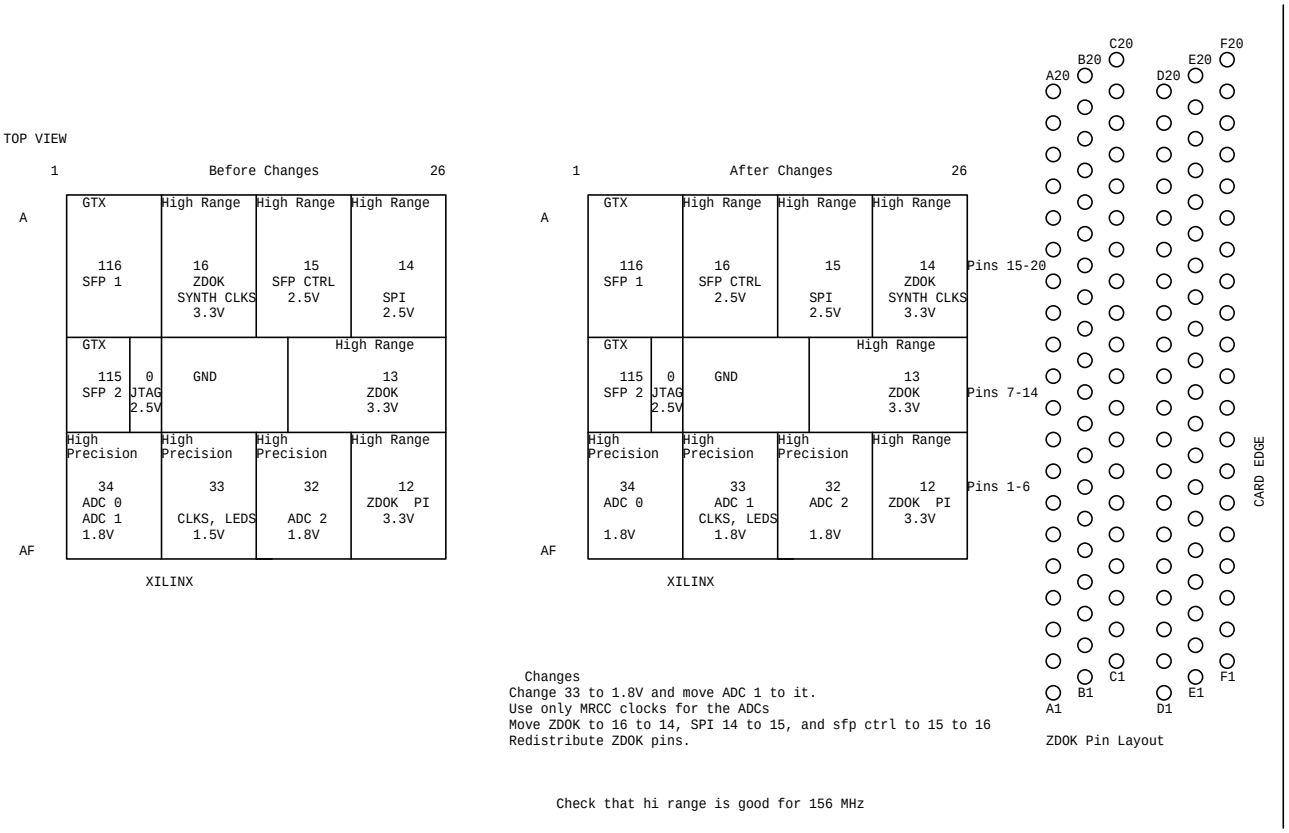
4.4.10 Raspberry PI Interface

PI2 is a 40 pin connector for interfacing with the Raspbery PI Version B+. This is an upgrade from the 26 pin connector for PI Version B.

The connector provides 5V to power the PI. 3.3V is generated from the 5V and fed back. This goes through a resistor and can be used to verify the PI powered up. On the 40 Pin connector there are provisions for UART, SPI, and IIC busses, as well as GPIO. This will use a 40 wire ribbon cable. The pins go to 3.3V VCCO Xilinx pins.

4.4.11 Floor Planning

The changes in the Xilinx pinout below were made to facilitate a floor planning with the most direct routing of signals. Special emphasis was give for the Xilinx to ZDOK differential signals.



5. Questions

5.1 Already Answered Questions

1. The KC705 Evaluation Board puts the TDI, TCK, and TMS of the JTAG signals through a voltage translator on sheet 14. However TDO signal is not buffered. Is this OK and desirable? No comments.
2. Do we want a USB interface to the FPGA (sheet 27)? Decide yes.
3. Regarding a connector for unused pins. The KC705 uses the Samtec ASP-134603-01 160 pin connector. Digikey lists this as not stocked. A 160 pin cable and connector might be awkward anyway. Would we be better off with multiple smaller connectors. Do you have any favorite connector to use? Decide to use a ZDOK, plus connectors for a Raspberry Pi, a Beagle Board, and possibly another small GPIO.
4. Regarding the 1 GBE connector and chip, Dan's comment was:

"I suggest we include the ethernet interface (sheet 25),
as it looks fairly simple (some R's, C's, and a connector),
and we don't have to stuff it."

This wasn't part of the original specification. The M88E1111_BAB1C000 is a 117 pin BGA. Adding and testing this complicated chip will be significant effort. Therefore, I feel we should discuss if this is a useful addition. Decide to not use this.

1. Should we use a clock input chip similar to used in the ALMA Correlator. Dan says will your circuit introduce much jitter? if not, it's fine with me. We usually just use a balun (not an active circuit) to convert 50 ohm input to 100 ohm differential and drive

the differential input of the clock driver chip. Rich's design does not use the clock chip.

2. Should we have active current measurement of the DC-DC Converters?
3. Should we have PWM System controllers for DC-DC Converters?

5.1.1 Eliminate a Power Controller

I can eliminate 1 of the 3 TI controllers if I set VCCAUX_IO = to VCCAUX
VCCAUX_IO should be connected
VCCAUX in all cases except
when needing to run at the
highest DDR3 line rates when
it should be connected to
2.0V.
And VADJ = to VCC2V5. It needs to be 2.5V to use the LVDS buffers.
Group thinks it's a good idea.

5.1.1 Replace 5V Linear with DC to DC

Looking at LMZ31710(ACTIVE) 10A SIMPLE SWITCHER® Power Module with 2.95V-17V Input in QFN package with Current Sharing . Group approves.

5.2 New Questions

5.2.1 Electronic Switch or not for the Synthesizer

We need a decision on whether to keep the electronic internal switch for the synthesizer or to route it out to a connector. Want bit to turn off synthesizer.

5.2.2 Addition of 3 db input pads?

We need a decision on whether to add 3 db pads to the input of the ADC. Dan likes the attenuators and so does Aaron.

5.2.3 Number of clocks from ADCs to FPGA

There are presently two clocks from each of the three ADC chips to the FPGA. Are there any objections to routing just two clocks from one ADC if routing becomes an issue? Ask Dave Mcmahon if need, not need all of them. They don't necessarily need to be controlled length for different ones. Want analogue inputs have same lengths . They suggest adding an extra ADC clock going directly to the fpga.

5.2.4 Number of clocks from ADCs to FPGA

We need a decision on Matt's suggestion of using a packaged 3 db attenuator from Mini-Circuits instead of using three chip resistors. The advantage of the packaged part is performance; the disadvantage is an increase in cost of about $2.00.

5.3 Comments from Schematic Reviewers

We have had various people review the schematic. Here we present their comments and actions taken.

Note the design is still in the stage where it is convenient to re-annotate. Hence reference numbers in the comments may not match those in the latest schematic.

5.3.1 Jason Ray's and Randy McCollough's Comments

Jason Ray and Randy McCollough of NRAO in Green Bank reviewed the design in 12/13. They returned a pdf of the schematic with comments attached. This pdf is posted as a file on the Casper page with the title SNAP_Schematic_JMR_RLM_JHG-1.pdf. The comments have been acted on and incorporated into the schematic.

5.3.2 Dan Werthimer Comments

matt - the main use of the board is for analog inputs with
IF from 100 to 200 MHz. we can drive the analog inputs
pretty hard, with short cables, as the second stage RF amps
will be in the same box as the kintex board. this RF board
is yet to be designed, so we can drive at whatever power levels

are needed.

do you have a suggestion for improving the input match?
(better set of resistor values? or different circuit altogether?)

rich, joe: we'd like a 1 PPS input of 50 ohms, 0 to 2.5 volts
(when terminated with 50 ohms).
it would be good if we can make it work from 2 to 3 volts Vinhigh,
and 0 to 0.5 volts Vinlow.
ADDED 1PPS WITH BUFFER TO GIVE VIH=2.0V, VIL=0.8V

i like matt's idea of skipping the clock mux and connecting the synth output
to an SMA, and connecting the ADC clock input to an SMA. people using
the internal synth can use an SMA cable to jumper. the HERA application
will not use the internal synth and will not need this jumper.
what do you think?
WE CAN DO THIS IF WE GET A CONSENSUS FROM BERKELEY. THE MECHANICAL SOLUTION WILL BE LESS RELIABLE BECAUSE OF THE MECHANICAL PARTS INVOLVED

5.3.3 Matt Dexter Comments

These are Matt's new comments dated 1/13/14:

after a super quick skim I ended up at page 28 of schematics
and have a few picky questions/comments...

So SNAP is a ZDOK host just like the RoachN or iBob - neat.
what is the "ZDOK board" which SNAP's connector is a mirror of ?
THIS IS A FLEXIBLE BOARD WE MADE FOR THE ALMA PHASING PROJECT. IT ACTS AS A CABLE TO CONNECT A ROACH II TO ANOTHER BOARD. I ADDED A NOTE TO THE SCHEMATIC

I'd find it helpful if there was a vertical line
showing the PCB edge added to the ZDOK Pin layout diagram.
(im pretty sure it's at the A1..A20 side) YOU ARE CORRECT. I ADDED A CARD EDGE LINE TO THE SCHEMATIC.

Why show F19, F20 as CLK1P/N but not show C19/C20 as
CLK0P/N ?
Just now I don't know one way or the other, but I can theorize

some existing CASPER adapter boards may supply their clock over C19/C20.
Thus it's best if C19/C20 route to clock pins on the SNAP FPGA
and calling them out as clock signals would help keep that straight.
CHANGED SIGNAL NAMES ON ZDOK TO CLK0P_C19 & CLK0N_C20.
MOVE C19 AND C20 SO GOING INTO MRCC XILINX INPUTS SO THEY CAN BE USED AS CLOCKS.

Is there some (easy) way in the schematics to show which nets
are differential pairs ?
this as part of the communication to the place and route step.
Certainly ok to id the diff. nets in a readme.txt file - but some tools have it
built in which is handy. IT TURNS OUT THE NEW ORCAD WE ARE USING HAS ADDED THE FEATURE OF TAGGING DIFFERENTIAL PAIRS. WE WILL GO AHEAD AND TAG THE PAIRS.

Matt

These are from Matt Dexter mdexter@berkeley.edu original comments
Specifications ?
ON THE WIKI
Yeah I know it's not the Berkeley way but it makes it
really hard to do a meaningful design review without them.

is there any way we can get a differently formatted version of the
block diagram ?
The tiff file is really hard to read especially when zoom in.
I ADDED A LINK TO AN EXISTING FILE WHICH HAS THE BLOCK DIAGRAM IN PDF FORMAT. THE NAME IS MISLEADING AND WE NEED TO CLEAN THAT UP AT SOME POINT. ALSO, WE HAVE NOT UPDATED THE BLOCK DIAGRAM IN A WHILE SO YOU MAY FIND A FEW DISCREPANCIES. FINALLY WE NO LONGER PLAN TO USE COAX BETWEEN THE THE SMAs AND THE BOARD. INSTEAD WE PLAN TO USE VERY SHORT JUMPERS.

I got tired of dealing with extra layer of indirection on the wiki page
so I added to the wiki directly links to the various PDFs.
NICE

The link to the KC705 datasheet was missing so I added that too.
However, that gets into the Xilinx web site but the link to the

KC 705 schematics page seems dead.
If you have a copy please enter it onto the CASPER wiki.
ENTERED Schematic on CASPER SNAP PAGE.
(the board files including Gerber files are all trivially available-
so far, it's just the schematics that aren't down loadable.)
This is referenced by upper left of page 24 of 27 of the DAB schematics
for example.

links to other datasheets were added too.

analog inputs
what is the bandwidth, not sample rate, of the analog signals to
be sampled vs 1, 2 and 4 input modes ?

what is the power level (dBm)

what is the required minimum matching performance (S11) ?
When do we get to place bets on when
Dave DeBoer and/or Aaron decide ~ 15dB S11 isn't good enough
and we'll need to add 3 or 6dB pads to the coax ends ?
WE WERE ASKED TO COPY THE BERKELY "COAX" DESIGN . AARON'S INTEREST IS 100 TO 200 MHz. THE BOARD SHOULD WORK FROM ABOUT 0 TO 500 MHz, BUT, AS YOU POINT OUT, S11 MAY BE AN ISSUE

The ordering of the schematic pages makes it a bit hard to follow.
eg page 8 shows how the 3 ADC ICs pages are called.
THE NATURAL WAY TO FOLLOW IS TO USE ORCAD AND CLICK THROUGH THE HIERARCHY, THEN IT IS EASY.

the VCM from the ADC IC's schematics are independent and will get
unique names when the netlists are generated. right ? RIGHT

I know the Xilinx part has lots of pins but why all the
independent SDATA and SCLK signals in addition to the
CSN signals ?
may be to minimize inter-ADC routing ?
THAT WAS AN OVERSIGHT ON OUR PART. WE CAN SIMPLY USE THREE INDEPENDENT CHIP SELECTS AND MAKE THE RESET COMMON.

1PPS input

do you really mean 0 to 2.5 V ?
eg 2V will not be considered a logic high ?
will it be captured via LVTTL to LVDS as on some CASPER boards
or with comparator as on Roach2 ?
or ?
where is the 1PPS logic in the schematics ?
searching for PPS, sync, pulse, sec all come up blank.

ADD 1PPS LOGIC

clocking
clock inputs ?
why have the switch on the clock ?
could have the synthesizer output to coax conn and instead use
external cable into the (external) clock input.
that way less parts in the path of the external clock.
and the SMA test connector is already in the design (TP2)
of course, maybe not interesting if primary operating mode is expected
to be external osc to on-board synthesizer.

EITHER WAY IS FINE. IT'S BERKELEY'S DECISION. AS STATED ABOVE, THE EXTERNAL PATH IS LESS RELIABLE. AS YOU STATE, THE MORE DIRECT PATH MAY BE MORE DESIRABLE IN TERMS OF PHASE NOISE ADDED TO THE CLOCK SIGNAL. THE SWITHCH ADDS VERY LITTLE NOISE.

is doubly terminated 1/2 swing at TP2 large enough ?
could add a 2 pin shunt, 0 ohm resistor or something so that
R80 is not in the path if really want full scale output.

IN THIS DESIGN, THE PURPOSE OF TP2 IS TO PROVIDE A WAY OF EVALUATING THE PHASE NOISE DURING INITIAL TESTING. WE WERE NOT PLANNING ON ROUTING THE TEST POINT OUT OF THE BOX. THIS CHANGES IF WE FOLLOW YOUR SUGGESTION AND ELIMINATE THE SWITCH. I'M NOT SURE EXACTLY WHAT YOU MEAN BY "DOUBLY TERMINATED ½ SWING". WE FOLLOWED THE RECOMMENDATIONS OF THE DATA SHEET FOR THAT OUTPUT.

SCLK, SDI, SEN = 0,1,0 : so out2, out7 and out 4 are enabled
this is OK - it matches how the outputs are used.
any reason to, for example changed SEN to 1 and make
pins 17 and/or 18 testable outputs ?

WE SHOULD BE ABLE TO TEST THE THREE USED OUTPUTS WITH A DIFFERENTIAL PROBE. POWERING ANOTHER OUTPUT WASTES A BIT OF POWER. WHAT EXACTLY DID YOU HAVE IN MIND?

why the 10 ohm outputs on the clock driver outputs ?
may be more hassle in place and route relative
to any signal integrity gain they may provide.
HITTITE SAYS THESE RESISTORS WILL IMPROVE S22. GIVEN THE PLACEMENT OF THE OUTPUT PINS WE ARE USING, I DON'T THINK THEY WILL HAVE MUCH EFFECT ON PLACE AND ROUTE. WE CAN REMOVE THEM IF THEY CAUSE HEADACHES; WE CAN ALSO REPLACE THEM WITH 0-OHM JUMPERS IF THEY SOMEHOW CAUSE A PERFORMANCE HIT

I'd place the AC coupling caps at the end of the transmission line
not the source. that way edge rates are as long as possible
and differences between the 2 caps will have less impact.
GOOD SUGGESTION!! IT LOOKS LIKE WE MAY HAVE SCLK1P AND SCLK1N SHORTED!!!

why the external 100 ohm clocks on the 100 and 156 MHz FPGA inputs ?
why not use the internal 100 ohm termination resistor ? FOLLOWING XILINX'S LEAD FROM THE EVALUATION BOARD. LESS POWER DISSIPATED IN CHIP.

Power
why only 16V cap C136 while C126 is 25V ?
I'd like to see both as 25V vs the VCC12_P they are bypassing.
REPLACE WITH 25V CAPACITORS

huh? TI ADP123AUJZ-R7 max Vin = 5.5V but it's driven by VCC12_P ???
this can't be right. GOOD CATCH. THAT SHOULD HAVE BEEN DRIVEN BY VCC5. MADE CHANGES.

the 6.3V C138 is a little tight relative to 5V it is bypassing
but it maybe fine.
I'd prefer a 10V part there.CHANGED TO 10V PART

something is wrong. The ADCs use VCC1V8_ADC but that has no
source. VCC1V8_ADC SOURCE IS ON THE ADC ANALOG REGULATORS PAGE

The LP3856 output is VCC1V8. I BELIEVE THAT WAS AN ERROR WE HAD ALREADY CAUGHT
maybe the idea was to have VCC1V8 drive the port(s)

VCC1V8_ADC at the 3 ADC hierarchical schematics blocks ???

ADC outputs Why the 3 different frame and line clocks ?
what will the FPGA do with all these ?
Are they needed because the board will support any of the analog inputs
to be the 1 and only 1 input in use ?
if so, the gateware is going to be a real mess.
this is also discussed on page 8.
THERE IS A NOTE THAT SAYS THAT WE CAN CONSIDER USING JUST ONE OR TWO CLOCKS. WE WERE JUST TRYING TO KEEP OPTIONS OPEN. YOU'VE BEEN DOWN THIS ROAD BEFORE AND WE HAVE NOT. SHOULD WE JUST GO WITH ONE CLOCK, OR PERHAPS ONE LCLK AND ONE FCLK?

5.3.4 Email thread between Matt,Rich, and Dan on ADC Pads

Hi Matt,

Yes, your mechanical arrangement for the pad sounds very fragile. Certainly pads on the board for three small resistors would be a lot more robust.

Your comment about the effectiveness of 0402 resistors versus a packaged part like the examples you showed from minicircuits makes a lot of sense. The physical size of on 0402 resistor would give about 1 nH of inductance I guess. This is significant at the operating frequencies especially relative to the 8.5-ohm resistor. Of course it's in series with a bunch of other things which aren't much better! I really
should pick the brain of some of our microwave gurus to see if they have any suggestions. I'll let you know if I turn up anything.

Thanks,
rich
On 1/22/2014 1:42 PM, Matthew R DEXTER wrote:
Hi Rich,
correct - we didn't revise the schematics so as to not (further) confuse Kelvin
and Mo @ Digicom. the schematics are the official CASPER ADC16x250-8 coax rev 2. not the PAPER ADC16 not the SERENDIP6 ADC16, not the ...
(there are lots of flavors of ADC16s out there and we've driven Digicom nuts with all these different customizations).

the 3 dB attenuators are the only difference when use
the CASPER wiki's rev 2.1 of BOM (as you've already done).

Calvin and I have been adding the 3 resistors.
I only have lousy pictures - our old camera just can't show this sort of detail clearly so won't bother to send unless you really want.

.085" hand formable coax (center conductor) ->
vertically mounted 8.5 ohm 0402 -> T point (is just above plane of PCB)
at T point is
143 ohm 0402 lies flat on PCB and solders to ground plane
perpendicular to coax cable run
and 2nd 8.5 ohm 0402 lies flat on PCB and is in line w/ coax run and
solders to the PCB pad for the balun input.
all this rework done under a stereo microscope. I have done 1 emergency resolder touch up job by naked eye but I got that to work just by dumb luck.

I suggest instead of discrete resistors the consideration of a MiniCircuits LAT-3 attenuator (http://www.minicircuits.com/pdfs/LAT-3+.pdf) or fancier
GAT-3 (http://www.minicircuits.com/pdfs/GAT-3+.pdf). Or something like that.
these sorts of things are definitely more expensive in $$ than the discrete parts but I'd hope they would work better too.

if the LAT-3/GAT-3 parts are deemed to fancy and costly then I would
add to schematics and PCB a discrete resistor solution. maybe take a few extra minutes to see if there's a higher freq version of the generic 0402 parts ?

On Wed, Jan 22, 2014 at 10:14 AM, Rich Lacasse <rlacasse@nrao.edu> wrote:
Hi Matt,

Thanks for all your words of wisdom. Sounds like you've been down in the trenches with this design for a long time!!

I've been amazed by the nice data that astronomers can pull out of apparent rubbish for many years. Differencing works wonders, so long as your "rubbish" is pretty stable.

On your schematic, I don't see the 3db pads in front of the baluns that you talk about in your email. I assume that that is a little T-pad for a 50-ohm system. Do you think we should add provisions for that in our circuitry?

I like your ideas for circuit improvement in the place and route phase. As always we'll honor the

feedback we get from Don and Aaron, but I'm copying our PC design engineer on copy to alert him to your advice.

Again, thanks for your time and advice!
rich

On 1/22/2014 11:44 AM, Matthew R DEXTER wrote:
Hi Rich,

I know Dan thinks the analog input circuitry is good enough for the intended application(s) - but I don't. I think there is way too much roll off vs frequency. I think the VSRW match is way too off. I think the baluns are too delicate (for assembly, use in lab, etc).
I would hope you and Joe would be allowed to use your skills to improve on
the circuit as used on the ADC16x250-8 coax rev 2.

For a direct answer yes the design matches.

The SNAP schematics do Not include the 3 dB pads at the balun inputs that are reworked into the circuit for PAPER's use of the ADC16x250-8 coax rev 2 boards. Adding those matching pads, as two 8.45 1% and one 143 1% 0402 resistors, was non trivial and added considerably to the schedule made testing, inspection and rework more difficult, etc.
I would like to see explicit verification direct
from both Dave DeBoer and Aaron Parsons before I'd release a board that didn't have the 3 dB pads or in some way had a convincing solution for S11 at 20 dB (or better). And reinforced by the recent PAPER discussions of strange artifacts in the PAPER data, I'd design for S11 at 20 dB out to the full operating frequency of the ADC IC and SNAP board (w/ wide bandwidth single input mode) and Not just PAPER's 100-200 MHz.

Even if the schematics aren't allowed to be improved there are things that can and I hope will be done during place and route to improve the performance.
eg optimize the stackup such as using ground planes farther away from top and bottom layers for fatter etch (less susceptible to FR4 weave grid on long X, Y etch runs, etc), maybe remove the ground from right under the baluns,
locate the clock AC coupling caps near RX rather than TX end of nets,
space parts better so as to not cause unwanted solder bridging during assembly and so on.

Matt

On Wed, Jan 22, 2014 at 4:58 AM, Rich Lacasse <rlacasse@nrao.edu> wrote:

Hi Matt,

Dan asked me to verify one more time that our ADC design uses the same input circuitry as yours that is documented at

https://casper.berkeley.edu/wiki/ADC16x250-8_coax_rev_2

I realize that there may be optimizations with respect to values of individual components yet to be made, but we want to get the topology the same.

Is what you have documented above identical to your latest design except for possible changes in resistor and capacitor values?

Thanks very much!
Rich

5.3.5 Honin's Comments (homin@asiaa.sinica.edu.tw)

We quickly read the design, mainly focus on the top level design, didn't go to the detail, it is time costly.
Just couple of concerns:

1. The hardware reliability of Raspberry Pi. It is a open source hardware, i don't know has it being tested like a commercial product, for example, thermal cycling, EMI ... ?
   GOOD POINT. THE PI IS VIEWED AS AN ACCESSORY THAT THE BOARD CAN FUNCTION WITHOUT. THEREFORE IT IS NOT AS CRITICAL FOR RELIABILITY.

2. power control for synthesizers. I guess the synthesizers will be used for calibrated only. Suggest that turn the power off remotely once it is not used. The synthesizers might generate noise more or less.
   RICH STATES" we could disable the synthesizer via the enable pin on the HMC976 regulator. It needs a voltage between 2 and 5.5 volts to enable the output, and 0 to 0.8 volts to disable the output. We should tie it to one the Xilinx banks that can do that. I will modify the schematic to reflect that after we run this by Dan and company."

3. I am confused about the 1GbE design. There is not on the schematic, but it mentioned on the design manual. There is 1GbE on the Raspberry, it might not necessary to duplicate on the SNAP board.

WE DECIDED TO NOT HAVE A SEPARATE 1GbE INTERFACE, AND THAT THE PI 1GbE WILL SUFFICE. THE 10GbE WILL BE THE MAIN COMMUNICATION ROUTE.

4. Howard Liu came up with the power budget calculation as attached. He think the Vcc 5V might not be enough once variety of Zdok board is plugged.

   GOOD CATCH AND NICE POWER MATRIX. WE DID NOT ALLOW FOR THE HIGHER LOAD ON THE 5V LINEAR REGULATOR.
   DO WE STILL WANT THE ZDOK, EVEN THOUGH IT MAY NECESSITATE ADDITIONAL COMPONENTS?
   SINCE THERE IS NOT REALLY A NEED FOR A LINEAR REGULATOR ON 5V, AND IT DISSIPATES A LOT OF POWER DUE THE VOLTAGE DROP FROM 12 VOLTS, WE PROPOSE USING A SWITCHING SUPPLY TO GO FROM 12 TO 5 VOLTS. THE TI PROGRAMMABLE SWITCHING SUPPLIES WE ARE USING DO NOT GO UP TO 5 VOLTS. DO PEOPLE AGREE TO GO TO A SWITCHING REGULATOR? 5V AT 10 AMPS SEEMS REASONABLE. ANYONE HAVE A RECOMMENDATION ON A PART NUMBER?

Item	Descriptions	VCC12_P (Source)	VCC5V0 (Linear)	VCC3V3 (SW.)	VCC3V3_SYN (Linear)	VCC3V3_DRV (Linear)	VCC2V5 (SW.)	VCC1V8 VCC1V8_ADC (Linear)	VCC1V5 (SW.)	VADJ (SW.)	VCCMGTA (SW.)	VTTMGTA (SW.)	VCCAUXMGT (SW.)	VCCAUX (SW.)	VCCAUX_ (SW.)
		12	5	3.3	3.3	3.3	2.5	1.8	1.5	3.3	1	1.2	1.8	1.8	1.8
FPGA	XC7K160T-2FFG676						0.7	0.7	0.7	0.7	1	0.6	0.02	1	0.06
ADC	HMCAD1511*3							1.185							
uC	Raspberry Pi		0.7												
CLK	LMX2581				0.178										
CLK MUX	HMC922LP4E, ignored														
CLK BUFFER	HMC987LP5E					0.234									
OSC	SiT9102AC-431N25E100						0.076								
OSC	SiT9120AI-2D3-33E156.25			0.055											
SFP CONN.	74441-0010*2			0.6											
USB to UART	CP2103-GM						0.026								
SPI FLASH	N25Q128														
SIGNAL TRANSLATOR	PCA9306DCUR*2			0.128			0.128								
LOGIC	SN74AVCH4T245DR(U14)			0.1					0.1						
LOGIC	SN74AVCH4T245DR(U16)			0.1					0.1						
LOGIC	SN74AVCH4T245DR(U20)			0.1			0.1								
LOGIC	SN74LVC1G18DBVR						0.1								
ZDOK	6367550-5-ND		2	2			2							2	
CONN.	PTC06DAAN(PI1)		0.5												
Current consumption by voltage (A)		0	3.2	3.083	0.178	0.234	3.13	1.885	0.9	0.7	1	0.6	0.02	3	
Power consumption by voltage (W)		0	16	10.1739	0.5874	0.7722	7.825	3.393	1.35	2.31	1	0.72	0.036	5.4	0.

SNAP total consumption (W)
77.5092

(The efficiency of DC-DC converters is

5.3.6 Henno Comments (Henno Kriel henno@ska.ac.za)

1) Block Diagram:
   a. ADC clock input Freq range?
   b. Why does the clock get squared? (More harmonic content generated)
   c. Add note that ADC to FPGA is via Z-DOK
2) Schematics:
   a. Sheet 9 (Oscillators) - 100MHz Osc -> Suggest 200MHz (MMCM in low or high mode), 100MHz MMCM low mode only. (Mixed Mode Clock Manager see XAPP888)
      EVALUATION BOARD ALSO USED 200MHZ. GOT 100 MHZ FROM THE ADC BLOCK DIAGRAM.
      SUGGEST CHANGING TO 200 MHZ. DOES THIS NEED TO GO TO A HIGH PRECISION INPUT OR IS HIGH RANGE OK? THE 100MHZ CURRENTLY GOES TO HIGH RANGE. RICH AGREES TO CHANGE BLOCK DIAGRAM AND WE CAN USE 200 MHZ. Done
   b. Sheet 9 - External 100R LVDS termination resistor not necessary - FPGA has internal term (better)
      XILINX STATES: “LVDS inputs are supported on an HP bank powered at Vcco=1.5V, but the swing must be below 1.7V. The internal DIFF_TERM is not supported on banks powered at 1.5V; therefore, an external 100 ohm differential termination resistor is

required." HOWEVER WE USE VCCO =1.8V FOR THE HP BANKS AND THEN THE 100 OHM TERMINATION IS NOT NEEDED.
NOTE ALSO FOR THE HR BLOCK WE MUST USE LVDS-25 AND USE VCCO =2.5V . SEE UG471. REMOVED 100 OHM RESISTORS

c. Sheet 9 - Not sure what the 156.25 ETH clock is for? See next bullet:
THE 156.25 CLOCK ALSO WAS NOT ON THE EVALUATION BOARD, BUT CAME FROM THE BLOCK DIAGRAM.
d. Sheet 12(SFPP) -> 156.25MHz 2.5V LVDS 20ppm (<0.3ps RMS jitter) Osc must be connected to MGT_REF_CLK1P/N via 100nF. AGREE DONE
e. Sheet 12 -> Move both SFP+ TX/RX to Bank 115 MGT's, then use 156.25MHz Osc as ref clk for both.I AGREE DONE
f. Sheet 12 -> MGTAVTTRCAL_115 must be connected to MGTAVTT. DONE.
g. Sheet 12 -> MGTRREF_115 must be connected to MGTAVTT via 100R 1%. DONE
h. Sheet 12 -> All unused MGTX**RX**/P/N_116..118 pins must be connected to GND. DONE.
i. Sheet 10 (FPGAJTAG)-> R154 & R155 seems unconnected.
THESE HAVE ALREADY BEEN DELETED.
j. Sheet 10 -> Add pull ups to JTAG signals connected to J3. DONE 4.7K TO VCC3V3.
k. Sheet 10 -> DXP/N not connected. No need to monitor FPGA die temp? ROUTE TO J3. EVAL BOARD HAD THEM GO TO A CONNECTOR. DONE
l. - also check floating VP/N, VREFP/N, VCCADC, GNDADC. THESE ALL WENT TO CONNECTORS TO THE EXTERNAL ADC BOARD ON THE EVALUATION BOARD.
m. Sheet 10 -> VCCBATT_0 connect to GND. DONE
n. Sheet 13 -> Serial Flash means no fall back configuration or multiple personalities? (Is that left to the Raspberry PI?) YES

5.3.7 Kim Guzzino Comments (kguzzino@hawaii.edu)

I went through the schematics and found the low 5V power that Howard and Homin mentioned.

I also agree with them that a remote control to turn off the synthesizers would be good.

RICH STATES: THIS FEATURE HAS BEEN ADDED

I did have a couple of other questions/comments.

First, when I was checking the synthesizer circuit I though the loop bandwidth was a little wide. But if it is to be for cal or selftest it is probably ok and probably ok even for operation, narrower ~150-200kHz would bring midrange phase noise down a little.

RICH STATES: USING THE T.I. PROVIDED TOOLS, PARAMETERS WERE VARIED IN AN ATTEMPT TO MINIMIZE THE RMS JITTER OF THE OUTPUT FREQUENCY AT 250 MHZ (526 FS) AND 750 MHZ (361 FS) . THESE MET THE OVERALL DESIGN REQUIREMENTS

Second, is on the 3.3V regulation at the top of the PWM controllers. There are a lot of parts put on to be able to use the internal (UCB9248) 3.3 regulator. It (3 of them) doesn't need to supply very much current and a single regulator or 3 very small linears could do the job with only a few parts. The ferrites and 5.1V zener could go away along with some caps.

THIS COPIES THE XILINX EVALUATION BOARD. NOT SURE OF THE EFFECT ON THE POWER CONTROLLER IF SHARING V3.3 IN A CONFIGURATION NOT MENTIONED BY TI.

I notices there is a PI filter (CLC) on the output of this 3.3 and the before filter(VCC3V3) and the after filter (VCC3V3A) drive the part at a couple of different places. I couldn't see where it would make a difference either way.(filtered/unfiltered)

JOE'S ANSWER:

http://www.ti.com/lit/pdf/sluu490 The UCD92xx Design Guide states:

The V33A pin requires very good decoupling. If desired, this pin can be

separated from the V33D and V33IO pins with a ferrite bead; in most cases, this bead is not necessary.

As a justification for the additional filter.

DAN ADDED:

i'm not sure where the 3.3 Vregs are used that kim is discussing.
as you know, we need a lot of isolation between the Vdd pins on the different ADC's to keep the cross talk down.
(eg: if it's a single regulator that supplies all the ADC"s, then they Vdd's need to be well isolated

from each other with LC filters on each Vddanalog (using beads (high freq L's)).

and we need a separate low noise regulator on the hittite clock distribution chip.
RICH ADDED: THIS IS INCLUDED AND IS IDENTICAL TO THE BERKELEY DESIGN

do we also need a low noise regulator for the synth?

RICH ADDED: WE COPIED THE BERKELEY DESIGN FOR REGULATORS FOR THE ADCS AND CLOCK DRIVER. FOR THE SYNTHESIZER, WHICH IS NOT IN THE BERKELEY DESIGN, WE ADDED A SECOND HM976 LOW-PHASE-NOISE-OPTIMIZED REGULATOR FOR THE SYNTHESIZER.

That's it. I didn't check every pin but overall it seems solid to me.

Programming should be interesting with the Rasberry, FPGA, PWM controller, ADC configuration and synthesizer setup. Looks like a good board to play with though.

Regards,

Kim

5.3.8 Alan Langman's Comments alan.langman@gmail.com

Alan: I took a quick look at some of the SNAP info.
Some questions
Sent at 12:50 PM on Thursday
Alan: 1) Do you only support configuration via the SPI? No remote upgrade?
2) I see someone mentioned ethernet, was it added to the later versions. And will it support updating the configuration memory.
3) If you reverse the connectors on a beagle bone you can plug into a board (so much better than RP)
Sent at 12:53 PM on Thursday
Alan: 4) All the clocks and ADCs are controlled via the FPGA. Are there any issues with the FPGA booting prior to ADC clock presenting at the FPGA? We had some issues with the Spartan 6 and locking to the ADC clock. So I thought I would ask.
Sent at 12:55 PM on Thursday
Alan: 5) Is there power supply monitoring on the board? through the fancy digital controllers?
6) Can one recycle power remote if things lock up?
7) I know the ZDOCK is placed for supporting legacy devices. And FMC + 4 signals and you can have an adapter card for ZDOCK. Then you can test out FMC and ZDOCK devices?

Alan Langman
(m) +27 (0)83 7767302

JOE'S REPLY:
Alan thanks for the comments and thanks Dan for the reply.

I will be updating the schematics before next Tuesday's teleconference. Also I'll post a complete BOM.

I have added a porting of the synthesizer clock directly to the Xilinx as discussed. There is also a dedicated 200MHz oscillator to the Xilinx.

As for monitoring the voltages, there is a PMBUS that goes to the TI Power Supply controllers. The normal interface is with a PC via a dedicated connector.
However the PMBUS also goes to pins on the Xilinx, so theoretically it can be controlled and monitored via the Xilinx.

I also replaced the 5V 2A supply with a 5V 10A supply. There is a power good line from this regulator that I have going to the Xilinx.

Joe

On 2/7/2014 2:30 PM, Alan Langman wrote:
Hi Dan et al,

W.r.t the Beagle board comment. Currently the beagle board is a "Motherboard" with female IDC headers on the top component side. If one replaces with male IDC on the bottom, then one can plug into sockets on the motherboard. Cheap SOM.

I never got to try out the FMC to ZDOCK adaptor; so its an untested idea.

SNAP looks like an awesome board!

Best regards,

Alan

On Thu, Feb 6, 2014 at 11:11 PM, Dan Werthimer <danw@ssl.berkeley.edu> wrote:

hi alan,

thanks for looking over the snap board !

i'm forwarding your questions and suggestions
(appended below) to board designers joe and rich at nrao.

some preliminary answers
(hopefully joe and rich will add, and correct me if i'm wrong).

a) i think the latest schematics are on the wiki, but not sure.

b) there a pair of 10Gbit ethernet SFP+ ports on the board,
and 1Gbit ethernet if you use the optional raspberry pi or beaglebone board.
any of these ports will allow remote configuration of the flash and fpga.

c) not sure what you meant in your "3)" about reversing connections
on beagle bone. is that so that boards can stack???

d) i think we should, if we don't already, bring one of the clocks
from the clock distribution chip, directly to the fpga.
the standard way we use this thing (as you know), is
to bring up the adc's, so that we have a good stable clock
to the fpga, and then program the fpga.
i think that remains the plan - joe and rich can comment.
i think there's also an xtal clock directly feeding the fpga ???

e) i don't think we are monitoring supply currents or voltages.
do you think we should do this??

f) yes, we can cycle power to boot to golden copy in flash.

g) we prefer zdoc over fmc, because there are a lot of
inexpensive adc cards available, and we have the interface

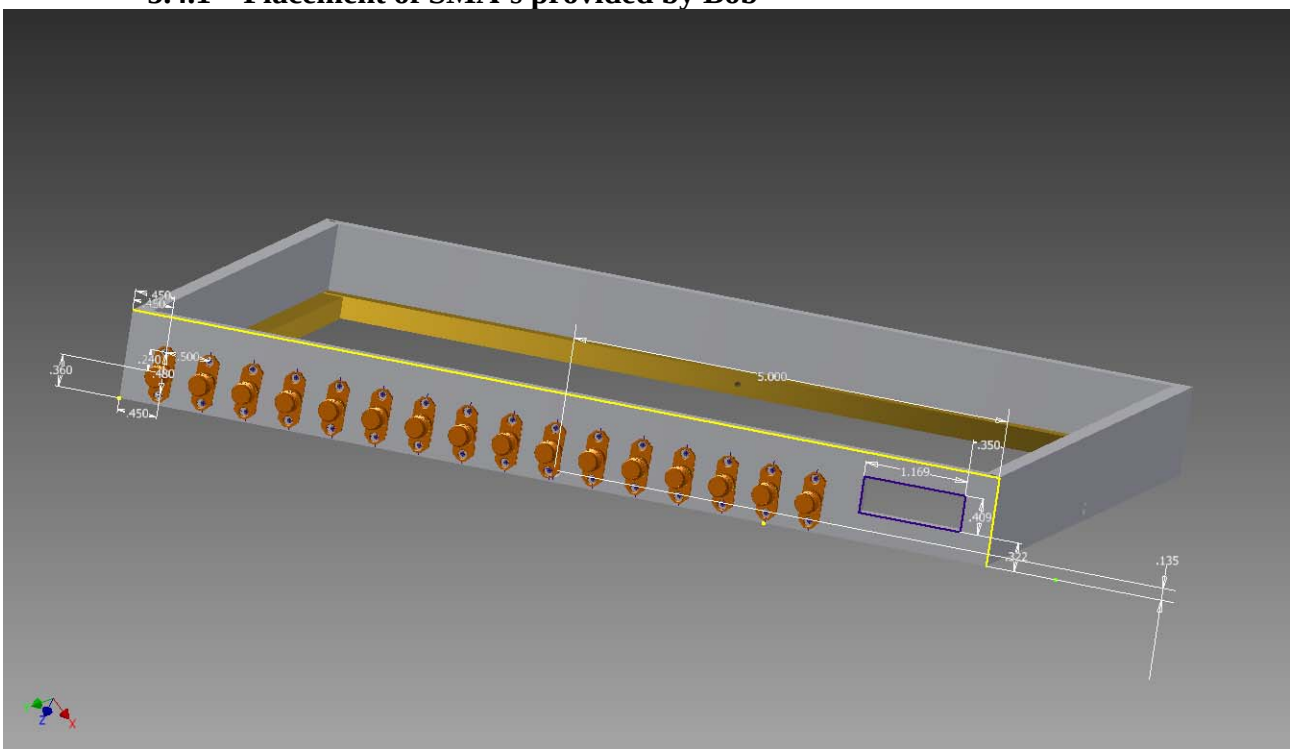
code developed for these adc's. if we were starting over,
we'd use fmc.

have you tried using casper adc's and zdoc to fmc adapter?
is signal integrity OK with the adapter?
is the adapter available and open source?

5.4 Comments from Review prior to Board Testing

This is the review prior to Jack testing the board.

5.4.1 Placement of SMA's provided by Bob



5.4.2 USB Placement

1) Action item for joe, rich, bob,
move both usb connectors, to either center or rear edge.
consider changing the non digilent usb connector to a dual row header,
that can be used with standard internal PC usb cable. egarding placement of USB connectors:

if you have room near the rear edge of the PCB,
my preference would be to mount the USB connectors
close to rear edge, but not right up against it,
leaving a bit of room for USB cables to squeeze into

Bob Responded: I propose we change (U4) the USB mini Type B from the present right angle part to a vertical through hole part with a metal shroud and board lock tabs instead of a header. If we put a USB header on the PCB it will require another connector level to transition just to mate with a USB cable. Using the USB mini type B vertical connector on the board will allow a USB cable connection directly to the PCB. If anyone wants to transition to the panel, they could still use a USB-USB extension cable and probably even adapt directly to a different USB connector type at the panel end of the cable if they want. Otherwise, perhaps having both a footprint pattern on the PCB for a header and vertical connector in parallel would cover all options.

the connectors if people take the cover off the box.

There was concern about the height of a vertical USB plus cable. eg:

1)
for people don't use the enclosure,
that put a lot of snap boards into a card cage,
then it would be useful if they can connect USB cables
from the back of the card cage.
the USB connectors won't be right up against the PCB edge,
but with some fiddling, they'll be able to get their connectors
on and off.

2)
for people that use the enclosure, it would be useful if
they can connect USB cables when they remove the cover.
if right angle USB cables are required, that's OK.

Solution: We put a vertical USB connector J10 in parallel with the horizontal USB J4. That way the most convenient can be used.

5.4.3 Sequencing Power Supplies

Action Item for Joe and Rich.
what are the power supply sequencing requirements?
can this sequencing be implemented with the two power controllers
that don't talk to each other?
(do we need to change anything?)
Jacks response:

I was looking at the power controller data sheet just after our telecon -- http://www.ti.com/lit/ds/symlink/ucd9248.pdf -- it seems
that sequencing between chips is possible in 3 ways (see page 26 "sequencing").

1) Programming power-on delays 0-3276 ms delays available (see TON_DELAY -- http://www.ti.com/lit/ug/sluu337/sluu337.pdf)

2) Chaining PWRGOOD to PMBUS_CTRL to have a master/slave relationship between controllers

3) Using GPIO_SYNC_CONFIG commands to set start/shutdown dependencies
based on internal rail power states and external gpio stimulii.

I would have thought just having delays configured would be fine, and
doesn't require any hardware changes. (Though the third option would
be nice)
Dave added:
Thanks for researching this so quickly. Using pre-defined delays can be problematic because it won't prevent voltages from turning on if one of the predecessor voltages fails to turn one. Ideally, you want voltage B to turn on after ***and only if*** voltage A turns on. Using pre-defined delays, the chip can command/request voltage B to turn some time after it commands/requests voltage A to turn on, but there is no feedback loop to prevent turning on voltage B if voltage A fails to turn on for some reason.

After thinking about this some more, I realized that it would be very nice to be able to talk to the PMBUS from the RasPi. This way users could query the state of the power supplies remotely (even if the voltage regulators fail). Basically it would be very nice if the RasPi could be used to do (almost?) everything that could be done from a desktop computer with various programming cables/gizmos. Maybe this is already planned? It's not a huge deal for HERA because I don't think HERA will deploy SNAP boards with RasPi boards installed (right?), but for single board systems it would greatly simplify the interfacing. Maybe some of the J8 pins could be used for this purpose?
Jack answered:
Agreed, although we get that level of control on rails that are on the same chip for free -- but we could investigate wiring up the SEQ-N sequencing io's (?)

Re. RasPi control: the data sheet also says the power controller can be programmed by JTAG -- might it be simplest just to add them to the chain, or do you think dedicated pins would be preferable (the RPi has some I2C pins which would do PMBus nicely)?
Jack responded: IMHO, it would be great if every JTAG-capable device were on one long JTAG chain (with 0-ohm resistors in various places to make it easy to bypass parts). This would enable some boundary scan testing via JTAG as part of the manufacturing/testing/debugging process. I know Digicom does this for (some/parts of?) the ROACH2 boards.

That said, talking to the PMBUS via I2C is much easier than via JTAG so I guess my answer is "both"! FWIW. the PMBUS of the UCD9248 seems to be supported by Linux (at least generally, I don't know whether that would work on RasPi).

It was determined that having SEQ 1 and SEQ 2 of the powers supply controller chips wire ored will facilitate the desired sequencing. This is how it was on the Kintex Evaluation Board.

5.4.4 SFP+ Capacitors

3) Action Item joe, rich
do we need coupling caps on SFP+ serdes lines?
Joe's Comment: Looked on the Kintex evaluation board. There are no serial capacitors for the SFP_RX and SFP_TX lines.

5.4.5 Raspberry Pi Programming and Interconnect

Action Item for Jack
how can we program FPGA from raspberry pi?
Jack suggests using PI GPIO pins for connecting to the PMBUS and also JTAGing the FPGA. This might involve level shifting. Currently the JTAG is from Bank 0. Bank 0 currently has a VCCO of 2.5 Volts. Jack will look into possibly making this 3.3V.

Jack Reported:
The I2C --> power controller interface seems to be working, so I suggest the following changes to the pinout on the Raspberry Pi 26-pin header?

Pin:
3. PMBUS_DATA
5. PMBUS_CLK
11. PMBUS_CTRL
12. PMBUS_ALERT

Joe: I moved the signals as above. These are 3.3V signals from the Pwr controller and 3.3V in the PI. I moved the level shifters to 1.8V for the FPGA to the FPGAADCS block.

13. JTAG_TMS
15. JTAG_TDI
16. JTAG_TDO
18. JTAG_TCLK

Joe: I moved the signals as above. Again these are all 3.3V signals.

It would be nice to have FPGA_DONE and FPGA_PROG_B also available (pins 22 and 26 would seem like a good choice), though these signals
are from bank 0 at 2V5,
(though FPGA_DONE would probably work fine as an RPi input, and FPGA_PROG_B is already pulled up, and only needs to be able to be pulled to ground from software to reset the chip) - if it's quick and easy to properly convert these to/from RPi voltages then please do, but it should work even without (I'll just have to make a mental note not to drive the FPGA_PROG_B pin high...)

Joe: I found extra level shifters to use for DONE and PROG_B PROG_B on the external header is now pulled up to 3.3V.

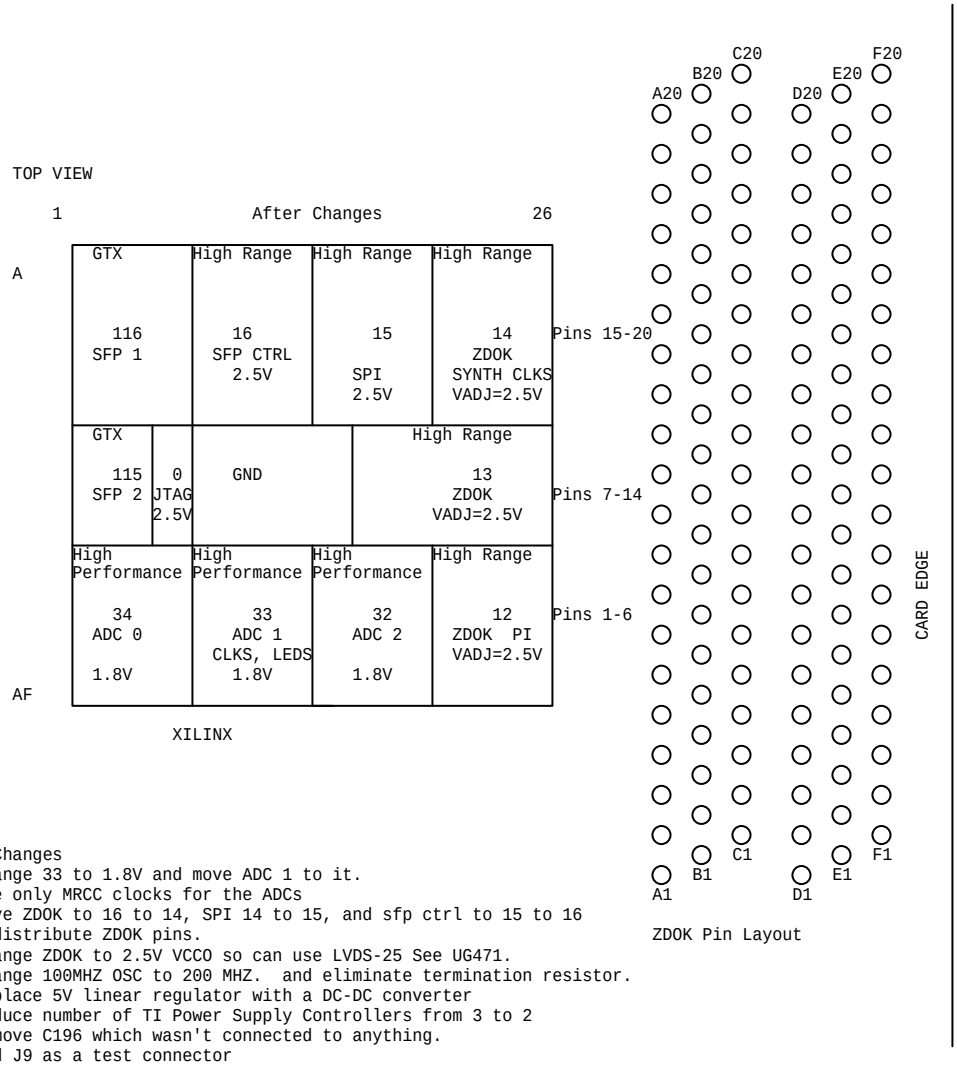
Given that the JTAG interface seems to happily program the FPGA in ~20s, I was not going to push for wiring the Raspberry Pi SPI bus to the the FPGA (or the Prom directly) as some of these banks are 2.5V

(Is there a good reason that the configuration banks and prom can't all operate at 3V3?)

Joe: Not that I know of. I just copied what was on the evaluation board.

One thing I did notice -- on the SNAP board the PROM SPI connections are all to bank 15, whilst in the KC705 they are to the bank 14, matching the specs in the config guide -- http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf
-- I could well be missing something, but is this correct?

Joe: Move back to Bank 14 with pinout as on Kintex Board.



Changes
Change 33 to 1.8V and move ADC 1 to it.
Use only MRCC clocks for the ADCs
Move ZDOK to 16 to 14, SPI 14 to 15, and sfp ctrl to 15 to 16
Redistribute ZDOK pins.
Change ZDOK to 2.5V VCCO so can use LVDS-25 See UG471.
Change 100MHZ OSC to 200 MHZ. and eliminate termination resistor.
Replace 5V linear regulator with a DC-DC converter
Reduce number of TI Power Supply Controllers from 3 to 2
Remove C196 which wasn't connected to anything.
Add J9 as a test connector
Go to a single dual SFP+ Cage instead of two single cages.
Add a vertical USP J10 in parallel with horizontal USB J4
Change U43 from a 128 MByte to a 256 MByte Flash Memory.

Add PU or PD to PD on the ADCs.

Cheers,
Jack

5.4.6 Daves Comments

I've been looking more at the ADC and ZDOK parts of the schematic. Here are a few more musings and questions on these areas:

5.4.7 ADC Power Down Pullups or Pulldowns

The PD (PowerDown) pin on the ADC chips is connected directly to the FPGA. This line should probably be pulled high or low depending on whether we want the ADC chips to be powered down when the FPGA pins are in the high impedance state (e.g. when the FPGA is reprogrammed). I'm thinking that if we want to initialize the ADCs and then reprogram the FGPA (like the current ADC16 works), then we will want the ADC pins to remain powered on if/when the FPGA is reprogrammed so the ADCs will stay running. Maybe have pads for both a pull-down and a pull-up, but only populate one so as to allow us to change our minds later without requiring much rework?

Joe: Does this also apply to the RESETN pin. The data sheet states:

Start up Initialization

As part of the HMCAD1511 power-on sequence both a reset and a power down cycle have to be applied to ensure correct start-up initialization. Make sure that the supply voltages are properly settled before the start up initialization
is being performed. Reset can be done in one of two ways:

1. By applying a low-going pulse (minimum 20 ns) on the RESETN pin (asynchronous).
2. By using the serial interface to set the 'rst' bit high. Internal registers are reset to default values when
this bit is set. The 'rst' bit is self-reset to zero. When using this method, do not apply any low-going pulse on the RESETN pin.

Power down cycling can be done in one of two ways:

1. By applying a high-going pulse (minimum 20 ns) on the PD pin (asynchronous).
2. By cycling the 'pd' bit in register 0Fhex to high (reg value '0200' hex) and then low (reg value '0000' hex).

Rich comments This will default the ADC to ON, which is what Dave wants when the Xilinx goes to high impedance so it does not forget its calibration. We should add a pull-up and pull down(DNP) on the PD pin. This will default the ADC to ON, which is what Dave wants when the Xilinx goes to high impedance so it does not forget its calibration. Add a pull-up only on the reset pin. We can use a value of 5K for all since these are CMOS-like inputs with +/- 10 ua input current spec. Done.

5.4.8 Dave On ADC Programming Pin Banks

It's not necessary to have the ADC programming pins (e.g. CSN, SCLK, etc.) in the same FPGA bank as the ADC serial outputs. It might even be beneficial to have these pins from all chips in the same bank since probably they will all be controlled via the same logic, but this is low bandwidth stuff so not a big deal either way.

Joe's comment: I agree this is not a big deal and vote to leave it the way it is. Rich also agrees.

5.4.9 Dave on ADC Output Pin Placement

The two serial lanes from a single ADC channel (e.g. diff pair ADC0_OUT{0,1} and diff pair ADC0_OUT{2,3}) will most likely get muxed together (after deserialization) to form a single parallel data stream, so it would be nice to verify that the current pinout places each pair of differential pairs in nearby IOSERDES sites. It looks like this might already be done, but I can't tell for sure from the pin names alone. For example, ADC2_OUT{12,13} on pins AC14/AD14

seem kind of far from ADC2_OUT{14,15} on pins Y15/Y16, but it might really be fine on the chip itself even though the pin pairs sound farther apart than others. Probably not the end of the world if we end up with some oddballs, but it can ease timing to put these close together to begin with.

Rich's comment: The way I read Dave's comment he wants to mux together bits 0 and 1, bits 2 and 3, etc. Going to nearby pins apparently helps with this and we should try to honor his request, consistent with keeping the layout sane (i.e., avoid criss-crossing paths and vias just to meet this requirement, but try to meet it, if it's not a big deal. We also ought to take into account where Bob is in the layout process. If this causes him a lot of work, then it's not worth doing either.

Joe's comment: I have rearranged the ADC OUT pins to keep pairs of pairs close together. However one consequence is that the 3 banks have the pins placed differently. Is this confusion worth the benefit?

5.4.10 Dave on ZDOK Bank Placement

3) Does the mapping from ZDOK pins to FPGA pins follow the same bank grouping as on ROACH1 and/or ROACH2? I'm not sure the ZDOK bank grouping is even consistent between ZDOK0 and ZDOK1 on ROACH1 and/or ROACH2. By "bank grouping" I mean that certain groups of ZDOK pins on ROACH2 go to certain FPGA banks. Does each such "bank group" (as defined by the ROACH2 schematic for lack of a formal CASPER standard ZDOK pinout) still go to a common bank on the SNAP board's FPGA?

4) Comment by Joe. No effort was made to use the same Bank groupings. Why is this important? Since they are different size Xilinx and different families (Kintex 7 vs Virtex 6) why is this relevant?

5.4.11 Raspberry PI to Xilinx Voltage Levels

5) There are numerous signal connected directly from the Raspberry Pi connector to the Xilinx pins. However the Xilinx is using a VCCO of 2.5 Volts and the Raspberry Pi uses 3.3 Volt levels. The Kintex Data sheet says the Absolute Maximum Vin is VCCO + 0.55 V. In this case it would be 2.5 + .55 = 3.05 Volts, which would be exceeded by the 3.3V from the PI. I propose that we configure bank 15 with a VCCO of 3.3V, then connect the PI signals to that. Bank 15 is conveniently available since we moved the SPI to bank 14. This has been done.

5.4.12 ZDOK Clock Pins

Some of the "data" pin pairs on the ROACH2 ZDOK connector go to "clock capable" pin pairs on the ROACH2 FPGA. Do these same ZDOK "data" pin pairs go to "clock capable" pin pairs on the SNAP FPGA? Some ZDOK cards use more clocks than just the two ZDOK "clock" pin pairs, so some of the "data" pin pairs that go to FPGA "clock capable" pin pairs end up being repurposed into de facto ZDOK "clock" pin pairs. It would be nice to match this as much as possible. I think the ADC16 pages on the wiki have a nice spreadsheet detailing this. Since this came about as an afterthought, the "de facto clock" pin pairs on ROACH2 unfortunately differ between ZDOK0 and ZDOK1, but maybe the SNAP FPGA has enough clock capable

pins to support a superset of the two. **oe responds: Looking at the ADC16 spreadsheet I see the following clock capable data pins:**

6) **Blue SRCC: F7F8,D3D4,D15D16,D17D18,D19D20,C1C2,C7C8,A19A20**
7) **Green MRCC: F9F10,F15F16,C1C2(both),C3C4,C9C10,C11C12,A1A2,A15A16**
8) **Red ZDOC MRCC dedicated Clock Pins F19F20,C19C20**

Thus we need 10 MRCC pairs and 7 SRCC.
Each bank has 2 MRCC and 2 SRCC pairs. Thus we would need 5 banks of MRCC and 4 Banks of SRCC.

To get this many clock inputs it would be necessary to gather the spare inputs from all the banks of the Xilinx. Does it matter that it is an assortment of VCCOs and and High Range and High Performance banks?

Using MRCC would be better than SRCC. Are there any objections to moving the moving the ADC FCLKs and LCLKS to SRCCs? It seems each ADC is processed in its own bank, so it shouldn't make a difference.

Dave MacMahon replied: Wow, this might be a case of "be careful what you ask for"!

I think it's probably best to keep the ZDOK pins all in the same 3 banks as they already are, but within those banks map as many Kintex7 clock capable pins as possible to ZDOK pins that map to clock capable pins on the ROACH2. Could some of the signals going to clock capable pins in the ZDOK banks (e,g, SCLK3, SPICLK, IICSCL, GPIO18, GCLK) be moved to clock capable pins in other banks? It seems like most of these signals don't even need to be on clock capable pins.

I think that would get us 6 SRCC pairs and 4 MRCC pairs (not counting the two MRCC pairs already used for dedicated ZDOK clocks on ZDOK F19/20 and C19/20, which covers more than half the cases. Maybe try to get the ADC16 LCLK ZDOK pairs to clock capable pins and then arbitrarily choose from the the remaining ZDOK-pairs-to-ROACH2-clock-capable-pairs to make up the 10 pairs? It looks like C1/C2 would be great to map to clock capable pins because that ZDOK pair happens to map to clock capable pins on both ZDOKs on ROACH2, but that pair is probably already covered in the ADC16 LCLK list.

FWIW, the ADC16 yellow block does not use the FCLKs at all.

9) Blue SRCC: F7F8,**D3D4**,D15D16,**D17D18**,**D19D20**,C1C2,**C7C8**,A19A20
10) Green MRCC: F9F10,F15F16,**C1C2(both)**,**C3C4**,**C9C10**,C11C12,**A1A2**,A15A16
11) Red ZDOC MRCC dedicated Clock Pins **F19F20,C19C20**

I have rearranged the clock lines so that now all the signals in bold above go to clock Xilinx clock lines in the 3 ZDOK banks. They all match the MRCC/SRCC status, except I had to put A1A2 as an SRCC. I'm not sure of the definition of the ADC 16 LCLK ZDOK pairs. Are they F19F20 and C19C20? Is this arrangement OK? Dave replies it is ok, so this is done.

5.4.13 Kintex Decoupling Capacitors

6) I noticed the following note in the 7 series packaging user guide: "Note: Pin compatible packages can have substantially different decoupling capacitor recommendations." Do the three SNAP-footprint-compatible Kintex 7 devices have different decoupling recommendations? If so, does the schematic specify decoupling caps for the most demanding device (presumably some could be specified as "do not populate" for the less capable FPGAs, if desired)?
Joe: The three Xilinx part numbers usable are:

XC7K160T-2FFG676C ($396) (1.4MB RAM)

XC7K325T-2FFG676C ($1359) (2MB RAM)

XC7K410T-2FFG676C ($2177) (3.5MB RAM)

According to Xilinx publication UG483:

ug483_7Series_PCB-3.pdf - Adobe Acrobat Pro

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table 2-2

XILINX. PCB Decoupling Capacitors

Table 2-2 lists the PCB decoupling capacitor guidelines per V_{CC} supply rail for Kintex-7 devices.

Table 2-2: **Required PCB Capacitor Quantities per Device: Kintex-7 Devices(1)(2)**

Package	Device	V_{CCINT}			V_{CCBRAM}				V_{CCAUX}		V_{CCAUX_IO} per Group(3)			V_{CCO} Bank 0	V_{CCO} all other Banks (per Bank)
		680 µF	330 µF	4.7 µF	660 µF	330 µF	100 µF	4.7 µF	47 µF	4.7 µF	100 µF	47 µF	4.7 µF	47 µF	100 µF
FBG484	XC7K70T	0	1	0	0	0	1	2	2	3	N/A	N/A	N/A	1	1
FBG484	XC7K160T	0	2	0	0	0	1	3	2	3	N/A	N/A	N/A	1	1
FBG676	XC7K70T	0	1	0	0	0	1	2	2	3	0	0	0	1	1
FBG676	XC7K160T	0	2	0	0	0	1	3	3	4	0	0	0	1	1
FBG676	XC7K325T	0	3	5	0	0	2	5	3	4	0	0	0	1	1
FBG676	XC7K410T	0	5	10	0	1	0	9	3	4	0	0	0	1	1

Added DNP capacitors per the above table to allow for the 3 Xilinx sizes.

5.4.14 Using a larger Personality Flash Memorhy

Jack comments:
I've just started looking at the 7-series configuration guide (which is a real page-turner, by the way) and one thing I've noticed is that the current 128Mb prom is only large enough for two firmware images if the chip used is the XC7K160T (as planned). The larger pin-compatible 325T and 410T chips would need 256Mb for two images (though they could fit one image in the 128Mb).
If we'd like to keep the other chips open as an option, can the memory size be increased to 256Mb? Otherwise it becomes harder (impossible(?)) to load new firmware on the board remotely without the raspberry pi. Micron have a 256 meg version of the currently selected part, though there doesn't seem to be one in the same package.
Joe's Response:
The original part was 557-1562-ND a N25Q128A3ESER0E in a 8-SOIC for $2.53 Digikey sells 557-1565-ND a N25Q256A13EF84E for $3.96. This is not offered in a 8-SOIC, so a design change would be required. It was decided to go ahead with using the bigger RAM, so it will be implemented. This is the same pinout, but a different package, so a different footprint is required, but no schematic changes. Done.

5.4.15 Xilinx Heat Sink Selection

Vaughan Moss comments If I recall, Henno mentioned a few months back that the kintex-7 still got pretty hot on the demo board he was using with the provided fansink.
We have a passive cooling method for the D-Engine which uses the kintex-7 - effectively the kintex-7 is being clam-shelled between to large blocks of aluminium.
We estimated the power dissipation to be around 15W from the kintex-7 in our use.

From your information both FPGA's are the FFG676 package which has a size of 27x27x2.1mm. Radian seem to be the only guys making heatsinks/fansinks specifically for Xilinx FPGA's that I could find.

This is from Xilinx, yours are highlighted in red.

5.4.16 Pin B25 PUDC Pullup and Pulldown needed

It was noted Pin B25 (IO_L3P_T0_DQS_PUDC_B_14) needs to have a pullup or pulldown on initialization. This determines if pins are pulled up or down during power up. Leaving it floating could cause oscillation. The Kintex Eval board had a pulldown, and one was recommended so this will be implemented. When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin. When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin. The state of this pin effects the state of the I/O from power-on until configuration completes. Therefore, the I/Os will be 3-stated after power-on when PUDC is High. Installed Pulldown and DNP pullup.

This Pin had CLK_SEL_B. I noticed from the comment that this needed > 3 Volts, and it was coming from bank 14 with a 2.5 V VCCO. Moved CLK_SEL_B and CLK_SEL_A to bank 15 which has a VCCO of 3.3V.

			Kintex-7 FPGAs Optimized for Best Price-Performance (1.0V, 0.9V)						
	Part Number		XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T
	EasyPath™ Cost Reduction Solutions[1]		—	—	XCE7K325T	XCE7K355T	XCE7K410T	XCE7K420T	XCE7K480T
Logic Resources	Slices		10,250	25,350	50,950	55,650	63,550	65,150	74,650
	Logic Cells		65,600	162,240	326,080	356,160	406,720	416,960	477,760
	CLB Flip-Flops		82,000	202,800	407,600	445,200	508,400	521,200	597,200
Memory Resources	Maximum Distributed RAM (Kb)		838	2,188	4,000	5,088	5,663	5,938	6,788
	Block RAM/FIFO w/ ECC (36 Kb each)		135	325	445	715	795	835	955
	Total Block RAM (Kb)		4,860	11,700	16,020	25,740	28,620	30,060	34,380
Clock Resources	CMTs (1 MMCM + 1 PLL)		6	8	10	6	10	8	8
I/O Resources	Maximum Single-Ended I/O		300	400	500	300	500	400	400
	Maximum Differential I/O Pairs		144	192	240	144	240	192	192
Integrated IP Resources	DSP48 Slices		240	600	840	1,440	1,540	1,680	1,920
	PCIe® Gen2[2]		1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC		1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks		1	1	1	1	1	1	1
	GTX Transceivers (12.5 Gb/s Max Rate)		8	8	16	24	16	32	32
Speed Grades	Commercial		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended		-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Package[4]	Dimensions (mm)	**Available User I/O**: 3.3V HR I/O, 1.8V HP I/Os (GTX)						
	FBG484	23 x 23	185, 100 (4)	185, 100 (4)					
Footprint Compatible	FBG676	27 x 27	200, 100 (8)	250, 150 (8)	250, 150 (8)		250, 150 (8)		
	FFG676	27 x 27		250, 150 (8)	250, 150 (8)		250, 150 (8)		
Footprint Compatible	FBG900	31 x 31			350, 150 (16)		350, 150 (16)		
	FFG900	31 x 31			350, 150 (16)		350, 150 (16)		
	FFG901	31 x 31				300, 0 (24)		380, 0 (28)	380, 0 (28)
	FFG1156	35 x 35						400, 0 (32)	400, 0 (32)

XMP085 (v3.6.2)

FBG: 1.0mm Lidless flip-chip; **FFG**: 1.0mm Flip-chip fine-pitch

Notes: 1. EasyPath™ solutions provide a fast and conversion-free path for cost reduction.
2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.

These are the suggested heatsink/fansinks from Radian(also highlighted in red):

Thermal Resistance C/W

Column headings are ……part number …… ….Hmm 200lfm 400 600

				HS2100DBP1705K22	round pin	12.7	28x28	7.2	4.9	4.1
				INL27001-6/1.7Y+T725	plate fin	6.3	31x36	4.6	3.5	3.0
				INL27001-10/1.7Y+T725	plate fin	9.5	31x36	3.8	2.7	2.2
				INL27001-13/1.7Y+T725	plate fin	12.7	31x36	3.1	2.2	1.8
FF668				INM27001-27.2W/2.2BU+T710	elliptical pin	27.2	32x32	2.5	1.7	1.4
FF676				INM27001-32.2W/2.2BU+T710	elliptical pin	32.2	32x32	2.2	1.6	1.3
FF672				INM27002-11.2P/2.2BU+T710	round pin	11.2	32x32	4.6	3.1	2.6
FF(G)665	2.1	27	Passive	INM27002-14.2P/2.2BU+T710	round pin	14.2	32x32	3.6	2.4	2.0
FF(G)676				INM27002-19.2P/2.2BU+T710	round pin	19.2	32x32	2.7	1.9	1.6
				INM27002-24.2P/2.2BU+T710	round pin	24.2	32x32	2.3	1.6	1.3
				INC27001-7/1.5O+Li98	plate fin	7.1	32x32	9.2	5.8	4.6
			Active	(12V) FI27+Y+T725	round pin	16.0	31x36		2.1	
				(5V) FJ27+Y+T725	round pin	16.0	31x36		2.1	

The big determining factors would be your xilinx-7 power consumption, ambient temperature in the enclosure and how much of the heated air you are pushing/pulling away from the FPGA. I increased the fan 'size' to increase the thermal conductivity between the FPGA junction and the case because the ambient in the ROACH 2 chassis is quite high thanks to the LED board effectively blocking any direct flow of air across the FPGA from the chassis fans.

Joe Comments: The Kintex Evaluation Board uses Radian INC3001-7_1.5BU_LI98 with a 12VDC fan. The heat sink selection also would depend on which Xilinx chip we used, with the larger chips capable of dissipating more power. We could select the worst case heat sink. If we are using a fan based heat sink, we need to incorporate an appropriate 12VDC receptacle for the fan. While the actual heat sink can be selected later, the fan receptacle needs to be part of the design. Looking at the evaluation board they use the receptacle J61 part number 22_11_2032. Implemented the Fan Plug with PWM. Plan on using the FI27+Y+T725 12V Fan based Radian Heatsink. This does not have a Tach. The larger heatsink for the larger Xilinx on the evaluation board had a tach.

5.5 10 GbE Interface design

5.6 Block Diagram

5.7 Data Acquisition Board schematic

5.8 Power requirements

5.8.1 ADC Linear Power Requirements

After a great deal of discussion, +12VDC was selected to be the input voltage level for the ADC. It high enough to keep currents reasonable and low enough to avoid safety issues and to keep wasted power in the module to a reasonable level.

As a starting point for DC power supplies for the ADCs, the approaches taken in three other designs were reviewed. These include the Berkeley ADC16x250 "rev 2" ADC, the Kintex evaluation board ( ), and the Hittite ADC evaluation board (EKIT01-HMCAD1511).

The Berkeley rev2 ADC board has the following approach. The ZDOK connector brings in 4 voltages, 5-volts (VCC5), 3.3-volts(+3.3V), 2.5-volts (VCC2_5) and 1.8-volts (1.8VD)). The "digital" supply voltages of the ADC chip, DVDD and OVDD come directly from the ZDOK 1.8VD. These are decoupled with 10 nf caps at each pin and a 1 uF cap placed a little further away. The "analog" supply voltage for the ADC is derived from the ZDOK 2.5 volts using an LP3856 regulator. It is heavily filtered (inductive and capacitive)at the input to the LP3856 regulator and at each ADC. Some of the logic uses 3.3 volts. However, the 3.3 volts available from the ZDOK is not used. Instead, 5 volts is regulated down to 3.3 volts and is heavily filtered on both side of the regulator. A common ground, brought in on the ZDOK, is used everywhere. (CHECK THE BOARD LAYOUT TO SEE WHAT MEANS ARE USED TO SEPARATE THE GROUNDS, IF ANY. Photos of the board don't show anything obvious.) (SEE IF THE PROPAGATION OF THE CLOCKS ACROSS THE BOARD IS A CONCERN. There will be a few nanoseconds difference in the clocks to each ADC due to propagation delay. Per conversation with Dan Werthimer, this is not a concern.)

The ADC evaluation board gets is power from the Spartan evaluation board to which it is mated by and FMC connector. The ADC board regulates the 3.3 volts taken directly from the FMC down to 1.8 volts, using an LM2831Z and uses it for both the digital and analog supplies of the ADC. Not very fancy!

The Kintex eval board has a complex power system. It has a 12-volt power input. This is converted to needed voltages using a TI chip set: the UDC9248 PWM controller and several PTD08D210W. It also uses some linear LDO regulators for some functions.

Our design should include the good design practices used in the Berkeley design. It could also include the regulator approach used in the Kintex board. We should also look at "simpler"

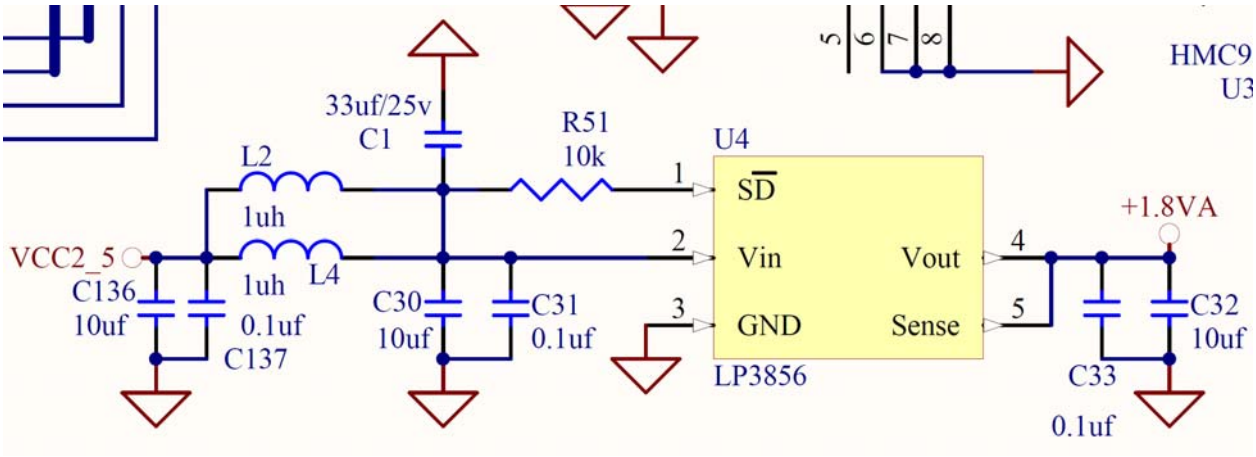
approaches, e.g. power bricks from Syncor. For ADC design, assume we get 3.3 volts from a regulator. From this 3.3 volts provide two regulators, one for digital and one for analog.

HMCAD1511 Required current (all input power pins = 1.8 volts, 50% clock (freq?), -1DBFS 71 MHz input:
IAVDD = 270 ma
IDVDD = 125 ma

Triple this since we have three converters and add some margin since our conditions are not the same (white noise and fairly high frequency clock).
IAVDD = 810 + 190 (about 20% margin) ma = 1.0 A
IDVDD = 375 + 75 (about 20% margin) ma = 450 ma

Check temperatures of regulators under these conditions and allow a lot of margin for reliability. Analyze the LP3856.

As a starting point, use the regulator circuit used in the Berkeley ADC circuit. It uses the TI LDO regulator chip LP3816ES-1.8.



The above circuit is taken from the Berkeley schematic.

Some important points from the LP3856 data sheet:

- Rating is 3 amps (we need 1.3 for the analog and a little for the Xilinx bank associated with the ADCs (so there is sufficient margin)
- Drop out voltage is max ~400 mv at 2A (so 2.5 volts at input is fine and we have it available)
- 3% accuracy over temperature

- The TO263-5 package is best suited for our PCB layout (same one used by Berkeley)
- 2.5 volts is the **minimum** operating voltage (so Berkeley design is on the edge)
- Supply ripple rejection improves from 57 db to 73 db as drop out voltage goes from 0.5 to 1 volt (again Berkeley is near the bottom edge on this.)
- Minimum input capacitance is 10 uF, ceramic or tantalum.
- Output capacitor must be with 1 cm of output pin, kelvin connected, at least 10 uF.
- There are several PCB Layout cautions (add note in schematic to review these)
- Tantalum capacitors show less variation with temperature than ceramic. Take this into account when calculating minimum capacitance. They also have low ESR. Recommended.
- At start up may see up to 2.2 volts at the output for a as the input supply rises. The 1511 can stand up to 2.3 volts.
- Built-in short circuit protection and thermal limiting
- Use a 10 K pull-up on the SD pin if not used (exactly what Berkeley does)
- With 1 square inch of copper plane for a heatsink, thermal resistance is 32^{o}C/W. (for the 2.5-volts case: Pd = (2.5V – 1.8V) * 2A = 1.2 W. Temp rise is 1.2 * 32 = 38.4^{o}C. Max junction temp is 125 C. So if copper plane must be less than 125 – 38.4 = 86.6 degrees C. It's likely we have no problem . For 3.3V input, Pd = (3.3 – 1.8) * 2A = 3W. Temp rise is 96 degrees. This is marginal even at 25 degrees C unless we use a heat sink. Best to go with 2.5 volts.
- At 2 amps, need ESR of output capacitor to be between 0.12 and 5 ohms

Taking into account all of the above, I conclude that we should use the Berkeley circuit with the output tantalum capacitor increased. Look at the next available value, 15 uF. Can get ESR from 100 mOhm to 7.7 ohms in stock at Digikey. Stay below 3 ohms. The Kemet or Vishay parts below would do fine.

Manuf	**P/N**	**ESR**	**Size**	**$/100**
Vishay	TR3A156K6R3C1000	1 ohm	1206	0.63
Kemet	T494A156K006AT	2 ohm	1206	0.51
AVX	F970J156KBA	2 ohm	1411	0.47
AVX	F930J156MAA	2.9 ohms	1206	0.15
Rohm	TCA0J156M8R	3 ohms	1206	0.46

We can use the corresponding 10 uF at the input: Kemet T494A106K006AT, $0.42 or Vishay TR3A106K6R3C1500, $0.57. The 33 uF cap on the input can copy Berkeley: Kemet T495D336K025ZTE230. The 33 uF does not need to be a 25-volt capacitor given our two layers of regulators. The Kemet 6.3 V, T491A336K006AT, with ESR of 2.5 ohms and cost of 0.31 is a bargain compared to the 25-volt part ($0.99).

5.8.2 Synthesizer and Clock Driver Regulators

Hittite recommends its **HMC976LP3E** regulator for use with its low-phase-noise synthesizers. We have opted not to use their synthesizers in favor of a less expensive one from TI. However, we do choose to use the HMC976. In fact this regulator is also useful for the clock driver chip which Berkeley uses in their design and which we copy. So our design includes two HMC976 low-noise, high PSRR regulators.

Critical specifications:

- Minimum required output load capacitance is 4.7 uF
- Thermal shutdown is 115°C

Design:

We want an output voltage of 3.3 volts with an input of 5 volts. Select R1 from this equation:

$$R1 = \frac{\left(\left(\frac{Vout}{1.17}\right)-1\right)*18.9}{1-0.32*\left(\left(\frac{Vout}{1.17}\right)-1\right)} \quad \text{(Kohms)}$$

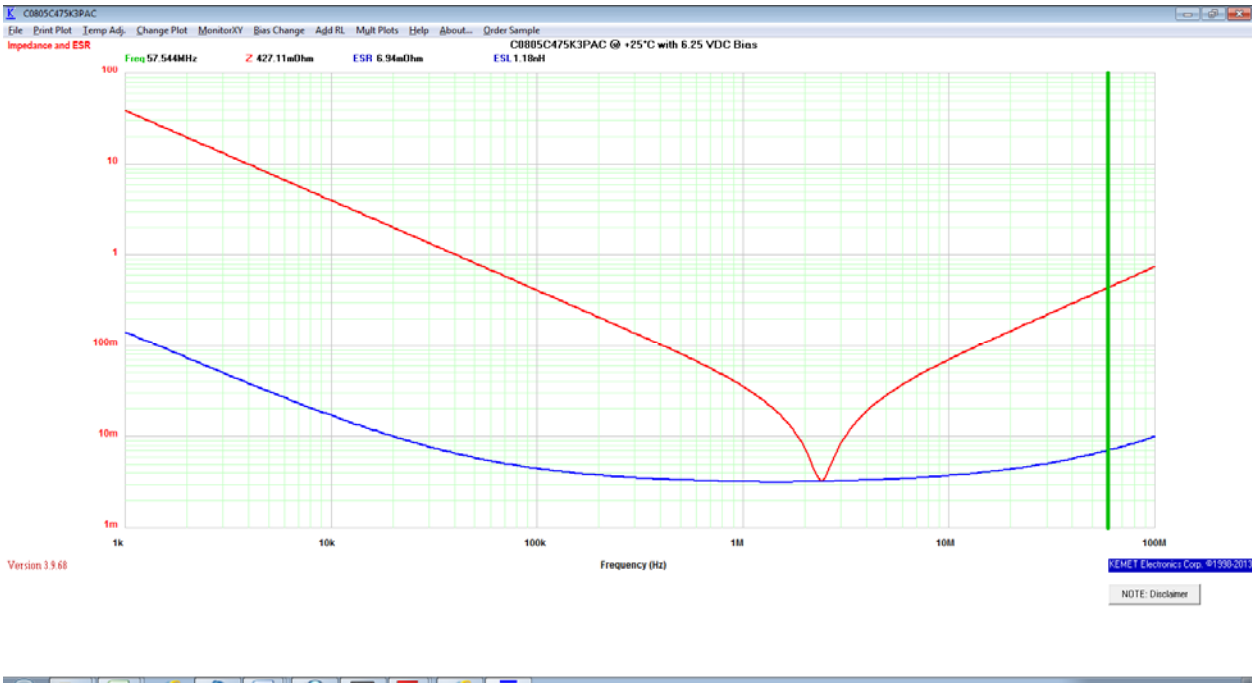
For Vout of 3.3 volts this yields R1 = 82.43K ohms.

We need a minimum of 4.7 uF at pin 4, VRX. Per the data sheet it must be low ESR ceramic. Select a dielectric with low temperature and voltage sensitivity. C0805C475K3PAC has an X5R dielectric has reasonable temperature at ESR stability. This is what was selected for the Berkeley application. The eval board did not specify dielectric but used an 0603 size part. Stick with the Berkeley part. The rest of the Berkeley design follows the eval board closely except for the LC filter at the power supply input and ouput. Follow this design as well.

Thermal: We expect a power dissipation of (5v – 3.3v) * ~200ma = .34W. The junction temp is calculated per the data sheet:

$$T_j = T_a + \left(P_d \times \theta_{ja} \right)$$

The device shuts down at 115°C. Assume 1000 mm2 of copper dedicated to each of these two chips. This gives a thermal resistance of 57.3 °C/W and a temperature rise of .34 * 57.3 = 19.5 °C. So the ambient could be as high as 95.5 °C. It's likely to be more like 40 °C, so we have a lot of margin.



ESR and impedance of 4.7 uF capacitors.

5.8.3 FPGA Linear Power Requirements

There are two linear supplies associated with the FPGA.

VCC5V0 is generated by a linear supply from 12 Volts. This provides 5 Volts at 2 Amps capacity. This goes to the ADC linear supplies and the Raspberry Pi.

VCC_SPI is generated by a linear supply from 12 Volts. It provides 2.8 Volts at 300 mA. It is used for the SPI flash memory that stores the Xilinx personality.

5.8.4 Power Supply Controllers with DC-DC Converters

There are three UCD9248PFC Digital Power Controllers. Each controller can control four DC-DC converters. There is a common PMBUS between the controllers. This can be used for programming the controllers. Following is a listing of the voltages from each controller.

Power Controller 1

VCCINT	1.0V	PTD08A020W	aka VCCINT_FPGA FPGA Internal Core
VCCAUX	1.8V	1st Half of PTD08A210W	
VCC3V3	3.3V	2nd Half of PTD08A210W	
VADJ	3.3V	PTD08A010W	aka VADJ_FPGA. Tie to VCC3V3?

Power Controller 2

VCC2V5	2.5V	1st Half of PTD08A210W	aka VCC2V5_FPGA
VCC1V5	1.5V	2nd Half of PTD08A210W	aka VCC1V5_FPGA
VCCMGTA	1.0V	1st Half of PTD08A210W	
VTTMGTA	1.2V	2nd Half of PTD08A210W	

Power Controller 3

VCCAUX_IO	1.8V	1st Half of PTD08A210W	See Note 2
VCCBRAM	1.0V	2nd Half of PTD08A210W	Tie to VCCINT? See Note 3
VCCAUXMGT	1.8V	PTD08A010W	
Not used			

Note 1:All DC-DC converters are 10 Amps, except VCCINT which is 20 Amps.

Note 2: 7 series FPGAs include an improved I/O driver structure allowing a higher pre-driver voltage (Vccaux_io) to achieve higher data rates. Vccaux_io is a separate rail providing power to the I/O circuitry in the High Performance banks. Vccaux_io must be set to 2.0V to achieve higher data rates and can be set to 1.8V for lower data rate. Setting Vccaux_io=2.0v does not affect other IO standards and unless it is being used for high performance memory applications Vccaux_io should be set to 1.8v.

Note 3: You can tie VCCINT and VCC BRAM together. The MGT supplies need to be independant.

Notice the actual Voltages provided are 3.3V, 2.5V,1.8V,1.5V, 1.2V, & 1.0V. Thus 6 Voltages can be provided by two controllers.

In the initial prototype boards all the controllers and converters will be used. For the production board, current usage will be known, along with optimal voltages. The number of components can be reduced to optimal then.

6. Use of the Raspberry Pi

6.1 Initial Set-up

See the book Raspberry Pi User Guide by Eben Upton. There is a copy in Joe Greenberg's office.
See page 14, Getting Started with the Raspberry Pi.
Connect a USB keyboard and mouse.
Connect a HDMI cable from the PI to the DVI-D input of a monitor.
Connect power via the mini USB plug via a cable with a wall transformer.
When you connect power you should get a raspberrypi **login:** prompt
Type **pi** as the login.pi
Type **maggieysharon** as the password.
At the **pi@raspberrypi ~$** prompt type **startx**. This should bring up the GUI.
An Ethernet connection can be made for web access.
Midori is provided as a web browser.
LXTerminal brings up a Linux pi@raspberrypi prompt.
The name on the network is raspberrypi.
The MAC is B8:27:EB:39:8D:E2
IT has to get it so its on the network.

6.2 Programming in C

See the book in Joe's office Programming the Raspberry Pi Getting Started with Python by Simon Monk.
See Chapter 2 Getting Started
Clicking on the File Manager icon gives access to the files present.
Clicking on LXTerminal gives a terminal with a command line prompt.

Clicking on IDLE brings up a text editor.
Go to File>RecentFiles and select blink.c
The program can then be edited and saved.

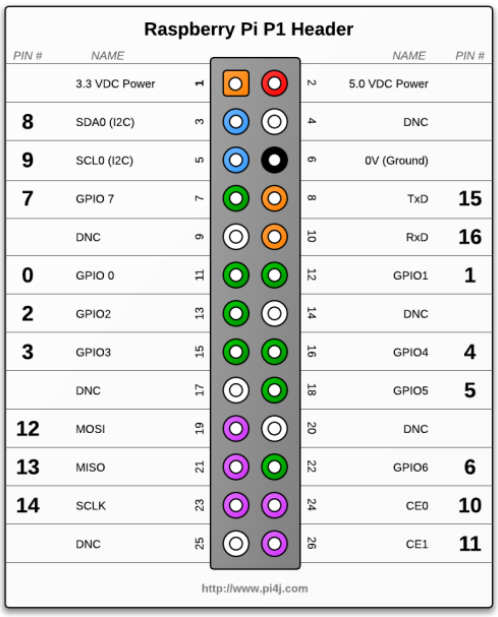
See page 155 in the Programming the Raspberry Pi book for info in Programming in C.
See:
https://projects.drogon.net/raspberry-pi/gertboard-and-wiringpi/blink/
For a description of a program for blinking an LED.
This uses the wiringPi library which has software for interfacing with the GPIO pins.
https://projects.drogon.net/raspberry-pi/wiringpi/

has information about wiringPi. Note this must be downloaded into the PI per the instructions. Once downloaded it stays in the memory card.

The program can be compiled by:

```
gcc -o blink blink.c –L/usr/local/lib –lwiringPi
The program can be run by:
sudo ./blink
^C stops the program.
```

http://iqjar.com/jar/connecting-to-the-gpio-pins-of-the-raspberry-pi/
This link shows the GPIO pin connections.



For blink to make an LED blink, connect a resistor connected to the anode of an led to GPIO0 pin 11.
Connect the cathode to pin 6 (ground).

7. SNAP Board testing

7.1 Stand-alone testing

To Test the board:

7.1.1 Do a visual inspection.

7.1.2 Measure the resistance of the power planes.

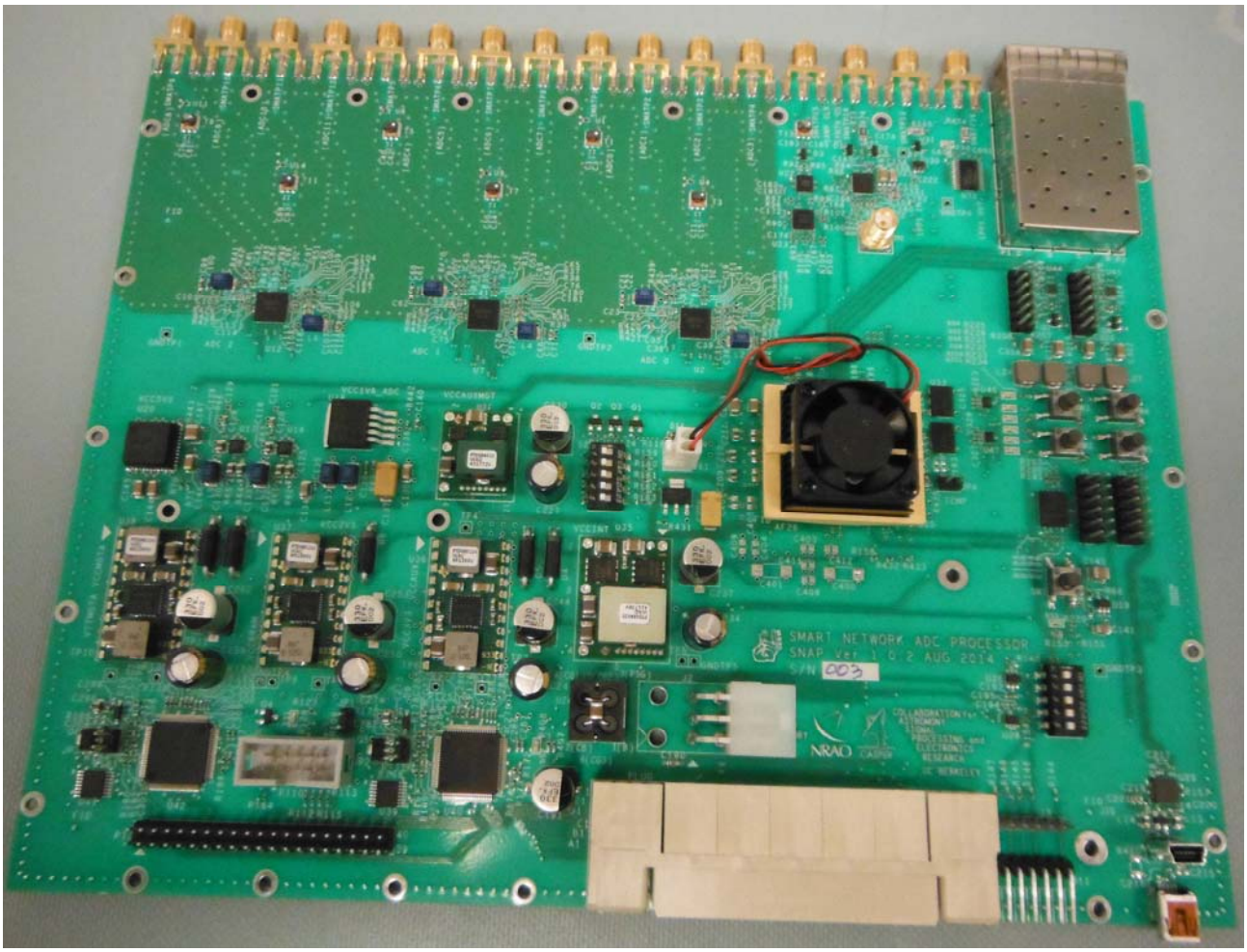
12V 120K at U24
VCCINT D4 183 Ohm
VCCAUX D5 1.8K
VCC3V3 U36-11 0.69 OHM SUSPICIOUS
VCC2V5 U37-22 3K
VCCBRAM U37-11 1.8K
VCCMGTA U380-22 3K
VTTMGTA U38-11 53K
VCCINT U35-4 260 OHM
VCCAUXMGT U34-4 1.78K
VCC5V0 R443-1 1.6K
VCC_SPI R68 1.4K
VCC3V3_PWRCTL on Q5 5K
VCC3V3_PWRCTL on Q6 6K
VCC3V3_SYN C121 or L8 3K
VCC3V3_DRV C128 or L10 .2 Ohm Suspicious
Net is VCC3V3_DRV R93 1 R90 1 D3 3 R99 1 U23 25 U23 16 U23 1 U23 9
C166 1 C176 1 C171 1 C172 1 C163 1 C164 1 C167 1 L10 2
C175 1 C129 1

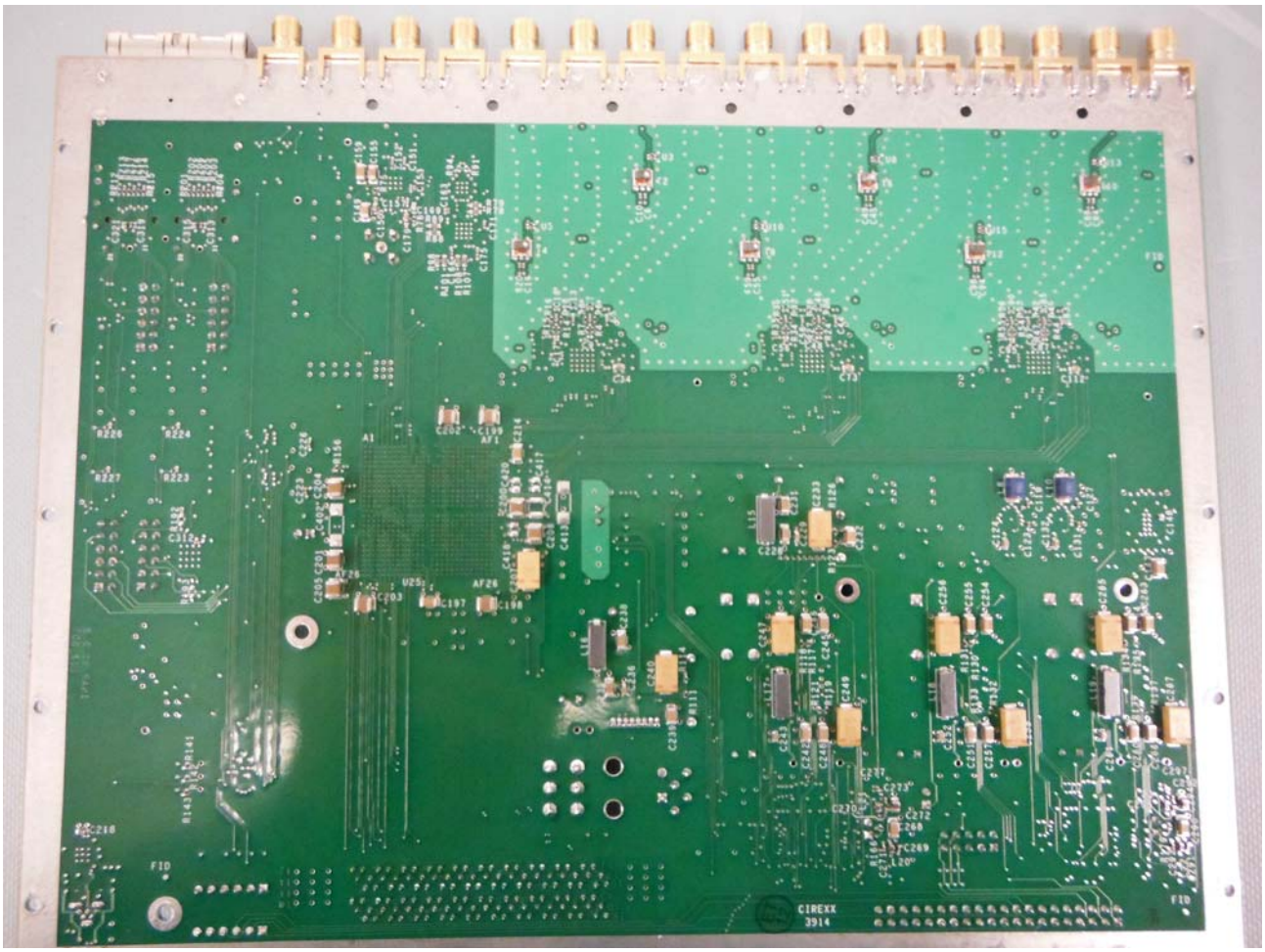
Apply 12V.
Check the DC Voltages which do not need Power Supply Programming
VCC5V0 L7 5.08V
VCC_SPI R68 2.8V
VCC3V3_SYN C121 0V Should be 3.3
VCC3V3_DRV C128 .2 Ohm Suspicious 0V, Should be 3.3V
VCC3V3_PWRCTL 3.4V on Q5
VCC3V3_PWRCTL 3.4V on Q6

Program the TI Power Supply Controllers
Program the Xilinx.
Check the ZDOK.
Check the Raspberry PI

Check the 10GB Ethernet.

Following are photos of the board.


SMART NETWORK ADC PROCESSOR
SNAP Ver 1.0.2 AUG 2014
S/N 003
NRAO



7.2 Tests

7.2.1 Dan Testing the short on SN3

```
i tried for a bit today,
but couldn't track down the short on
Vcc3V3  on SNAP  serial number 3.

it's not a 0 ohm short - it's about 0.7 ohms.

i connected an external lab supply to Vcc3V3
(soldering wires to U36 pin 11, and ground)

i slowly ramped up the voltage and current,
all the way up to 3 volts at 5 amps (15 watts).

the only thing i found (with my finger) that got warm was a
chip on the U36 TI dual switching power supply module.
```

```
but i'm not sure if that's the problem, or it's warm
perhaps because  one is not supposed to drive the output
of a TI switcher module.

i'd like to remove U36 and try again some time,
but i need help - it's 22 pin SMD module.

one wierd thing - i didn't see any of the voltage i was
injecting on C283 or R119.  but perhaps i wasn't probing
them correctly (they are teeny parts).

another wierd thing - D5 zener seemed to be getting a bit
warm and had 0.9 volts across it.
```

7.3 Jack Hickish Test Results

7.3.1 Power Controller Programming

I've now got some working power controller configurations for all 8 controllable rails. There are still some remaining issues, e.g., the current monitoring and voltage in monitoring don't seem quite correct. I need to translate some of the resistor networks in the schematics into the controller GUI to sort this out. However, the voltage outputs are being monitored correctly, and are coming up to the right levels.

The order of power ups I have configured is --

VCCINT
VCCBRAM
VCCAUX / VCCAUX_IO
VCC2V5, VCC3V3
VMGTAVCC
VMGTAVTT
VCCAUXMGT

The turn off order is the same in reverse, with VCCAUXMGT and VMGTAVTT turning off together, and then successive supplies shutting down after 10ms.

The ordering between the two controller chips use the PWRCTL_SRE_GPIOx signals, with them configured in the controllers as:
GPIO1 (pin 11), U40 output, U42 input. High if VCCINT regulating
GPIO2 (pin 37), U40 output, U42 input. High if VCCINT & VCCAUX regulating
GPIO3 (pin 52), U40 input, U42 output. High if VCCBRAM regulating
GPIO4 (pin 50), U40 input, U42 output. High if VCCBRAM & VCC2V5 & VMGTAVCC & VMGTAVTT regulating

I've attached the projects and hex files I used for the configuration. I haven't found a good way to load multiple controllers simultaneously, so what I did was --

1. Connect to board and let it auto detect settings
2. Switch to address 52, rail 1
3. Import address 52 hex file (Data Flash Mode)
4. Switch to address 53, rail 1
5. Import address 53 hex file
6. Restart board, so everything comes up in order

I've attached measurements I made of all the controlled regulators with these hex files. I've only tried board SNs 1 and 2 since Matt's tests suggest 3 has a 3V3 short. On power up, the two boards I've tried draw about 0.79A.
So far, I haven't actually done any tests to verify the ordering is being carried out correctly.

For added fun, I've also attached a xilinx personality to flash an LED which works on both the boards I've powered up when programmed with a Xilinx JTAG programmer.

7.4 Programming the NRAO SN4 Power Supplies

Using Jack's files, I obtained the following results, which are added to his table:

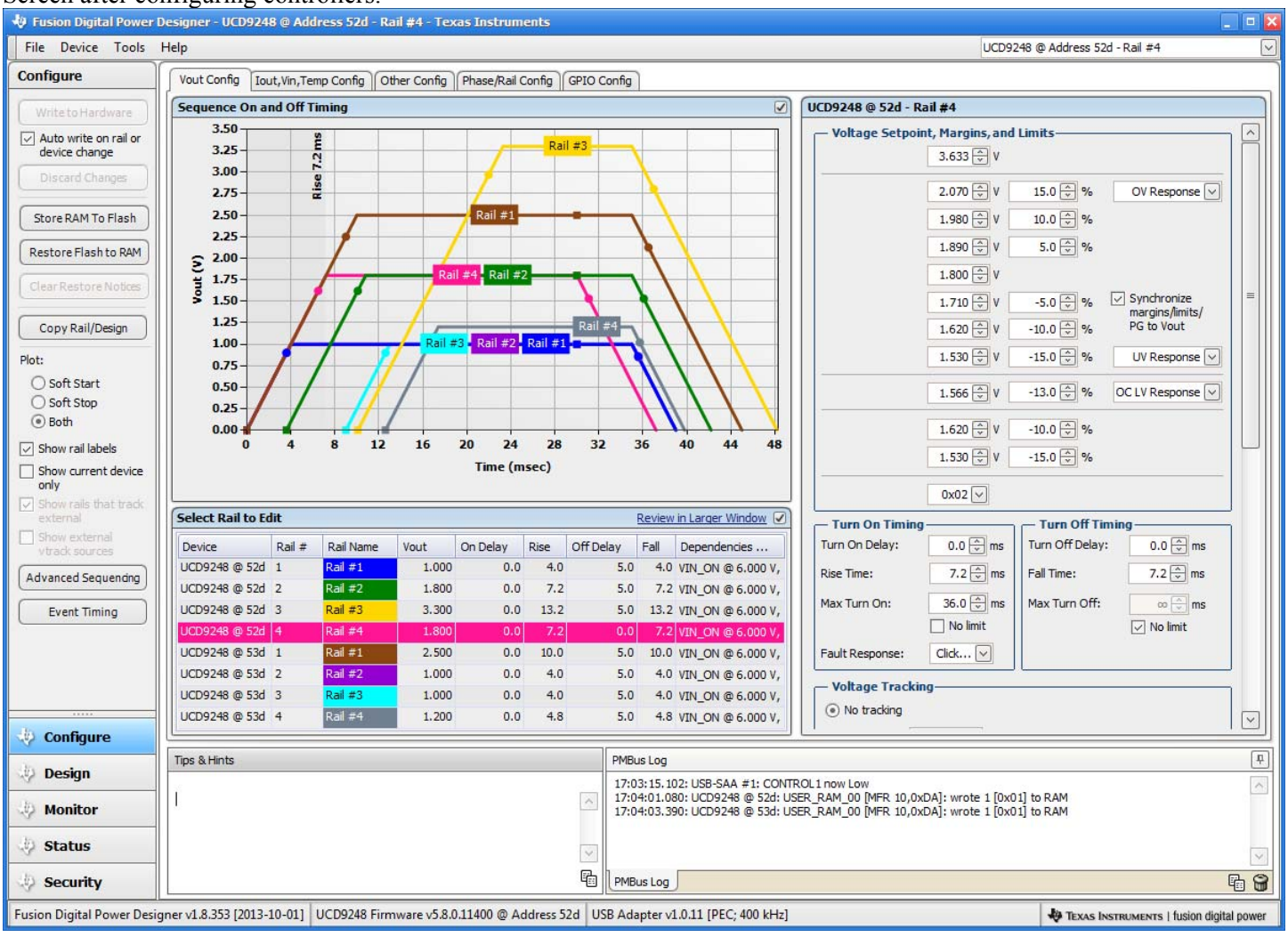
Voltages to ground
SNAP Rev 1.0.2

			Serial 1	2	3.00	4	
U34-4	52-4	VCCAUXMGT	1.83	1.832		1.84	
U35-4	52-1	VCCINT	1.005	1.004		1.00	
U36-22 (A)	52-2	VCCAUX	1.814	1.815		1.82	
U36-11 (B)	52-3	VCC3V3	3.31	3.32		0.00	0.4 Ohms
U37-22 (A)	53-1	VCC2V5	2.52	2.521		2.52	
U37-11 (B)	53-2	VCCBRAM	1.005	1.009		1.01	
U38-22 (A)	53-3	VCCMGTA	1.008	1.009		1.01	
U38-11 (B)	53-4	VTTMGTA	1.205	1.208		1.21	

Programmed with power firmware:

UCD9248 5.8.0.11400 Address 52 Data Flash_gpio.hex	MD5 hash	9e65ceef711ba2c8452bf0ca5c6cb35a
UCD9248 5.8.0.11400 Address 53 Data Flash_gpio.hex	MD5 hash	20e611be7c7d2ebc57bec733f2f88c4b

Screen after configuring controllers.



7.4.1 Programming the Raspberry Pi

I just connected a raspberry pi B+ running Raspbian Wheezy to SNAP S/N 002

(The Pi OS I used is available at http://www.raspberrypi.org/downloads/
version: 2014-09-09-wheezy-raspbian.img
md5sum (of the image, not the zip): c8e331ea6965905d63ccca8388460cf3)

Once connected with a ribbon cable, there is software to program the snap from the pi in the git repository at https://github.com/jack-h/RpiJtag

You can test this on your own snaps with

```
# checkout repo
git clone https://github.com/jack-h/RpiJtag.git
# build software
cd RpiJtag
make
# program demo firmware
sudo ./RpiJtag -i snap_blinky.bit
```

Using a ribbon cable to connect the pi to the snap (the one I have is ~2 foot long) this seems to work fine. I intially had some problems at first, but after connecting and disconnecting scopes / ribbon

cables, they seem to have gone away by magic. I've successfully programmed the board about a dozen times without issue, including doing a few power cycles.

So far so good....

That's right, I've programmed over JTAG and via the raspberry pi (although this is really just JTAG using the Pi's GPIO, I haven't done anything fancy like program the flash via the pi). Having said that, when I left the lab this evening I'd attempted to program the flash chip over JTAG using Vivado, which appeared to work.

7.4.2 Programming the SPI Flash

I'm ready to call good on the SPI flash chip, at least to the extent of programming a image to it via JTAG and it successfully coming up after reboot. I haven't tried any fancy dual-image, watchdog timer cleverness stuff. FWIW, I'm using a configuration clock of 50 MHz.

7.5 Bob Treacy's Progress Reports

SNAP Report Nov 17, 2014
Bob Treacy
PCB Items either driving or to incorporate in a re-spin

7.5.1 PAPER/ HERA Compaq enclosure design

Work going forward
Ongoing work for the PAPER/ HERA Compaq enclosure design, the thermal design work, RF testing of the Compaq enclosure design, and the 1U rack mount chassis design were all approved under funding through NRAO to follow expiration of PAPER/HERA funds. The 1U enclosure design will not begin until the enclosure and thermal design for PAPER/HERA is nearly complete.
I am back to multi-tasking across several assignments and between vacation and holidays, have been out nearly two of the last four weeks. I will work the Compaq enclosure and thermal design together using Inventor, for which we have the Computational Flow Dynamics (CFD) simulator add-on. There was some question about renewing our licensing for the CFD, since it is kind of pricey and gets infrequent use. As I understand the current situation, we own the software and plan to drop the maintenance fee so I will not have support through AutoDesk under this scenario. However, there is a possibility we may qualify for academic license, where the support may then be available in full, or to some degree. This is still evolving, but under one scenario or the other, I think the software will be available and will be worth the time invested to pursue a model. The alternative is largely trial and error with prototype hardware.
Recapping the challenges and proposed design concepts
The enclosure design shall incorporate RF suppression and acceptable thermal performance, the latter of which can be quantified by maintaining the vendor recommended die temperatures. The

RF suppression has not been quantified, which has driven the design concept (at least initially) to an airtight enclosure.
Design concepts targeting the RF suppression will include a best effort RF shielding on all enclosure penetrations. The resulting design will be tested in Green Bank for radiated emissions.
Inside the enclosure, the thermal design depends primarily upon multiple conducted paths for heat flow from the chips on the PCB to the exterior of the enclosure; secondary paths are

through radiation to the interior walls of the enclosure, then convection from the exterior of the enclosure to the ambient environment. Inside the enclosure, one conducted path is through the thermal pads on the chips to the ground plane, to the mounting rails, to the enclosure wall. The thermal vias that complete this path should be filled rather than tented with solder mask. In the SNAP Ver1.0.2, the thermal vias are filled with solder. I have since learned these could also be copper filled to conduct heat more efficiently. I will investigate tradeoffs considering this option in simulation for potential use in the next PCB spin. Another conducted path is through some sort of heat sink to the enclosure lid, which would only apply to chips for which the conducted path through the ground plane proves inadequate. Rich has proposed two possible concepts for this path, for which a highly compliant mechanical interface to the chip package is critical in order to avoid stress on the solder joints. One concept proposes custom (aluminum) heat sinks between the packages and the lid using a highly compliant thermal pad. The other concept proposes a flexible copper ribbon between the packages and the lid, perhaps 'S' or 'C' shaped. Radiated paths are simply from the components through the air to the interior enclosure walls; these will likely contribute very little to the solution.

I have ordered two of the RFT Compaq enclosures R58010-100-1 and four of the MB700 mounting rails. These are stock items, delivery is promised by first week of December 2015.

I have also located a vendor for the SMA bulkhead connectors (VidaRF) who makes a reasonably priced connector with an 80 mil center pin, or I can probably request a semi-custom part with a longer pin for the ~1.5K quantities needed for the SNAP project. Direct solder of the SMA center pin to the PCB simplifies assembly, where the alternative is to connect short jumpers from the connectors to the PCB.

I have also acquired samples from Bergquist for some thermal pads. One is a marketed as a high compliance pad (Gap Pad HC3.0) the other is highly conformable (Gap Pad 3500 ULM). These were selected by the Bergquist rep based on my description of the application. I have not yet looked closely at either of these pads, or to other vendors.

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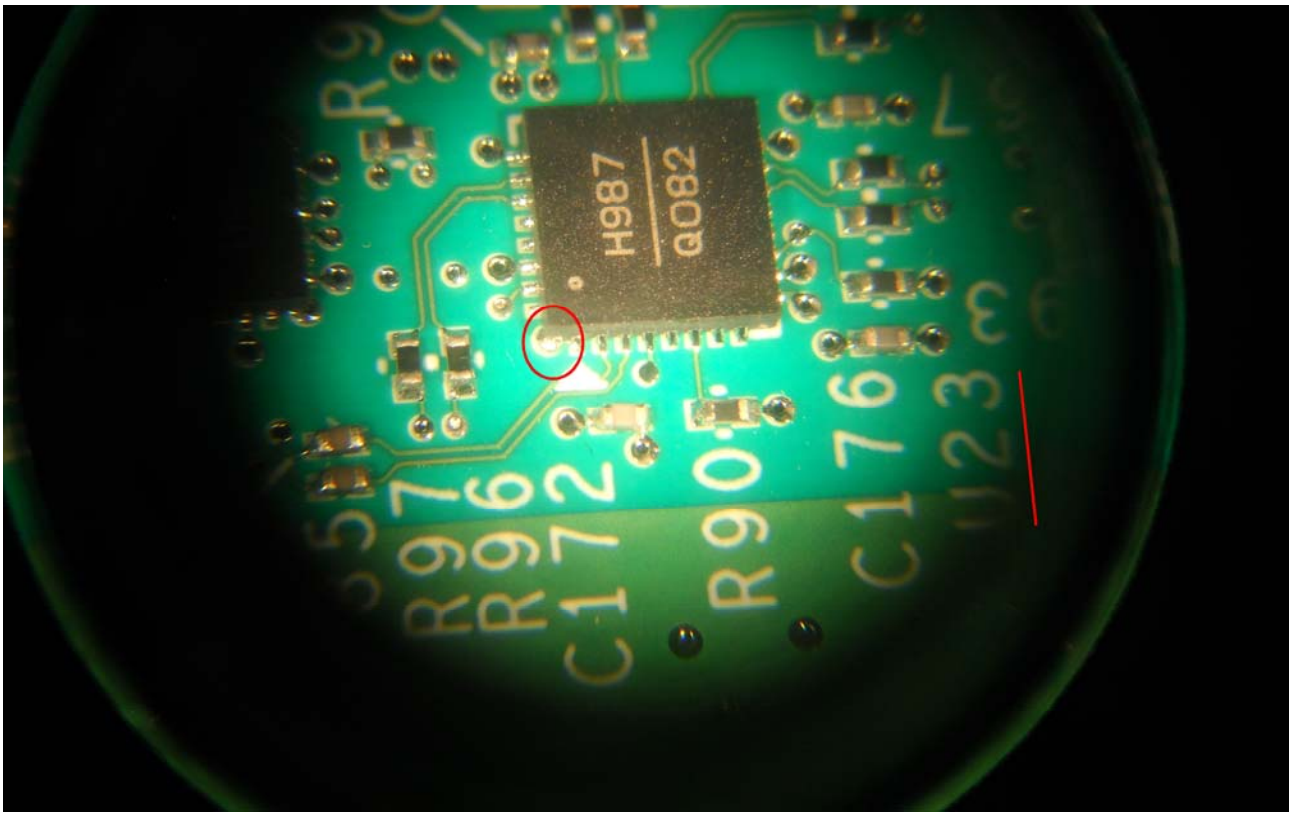
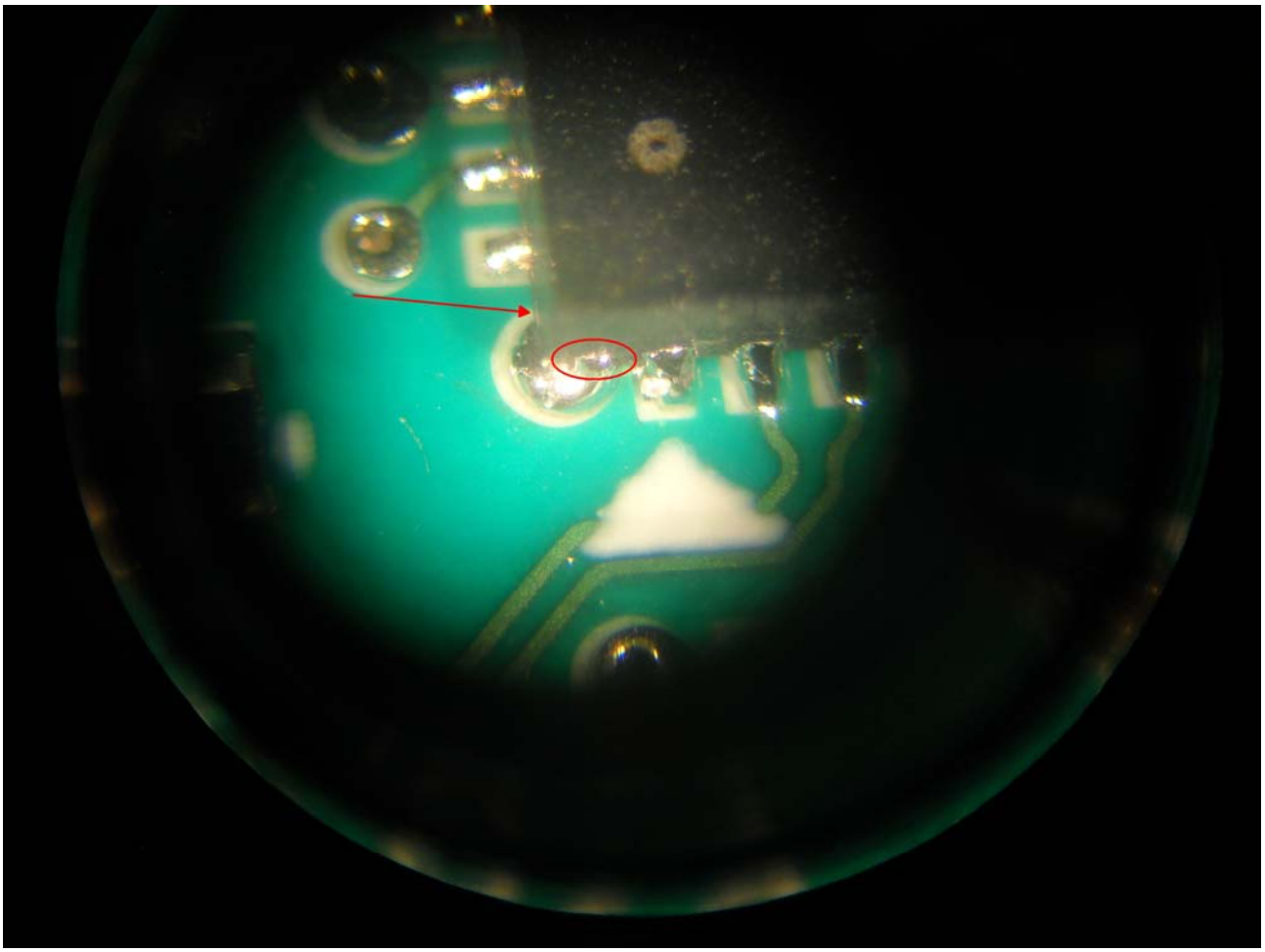
7.5.2 Solder Bridge on U23

On one of the shorted boards, we had earlier removed a solder short adjacent to pin 1 of U23. This package has exposed metal at each corner, in the same plane as where the pins exit the package. This exposed metal is flush with the package surface and is pointed out with the arrow in U23-B. The short occurred between the exposed metal adjacent to pin 1 and the via which is directly beneath it. As far as I know, this only occurred on one assembly. I will see about moving that via in the respin to reduce the risk of this happening. The solder on this via seemed a bit excessive, but I could not determine if it crept in from the solder applied to the thermal pad or another part of the process.

The following photos show the solder bridge.


H987
Q082
R96
C17
R90
C176



8. Un-Resolved Problems

8.1 VCC3V3 Short

8.1.1 The Problem

Both boards SN3 and SN4 have the VCC3V3 plane shorted to ground. SN1 and SN2 work fine.

8.1.2 SN3 Joe's Report

On SN3, Joe programmed the 8 programmable supplies. The VCC3V3 rail showed 0 Volts. Lowering the Voltage and shutting off current limits did not effect the 0 Volt reading. The short measures 0.4 Ohms with a meter. Visual searching of all the VCC3V3 nodes did not show any anomalies. There were numerous nodes under the Xilinx that were not visible. This leads to the suspicion of a short under the Xilinx.

8.1.3 SN4 Dan's Report

```
I tried for a bit today,but couldn't track down the short on Vcc3V3  on SNAP
serial number 3.

It's not a 0 ohm short - it's about 0.7 ohms.

I connected an external lab supply to Vcc3V3(soldering wires to U36 pin 11, and
ground). I slowly ramped up the voltage and current,all the way up to 3 volts at
5 amps (15 watts).

The only thing i found (with my finger) that got warm was a chip on the U36 TI
dual switching power supply module. but i'm not sure if that's the problem, or
it's warm perhaps because  one is not supposed to drive the output
of a TI switcher module.

I'd like to remove U36 and try again some time, but i need help - it's 22 pin
SMD module.

One wierd thing - i didn't see any of the voltage i was injecting on C283 or
R119.  but perhaps i wasn't probing them correctly (they are teeny parts).

Another wierd thing - D5 zener seemed to be getting a bit warm and had 0.9 volts
across it.
```

8.1.4 Next Steps

On SN4, they are going to try removing the power supply. If the short is still there, then they will again attach an external supply. Perhaps either Voltage drops will point to the short, or they will melt it.

Bob has contacted Mo to see if X-rays were taken of the boards during fabrication.

9. What NRAO will do going forward per Rich Lacasse

I spoke with our management about continuing with SNAP project development after the grant money runs out. They have agreed to the following scope of work:

1. Packaging the SNAP board in an RFI case and building a prototype;
2. Testing the shielding effectiveness of (1) using the anechoic chamber in Green Bank. Improve within reason.
3. Modeling the thermal behavior of the packaged board using the AutoCad thermal analysis package or direct measurement if gateware with known power dissipation and temperature measurement capability can be supplied by Berkeley. This should result in the determination of safe operating conditions for the module.
4. Designing a 1-U enclosure for the board including selecting components, chassis layout and thermal analysis or measurement.
5. Minor follow-up work on the SNAP board design

Item 1 will be covered by the money remaining in the grant. The other items would be funded by NRAO internally.

We estimate that items 1 to 4 above entail 500 hours of work and that we can work on these tasks at about 50% FTE. So we're looking at about 25 weeks to finish the above. NRAO will re-evaluate its continued participation in the SNAP effort beyond the initial 25-week effort.

Out of scope are design of a card cage packaging system and any non-trivial follow-up work on the design.

10. Changes for the Next Version of the SNAP Board

10.1 Introduction

This represents a collection of changes and explanations for the next version of the SNAP Board.

10.2 ZDOK Footprint

Land pattern for the ZDOK needs revision, the power pins need offset from current position. Signal pins are OK if power pins are trimmed from connector.

10.3 12 Volt Connector Placement

Inadequate clearance to mate with the right angle 12V input connector (J2), installed connector in 180 degree orientation so board could be powered. Move J2 to the board edge.

10.4 Gerber File Edits

PCB Fabricator made some edits to the Gerbers (primarily clearances) that should be incorporated into native design files.

10.5 Silk Screen Changes

- Some of the pin 1 markings were trimmed away by PCB fabricator, these markings should be well outside the trim zone
- On the Xilinx silkscreen label pins from A1 to A26, not A1 to AF26.

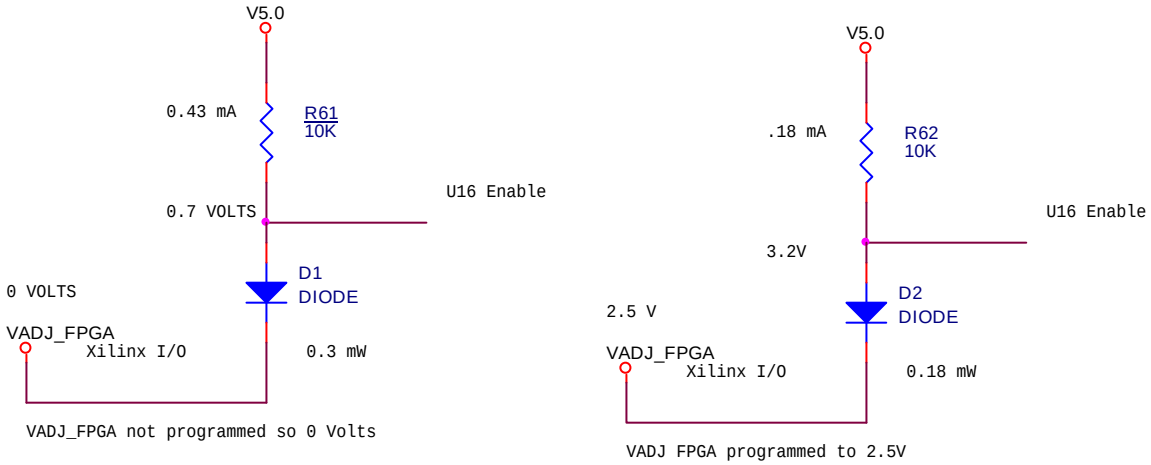
10.6 Remove Laquer from Xilinx Probe Vias

The Xilinx pins were intentionally brought through to the back of the card as an array of vias. This provides a convenient way to probe the pins, since they are not accessable under the BGA. However the Vias were covered with laquer in fabrication, making them unprobable.

10.7 U16 Enable Over-Voltage

The below schematic shows what I believe is the current situation. 5V goes through a protection diode in the Xilinx which then goes its Vcco of VADJ_FPGA.
Since this is unprogrammed VADJ_FPGA = 0 V.
We thus measure 0.7V to the Enable of U16.
The 10K resistor limits the power in the diode to 0.3 mW, which should be safe.
Once VADJ_FPGA is programmed to 2.5V, then there should be 3.2 V to U16's Enable. Diode dissipation would then be 0.18V.

Since we are exceeding the maximum input voltage, a proper change for the next version would be to use VADJ_FPGA as the pullup voltage instead of V5.0.
However for now, I don't think it hurts anything so we can leave it be for the prototype.

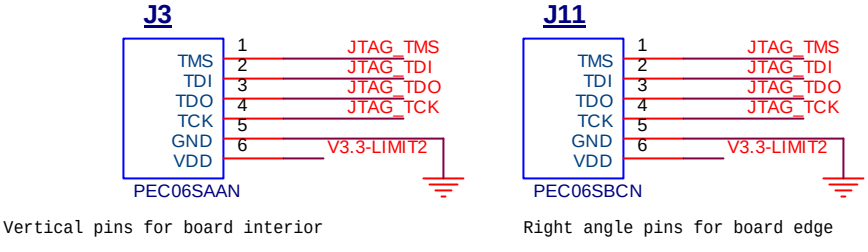


10.8 SM_FAN_PWM Overvoltage

Similar to the above situation, R431 the 1K Pullup for SM_FAN_PWM is pulled up by VCC2V5, While SM_FAN_PWM has a VCCO of VCC3V3. This results in a 1.8ma current in the Xilinx diode. It should be changed to have its Pullup be VCC3V3.

10.9 Make JTAG Connectors Standard Pinout

J3 and J11 are currently wired as shown below. This corresponds to the standard used on NRAO boards.

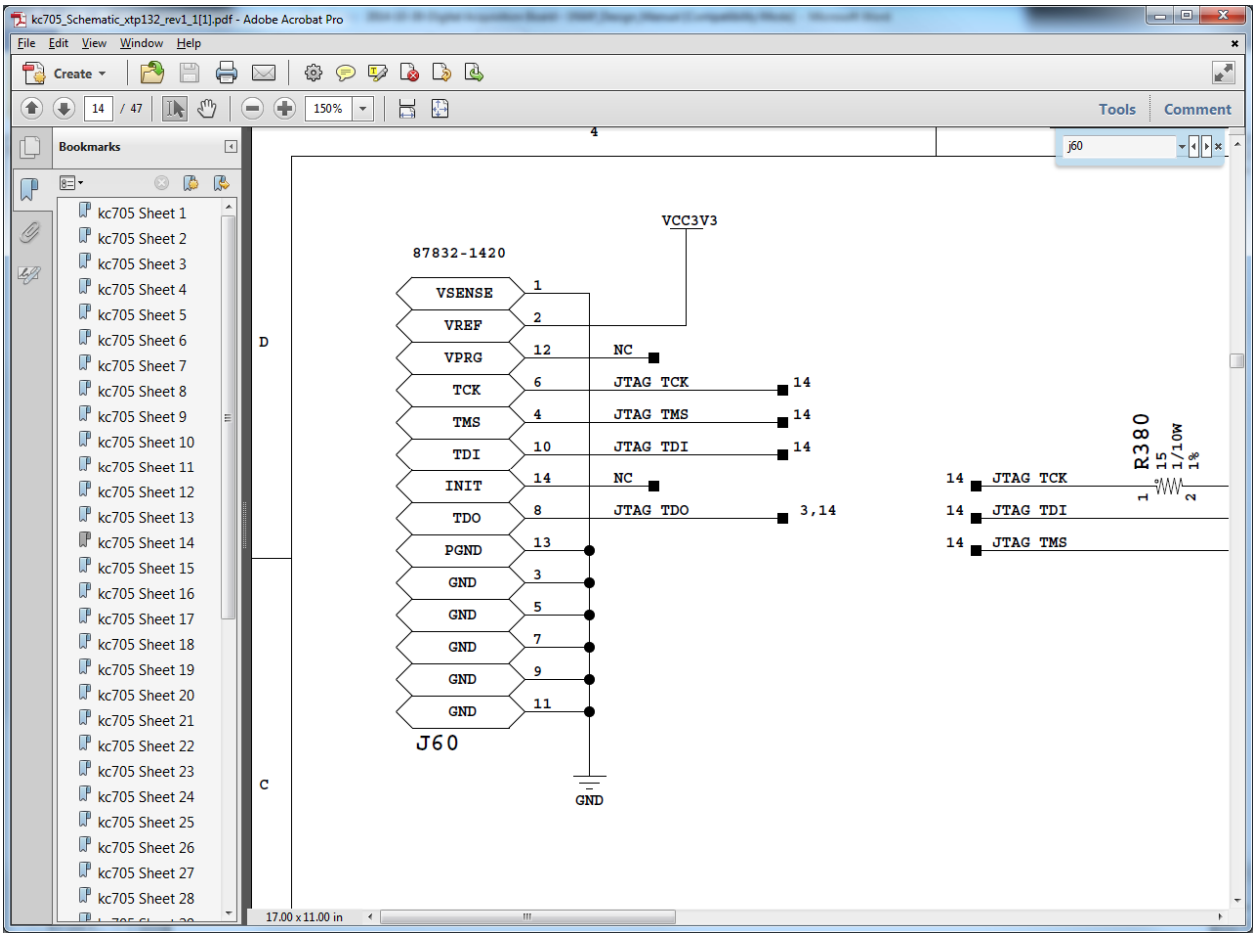


Vertical pins for board interior

Right angle pins for board edge

For use with Digilent JTAG USB Cable Part#250-003P

Ideally the connector would be that used on the KC705 (J60) as shown below:



It's a 2x7 pin connector -- 0.5 mm square posts on 2mm centers.

Page 15 of http://www.xilinx.com/support/documentation/data_sheets/ds593.pdf for pinouts and some part numbers in vertical and right angled configurations. This is show below:

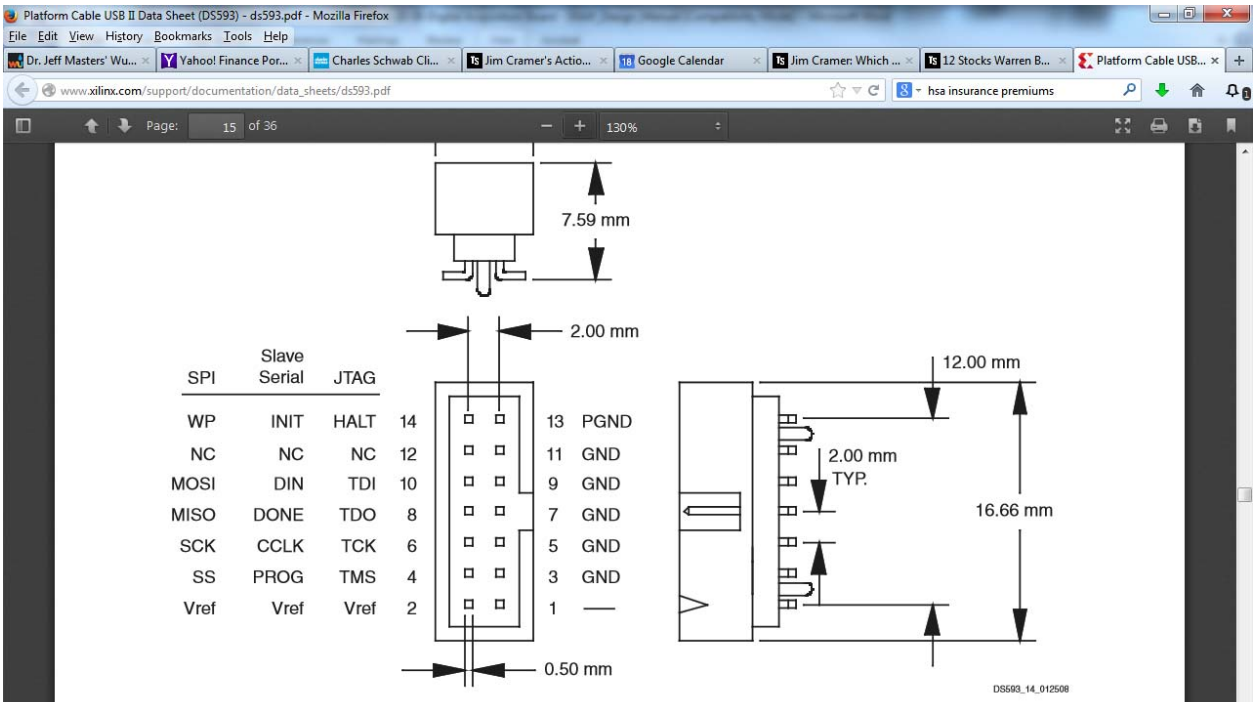


Figure 14: **Target Interface Connector Dimensions and Signal Assignments**

Table 5: **Mating Connectors for 2 mm pitch, 14-Conductor Ribbon Cable**

Manufacturer(1)	SMT, Vertical	Through-Hole, Vertical	Through-Hole, Right Angle	Web Site
Molex	87832-1420	87831-1420	87833-1420	www.molex.com
FCI	98424-G52-14	98414-G06-14	98464-G61-14	www.fciconnect.com
Comm Con Connectors	2475-14G2	2422-14G2	2401R-G2-14	www.commcon.com

Notes:

1. Some manufacturer pin assignments do not conform to Xilinx pin assignments. Please refer to the manufacturer's data sheet for more information.
2. Additional ribbon cables can be purchased separately from the Xilinx Online Store.

11. Appendix 1: Schematics

Supplied as a separate set of PDFs.