



	8	7	6	5	4	3	2	1	
			<u> </u>						
	CAP_0402_INFINIBAND_CO INFINIBAND_CON_1_RX_P_INFINIBAND_1_RX_P<2>	IN_1_RX_P_INFINIBAND_1_RX_P_TS_2	BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_4						
	INFINIBAND_CON_1_RX_P_INFINIBAND_1_RX_P<1>	IN_1_RX_P_INFINIBAND_1_RX_P_TS_1	BYPASS_CAP_25_FPGA_VCĆÄŬX_HSPEED_47NF_9 VCC2_5						
		DN_1_RX_P_INFINIBAND_1_RX_P_TS_0	BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_8 VCC2_5 =						
	INFINIBAND_CON_0_RX_M_INFINIBAND_0_RX_M<3>	IN_0_RX_M_INFINIBAND_0_RX_M_TS_3 INFINIBAND_0_RX_M IN_0_RX_M_INFINIBAND_0_RX_M_TS_2	BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_7 VCC2_5						
	INFINIBAND_CON_0_RX_M_INFINIBAND_0_RX_M<2> CAP_0402_INFINIBAND_CO	- INFINIBAND_0_RX_M<2>	VCC1_5GNDGND						D
	INFINIBAND_CON_0_RX_M_INFINIBAND_0_RX_M<1>	N_0_RX_M_INFINIBAND_0_RX_M_IS_1 Second Rights	BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_5						
		N_O_RX_P\text{N=0} INFINIBAND_0_RX_P\text{N=0} INFINIBAND_0_RX_P\text{TS_3}	DVDAGG CAR OF EDGA VIGORED 47NE 4						
		N_0_RX_P_INFINIBAND_0_RX_P_TS_2	BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_3 VC2.5 = 1						
	CAP_0402_INFINIBAND_CO INFINIBAND_CON_0_RX_P_INFINIBAND_0_RX_P<1>	DN_0_RX_P_INFINIBAND_0_RX_P_TS_1	BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_2		BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_470NF_5				
	CAP_0402_INFINIBAND_CO	N_0_RX_P_INFINIBAND_0_RX_P_TS_0	BYPASS_CAP_25_FPGA_VCCÄÜX_HSPEED_47NF_1 VCC2_5 GND		BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_470NF_4				
	BYPASS_CAP_25_M	GT_BOTTOM_OSC2_HSPEED_100NF_0	BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_47NF_0 VC2.5 = 1		BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_470NF_3 VCCO_BANK01	3			
			BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_2 VCC1_5 =		BYPASS_CAP_BK01_FPGA_VČČO_HSPEED_470NF_2	2			
		GT_BOTTOM_OSC1_HSPEED_100NF_0 VCC2_5GND MGT_TOP_OSC2_HSPEED_100NE_0	- CAP - CAP		VCCO_BANKO1 - GND	BYPASS_CAP_BK01_FPGA_VCCO_BU	LK_4UF7_2		
	BYPASS CAP 15	MGT_TOP_OSC2_HSPEED_100NF_0 VCC2_5	CAP_0402_FPGA_PUSHBUTTON2_GND_TD_0 PUSHBUTTON2		BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_470NF_0 VCCO_BANK01	BYPASS_CAP_BK01_FPGA_VCCO_BU BYPASS_CAP_BK01_FPGA_VCCO_BU VCO_BAN01	LK_4UF7_1		
	BYPASS_CAP_25	VCC1_5GND MGT_TOP_OSC1_HSPEED_100NF_0	PUSHBUTTONI - GND GND TD 0		VCC2_5CND BYPASS CAP 25 FPGA VCCAUX HSPEED 470NF 3	BYPASS_CAP_BK01_F0A_VCC0_BU VCC0_BAN001	LK_4UF7_0		
	RYPASS CAP 15	VCC2.5 - GND GND H94 FPGA_VCCINT_HSPEED_47NF_19	PUSHBUTTON0GND CAP_0402_FPGA_PROG_B_GND_TD_0		VCC2.5GNO 	· · · · · · · · · · · · · · · · · · ·			
c	BYPASS_CAP_15	VCC1.5 - GND FPGA_VCCINT_HSPEED_47NF_18 VCC1.5 - GND	BYPASS_CAP_15_FPGA_VCCINT_HSPEED_47NF_1 VCC1.5 Good GND		BYPASS_CAP_25_FPGA_VCCAUX_HSPEED_470NF_1	BYPASS_CAP_25_FPGA_VCCAUX_BU			
	BYPASS CAP 15	5 FPGA_VCCINT_HSPEED_47NF_0	BYPASS_CAP_33_SYSCLK_OSC_HSPEED_100NF_0	BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_15 VCC2.5 = 1	DVDAGE CAD OF EDGA VCCATIV HEDEED 470NE O	BYPASS_CAP_15_FPGA_VCCINT_BUL VCC1.5 - GND BYPASS_CAP_15_FPGA_VCCINT_BUL	K_4UF7_5		
	RVDASS CAD 15	FPGA_VCCINT_HSPEED_47NF_17	CAP_0402_FPGA_SYSCLK_M_GND_TD_0 SYSCK_DIVGND	BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_14	VCC.5 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -	BYPASS_CAP_15_FPGA_VCCINT_BUL VCT.5 = GNO BYPASS_CAP_25_RS232_IF_BULK VCZ.5 = GNO RS232_CAP_CHARGEPUMF	1UF 0		
	BYPASS_CAP_15	_FPGA_VCCINT_HSPEED_47NF_16 VCC1_5 GND	BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_11	BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_13 VCC2_5	BYPASS_CAP_15_FPGA_VCCINI_HSPEED_470NF_10 VCC1_5	RS232_CAP_CHARGEPUMF	2_0		
	BYPASS_CAP_15		BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_10 VCC2.5 - [-GND]_GND	BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_12 VCC2.5 = 1 CND	BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_9	BYPASS CAP 15 FPGA VCCINT BUL	_v_M K_4UF7_3		
		_FPGA_VCCINT_HSPEED_47NF_14 VCC1_5	BYPASS_CAP_25_ZBT_SRAM1 HSPEED_100NF_9	BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_11 VCC2_5	BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_8	RS232_CAP_CHARGEPUMF	1_0		
	BYDASS CAD 15	_FPGA_VCCINT_HSPEED_47NF_13 VCC1_5	BYPASS_CAP_25_ZBT_SRAMI_HSPEED_100NF_8 VCC2.5 = 1 out Out Out HSP BYPASS_CAP_25_ZBT_SRAMI_HSPEED_100NF_7	BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_10 VCC.5 = 1	BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_7 VCC1.5	BYPASS_CAP_15_FPGA_VCCINT_BUL	K_4UF7_2 BYPASS CAP ISR3 3IN_BUI	ĸ n	
		VCC1_5 GND GND	VCC2_5 GND	VCC2_5 GND	VCC1_5 GND	BYPASS_CAP_15_FPGA_VCCINT_BUL VCC1_5 = GND	K_4UF7_1 BYPASS_CAP_ISR3_3OUT_BU		
	BYPASS_CAP_15	_FPGA_VCCINT_HSPEED_47NF_11 VCC1.5 _1	BYPASS_CAP_25_ZBT_SRAMM*_HSPEED_100NF_6 VC2.5 =	BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_8 VCQ.5 = 1 - co s GOOD BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_7 VCQ.5 = 1 - co s GOOD BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_6	BYPASS_CAP_15_FPGA_VCCWT_HSPEED_470NF_5 VCX1.5	BYPASS_CAP_15_FPGA_VCCINT_BUL	BYPASS_CAP_ISR3_3OUT_BU K_4UF7_0 BYPASS_CAP_ISR3_5IN_BUIL	K_0	
	BYPASS CAP 2	5 FPGA VCCO HSPFFD 47NF 35		BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_6		- CAP	BYPASS_CAP_ISR2_5IN_BUIL (_10UF_1	JLK_0	
	BYPASS_CAP_2	VCC2.5 - GND 5_FPGA_VCC0_HSPEED_47NF_34 VCC2.5 - GND	VCC2.5OND	VCC2.5 - COND BYPASS_CAP_15_FPGA_VCCNT_HSPEED_47NF_7 VCC1.5 CNT_COND	WCC1_5 - GND BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_2 VCC1_5 - GND	BYPASS_CAP_25_ZBT_SRAMT_BULI	BYPASS_CAP_ISR1_8IN_BUL	κ_0	
	BYPASS_CAP_2	5_FPGA_VCCO_HSPEED_47NF_33	BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_2	BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_5	BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_1	VCC2_5 - GND	BYPASS_CAP_ISR1_8OUT_BU	JLK_0	
В	BYPASS_CAP_2	S_FPGA_VCCO_HSPEED_47NF_32 VCC2_5GND	BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_1	BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_4 VCC2_5GND	BYPASS_CAP_15_FPGA_VCCINT_HSPEED_470NF_0 VCCI_5	VOL25 - GND	BYPASS_CAP_ISR1"_5IN_BUL VCCS - ONL	K_0	В
		5_FPGA_VCCO_HSPEED_47NF_31 VCC2_5GND	BYPASS_CAP_25_ZBT_SRAM1_HSPEED_100NF_0	BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_3	VCC2_5 i i GND	BYPASS CAP 25 MGT BOTTOM OSC1	BYPASS_CAP_ISR1_5OUT_BU VCC1_5 - CND VCC1_5 - CND	JLK_0	
		S_FPGA_VCCO_HSPEED_47NF_30 VCC2_5	BYPASS_CAP_25_ZBT_SRAMO_HSPEED_100NF_11 VCC2.5 = GND GND	BYPASS_CAP_25_FPGA_VCCO HSPEED_47NF_2 VCC2_5 CND	BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_16 VCC2_5 - OND OND	BYPASS_CAP_25_MGT_TOP_OSC2_BU	BYPASS_CAP_18_18_REĞULATION VTT1_8 - MGT_G MGT_G	NO	
	BYPASS_CAP_2	5_FPGA_VCCO_HSPEED_47NF_29 VCC2_5GND 5_FPGA_VCCO_HSPEED_47NF_28	BYPASS_CAP_25_ZBT_SRAMO_HSPEED_100NF_10 VCC2.5	BYPASS_CAP_25_FPGA_VCOO_HSPEED_47NF_1 VCC2.5CND BYPASS_CAP_25_FPGA_VCOO_HSPEED_47NF_0	BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_15 VCC2_5CND BYPASS_CAP_25_EPGA_VCCO_HSPEED_470NF_14	BYPASS CAP 25 MGT TOP OSC1 BU	BYPASS_CAP_25_25_REGULATION VCCA2_5MGT_G	NOU12_U ND	
	DVD400 CAD 0	5_FPGA_VCCO_HSPEED_47NF_28 VCC2_5	BYPASS_CAP_25_ZBT_SRAMO_HSPEED_100NF_9 VCC2.5GND BYPASS_CAP_25_ZBT_SRAMO_HSPEED_100NF_8	BYPASS_CAP_25_FPGA_VCCO_HSPEED_47NF_0 VCC2.5 = COUNT_HSPEED_47NF_6	BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_14 VC2_5	BYPASS_CAP_33_18_REGULATIO	N_IN_0 BYPASS_CAP_BK01_FPGA_VCCO_B	ULK_47UF_1	
	,	5_FPGA_VCCO_HSPEED_4/NF_2/ VCC2.5	VCC2.5 - CDP 1 CND HOUSE TO SEAMON HSPEED 100NF 7	BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_11	RYPASS CAP 25 FPGA VCCO HSPEED 470NF 12	BYPASS_CAP_33_25_REGULATIO	N_IN_0 BYPASS_CAP_BK01_FPGA_VCCO_B	ULK_47UF_0	
H	BYPASS_CAP_15	5_FPGA_VCCINT_HSPEED_47NF_9	BYPASS_CAP_25_ZBT_SRAMO HSPEED_100NF_6	BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_10 VCC0_BAN01 = 1	VCC2.5	BYPASS CAP 25 FPGA VCCO BUIL	K_4UF7_8 BYPASS_CAP_25_FPGA_VCCAUX_BI	JLK_47UF_0	\vdash
	BYPASS_CAP_2	5_FPGA_VCCO_HSPEED_47NF_9 VCC1.5	BYPASS_CAP_25_ZBT_SRAMO_HSPEED_100NF_5	BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_9	BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_11 WCC2.5	BYPASS_CAP_25_FPGA_VCCO_BUL	K_4UF7_7 BYPASS_CAP_15_FPGA_VČČINT_BU VCC1_5 - OND OND	LK_47UF_1	
	BYPASS_CAP_2	5_FPGA_VCCO_HSPEED_47NF_24 VCC2_5GND	BYPASS_CAP_25_ZBT_SRAMO_HSPEED_100NF_4	BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_9 WCC0_BMX01	BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_9	BYPASS CAP 25 FPGA VCCO BUL	K_4UF7_6 BYPASS_CAP_15_FPGA_VCCINT_BU VCC_5 - GND VCC_5 - GND K_4UF7_5 BYPASS_CAP_18_18_REGULATION	V_OUT1_0	
	BYPASS_CAP_2	5_FPGA_VCCO_HSPEED_47NF_23 VCC2_5GND	BYPASS_CAP_25_ZBT_SRAMO_HSPEED_100NF_3 VCC2_5 - GND GND	7 og	VCC2.5	BYPASS CAP 25 EPGA VCCO BUIL	VIT1_8MGT_G	NO COUT1_0	
	BYPASS_CAP_2	S_FPGA_VCCO_HSPEED_47NF_22 VCC2_5GND	BYPASS_CAP_25_ZBT_SRAMO_HSPEED_100NF_2 VCC2_5 - GND	BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_7 VCCO_BANK01	BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_7 VCC2_5GND	BYPASS CAP 25 FPGA VCCO BUIL	K_4UF7_4 BYPASS_CAP_25_25_REĞÜLATION VCD2.5	ND LK_47UF_3	
	BYPASS_CAP_2	5_FPGA_VCCO_HSPEED_47NF_21 VCC2_5	BYPASS_CAP_25_ZBT_SRAMO_HSPEED_100NF_1	BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_6 WCCO_BMW01	BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_6 VCC2.5	BYPASS_CAP_25_FPGA_VCCO_BUL BYPASS_CAP_25_FPGA_VCCO_BUL BYPASS_CAP_25_FPGA_VCCO_BUL	K_4UF7_3 BYPASS_CAP_25_FPGA_VÖCO_BU VOC2.5	LK_47UF_2	
A	DVDACC CAR O	5 FPGA VCCO HSPEED 47NF 19	BYPASS_CAP_25_ZBT_SRAMO_HSPEED_100NF_0 VCC2.5PAND CAP_0402_INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M_TS_3	BYPASS_CAP_BK01_FPGA_VČČCO_HSPEED_47NF_5 VCCO_BAN001 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1	BYPASS CAP 25 FPGA VCCO HSPEED 470NF 5 VCC2.5		K_4UF7_2 BYPASS_CAP_25_FPGA_VCCO_BU VCC2.5	LK_47UF_1	A
			CAP_0402_INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M_TS_3 RX_M_INFINIBAND_1_RX_M-SSINFINIBAND_1_RX_M-SS	VCCO_BANK01 GND	BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_4 VCC2.5GND BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_3	BYPASS_CAP_25_FPGA_VCCO_BUL	K_4UF7_0 BYPASS_CAP_25_FPGA_VCCO_BU	LK_47UF_0	
	BYPASS_CAP_2	VCC2_5 GND INFINIBAND_CON_1_	CAP_0402_INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M_TS_2 RX_MUJHSNIBAND_1_RX_M_CS CAP_0402_INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M_TS_1 PARTICIPATION AND ADMINISTRATION ADMINISTRATION ADMINISTRATION ADMINISTRATION ADMINISTRATION ADMINISTRATION ADMINISTRATION ADMINISTRATION ADMINISTRATION ADMINISTRA	BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_3 vcco_bww01 =	BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_3 VC2.5GNO BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_2				
	BYPASS_CAP_2	VUZ_5 - GND INFINIBAND_CON_1 5_FPGA_VCCO_HSPEED_47NF_16	CAP_0402_INFINIBAND_CON_1_RX_M_INFINIBAND_1_RX_M_TS_1 RX_M_NFINIBAND_1_RX_M-ts	BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_1	BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_2 VCC2.5		CHEN CHANG EECS UC BERKELEY	CAPS	
	BYPASS_CAP_15	5_FPGA_VCCINT_HSPEED_47NF_8 VCC1_5GND INFINIBAND_CON_1	CAP_0402_INFINIBAND_CON_1_RX_P_INFINIBAND_1_RX_P_TS_3	BYPASS_CAP_BK01_FPGA_VCCO_HSPEED_47NF_0	BYPASS_CAP_25_FPGA_VCCO_HSPEED_470NF_0		BEE2 GROUP BERKELEY WIRELESS RESEARCH CENTER	BEE2 DIC BOARD	
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D	PULLUP_F FROA_GYGMODE-S PULLUP_F FROA_GYGMODE-S RES_0603_DON DONE_LED_A_VCCZ_S PULLUS JY7A_TDC PULL REV PULL REV PULL PEC PULL PEC PULL PEC PULLUT PEC PULL PEC PULL PEC PULLUT	PGA_CFGMODE_0_1						D
С	RES_0603_FPGA PPGA_UPIED_9_C_0M0 RES_0603_FPGA	CPLED 3. C. GND_TS_0		IND_1812_RS232_IF_LX_VCC2_5_TD_0 RS232_IF_LX FILTER_IND_MG6_GND_0 GND				C
В	MET.BOTTOM, OSCILOR PULLLUP_MC MGT_NOP_OSCILOR PULLUP_MC MGT_TOP_OSCILOR MGT_TOP_OSCILOR RES_0803_MGT_REGULA MGT_REGULATOR_SENSE RES_0803_MGT_REGULA MGT_REGULATOR_SENSE LVDS_TERM_ MGT_REGULATOR_SENSE LVDS_TERM_ MGT_ROTTOM_CAL_P LVDS_TERM_ MGT_NOP_CAL_P RES_0803_FPCA_PPSCA_VPB_BCV RES_0803_FPCA_ RFSCA_VPB_BCV		RES_0603_VCC5_LED ¹ _A_VCC5_TS_0 VOS_LED_A_VCC5	FILTER_IND_MGT_VTTX_4 VTTX_6 FILTER_IND_MGT_VTTX_3 VTTX_6 FILTER_IND_MGT_VTTX_2 VTTX_6 FILTER_IND_MGT_VTTX_1 VTTX_1 VTTX_1 VTTX_1 VTTX_1 VTTX_1 VTTX_1 FILTER_IND_MGT_VTTX_0 VTTX_6 FILTER_IND_MGT_VTTX_0 FILTER_IND_MGT_VTTX_6 FILTER_IND_MGT_VTX_6 ACCALIBROS_5 FILTER_IND_MGT_AVCCALUXTX_7 ACCALIBROS_6 ACCALIBROS_6 FILTER_IND_MGT_AVCCALUXTX_6 ACCALIBROS_6 FILTER_IND_MGT_AVCCALUXTX_5 ACCALIBROS_6 FILTER_IND_MGT_AVCCALUXTX_5 ACCALURX_6 ACCALUR				В
A	RES_0603_FPGA_PPGA_VRP_BMA RES_0603_FPGA_VRP_BMG RES_0603_FPGA_VRP_BMG RES_0603_FPGA_VRP_BMG RES_0603_FPGA_VRP_BMG RES_0603_FPGA_VRP_BMG RES_0603_FPGA_PPGA_VRP_BMG RES_0603_FPGA_PPGA_VRP_BMG RES_0603_FPGA_PPGA_VRP_BMG RES_0603_FPGA_PPGA_VRP_BMG RES_0603_FPGA_VRP_BMG	A VRP_BK8_GND_TD_0	PULLUP_PUSHBUTTONS_0_0 PUSHBUTTONS_1	FILTER_IND_MGT_AVCCAUXTX_4 AVCAUXTX45 FILTER_IND_MGT_AVCCAUXTX_2 AVCAUXTX45 FILTER_IND_MGT_AVCCAUXTX_1 AVCAUXTX45 FILTER_IND_MGT_AVCCAUXTX_7 AVCAUXTX45 FILTER_IND_MGT_AVCCAUXTX_7 AVCAUXTX45 FILTER_IND_MGT_AVCCAUXTX_6 AVCAUXTX45 FILTER_IND_MGT_AVCCAUXTX_7 AVCAUXTX45 FILTER_IND_MGT_AVCAUXTX_7 AVCAUXTX45 FILTER_IND_MGT_AVCA			CHEN CHANG EECS UC BERKELEY BEE2 GROUP PRINCELES RESEARCH CENTER 210: ALISTON WAY BERKELEY, CA-48704-1302 HTTP://BWRC.EECS.BERKELEY.EDU	MISC BEE2 DIC BOARD SIZE SHEET 4 0F 4
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