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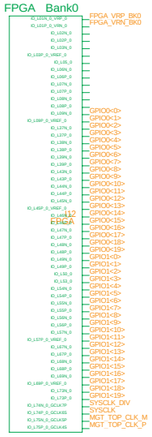
D C B A

FPGA Bank0



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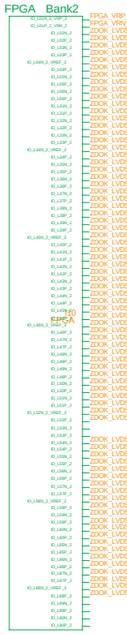
FPGA Bank2



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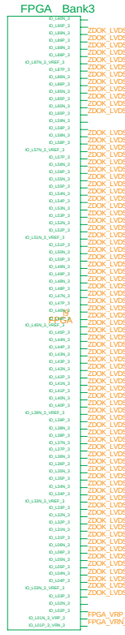

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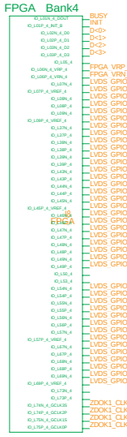

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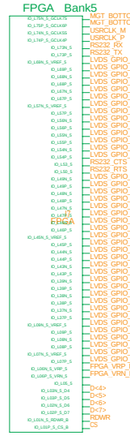

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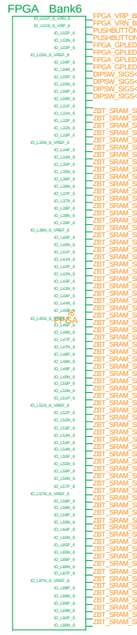

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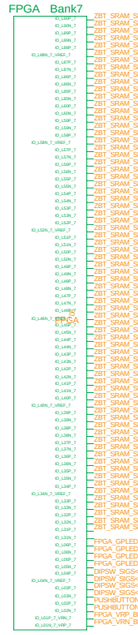
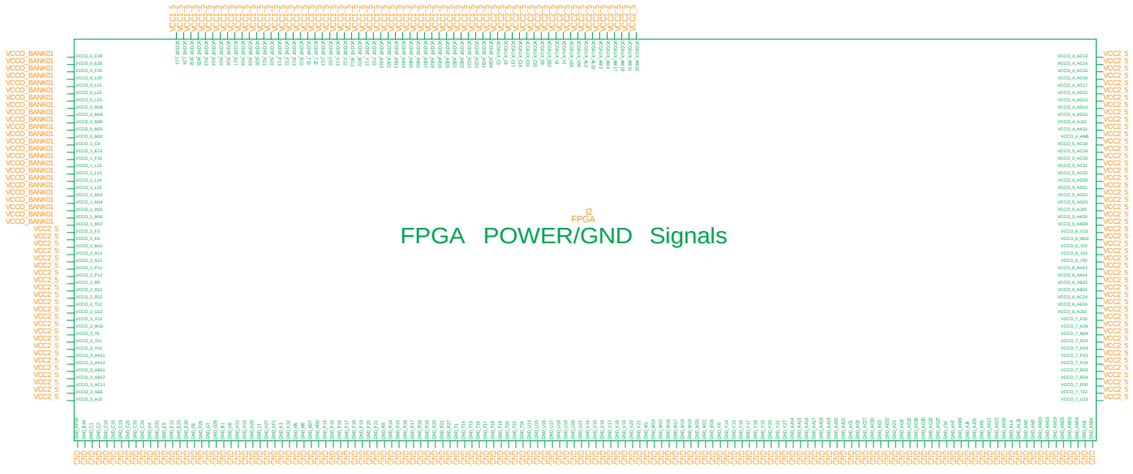
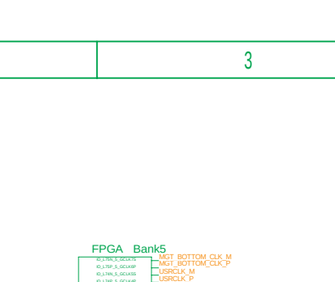
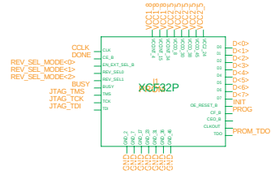
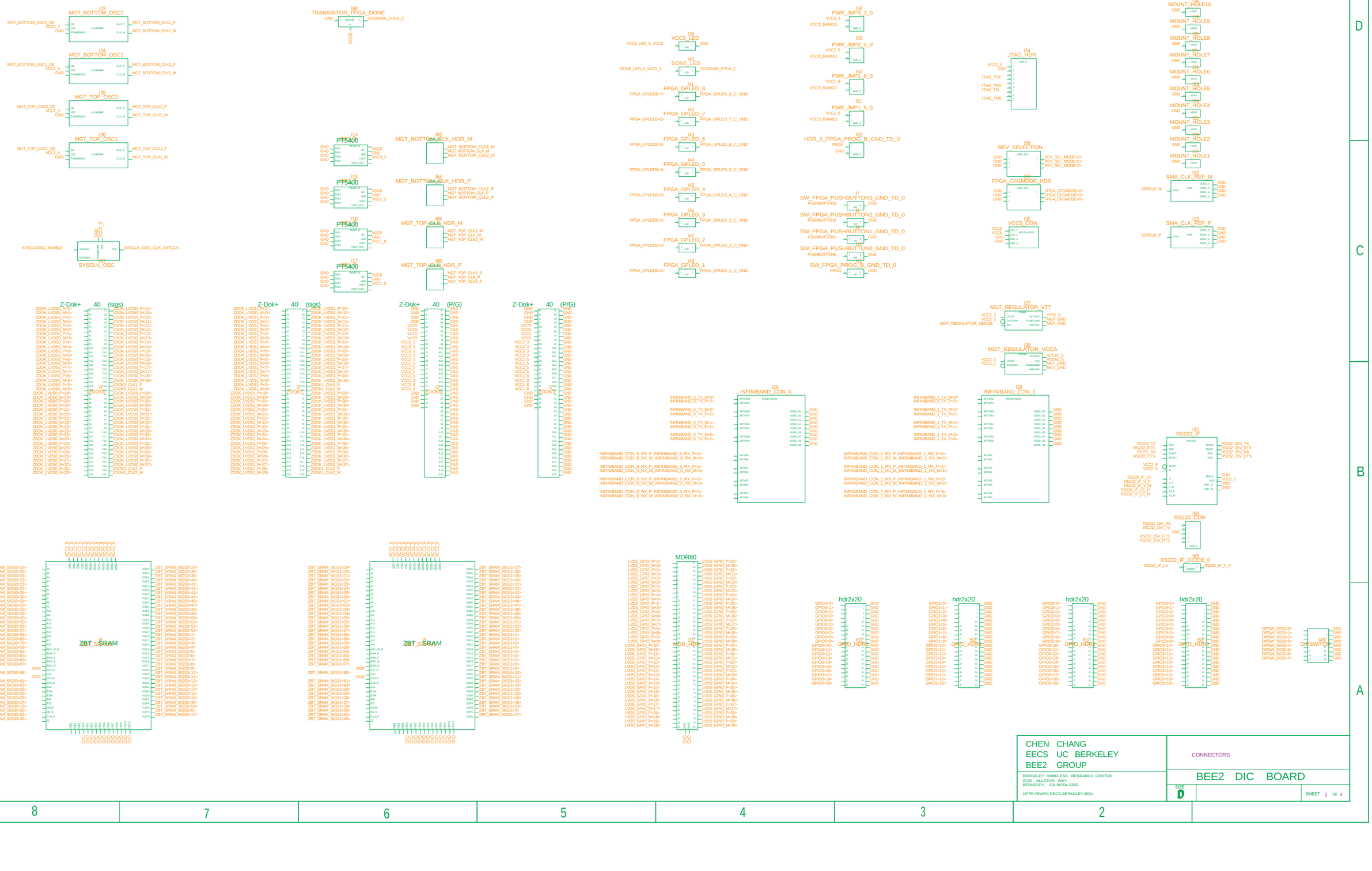








CHEN CHANG EECS UC BERKELEY BEE2 GROUP BERKELEY WIRELESS RESEARCH CENTER 2108 ALLSTON WAY BERKELEY, CA-94704-1302 HTTP://BWRC.EECS.BERKELEY.EDU	FPGA BEE2 DIC BOARD	SIZE D SHEET 1 OF 4



8	7	6	5	4	3	2	1	

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2108 ALLSTON WAY
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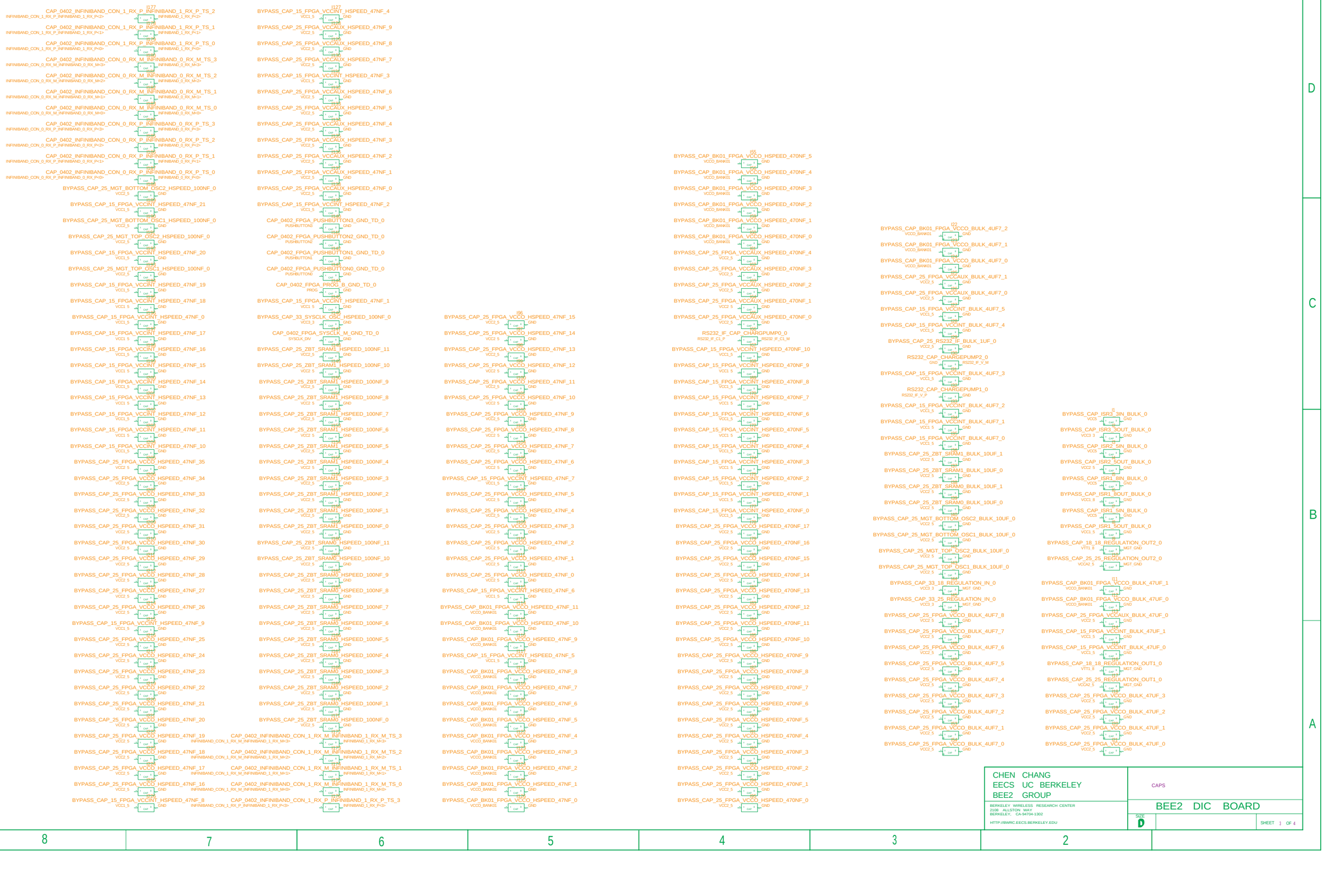
CONNECTORS

BEE2 DIC BOARD

SIZE D

SHEET 2 OF 4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D
C
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A
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CAPS
BEE2 DIC BOARD
SIZE
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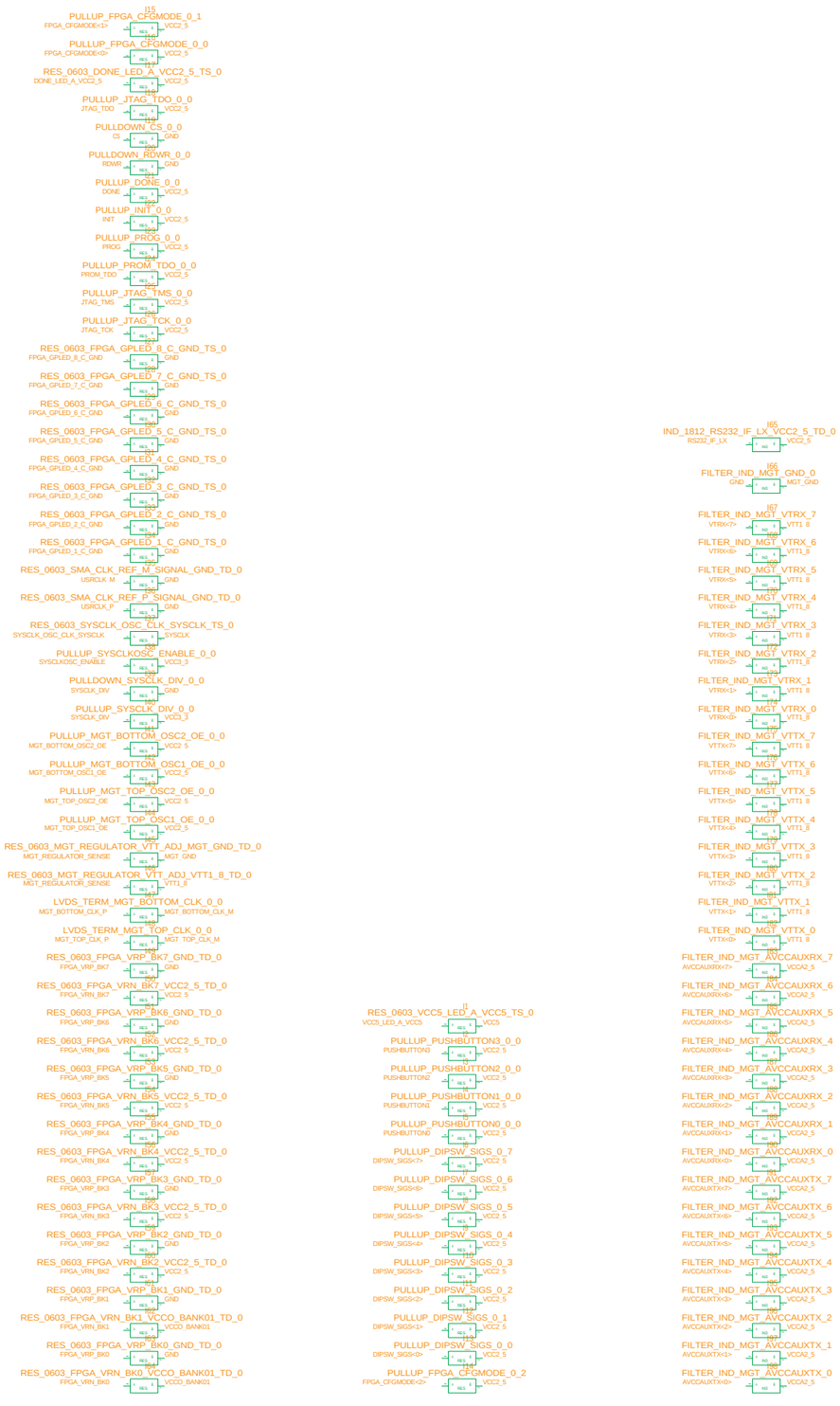
SHEET 3 OF 4



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	SIZE D	SHEET 4 OF 4