CMPEN 270: Digital Design: Theory and Practice

Module 6 Lab: Combinational Building Blocks Due: 2/18/2024

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Grading Rubric

Initial grade, based on how well the functional specification is met Excellent (exceptional achievement) 90-100% Good (extensive achievement) 80-89% Satisfactory (acceptable achievement) 72-79% Poor (minimal achievement) 65 to 71% Failure (inadequate achievement) 0-64% Modification for design documents Block diagrams State diagrams State tables Other Modification for coding style, comments, efficiency Header comments for files Other comments (informative but not excessive) Proper code indenting, alignment, use of whitespace Code is clean (doesn't have commented out code without a good reason) Self documenting code (good signal and component names, clear structure, etc.) General approach (algorithms) Coding details (operations) Proper use of components VHDL matches design documents	/25
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Other	
Modification for sections in this report	
Design	
Verification	
Evaluation	
Questions	
Other	
Bonus (optional challenge, etc.)	
Penalties	
No grade until all deliverables are submitted, late submission penalty for anything submitted late	
Late submission: (<1 day) -10%, (<1 week) -30%, (<2 weeks) -50%, (>=2 weeks) -99%	
Attachments missing, not in order, instructions not followed: -10%	
Other	
TOTAL (Max is 100% of total points unless specified otherwise in handout)	/ 25
101712 (1914) 15 100 /0 Of total points unless specified otherwise in handout)	1 43

ACKNOWLEDGEMENT

This work is entirely my	own and I did not provide any assistance except as noted.
100% Rocco Leporace	

ATTACHMENTS

The following are attached, in this order:

There are no attachments required for the report. Be sure to submit all files needed to recreate and test your design (all VHDL files, Tcl test files, and the XDC file). Also be sure to submit your demo video or pictures.

DESIGN

There was no design for this lab.

VERIFICATION

For this lab, I frequently switched between the circuits that were given, and the VHDL files that were given in order to create the new VHDL files. I also simulated the files and ran the scripts that were given in order to see if I got the right output. If I received an error, I would go back and fix it, and if not, I would move on.

EVALUATION

No performance metrics are required for this lab.

QUESTIONS

There are no questions for this lab.