CMPEN 270: Digital Design: Theory and Practice

Module 7 Lab: Introduction to Sequential Logic Circuits
Due: 2/25/2024

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Grading Rubric

Criteria	Grade
Initial grade, based on how well the functional specification is met Excellent (exceptional achievement) 90-100% Good (extensive achievement) 80-89% Satisfactory (acceptable achievement) 72-79% Poor (minimal achievement) 65 to 71% Failure (inadequate achievement) 0-64%	/ 35
Modification for design documents Block diagrams State diagrams State tables Other	
Modification for coding style, comments, efficiency Header comments for files Other comments (informative but not excessive) Proper code indenting, alignment, use of whitespace Code is clean (doesn't have commented out code without a good reason) Self documenting code (good signal and component names, clear structure, etc.) General approach (algorithms) Coding details (operations) Proper use of components VHDL matches design documents Other	
Modification for sections in this report Design Verification Evaluation Questions Other	
Bonus (optional challenge, etc.)	
Penalties No grade until all deliverables are submitted, late submission penalty for anything submitted late Late submission: (<1 day) -10%, (<1 week) -30%, (<2 weeks) -50%, (>=2 weeks) -99% Attachments missing, not in order, instructions not followed: -10% Other	
TOTAL (Max is 100% of total points unless specified otherwise in handout)	/ 35

ACKNOWLEDGEMENT

This work is entirely my own and I did not provide any assistance except as noted.

100% Rocco Leporace _____

ATTACHMENTS

The following are attached, in this order:

- Circuit implementation for DFF_EN_RESET
- Circuit implementation for Reg_LOAD_CLR_4bit
- Verification worksheet

Be sure to submit all files needed to recreate and test your design (all VHDL files, Tcl test files, and the XDC file). Also be sure to submit your demo video or pictures.

DESIGN

See attached drawings for D flip-flop and register circuit implementations.

VERIFICATION

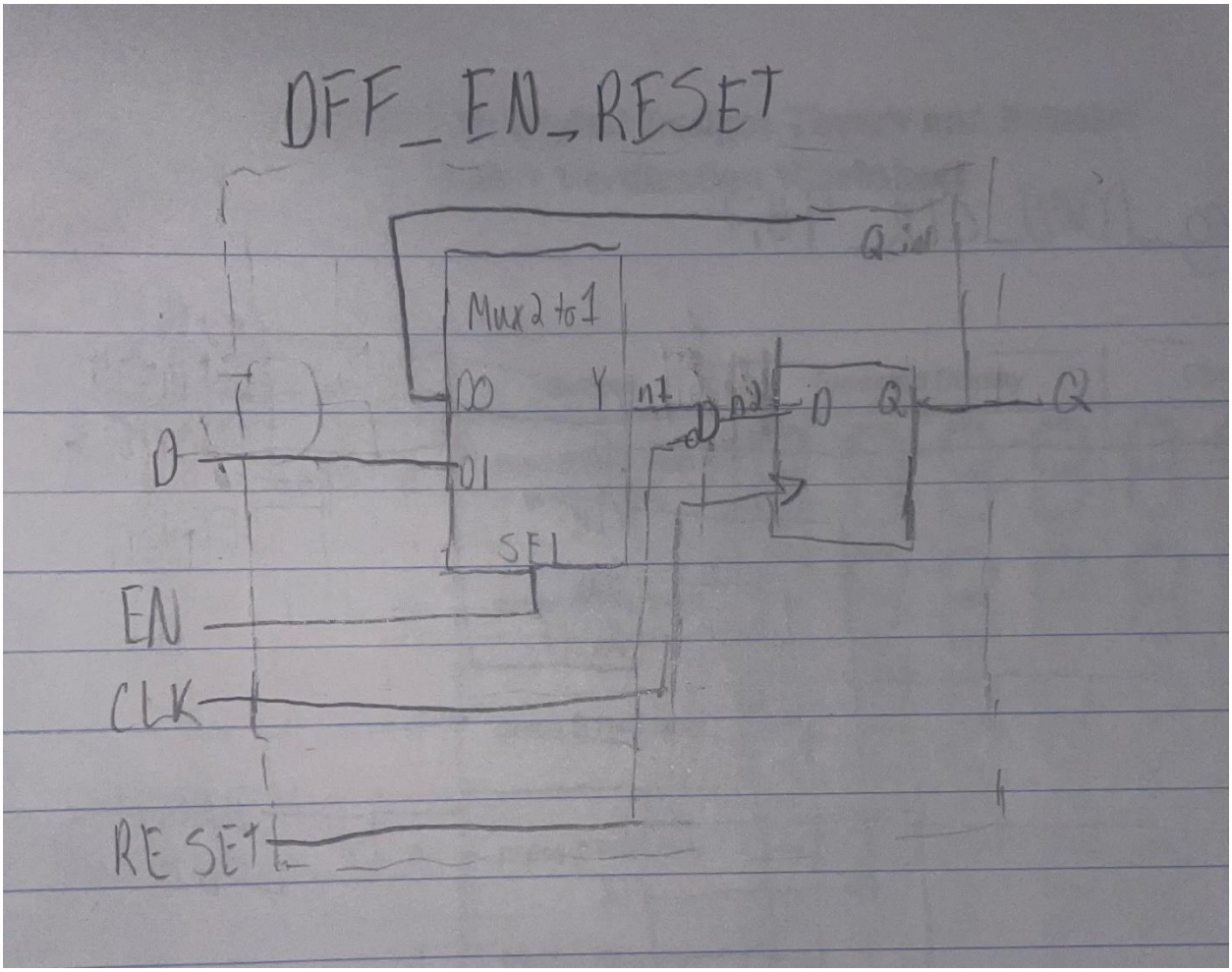
For this lab, I followed the components file that was given in order to properly set up the vhl files. I would then run the tcl scripts in order to see if there were any errors. If there were errors, I would fix the mistake. If not, I would continue to the next step.

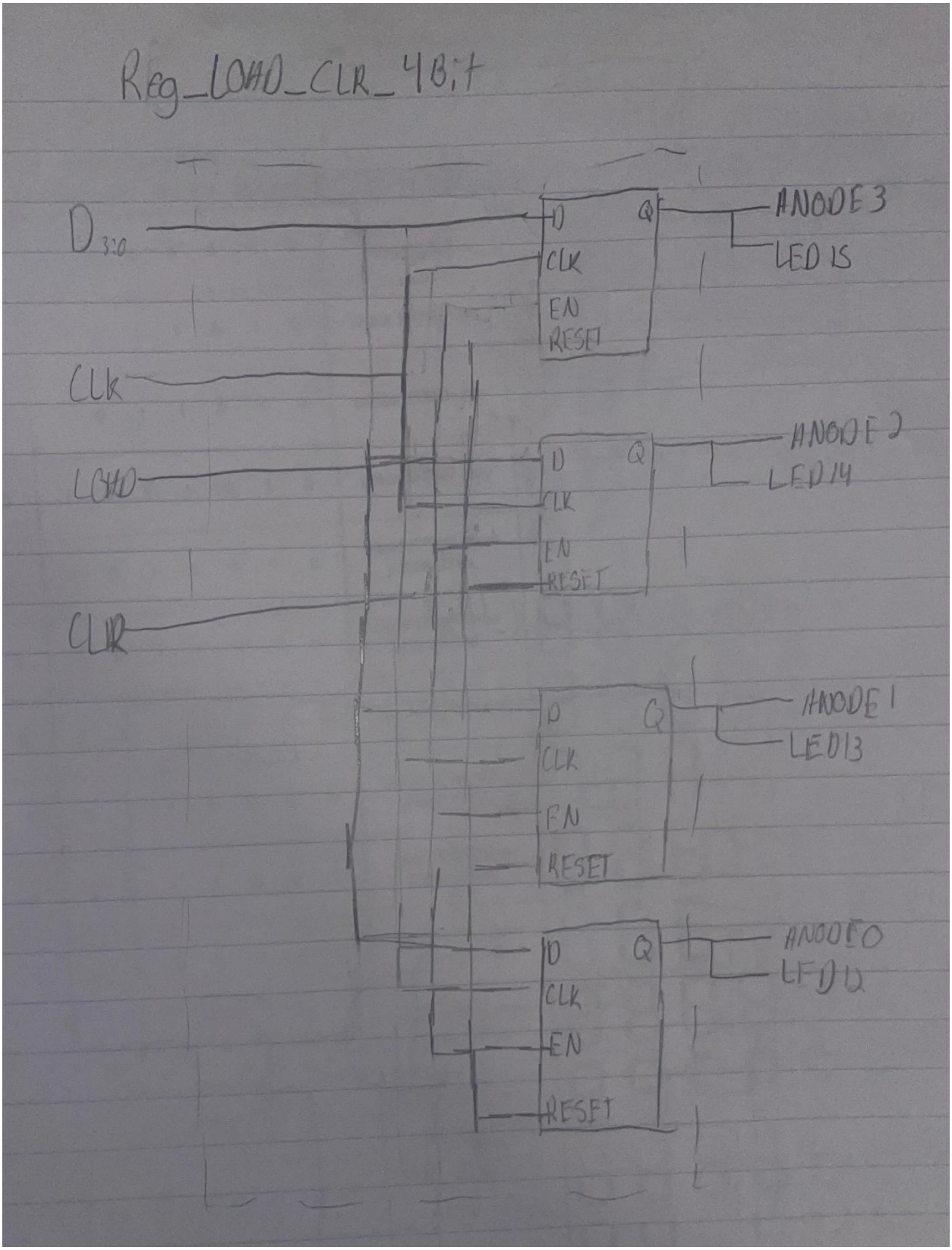
EVALUATION

No performance metrics are required for this lab.

QUESTIONS

There are no questions for this lab.


DFF_EN_RESET
Qin
Mux2to1
D0
Y
n1
n2
D
Q
Q
D
D1
SEL
EN
CLK
RESET


Reg_LOAD_CLR_4Bit
D3:0
CLK
LOAD
CLR
D
Q
CLK
EN
RESET
ANODE3
LED15
ANODE2
LED14
ANODE1
LED13
ANODE0
LED12

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Lab 7 Verification Worksheet

Anodes ($SWITCH_{15:12}$) SW_{15} SW_{14} SW_{13} SW_{12}	Segments ($SWITCH_{11:5}$) SW_{11} SW_{10} SW_9 SW_8 SW_7 SW_6 SW_5	Buttons	Expected Display	Observed Display
0 0 0 0	0 0 0 0 0 0 0	Hold BTNC then press BTNL		
0 0 0 0	1 0 1 1 0 1 0	press BTNL only		
0 0 0 0	1 0 1 1 0 1 0	press BTNC only		
0 0 0 0	1 0 1 1 0 1 0	press BTNR only		
0 0 0 0	1 0 1 1 0 1 0	Hold BTNC then press BTNL		
0 0 0 0	1 0 1 1 0 1 0	Hold BTNR then press BTNL		
0 0 0 0	1 1 1 1 0 0 0	press BTNL only		
0 0 0 0	1 1 1 1 0 0 0	Hold BTNC then press BTNL		
0 0 0 0	1 1 1 1 0 0 0	Hold BTNR then press BTNL		
1 0 0 1	1 0 0 0 1 1 0	Hold BTNC then press BTNL		
1 0 0 1	1 0 0 0 1 1 0	Hold BTNR then press BTNL		
0 0 0 0	0 0 1 1 1 0 0	Hold BTNC press BTNL		
0 0 0 0	b'1 0 0 0 1 1'	Hold BTNC press BTNL		
0 0 1 1	0 0 1 0 1 0 1	Hold BTNC press BTNL		
1 1 0 0	1 0 1 0 0 1 0	Hold BTNC press BTNL		
1 0 1 0	0 1 1 0 1 1 0	Hold BTNC press BTNL