DesignWare Cores PCI Express Controller

Release Notes

Version 6.00a
June 2022

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Release Notes: 6.00a

These release notes describe the changes in this release *(6.00a)* relative to the previous production release *(5.97a)*.This release note contains the following sections:

- "Changes from the Last Release" on page 6
- "Converting to the Current Release" on page 78
- "Fixed Defects and Enhancements (STARs on the Web)" on page 79
- "Known Issues and Limitations" on page 80
- "Synopsys Statement on Inclusivity and Diversity" on page 83
- "Web Resources" on page 82
- "Customer Support" on page 84

1.1 Changes from the Last Release

This release contains the following major updates and other minor updates (indicated in "Fixed Defects and Enhancements (STARs on the Web)" on page 79).

Note

- In this release, CXL controller is available as an EA feature.
- IDE configurations (`CX_IDE_ENABLE =1`) have been verified with an internal Synopsys VIP version. This VIP version might not correspond with your VIP version. For more information, contact Synopsys support through SolvNetPlus.

1.1.1 CXL 3.0 Early Access Features

The controller now supports the *Compute Express link Specification Revision 3.0, Version 0.7* with the following qualifications: (This is for evaluation purpose only).

Table 1-1 CXL 3.0 Specification Compliance

Feature	Description
Link Width Support	x4 and x8 only
CXS Interface	Supported
Native Interface	Not Supported
256B Standard Flit	Supported
256B Latency Optimized Flit	Not Supported
APN Negotiation for Flit Mode	Not Supported
IDE	Not Supported

This release of CXL 3.0 controller requires connection to PCIe 6.0 PHY through built in PIPE6 interface.

1.1.2 CXL Documentation Updates

The CXL Databook covers the following updates:

- A dedicated 'Receive Queues' section in the *CXL Databook*, that explains the RADM queue bypass mode for posted TLP's
- Limitation stating that L1 substate and P1.CPM are not supported in CXL mode.

For more information, see *CXL Databook*.

1.1.3 PCIe Gen6 Features

The controller now supports the *PCI Express Base Specification, Revision 6.0, Version 1.0*.

For more information on the features, see "Features and Limitations" section in the "Product Overview" chapter of the *Databook*.

This is for evaluation purpose only.

1.1.4 T-bit Updates for Native PCIe Controller

In this enhancement, the PCIe IDE allows the application to drive the T-bit value for each transmitted TLP. T-bit is not supported in AXI configurations.

For more information, see “Signal Descriptions” chapter of the *Reference Manual*.

1.1.5 BSA1.0 / SBSA 7 Interrupt Compliance

In this enhancement, the controller supports the generation of MSI from internal interrupts on Order buffer configurations when `CC_SII2MSI_EN` parameter is set to '1'. The MSIs are delivered through the MSI-GIC interface (or AXI if MSI-GIC is not present).

Note In this release, the BSA1.0 / SBSA 7 Interrupt Compliance is available as an EA (Early Adopter) feature and must not be used for tape out. Contact Synopsys Support through SolvNetPlus for an unlocking key for this feature.

1.1.6 Physical Functions Configuration Updates

In this enhancement, the coreConsultant allows independent configuration of the first nine Physical Functions (from PF0 to PF8), whereas any Physical Function from PF9 and above uses the same configuration parameters as PF8. There is no change in the hardware structure of the Physical Functions, they retain independent registers that can be independently configured at runtime. The controller supports up to 129 PFs.

For more information, see `CX_NFUNC` parameter in the “Parameter Descriptions” chapter of the *Reference Manual*.

1.1.7 HDMA 10-bit TAG Support

In this enhancement, the HDMA supports 10-bit Tag.

Note In this release, the HDMA 10-bit TAG Support is available as an EA (Early Adopter) feature and must not be used for tape out. Contact Synopsys Support through SolvNetPlus for an unlocking key for this feature.

1.1.8 Changes to I/O

This section details any changes to the I/O of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the I/O are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

The following table enlists the I/O changes that have occurred for all configurations:

Table 1-2 I/O Signals Added, Removed, or Renamed

Name	Type	Change	Comment
cxsrxlast	I	Registered	Registered is changed **From:** Yes **To:** CX_CXS_RX_INPUT_REG ? "Yes" : "No"
ide_msg_grant	O	Exists condition	The exists condition is changed **From:** (CX_IDE_ENABLE) && (!(CX_IDE_ENABLE) && (CC_DEVICE_TYPE==CC_SW)) **To:** (CX_IDE_ENABLE) && !CX_SW_PASS_IDE_TLP_WITH_MAC_SUPPORTED
ide_msg_req	I		
ide_msg_sync_fail	I		
ide_msg_selec_link	I		
ide_msg_tc[2:0]	I		
ide_msg_th	I		
ide_msg_td	I		
ide_msg_ep	I		
ide_msg_func_num[7:0]	I		
ide_msg_dst_rid[15:0]	I		

Name	Type	Change	Comment
ide_msg_stream_id[7:0]	O	Exists condition	The exists condition is changed **From:** (CX_IDE_ENABLE) && (!(CX_IDE_ENABLE) && (CC_DEVICE_TYPE==CC_SW)) **To:** (CX_IDE_ENABLE) && !CX_SW_PASS_IDE_TLP_WITH_MAC_SUPPORTED
pcie_ide_tx_prefix[((IDE_NPKTS_TX*IDE_PRFX_W_PROT)-1):0]	O		
pcie_ide_tx_local_prefix_size[((IDE_NPKTS_TX*clog2((NW_PRFX+1)))-1):0]	O		
pcie_ide_tx_e2e_prefix_size[((IDE_NPKTS_TX*clog2((NW_PRFX+1)))-1):0]	O		
pcie_ide_tx_hdr[((IDE_NPKTS_TX*IDE_HDR_W_PROT)-1):0]	O		
pcie_ide_tx_hdr_size[((IDE_NPKTS_TX*IDE_HDR_NW_WD)-1):0]	O		
pcie_ide_tx_data[((IDE_NPKTS_TX*IDE_DATA_W_PROT)-1):0]	O		
pcie_ide_tx_data_size[((IDE_NPKTS_TX*clog2((NW+1)))-1):0]	O		
pcie_ide_tx_sop[(IDE_NPKTS_TX-1):0]	O		
pcie_ide_tx_eop[(IDE_NPKTS_TX-1):0]	O		
pcie_ide_tx_control[((IDE_NPKTS_TX*IDE_CTRLW_TX)-1):0]	O		
pcie_ide_tx_dllp_error[(IDE_NPKTS_TX-1):0]	O		
ide_pcie_tx_halt	I		
ide_pcie_tx_prefix[((IDE_NPKTS_TX*IDE_PRFX_W_PROT)-1):0]	I		
ide_pcie_tx_hdr[((IDE_NPKTS_TX*IDE_HDR_W_PROT)-1):0]	I		
ide_pcie_tx_data[((IDE_NPKTS_TX*IDE_DATA_W_PROT)-1):0]	I		
ide_pcie_tx_data_size[((IDE_NPKTS_TX*clog2((NW+1)))-1):0]	I		
ide_pcie_tx_sop[(IDE_NPKTS_TX-1):0]	I		
ide_pcie_tx_eop[(IDE_NPKTS_TX-1):0]	I		
ide_pcie_tx_control[((IDE_NPKTS_TX*IDE_CTRLW_TX)-1):0]	I		
ide_pcie_tx_discard[(IDE_NPKTS_TX-1):0]	I		

Name	Type	Change	Comment
ide_pcie_tx_dllp_error[(IDE_NPKTS_TX-1):0]	I	Exists condition	The exists condition is changed **From:** (CX_IDE_ENABLE) && (!(CX_IDE_ENABLE) && (CC_DEVICE_TYPE==CC_SW)) **To:** (CX_IDE_ENABLE) && !CX_SW_PASS_IDE_TLP_WITH_MAC_SUPPORTED
pcie_ide_tx_halt	O		
pcie_ide_rx_prefix[((IDE_NPKTS_RX*IDE_PRFX_W_PROT)-1):0]	O		
pcie_ide_rx_local_prefix_size[((IDE_NPKTS_RX*clog2((NW_PRFX+1)))-1):0]	O		
pcie_ide_rx_e2e_prefix_size[((IDE_NPKTS_RX*clog2((NW_PRFX+1)))-1):0]	O		
pcie_ide_rx_hdr[((IDE_NPKTS_RX*IDE_HDR_W_PROT)-1):0]	O		
pcie_ide_rx_hdr_size[((IDE_NPKTS_RX*IDE_HDR_NW_WD)-1):0]	O		
pcie_ide_rx_data[((IDE_NPKTS_RX*IDE_DATA_W_PROT)-1):0]	O		
pcie_ide_rx_data_size[((IDE_NPKTS_RX*clog2((NW+1)))-1):0]	O		
pcie_ide_rx_pcrc_mac[((IDE_NPKTS_RX*IDE_PCRC_MAC_W_PROT)-1):0]	O		
pcie_ide_rx_pcrc_mac_size[((IDE_NPKTS_RX*3)-1):0]	O		
pcie_ide_rx_sop[(IDE_NPKTS_RX-1):0]	O		
pcie_ide_rx_eop[(IDE_NPKTS_RX-1):0]	O		
pcie_ide_rx_control[((IDE_NPKTS_RX*IDE_CTRLW_RX)-1):0]	O		
pcie_ide_rx_order	O		
pcie_ide_rx_dllp_error[(IDE_NPKTS_RX-1):0]	O		
ide_pcie_rx_halt	I		
ide_pcie_rx_prefix[((IDE_NPKTS_RX*IDE_PRFX_W_PROT)-1):0]	I		
ide_pcie_rx_hdr[((IDE_NPKTS_RX*IDE_HDR_W_PROT)-1):0]	I		
ide_pcie_rx_data[((IDE_NPKTS_RX*IDE_DATA_W_PROT)-1):0]	I		
ide_pcie_rx_data_size[((IDE_NPKTS_RX*clog2((NW+1)))-1):0]	I		

Name	Type	Change	Comment
ide_pcie_rx_sop[(IDE_NPKTS_RX-1):0]	I	Exists condition	The exists condition is changed **From:** (CX_IDE_ENABLE) && (!(CX_IDE_ENABLE) && (CC_DEVICE_TYPE==CC_SW)) **To:** (CX_IDE_ENABLE) && !CX_SW_PASS_IDE_TLP_WITH_MAC_SUPPORTED
ide_pcie_rx_eop[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_control[((IDE_NPKTS_RX*IDE_CTRLW_RX)-1):0]	I		
ide_pcie_rx_ide_check_failed[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_pcrc_check_failed[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_misrouted_ide_tlp[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_report_ide_check_faild[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_dllp_error[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_order	I		
pcie_ide_rx_halt	O		
ide_cfg_device_type[2:0]	O		
ide_cfg_cs	O		
ide_cfg_wr_en[3:0]	O		
ide_cfg_addr[9:0]	O		
ide_cfg_wdata[31:0]	O		
ide_cfg_from_wire	O		
ide_cfg_rdata[31:0]	I		
ide_cfg_ack	I		
ide_cfg_ro_wr_en	O		
ide_pcie_tx_dp_unc_err	I		
ide_pcie_rx_dp_unc_err	I		

Name	Type	Change	Comment
ide_pcie_tx_dp_cor_err	I	Exists condition	The exists condition is changed **From:** (CX_IDE_ENABLE) && (!(CX_IDE_ENABLE) && (CC_DEVICE_TYPE==CC_SW)) **To:** (CX_IDE_ENABLE) && !CX_SW_PASS_IDE_TLP_WITH_MAC_SUPPORTED
ide_pcie_rx_dp_cor_err			
ide_pcie_tx_pcrc[((IDE_NPKTS_TX*IDE_PCRC_W_PROT)-1):0]	I		The exists condition is changed **From:** (CX_IDE_ENABLE) && (!((CX_IDE_ENABLE) && (CC_DEVICE_TYPE==CC_SW)) && (CX_IDE_DEDICATED_BUS_PCRC) **To:** (CX_IDE_ENABLE) && !CX_SW_PASS_IDE_TLP_WITH_MAC_SUPPORTED)&& (CX_IDE_DEDICATED_BUS_PCRC)
ide_pcie_tx_merge_pcrc[(IDE_NPKTS_TX-1):0]	I		
ide_pcie_tx_mac[((IDE_NPKTS_TX*IDE_MAC_W_PROT)-1):0]	I		The exists condition is changed **From:** (CX_IDE_ENABLE) && (!((CX_IDE_ENABLE) && (CC_DEVICE_TYPE==CC_SW)) && (CX_IDE_DEDICATED_BUS_MAC) **To:** (CX_IDE_ENABLE) && !CX_SW_PASS_IDE_TLP_WITH_MAC_SUPPORTED)&& (CX_IDE_DEDICATED_BUS_MAC)

Documentation Changes

A number of signals were incorrectly described in the *Databook*. These are also highlighted in the change-tracked version of the *Reference Manual*. These are *not* RTL changes.

The following table enlists the I/O changes that have occurred for all configurations:

Table 1-3 Documentation Changes (Non-RTL)

Name	Type	Change	Comment
For many signals **Synchronous To** is corrected. These corrections are indicated in the change-tracked version of the Databook PDF which can be found at the location identified in the Databook revision history.			

1.1.9 Changes to Software View (Register Map)

This section discusses changes to the register map of the controller that have occurred in this release.

- It lists renamed registers.
- It lists deleted registers.
- It does *not* list new registers.
- *All* changes to the software map are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

The following changes have occurred for all configurations.

Table 1-4 Register Deletions/Renaming

Register	Nature of Change
No changes in this release.	

Documentation Changes

A number of registers were incorrectly described in the IP-XACT XML, DocBook XML, RAL files, header files, and *Register Descriptions* PDF. These are also highlighted in the change-tracked version of the *Reference Manual* PDF. These are *not* RTL changes.

Table 1-5 Documentation Changes (Non-RTL)

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
BAR0_MASK_REG	PCI_TYPE0_BAR0_MASK		Y		
BAR1_MASK_REG	PCI_TYPE0_BAR1_MASK		Y		
BAR2_MASK_REG	PCI_TYPE0_BAR2_MASK		Y		
BAR3_MASK_REG	PCI_TYPE0_BAR3_MASK		Y		
BAR4_MASK_REG	PCI_TYPE0_BAR4_MASK		Y		
BAR5_MASK_REG	PCI_TYPE0_BAR5_MASK		Y		
VPD_BASE	VPD_PCIE_EXTENDED_CAP_ID				Y
	VPD_NEXT_OFFSET				Y
	VPD_ADDRESS				Y
	VPD_FLAG				Y
DATA_REG	VPD_DATA				Y
SRIOV_BASE_REG	SRIOV_PCIE_EXTENDED_CAP_ID				Y
	SRIOV_CAP_VERSION				Y
	SRIOV_NEXT_OFFSET				Y
CAPABILITIES_REG	SRIOV_VF_10BIT_TAG_REQ_CAP				Y
	SRIOV_VF_MIGRATION_INT_MSG_NUM				Y
	SRIOV_ARI_CAP_HIER_PRESERVED				Y
	SRIOV_VF_MIGRATION_CAP				Y
STATUS_CONTROL_REG	SRIOV_VF_10BIT_TAG_REQ_ENABLE				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	SRIOV_ARI_CAPABLE_HIER				Y
	SRIOV_VF_MSE				Y
	SRIOV_VF_MIGRATION_INT_ENABLE				Y
	SRIOV_VF_MIGRATION_ENABLE				Y
	SRIOV_VF_ENABLE				Y
TOTAL_VFS_INITIAL_VFS_REG	SRIOV_TOTAL_VFS				Y
	SRIOV_INITIAL_VFS				Y
SRIOV_NUM_VFS	SRIOV_FDL				Y
	SRIOV_NUM_VFS				Y
SRIOV_VF_OFFSET_POSITION	SRIOV_VF_STRIDE				Y
	SRIOV_VF_OFFSET				Y
VF_DEVICE_ID_REG	SRIOV_VF_DEVICE_ID				Y
SUP_PAGE_SIZES_REG	SRIOV_SUP_PAGE_SIZE				Y
SYSTEM_PAGE_SIZE_REG	SYSTEM_PAGE_SIZE_REG				Y
SRIOV_BAR0_REG	SRIOV_VF_BAR0_START				Y
	SRIOV_VF_BAR0_PREFETCH				Y
	SRIOV_VF_BAR0_TYPE				Y
SRIOV_BAR1_REG	SRIOV_VF_BAR1_START				Y
	SRIOV_VF_BAR1_PREFETCH				Y
	SRIOV_VF_BAR1_TYPE				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RSVDP_SRIOV_VF_BAR1				Y
SRIOV_BAR2_REG	SRIOV_VF_BAR2_START				Y
	SRIOV_VF_BAR2_PREFETCH				Y
	SRIOV_VF_BAR2_TYPE				Y
SRIOV_BAR3_REG	SRIOV_VF_BAR3_START				Y
	SRIOV_VF_BAR3_PREFETCH				Y
	SRIOV_VF_BAR3_TYPE				Y
SRIOV_BAR4_REG	SRIOV_VF_BAR4_START				Y
	SRIOV_VF_BAR4_PREFETCH				Y
	SRIOV_VF_BAR4_TYPE				Y
SRIOV_BAR5_REG	SRIOV_VF_BAR5_START				Y
	SRIOV_VF_BAR5_PREFETCH				Y
	SRIOV_VF_BAR5_TYPE				Y
	RSVDP_SRIOV_VF_BAR5				Y
VF_MIGRATION_STATE_ARRAY_REG	SRIOV_VF_MIGRATION_STATE_OFFSET				Y
	SRIOV_VF_MIGRATION_STATE_BIR				Y
SHADOW_SRIOV_VF_OFFSET_POSITION	SHADOW_SRIOV_VF_STRIDE				Y
	SHADOW_SRIOV_VF_OFFSET				Y
SRIOV_BAR0_MASK_REG	PCI_SRIOV_BAR0_ENABLED				Y
	PCI_SRIOV_BAR0_MASK		Y		Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
SRIOV_BAR1_MASK_REG	PCI_SRIOV_BAR1_ENABLED				Y
	PCI_SRIOV_BAR1_MASK		Y		Y
SRIOV_BAR2_MASK_REG	PCI_SRIOV_BAR2_ENABLED				Y
	PCI_SRIOV_BAR2_MASK		Y		Y
SRIOV_BAR3_MASK_REG	PCI_SRIOV_BAR3_ENABLED				Y
	PCI_SRIOV_BAR3_MASK		Y		Y
SRIOV_BAR4_MASK_REG	PCI_SRIOV_BAR4_ENABLED				Y
	PCI_SRIOV_BAR4_MASK		Y		Y
PCI_SRIOV_BAR4_MASK	PCI_SRIOV_BAR5_ENABLED				Y
	PCI_SRIOV_BAR5_MASK		Y		Y
SN_BASE	SN_PCIE_EXTENDED_CAP_ID				Y
	SN_CAP_VERSION				Y
	SN_NEXT_OFFSET				Y
SER_NUM_REG_DW_1	SN_SER_NUM_REG_1_DW				Y
SN_SER_NUM_REG_1_DW	SN_SER_NUM_REG_2_DW				Y
RASDP_VENDOR_SPECIFIC_HDR_OFF	VSEC_LENGTH		Y		
RASDP_ERROR_PROT_CTRL_OFF	ERROR_PROT_DISABLE_LTIM				Y
	ERROR_PROT_DISABLE_CXS_RX				Y
	ERROR_PROT_DISABLE_ADM_RX				Y
	ERROR_PROT_DISABLE_LAYER3_RX				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	ERROR_PROT_DISABLE_LAYER2_RX				Y
	ERROR_PROT_DISABLE_DMA_READ				Y
	ERROR_PROT_DISABLE_AXI_BRIDGE_INBOUND_REQUEST				Y
	ERROR_PROT_DISABLE_AXI_BRIDGE_INBOUND_COMPLETION				Y
	ERROR_PROT_DISABLE_RX				Y
	ERROR_PROT_DISABLE_CXL_TX				Y
	ERROR_PROT_DISABLE_DTIM_TX				Y
	ERROR_PROT_DISABLE_CXS_TX				Y
	ERROR_PROT_DISABLE_ADM_TX				Y
	ERROR_PROT_DISABLE_LAYER3_TX				Y
	ERROR_PROT_DISABLE_LAYER2_TX				Y
	ERROR_PROT_DISABLE_DMA_WRITE				Y
	ERROR_PROT_DISABLE_AXI_BRIDGE_OUTBOUND				Y
	ERROR_PROT_DISABLE_AXI_BRIDGE_MASTER				Y
	ERROR_PROT_DISABLE_TX				Y
RASDP_CORR_COUNTER_CTRL_OFF	CORR_COUNTER_SELECTION				Y
	CORR_COUNTER_SELECTION_REGION				Y
	CORR_EN_COUNTERS				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	CORR_CLEAR_COUNTERS				Y
RASDP_CORR_COUNT_REPORT_OFF	CORR_COUNTER_SELECTED				Y
	CORR_COUNTER_SELECTED_REGION				Y
	CORR_COUNTER				Y
RASDP_UNCORR_COUNTER_CTRL_OFF	UNCORR_COUNTER_SELECTION				Y
	UNCORR_COUNTER_SELECTION_REGION				Y
	UNCORR_EN_COUNTERS				Y
	UNCORR_CLEAR_COUNTERS				Y
RASDP_UNCORR_COUNT_REPORT_OFF	UNCORR_COUNTER_SELECTED				Y
	UNCORR_COUNTER_SELECTED_REGION				Y
	UNCORR_COUNTER				Y
RASDP_ERROR_INJ_CTRL_OFF	ERROR_INJ_LOC				Y
	ERROR_INJ_COUNT				Y
	ERROR_INJ_TYPE				Y
	ERROR_INJ_EN				Y
RASDP_CORR_ERROR_LOCATION_OFF	LOC_LAST_CORR_ERROR				Y
	REG_LAST_CORR_ERROR				Y
	LOC_FIRST_CORR_ERROR				Y
	REG_FIRST_CORR_ERROR				Y
RASDP_UNCORR_ERROR_LOCATION_OFF	LOC_LAST_UNCORR_ERROR				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	REG_LAST_UNCORR_ERROR				Y
	LOC_FIRST_UNCORR_ERROR				Y
	REG_FIRST_UNCORR_ERROR				Y
RASDP_RAM_ADDR_CORR_ERROR_OFF	RAM_INDEX_CORR_ERROR				Y
	RAM_ADDR_CORR_ERROR				Y
RASDP_RAM_ADDR_UNCORR_ERROR_OFF	RAM_INDEX_UNCORR_ERROR				Y
	RAM_ADDR_UNCORR_ERROR				Y
CXL_TEST_CONFIG_BASE_LOW_OFF	CXL_DEVICE_TEST_BASE_LOW		Y		
CXL_TEST_CONFIG_BASE_HIGH_OFF	CXL_DEVICE_TEST_BASE_HIGH		Y		
CAP_ID_NXT_PTR_REG	PME_SUPPORT		Y		
PB_BASE	PB_PCIE_EXTENDED_CAP_ID				Y
	PB_CAP_VERSION				Y
	PB_NEXT_OFFSET				Y
PB_DATA_SELECT	PB_DATA_SEL				Y
DATA_REG_PB	PB_POWER_RAIL_STATE				Y
	PB_TYPE				Y
	PB_PM_STATE				Y
	PB_PM_SUB_STATE				Y
	PB_DATA_SCALE				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	PB_BASE_POWER				Y
CAP_REG_PB	PB_SYS_ALLOC				y
LINK_CAPABILITIES_REG	PCIE_CAP_L1_EXIT_LATENCY	Y			
	PCIE_CAP_L0S_EXIT_LATENCY	Y			
DEVICE_CAPABILITIES2_REG	PCIE_CAP_128_CAS_CPL_SUPP	Y		Y	
	PCIE_CAP_64_ATOMIC_CPL_SUPP	Y		Y	
	PCIE_CAP_32_ATOMIC_CPL_SUPP	Y		Y	
LINK_CAPABILITIES2_REG	PCIE_CAP_SUPPORT_LINK_SPEED_VECTOR		Y		
LINK_CONTROL2_LINK_STATUS2_REG	DOWNSTREAM_COMPO_PRESENCE				Y
SHADOW_LINK_CAPABILITIES_REG	SHADOW_PCIE_CAP_L0S_EXIT_LATENCY	Y	Y		Y
	SHADOW_PCIE_CAP_L1_EXIT_LATENCY	Y	Y		Y
	PCIE_CAP_PORT_NUM				Y
	PCIE_CAP_ASPM_OPT_COMPLIANCE				Y
	PCIE_CAP_LINK_BW_NOT_CAP				Y
	PCIE_CAP_DLL_ACTIVE_REP_CAP				Y
	PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP				Y
	PCIE_CAP_CLOCK_POWER_MAN				Y
	PCIE_CAP_ACTIVE_STATE_LINK_PM_SUPPORT				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	PCIE_CAP_MAX_LINK_WIDTH				Y
	PCIE_CAP_MAX_LINK_SPEED				Y
RESBAR_CAP_REG_0_128TB	RESBAR_CAP_REG_0_128TB		Y		
	RESBAR_CAP_REG_0_64TB		Y		
	RESBAR_CAP_REG_0_32TB		Y		
	RESBAR_CAP_REG_0_16TB		Y		
	RESBAR_CAP_REG_0_8TB		Y		
	RESBAR_CAP_REG_0_4TB		Y		
	RESBAR_CAP_REG_0_2TB		Y		
	RESBAR_CAP_REG_0_1TB		Y		
	RESBAR_CAP_REG_0_512GB		Y		
	RESBAR_CAP_REG_0_256GB		Y		
	RESBAR_CAP_REG_0_128GB		Y		
	RESBAR_CAP_REG_0_64GB		Y		
	RESBAR_CAP_REG_0_32GB		Y		
	RESBAR_CAP_REG_0_16GB		Y		
	RESBAR_CAP_REG_0_8GB		Y		
	RESBAR_CAP_REG_0_4GB		Y		
	RESBAR_CAP_REG_0_2GB		Y		
	RESBAR_CAP_REG_0_1GB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CAP_REG_0_512MB		Y		
	RESBAR_CAP_REG_0_256MB		Y		
	RESBAR_CAP_REG_0_128MB		Y		
	RESBAR_CAP_REG_0_64MB		Y		
	RESBAR_CAP_REG_0_32MB		Y		
	RESBAR_CAP_REG_0_16MB		Y		
	RESBAR_CAP_REG_0_8MB		Y		
	RESBAR_CAP_REG_0_4MB		Y		
	RESBAR_CAP_REG_0_2MB		Y		
	RESBAR_CAP_REG_0_1MB		Y		
RESBAR_CTRL_REG_0_REG	RESBAR_CTRL_REG_0_8EB		Y		
	RESBAR_CTRL_REG_0_4EB		Y		
	RESBAR_CTRL_REG_0_2EB		Y		
	RESBAR_CTRL_REG_0_1EB		Y		
	RESBAR_CTRL_REG_0_512PB		Y		
	RESBAR_CTRL_REG_0_256PB		Y		
	RESBAR_CTRL_REG_0_128PB		Y		
	RESBAR_CTRL_REG_0_64PB		Y		
	RESBAR_CTRL_REG_0_32PB		Y		
	RESBAR_CTRL_REG_0_16PB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CTRL_REG_0_8PB		Y		
	RESBAR_CTRL_REG_0_4PB		Y		
	RESBAR_CTRL_REG_0_2PB		Y		
	RESBAR_CTRL_REG_0_1PB		Y		
	RESBAR_CTRL_REG_0_512TB		Y		
	RESBAR_CTRL_REG_0_256TB		Y		
RESBAR_CAP_REG_1_REG	RESBAR_CAP_REG_1_128TB		Y		
	RESBAR_CAP_REG_1_64TB		Y		
	RESBAR_CAP_REG_1_32TB		Y		
	RESBAR_CAP_REG_1_16TB		Y		
	RESBAR_CAP_REG_1_8TB		Y		
	RESBAR_CAP_REG_1_4TB		Y		
	RESBAR_CAP_REG_1_2TB		Y		
	RESBAR_CAP_REG_1_1TB		Y		
	RESBAR_CAP_REG_1_512GB		Y		
	RESBAR_CAP_REG_1_256GB		Y		
	RESBAR_CAP_REG_1_128GB		Y		
	RESBAR_CAP_REG_1_64GB		Y		
	RESBAR_CAP_REG_1_32GB		Y		
	RESBAR_CAP_REG_1_8GB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CAP_REG_1_4GB		Y		
	RESBAR_CAP_REG_1_2GB		Y		
	RESBAR_CAP_REG_1_1GB		Y		
	RESBAR_CAP_REG_1_512MB		Y		
	RESBAR_CAP_REG_1_256MB		Y		
	RESBAR_CAP_REG_1_128MB		Y		
	RESBAR_CAP_REG_1_64MB		Y		
	RESBAR_CAP_REG_1_32MB		Y		
	RESBAR_CAP_REG_1_16MB		Y		
	RESBAR_CAP_REG_1_8MB		Y		
	RESBAR_CAP_REG_1_4MB		Y		
	RESBAR_CAP_REG_1_2MB		Y		
	RESBAR_CAP_REG_1_1MB		Y		
RESBAR_CTRL_REG_1_REG	RESBAR_CTRL_REG_1_8EB		Y		
	RESBAR_CTRL_REG_1_4EB		Y		
	RESBAR_CTRL_REG_1_2EB		Y		
	RESBAR_CTRL_REG_1_1EB		Y		
	RESBAR_CTRL_REG_1_512PB		Y		
	RESBAR_CTRL_REG_1_256PB		Y		
	RESBAR_CTRL_REG_1_128PB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CTRL_REG_1_64PB		Y		
	RESBAR_CTRL_REG_1_32PB		Y		
	RESBAR_CTRL_REG_1_16PB		Y		
	RESBAR_CTRL_REG_1_8PB		Y		
	RESBAR_CTRL_REG_1_4PB		Y		
	RESBAR_CTRL_REG_1_2PB		Y		
	RESBAR_CTRL_REG_1_1PB		Y		
	RESBAR_CTRL_REG_1_512TB		Y		
	RESBAR_CTRL_REG_1_256TB		Y		
RESBAR_CAP_REG_2_REG	RESBAR_CAP_REG_2_128TB		Y		
	RESBAR_CAP_REG_2_64TB		Y		
	RESBAR_CAP_REG_2_32TB		Y		
	RESBAR_CAP_REG_2_16TB		Y		
	RESBAR_CAP_REG_2_8TB		Y		
	RESBAR_CAP_REG_2_4TB		Y		
	RESBAR_CAP_REG_2_2TB		Y		
	RESBAR_CAP_REG_2_1TB		Y		
	RESBAR_CAP_REG_2_512GB		Y		
	RESBAR_CAP_REG_2_256GB		Y		
	RESBAR_CAP_REG_2_128GB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CAP_REG_2_64GB		Y		
	RESBAR_CAP_REG_2_32GB		Y		
	RESBAR_CAP_REG_2_16GB		Y		
	RESBAR_CAP_REG_2_8GB		Y		
	RESBAR_CAP_REG_2_4GB		Y		
	RESBAR_CAP_REG_2_2GB		Y		
	RESBAR_CAP_REG_2_1GB		Y		
	RESBAR_CAP_REG_2_512MB		Y		
	RESBAR_CAP_REG_2_256MB		Y		
	RESBAR_CAP_REG_2_128MB		Y		
	RESBAR_CAP_REG_2_64MB		Y		
	RESBAR_CAP_REG_2_32MB		Y		
	RESBAR_CAP_REG_2_16MB		Y		
	RESBAR_CAP_REG_2_8MB		Y		
	RESBAR_CAP_REG_2_4MB		Y		
	RESBAR_CAP_REG_2_2MB		Y		
	RESBAR_CAP_REG_2_1MB		Y		
RESBAR_CTRL_REG_2_REG	RESBAR_CTRL_REG_2_8EB		Y		
	RESBAR_CTRL_REG_2_4EB		Y		
	RESBAR_CTRL_REG_2_2EB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CTRL_REG_2_1EB		Y		
	RESBAR_CTRL_REG_2_512PB		Y		
	RESBAR_CTRL_REG_2_256PB		Y		
	RESBAR_CTRL_REG_2_128PB		Y		
	RESBAR_CTRL_REG_2_64PB		Y		
	RESBAR_CTRL_REG_2_32PB		Y		
	RESBAR_CTRL_REG_2_16PB		Y		
	RESBAR_CTRL_REG_2_8PB		Y		
	RESBAR_CTRL_REG_2_4PB		Y		
	RESBAR_CTRL_REG_2_2PB		Y		
	RESBAR_CTRL_REG_2_1PB		Y		
	RESBAR_CTRL_REG_2_512TB		Y		
	RESBAR_CTRL_REG_2_256TB		Y		
RESBAR_CAP_REG_3_REG	RESBAR_CAP_REG_3_128TB		Y		
	RESBAR_CAP_REG_3_64TB		Y		
	RESBAR_CAP_REG_3_32TB		Y		
	RESBAR_CAP_REG_3_16TB		Y		
	RESBAR_CAP_REG_3_8TB		Y		
	RESBAR_CAP_REG_3_4TB		Y		
	RESBAR_CAP_REG_3_2TB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CAP_REG_3_1TB		Y		
	RESBAR_CAP_REG_3_512GB		Y		
	RESBAR_CAP_REG_3_256GB		Y		
	RESBAR_CAP_REG_3_128GB		Y		
	RESBAR_CAP_REG_3_64GB		Y		
	RESBAR_CAP_REG_3_32GB		Y		
	RESBAR_CAP_REG_3_16GB		Y		
	RESBAR_CAP_REG_3_8GB		Y		
	RESBAR_CAP_REG_3_4GB		Y		
	RESBAR_CAP_REG_3_2GB		Y		
	RESBAR_CAP_REG_3_1GB		Y		
	RESBAR_CAP_REG_3_512MB		Y		
	RESBAR_CAP_REG_3_256MB		Y		
	RESBAR_CAP_REG_3_128MB		Y		
	RESBAR_CAP_REG_3_64MB		Y		
	RESBAR_CAP_REG_3_32MB		Y		
	RESBAR_CAP_REG_3_16MB		Y		
	RESBAR_CAP_REG_3_8MB		Y		
	RESBAR_CAP_REG_3_4MB		Y		
	RESBAR_CAP_REG_3_2MB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CAP_REG_3_1MB		Y		
RESBAR_CTRL_REG_3_REG	RESBAR_CTRL_REG_3_8EB		Y		
	RESBAR_CTRL_REG_3_8EB		Y		
	RESBAR_CTRL_REG_3_2EB		Y		
	RESBAR_CTRL_REG_3_1EB		Y		
	RESBAR_CTRL_REG_3_512PB		Y		
	RESBAR_CTRL_REG_3_256PB		Y		
	RESBAR_CTRL_REG_3_128PB		Y		
	RESBAR_CTRL_REG_3_64PB		Y		
	RESBAR_CTRL_REG_3_32PB		Y		
	RESBAR_CTRL_REG_3_16PB		Y		
	RESBAR_CTRL_REG_3_8PB		Y		
	RESBAR_CTRL_REG_3_4PB		Y		
	RESBAR_CTRL_REG_3_2PB		Y		
	RESBAR_CTRL_REG_3_1PB		Y		
	RESBAR_CTRL_REG_3_512TB		Y		
	RESBAR_CTRL_REG_3_256TB		Y		
RESBAR_CAP_REG_4_REG	RESBAR_CAP_REG_4_128TB		Y		
	RESBAR_CAP_REG_4_64TB		Y		
	RESBAR_CAP_REG_4_32TB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CAP_REG_4_16TB		Y		
	RESBAR_CAP_REG_4_8TB		Y		
	RESBAR_CAP_REG_4_4TB		Y		
	RESBAR_CAP_REG_4_2TB		Y		
	RESBAR_CAP_REG_4_1TB		Y		
	RESBAR_CAP_REG_4_512GB		Y		
	RESBAR_CAP_REG_4_256GB		Y		
	RESBAR_CAP_REG_4_128GB		Y		
	RESBAR_CAP_REG_4_64GB		Y		
	RESBAR_CAP_REG_4_32GB		Y		
	RESBAR_CAP_REG_4_16GB		Y		
	RESBAR_CAP_REG_4_8GB		Y		
	RESBAR_CAP_REG_4_4GB		Y		
	RESBAR_CAP_REG_4_2GB		Y		
	RESBAR_CAP_REG_4_1GB		Y		
	RESBAR_CAP_REG_4_512MB		Y		
	RESBAR_CAP_REG_4_256MB		Y		
	RESBAR_CAP_REG_4_128MB		Y		
	RESBAR_CAP_REG_4_64MB		Y		
	RESBAR_CAP_REG_4_32MB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CAP_REG_4_16MB		Y		
	RESBAR_CAP_REG_4_8MB		Y		
	RESBAR_CAP_REG_4_4MB		Y		
	RESBAR_CAP_REG_4_2MB		Y		
	RESBAR_CAP_REG_4_1MB		Y		
RESBAR_CTRL_REG_4_8EB	RESBAR_CTRL_REG_4_8EB		Y		
	RESBAR_CTRL_REG_4_4EB		Y		
	RESBAR_CTRL_REG_4_2EB		Y		
	RESBAR_CTRL_REG_4_1EB		Y		
	RESBAR_CTRL_REG_4_512PB		Y		
	RESBAR_CTRL_REG_4_256PB		Y		
	RESBAR_CTRL_REG_4_128PB		Y		
	RESBAR_CTRL_REG_4_64PB		Y		
	RESBAR_CTRL_REG_4_32PB		Y		
	RESBAR_CTRL_REG_4_16PB		Y		
	RESBAR_CTRL_REG_4_8PB		Y		
	RESBAR_CTRL_REG_4_4PB		Y		
	RESBAR_CTRL_REG_4_2PB		Y		
	RESBAR_CTRL_REG_4_1PB		Y		
	RESBAR_CTRL_REG_4_512TB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CTRL_REG_4_256TB		Y		
RESBAR_CAP_REG_5_REG	RESBAR_CAP_REG_5_128TB		Y		
	RESBAR_CAP_REG_5_64TB		Y		
	RESBAR_CAP_REG_5_32TB		Y		
	RESBAR_CAP_REG_5_16TB		Y		
	RESBAR_CAP_REG_5_8TB		Y		
	RESBAR_CAP_REG_5_4TB		Y		
	RESBAR_CAP_REG_5_2TB		Y		
	RESBAR_CAP_REG_5_1TB		Y		
	RESBAR_CAP_REG_5_512GB		Y		
	RESBAR_CAP_REG_5_256GB		Y		
	RESBAR_CAP_REG_5_128GB		Y		
	RESBAR_CAP_REG_5_64GB		Y		
	RESBAR_CAP_REG_5_32GB		Y		
	RESBAR_CAP_REG_5_16GB		Y		
	RESBAR_CAP_REG_5_8GB		Y		
	RESBAR_CAP_REG_5_4GB		Y		
	RESBAR_CAP_REG_5_2GB		Y		
	RESBAR_CAP_REG_5_1GB		Y		
	RESBAR_CAP_REG_5_512MB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CAP_REG_5_256MB		Y		
	RESBAR_CAP_REG_5_128MB		Y		
	RESBAR_CAP_REG_5_64MB		Y		
	RESBAR_CAP_REG_5_32MB		Y		
	RESBAR_CAP_REG_5_16MB		Y		
	RESBAR_CAP_REG_5_8MB		Y		
	RESBAR_CAP_REG_5_4MB		Y		
	RESBAR_CAP_REG_5_2MB		Y		
	RESBAR_CAP_REG_5_1MB		Y		
RESBAR_CTRL_REG_5_REG	RESBAR_CTRL_REG_5_8EB		Y		
	RESBAR_CTRL_REG_5_4EB		Y		
	RESBAR_CTRL_REG_5_2EB		Y		
	RESBAR_CTRL_REG_5_1EB		Y		
	RESBAR_CTRL_REG_5_512PB		Y		
	RESBAR_CTRL_REG_5_256PB		Y		
	RESBAR_CTRL_REG_5_128PB		Y		
	RESBAR_CTRL_REG_5_64PB		Y		
	RESBAR_CTRL_REG_5_32PB		Y		
	RESBAR_CTRL_REG_5_16PB		Y		
	RESBAR_CTRL_REG_5_8PB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESBAR_CTRL_REG_5_4PB		Y		
	RESBAR_CTRL_REG_5_2PB		Y		
	RESBAR_CTRL_REG_5_1PB		Y		
	RESBAR_CTRL_REG_5_512TB		Y		
	RESBAR_CTRL_REG_5_256TB		Y		
VF_RESBAR_CAP_REG_0_REG	VF_RESBAR_CAP_REG_0_128TB		Y		
	VF_RESBAR_CAP_REG_0_64TB		Y		
	VF_RESBAR_CAP_REG_0_32TB		Y		
	VF_RESBAR_CAP_REG_0_16TB		Y		
	VF_RESBAR_CAP_REG_0_8TB		Y		
	VF_RESBAR_CAP_REG_0_4TB		Y		
	VF_RESBAR_CAP_REG_0_2TB		Y		
	VF_RESBAR_CAP_REG_0_1TB		Y		
	VF_RESBAR_CAP_REG_0_512GB		Y		
	VF_RESBAR_CAP_REG_0_256GB		Y		
	VF_RESBAR_CAP_REG_0_128GB		Y		
	VF_RESBAR_CAP_REG_0_64GB		Y		
	VF_RESBAR_CAP_REG_0_32GB		Y		
	VF_RESBAR_CAP_REG_0_16GB		Y		
	VF_RESBAR_CAP_REG_0_8GB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	VF_RESBAR_CAP_REG_0_4GB		Y		
	VF_RESBAR_CAP_REG_0_2GB		Y		
	VF_RESBAR_CAP_REG_0_1GB		Y		
	VF_RESBAR_CAP_REG_0_512MB		Y		
	VF_RESBAR_CAP_REG_0_256MB		Y		
	VF_RESBAR_CAP_REG_0_128MB		Y		
	VF_RESBAR_CAP_REG_0_64MB		Y		
	VF_RESBAR_CAP_REG_0_32MB		Y		
	VF_RESBAR_CAP_REG_0_16MB		Y		
	VF_RESBAR_CAP_REG_0_8MB		Y		
	VF_RESBAR_CAP_REG_0_4MB		Y		
	VF_RESBAR_CAP_REG_0_2MB		Y		
	VF_RESBAR_CAP_REG_0_1MB		Y		
VF_RESBAR_CTRL_REG_0_REG	VF_RESBAR_CTRL_REG_0_8EB		Y		
	VF_RESBAR_CTRL_REG_0_4EB		Y		
	VF_RESBAR_CTRL_REG_0_2EB		Y		
	VF_RESBAR_CTRL_REG_0_1EB		Y		
	VF_RESBAR_CTRL_REG_0_512PB		Y		
	VF_RESBAR_CTRL_REG_0_256PB		Y		
	VF_RESBAR_CTRL_REG_0_128PB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	VF_RESBAR_CTRL_REG_0_64PB		Y		
	VF_RESBAR_CTRL_REG_0_32PB		Y		
	VF_RESBAR_CTRL_REG_0_16PB		Y		
	VF_RESBAR_CTRL_REG_0_8PB		Y		
	VF_RESBAR_CTRL_REG_0_4PB		Y		
	VF_RESBAR_CTRL_REG_0_2PB		Y		
	VF_RESBAR_CTRL_REG_0_1PB		Y		
	VF_RESBAR_CTRL_REG_0_512TB		Y		
	VF_RESBAR_CTRL_REG_0_256TB		Y		
VF_RESBAR_CAP_REG_1_REG	VF_RESBAR_CAP_REG_1_128TB		Y		
	VF_RESBAR_CAP_REG_1_64TB		Y		
	VF_RESBAR_CAP_REG_1_32TB		Y		
	VF_RESBAR_CAP_REG_1_16TB		Y		
	VF_RESBAR_CAP_REG_1_8TB		Y		
	VF_RESBAR_CAP_REG_1_4TB		Y		
	VF_RESBAR_CAP_REG_1_2TB		Y		
	VF_RESBAR_CAP_REG_1_1TB		Y		
	VF_RESBAR_CAP_REG_1_512GB		Y		
	VF_RESBAR_CAP_REG_1_256GB		Y		
	VF_RESBAR_CAP_REG_1_128GB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	VF_RESBAR_CAP_REG_1_64GB		Y		
	VF_RESBAR_CAP_REG_1_32GB		Y		
	VF_RESBAR_CAP_REG_1_16GB		Y		
	VF_RESBAR_CAP_REG_1_8GB		Y		
	VF_RESBAR_CAP_REG_1_4GB		Y		
	VF_RESBAR_CAP_REG_1_2GB		Y		
	VF_RESBAR_CAP_REG_1_1GB		Y		
	VF_RESBAR_CAP_REG_1_512MB		Y		
	VF_RESBAR_CAP_REG_1_256MB		Y		
	VF_RESBAR_CAP_REG_1_128MB		Y		
	VF_RESBAR_CAP_REG_1_64MB		Y		
	VF_RESBAR_CAP_REG_1_32MB		Y		
	VF_RESBAR_CAP_REG_1_16MB		Y		
	VF_RESBAR_CAP_REG_1_8MB		Y		
	VF_RESBAR_CAP_REG_1_4MB		Y		
	VF_RESBAR_CAP_REG_1_2MB		Y		
	VF_RESBAR_CAP_REG_1_1MB		Y		
VF_RESBAR_CTRL_REG_1_REG	VF_RESBAR_CTRL_REG_1_8EB		Y		
	VF_RESBAR_CTRL_REG_1_4EB		Y		
	VF_RESBAR_CTRL_REG_1_2EB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	VF_RESBAR_CTRL_REG_1_1EB		Y		
	VF_RESBAR_CTRL_REG_1_512PB		Y		
	VF_RESBAR_CTRL_REG_1_256PB		Y		
	VF_RESBAR_CTRL_REG_1_128PB		Y		
	VF_RESBAR_CTRL_REG_1_64PB		Y		
	VF_RESBAR_CTRL_REG_1_32PB		Y		
	VF_RESBAR_CTRL_REG_1_16PB		Y		
	VF_RESBAR_CTRL_REG_1_8PB		Y		
	VF_RESBAR_CTRL_REG_1_4PB		Y		
	VF_RESBAR_CTRL_REG_1_2PB		Y		
	VF_RESBAR_CTRL_REG_1_1PB		Y		
	VF_RESBAR_CTRL_REG_1_512TB		Y		
	VF_RESBAR_CTRL_REG_1_256TB		Y		
VF_RESBAR_CAP_REG_2_REG	VF_RESBAR_CAP_REG_2_128TB		Y		
	VF_RESBAR_CAP_REG_2_64TB		Y		
	VF_RESBAR_CAP_REG_2_32TB		Y		
	VF_RESBAR_CAP_REG_2_16TB		Y		
	VF_RESBAR_CAP_REG_2_8TB		Y		
	VF_RESBAR_CAP_REG_2_4TB		Y		
	VF_RESBAR_CAP_REG_2_1TB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	VF_RESBAR_CAP_REG_2_512GB		Y		
	VF_RESBAR_CAP_REG_2_256GB		Y		
	VF_RESBAR_CAP_REG_2_128GB		Y		
	VF_RESBAR_CAP_REG_2_64GB		Y		
	VF_RESBAR_CAP_REG_2_32GB		Y		
	VF_RESBAR_CAP_REG_2_16GB		Y		
	VF_RESBAR_CAP_REG_2_8GB		Y		
	VF_RESBAR_CAP_REG_2_4GB		Y		
	VF_RESBAR_CAP_REG_2_2GB		Y		
	VF_RESBAR_CAP_REG_2_1GB		Y		
	VF_RESBAR_CAP_REG_2_512MB		Y		
	VF_RESBAR_CAP_REG_2_256MB		Y		
	VF_RESBAR_CAP_REG_2_128MB		Y		
	VF_RESBAR_CAP_REG_2_64MB		Y		
	VF_RESBAR_CAP_REG_2_32MB		Y		
	VF_RESBAR_CAP_REG_2_16MB		Y		
	VF_RESBAR_CAP_REG_2_8MB		Y		
	VF_RESBAR_CAP_REG_2_4MB		Y		
	VF_RESBAR_CAP_REG_2_2MB		Y		
	VF_RESBAR_CAP_REG_2_1MB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
VF_RESBAR_CTRL_REG_2_REG	VF_RESBAR_CTRL_REG_2_8EB		Y		
	VF_RESBAR_CTRL_REG_2_4EB		Y		
	VF_RESBAR_CTRL_REG_2_2EB		Y		
	VF_RESBAR_CTRL_REG_2_1EB		Y		
	VF_RESBAR_CTRL_REG_2_512PB		Y		
	VF_RESBAR_CTRL_REG_2_256PB		Y		
	VF_RESBAR_CTRL_REG_2_128PB		Y		
	VF_RESBAR_CTRL_REG_2_64PB		Y		
	VF_RESBAR_CTRL_REG_2_64PB		Y		
	VF_RESBAR_CTRL_REG_2_16PB		Y		
	VF_RESBAR_CTRL_REG_2_8PB		Y		
	VF_RESBAR_CTRL_REG_2_4PB		Y		
	VF_RESBAR_CTRL_REG_2_2PB		Y		
	VF_RESBAR_CTRL_REG_2_1PB		Y		
	VF_RESBAR_CTRL_REG_2_512TB		Y		
	VF_RESBAR_CTRL_REG_2_256TB		Y		
VF_RESBAR_CAP_REG_3_REG	VF_RESBAR_CAP_REG_3_128TB		Y		
	VF_RESBAR_CAP_REG_3_64TB		Y		
	VF_RESBAR_CAP_REG_3_32TB		Y		
	VF_RESBAR_CAP_REG_3_16TB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	VF_RESBAR_CAP_REG_3_8TB		Y		
	VF_RESBAR_CAP_REG_3_4TB		Y		
	VF_RESBAR_CAP_REG_3_2TB		Y		
	VF_RESBAR_CAP_REG_3_1TB		Y		
	VF_RESBAR_CAP_REG_3_512GB		Y		
	VF_RESBAR_CAP_REG_3_256GB		Y		
	VF_RESBAR_CAP_REG_3_128GB		Y		
	VF_RESBAR_CAP_REG_3_64GB		Y		
	VF_RESBAR_CAP_REG_3_32GB		Y		
	VF_RESBAR_CAP_REG_3_16GB		Y		
	VF_RESBAR_CAP_REG_3_8GB		Y		
	VF_RESBAR_CAP_REG_3_4GB		Y		
	VF_RESBAR_CAP_REG_3_2GB		Y		
	VF_RESBAR_CAP_REG_3_1GB		Y		
	VF_RESBAR_CAP_REG_3_512MB		Y		
	VF_RESBAR_CAP_REG_3_256MB		Y		
	VF_RESBAR_CAP_REG_3_128MB		Y		
	VF_RESBAR_CAP_REG_3_64MB		Y		
	VF_RESBAR_CAP_REG_3_32MB		Y		
	VF_RESBAR_CAP_REG_3_16MB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	VF_RESBAR_CAP_REG_3_8MB		Y		
	VF_RESBAR_CAP_REG_3_4MB		Y		
	VF_RESBAR_CAP_REG_3_2MB		Y		
	VF_RESBAR_CAP_REG_3_1MB		Y		
VF_RESBAR_CTRL_REG_3_REG	VF_RESBAR_CTRL_REG_3_8EB		Y		
	VF_RESBAR_CTRL_REG_3_4EB		Y		
	VF_RESBAR_CTRL_REG_3_2EB		Y		
	VF_RESBAR_CTRL_REG_3_1EB		Y		
	VF_RESBAR_CTRL_REG_3_512PB		Y		
	VF_RESBAR_CTRL_REG_3_256PB		Y		
	VF_RESBAR_CTRL_REG_3_128PB		Y		
	VF_RESBAR_CTRL_REG_3_64PB		Y		
	VF_RESBAR_CTRL_REG_3_32PB		Y		
	VF_RESBAR_CTRL_REG_3_16PB		Y		
	VF_RESBAR_CTRL_REG_3_8PB		Y		
	VF_RESBAR_CTRL_REG_3_4PB		Y		
	VF_RESBAR_CTRL_REG_3_2PB		Y		
	VF_RESBAR_CTRL_REG_3_1PB		Y		
	VF_RESBAR_CTRL_REG_3_512TB		Y		
	VF_RESBAR_CTRL_REG_3_256TB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
VF_RESBAR_CAP_REG_4_REG	VF_RESBAR_CAP_REG_4_128TB		Y		
	VF_RESBAR_CAP_REG_4_64TB		Y		
	VF_RESBAR_CAP_REG_4_32TB		Y		
	VF_RESBAR_CAP_REG_4_16TB		Y		
	VF_RESBAR_CAP_REG_4_8TB		Y		
	VF_RESBAR_CAP_REG_4_4TB		Y		
	VF_RESBAR_CAP_REG_4_2TB		Y		
	VF_RESBAR_CAP_REG_4_1TB		Y		
	VF_RESBAR_CAP_REG_4_512GB		Y		
	VF_RESBAR_CAP_REG_4_256GB		Y		
	VF_RESBAR_CAP_REG_4_128GB		Y		
	VF_RESBAR_CAP_REG_4_64GB		Y		
	VF_RESBAR_CAP_REG_4_32GB		Y		
	VF_RESBAR_CAP_REG_4_16GB		Y		
	VF_RESBAR_CAP_REG_4_8GB		Y		
	VF_RESBAR_CAP_REG_4_4GB		Y		
	VF_RESBAR_CAP_REG_4_2GB		Y		
	VF_RESBAR_CAP_REG_4_1GB		Y		
	VF_RESBAR_CAP_REG_4_512MB		Y		
	VF_RESBAR_CAP_REG_4_256MB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	VF_RESBAR_CAP_REG_4_128MB		Y		
	VF_RESBAR_CAP_REG_4_64MB		Y		
	VF_RESBAR_CAP_REG_4_32MB		Y		
	VF_RESBAR_CAP_REG_4_16MB		Y		
	VF_RESBAR_CAP_REG_4_8MB		Y		
	VF_RESBAR_CAP_REG_4_4MB		Y		
	VF_RESBAR_CAP_REG_4_2MB		Y		
	VF_RESBAR_CAP_REG_4_1MB		Y		
VF_RESBAR_CTRL_REG_4_REG	VF_RESBAR_CTRL_REG_4_8EB		Y		
	VF_RESBAR_CTRL_REG_4_4EB		Y		
	VF_RESBAR_CTRL_REG_4_2EB		Y		
	VF_RESBAR_CTRL_REG_4_1EB		Y		
	VF_RESBAR_CTRL_REG_4_512PB		Y		
	VF_RESBAR_CTRL_REG_4_256PB		Y		
	VF_RESBAR_CTRL_REG_4_128PB		Y		
	VF_RESBAR_CTRL_REG_4_64PB		Y		
	VF_RESBAR_CTRL_REG_4_32PB		Y		
	VF_RESBAR_CTRL_REG_4_16PB		Y		
	VF_RESBAR_CTRL_REG_4_8PB		Y		
	VF_RESBAR_CTRL_REG_4_4PB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	VF_RESBAR_CTRL_REG_4_2PB		Y		
	VF_RESBAR_CTRL_REG_4_1PB		Y		
	VF_RESBAR_CTRL_REG_4_512TB		Y		
	VF_RESBAR_CTRL_REG_4_256TB		Y		
VF_RESBAR_CAP_REG_5_REG	VF_RESBAR_CAP_REG_5_128TB		Y		
	VF_RESBAR_CAP_REG_5_64TB		Y		
	VF_RESBAR_CAP_REG_5_32TB		Y		
	VF_RESBAR_CAP_REG_5_16TB		Y		
	VF_RESBAR_CAP_REG_5_8TB		Y		
	VF_RESBAR_CAP_REG_5_4TB		Y		
	VF_RESBAR_CAP_REG_5_2TB		Y		
	VF_RESBAR_CAP_REG_5_1TB		Y		
	VF_RESBAR_CAP_REG_5_512GB		Y		
	VF_RESBAR_CAP_REG_5_256GB		Y		
	VF_RESBAR_CAP_REG_5_128GB		Y		
	VF_RESBAR_CAP_REG_5_64GB		Y		
	VF_RESBAR_CAP_REG_5_32GB		Y		
	VF_RESBAR_CAP_REG_5_16GB		Y		
	VF_RESBAR_CAP_REG_5_8GB		Y		
	VF_RESBAR_CAP_REG_5_4GB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	VF_RESBAR_CAP_REG_5_2GB		Y		
	VF_RESBAR_CAP_REG_5_1GB		Y		
	VF_RESBAR_CAP_REG_5_512MB		Y		
	VF_RESBAR_CAP_REG_5_256MB		Y		
	VF_RESBAR_CAP_REG_5_128MB		Y		
	VF_RESBAR_CAP_REG_5_64MB		Y		
	VF_RESBAR_CAP_REG_5_32MB		Y		
	VF_RESBAR_CAP_REG_5_16MB		Y		
	VF_RESBAR_CAP_REG_5_8MB		Y		
	VF_RESBAR_CAP_REG_5_4MB		Y		
	VF_RESBAR_CAP_REG_5_2MB		Y		
	VF_RESBAR_CAP_REG_5_1MB		Y		
VF_RESBAR_CTRL_REG_5_REG	VF_RESBAR_CTRL_REG_5_8EB		Y		
	VF_RESBAR_CTRL_REG_5_4EB		Y		
	VF_RESBAR_CTRL_REG_5_2EB		Y		
	VF_RESBAR_CTRL_REG_5_1EB		Y		
	VF_RESBAR_CTRL_REG_5_512PB		Y		
	VF_RESBAR_CTRL_REG_5_256PB		Y		
	VF_RESBAR_CTRL_REG_5_128PB		Y		
	VF_RESBAR_CTRL_REG_5_64PB		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	VF_RESBAR_CTRL_REG_5_32PB		Y		
	VF_RESBAR_CTRL_REG_5_16PB		Y		
	VF_RESBAR_CTRL_REG_5_8PB		Y		
	VF_RESBAR_CTRL_REG_5_4PB		Y		
	VF_RESBAR_CTRL_REG_5_2PB		Y		
	VF_RESBAR_CTRL_REG_5_1PB		Y		
	VF_RESBAR_CTRL_REG_5_512TB		Y		
	VF_RESBAR_CTRL_REG_5_256TB		Y		
PCI_MSI_CAP_ID_NEXT_CTRL_REG	PCI_MSI_EXT_DATA_EN				Y
	PCI_MSI_EXT_DATA_CAP				Y
	PCI_PVM_SUPPORT				Y
	PCI_MSI_64_BIT_ADDR_CAP				Y
	PCI_MSI_MULTIPLE_MSG_EN				Y
	PCI_MSI_MULTIPLE_MSG_CAP				Y
	PCI_MSI_ENABLE				Y
	PCI_MSI_CAP_NEXT_OFFSET				Y
	PCI_MSI_CAP_ID				Y
MSI_CAP_OFF_04H_REG	PCI_MSI_CAP_OFF_04H				Y
MSI_CAP_OFF_08H_REG	PCI_MSI_CAP_OFF_0AH				Y
	PCI_MSI_CAP_OFF_08H				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
MSI_CAP_OFF_0CH_REG	PCI_MSI_CAP_OFF_0EH				Y
	PCI_MSI_CAP_OFF_0CH				Y
MSI_CAP_OFF_10H_REG	PCI_MSI_CAP_OFF_10H				Y
MSI_CAP_OFF_14H_REG	PCI_MSI_CAP_OFF_14H				Y
VF_DEVICE_CAPABILITIES2_REG	PCIE_CAP_TPH_CMPLT_SUPPORT_0		Y		
	PCIE_CAP_128_CAS_CPL_SUPP			Y	
	PCIE_CAP_64_ATOMIC_CPL_SUPP			Y	
	PCIE_CAP_32_ATOMIC_CPL_SUPP			Y	
VF_DEVICE_CONTROL2_DEVICE_STATUS2_REG	PCIE_CAP_EMERGENCY_PWR_RED_REQUEST			Y	
VF_LINK_CAPABILITIES2_REG	PCIE_CAP_SUPPORT_LINK_SPEED_VECTOR			Y	
VF_LINK_CONTROL2_LINK_STATUS2_REG	DOWNSTREAM_COMPO_PRESENCE				Y
DMA_CTRL_DATA_ARB_PRIOR_OFF	VERSION				Y
	RDBUFF_TRGT_WEIGHT				Y
	RD_CTRL_TRGT_WEIGHT				Y
	WR_CTRL_TRGT_WEIGHT				Y
	RTRGT1_WEIGHT				Y
DMA_CTRL_OFF	NUM_DMA_RD_CHAN				Y
	NUM_DMA_WR_CHAN				Y
	DIS_C2W_CACHE_RD				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	DIS_C2W_CACHE_WR				Y
DMA_WRITE_ENGINE_EN_OFF	DMA_WRITE_ENGINE_EN_HSHAKE_CH7				Y
	DMA_WRITE_ENGINE_EN_HSHAKE_CH6				Y
	DMA_WRITE_ENGINE_EN_HSHAKE_CH5				Y
	DMA_WRITE_ENGINE_EN_HSHAKE_CH4				Y
	DMA_WRITE_ENGINE_EN_HSHAKE_CH3				Y
	DMA_WRITE_ENGINE_EN_HSHAKE_CH2				Y
	DMA_WRITE_ENGINE_EN_HSHAKE_CH1				Y
	DMA_WRITE_ENGINE_EN_HSHAKE_CH0				Y
	DMA_WRITE_ENGINE				Y
DMA_WRITE_DOORBELL_OFF	WR_STOP				Y
	WR_DOORBELL_NUM				Y
DMA_WRITE_ENGINE_PF_OFF	RSVDP_WRITE_ENGINE_PF				Y
	DMA_WRITE_ENGINE_MAX_PRE_FETCH				Y
DMA_WRITE_CHANNEL_ARB_WEIGHT_LOW_OFF	WRITE_CHANNEL3_WEIGHT				Y
	WRITE_CHANNEL2_WEIGHT				Y
	WRITE_CHANNEL1_WEIGHT				Y
	WRITE_CHANNEL0_WEIGHT				Y
DMA_WRITE_CHANNEL_ARB_WEIGHT_HIGH_OFF	WRITE_CHANNEL7_WEIGHT				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	WRITE_CHANNEL6_WEIGHT				Y
	WRITE_CHANNEL5_WEIGHT				Y
	WRITE_CHANNEL4_WEIGHT				Y
DMA_READ_ENGINE_EN_OFF	DMA_READ_ENGINE_EN_HSHAKE_CH7				Y
	DMA_READ_ENGINE_EN_HSHAKE_CH6				Y
	DMA_READ_ENGINE_EN_HSHAKE_CH5				Y
	DMA_READ_ENGINE_EN_HSHAKE_CH4				Y
	DMA_READ_ENGINE_EN_HSHAKE_CH3				Y
	DMA_READ_ENGINE_EN_HSHAKE_CH2				Y
	DMA_READ_ENGINE_EN_HSHAKE_CH1				Y
	DMA_READ_ENGINE_EN_HSHAKE_CH0				Y
	DMA_READ_ENGINE				Y
DMA_READ_DOORBELL_OFF	RD_STOP				Y
	RD_DOORBELL_NUM				Y
DMA_READ_ENGINE_PF_OFF	RSVDP_READ_ENGINE_PF				Y
	DMA_READ_ENGINE_MAX_PRE_FETCH				Y
DMA_READ_CHANNEL_ARB_WEIGHT_LOW_OFF	READ_CHANNEL3_WEIGHT				Y
	READ_CHANNEL2_WEIGHT				Y
	READ_CHANNEL1_WEIGHT				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	READ_CHANNEL0_WEIGHT				Y
DMA_READ_CHANNEL_ARB_WEIGHT_HIGH_OFF	READ_CHANNEL7_WEIGHT				Y
	READ_CHANNEL6_WEIGHT				Y
	READ_CHANNEL5_WEIGHT				Y
	READ_CHANNEL4_WEIGHT				Y
DMA_WRITE_INT_STATUS_OFF	WR_ABORT_INT_STATUS				Y
	WR_DONE_INT_STATUS				Y
DMA_WRITE_INT_MASK_OFF	WR_ABORT_INT_MASK				Y
	WR_DONE_INT_MASK				Y
DMA_WRITE_INT_CLEAR_OFF	WR_ABORT_INT_CLEAR				Y
	WR_DONE_INT_CLEAR				Y
DMA_WRITE_ERR_STATUS_OFF	LINKLIST_ELEMENT_FETCH_ERR_DETECT				Y
	APP_READ_ERR_DETECT				Y
DMA_WRITE_DONE_IMWR_LOW_OFF	DMA_WRITE_DONE_LOW_REG				Y
DMA_WRITE_DONE_IMWR_HIGH_OFF	DMA_WRITE_DONE_HIGH_REG				Y
DMA_WRITE_ABORT_IMWR_LOW_OFF	DMA_WRITE_ABORT_LOW_REG				Y
DMA_WRITE_ABORT_IMWR_HIGH_OFF	DMA_WRITE_ABORT_HIGH_REG				Y
DMA_WRITE_CH01_IMWR_DATA_OFF	WR_CHANNEL_1_DATA				Y
	WR_CHANNEL_0_DATA				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
DMA_WRITE_CH23_IMWR_DATA_OFF	WR_CHANNEL_3_DATA				Y
	WR_CHANNEL_2_DATA				Y
DMA_WRITE_CH45_IMWR_DATA_OFF	WR_CHANNEL_5_DATA				Y
	WR_CHANNEL_4_DATA				Y
DMA_WRITE_CH67_IMWR_DATA_OFF	WR_CHANNEL_7_DATA				Y
	WR_CHANNEL_6_DATA				Y
DMA_WRITE_LINKED_LIST_ERR_EN_OFF	WR_CHANNEL_LLLAIE				Y
	WR_CHANNEL_LLRAIE				Y
DMA_READ_INT_STATUS_OFF	RD_ABORT_INT_STATUS				Y
	RD_DONE_INT_STATUS				Y
DMA_READ_INT_MASK_OFF	RD_ABORT_INT_MASK				Y
	RD_DONE_INT_MASK				Y
DMA_READ_INT_CLEAR_OFF	RD_ABORT_INT_CLEAR				Y
	RD_DONE_INT_CLEAR				Y
DMA_READ_ERR_STATUS_LOW_OFF	LINK_LIST_ELEMENT_FETCH_ERR_DETECT				Y
	APP_WR_ERR_DETECT				Y
DMA_READ_ERR_STATUS_HIGH_OFF	DATA_POISIONING				Y
	CPL_TIMEOUT				Y
	CPL_ABORT				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	UNSUPPORTED_REQ				Y
DMA_READ_LINKED_LIST_ERR_EN_OFF	RD_CHANNEL_LLLAIE				Y
	RD_CHANNEL_LLRAIE				Y
DMA_READ_DONE_IMWR_LOW_OFF	DMA_READ_DONE_LOW_REG				Y
	DMA_READ_DONE_HIGH_REG				Y
DMA_READ_ABORT_IMWR_LOW_OFF	DMA_READ_ABORT_LOW_REG				Y
DMA_READ_ABORT_IMWR_HIGH_OFF	DMA_READ_ABORT_HIGH_REG				Y
DMA_READ_CH01_IMWR_DATA_OFF	RD_CHANNEL_1_DATA				Y
	RD_CHANNEL_0_DATA				Y
DMA_READ_CH23_IMWR_DATA_OFF	RD_CHANNEL_3_DATA				Y
	RD_CHANNEL_2_DATA				Y
DMA_READ_CH45_IMWR_DATA_OFF	RD_CHANNEL_5_DATA				Y
	RD_CHANNEL_4_DATA				Y
DMA_READ_CH67_IMWR_DATA_OFF	RD_CHANNEL_7_DATA				Y
	RD_CHANNEL_6_DATA				Y
DMA_WRITE_ENGINE_CHGROUP_OFF	DMA_WRITE_ENGINE_CHGROUP_ENABLE				Y
	DMA_WRITE_ENGINE_CHGROUP_END				Y
	DMA_WRITE_ENGINE_CHGROUP_START				Y
DMA_READ_ENGINE_CHGROUP_OFF	DMA_READ_ENGINE_CHGROUP_ENABLE				Y
	DMA_READ_ENGINE_CHGROUP_END				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	DMA_READ_ENGINE_CHGROUP_START				Y
DMA_WRITE_ENGINE_HSHAKE_CNT_LOW_OFF	DMA_WRITE_ENGINE_HSHAKE_CNT_CH3				Y
	DMA_WRITE_ENGINE_HSHAKE_CNT_CH2				Y
	DMA_WRITE_ENGINE_HSHAKE_CNT_CH1				Y
	DMA_WRITE_ENGINE_HSHAKE_CNT_CH0				Y
DMA_WRITE_ENGINE_HSHAKE_CNT_HIGH_OFF	DMA_WRITE_ENGINE_HSHAKE_CNT_CH7				Y
	DMA_WRITE_ENGINE_HSHAKE_CNT_CH6				Y
	DMA_WRITE_ENGINE_HSHAKE_CNT_CH5				Y
	DMA_WRITE_ENGINE_HSHAKE_CNT_CH4				Y
DMA_READ_ENGINE_HSHAKE_CNT_LOW_OFF	DMA_READ_ENGINE_HSHAKE_CNT_CH3				Y
	DMA_READ_ENGINE_HSHAKE_CNT_CH2				Y
	DMA_READ_ENGINE_HSHAKE_CNT_CH1				Y
	DMA_READ_ENGINE_HSHAKE_CNT_CH0				Y
DMA_READ_ENGINE_HSHAKE_CNT_HIGH_OFF	DMA_READ_ENGINE_HSHAKE_CNT_CH7				Y
	DMA_READ_ENGINE_HSHAKE_CNT_CH6				Y
	DMA_READ_ENGINE_HSHAKE_CNT_CH5				Y
	DMA_READ_ENGINE_HSHAKE_CNT_CH4				Y
DMA_WRITE_CH0_PWR_EN_OFF	DMA_WRITE_CH0_PWR_EN				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
DMA_WRITE_CH1_PWR_EN_OFF	DMA_WRITE_CH1_PWR_EN				Y
DMA_WRITE_CH2_PWR_EN_OFF	DMA_WRITE_CH2_PWR_EN				Y
DMA_WRITE_CH3_PWR_EN_OFF	DMA_WRITE_CH3_PWR_EN				Y
DMA_WRITE_CH4_PWR_EN_OFF	DMA_WRITE_CH4_PWR_EN				Y
DMA_WRITE_CH5_PWR_EN_OFF	DMA_WRITE_CH5_PWR_EN				Y
DMA_WRITE_CH6_PWR_EN_OFF	DMA_WRITE_CH6_PWR_EN				Y
DMA_WRITE_CH7_PWR_EN_OFF	DMA_WRITE_CH7_PWR_EN				Y
DMA_READ_CH0_PWR_EN_OFF	DMA_READ_CH0_PWR_EN				Y
DMA_READ_CH1_PWR_EN_OFF	DMA_READ_CH1_PWR_EN				Y
DMA_READ_CH2_PWR_EN_OFF	DMA_READ_CH2_PWR_EN				Y
DMA_READ_CH3_PWR_EN_OFF	DMA_READ_CH3_PWR_EN				Y
DMA_READ_CH4_PWR_EN_OFF	DMA_READ_CH4_PWR_EN				Y
DMA_READ_CH5_PWR_EN_OFF	DMA_READ_CH5_PWR_EN				Y
DMA_READ_CH6_PWR_EN_OFF	DMA_READ_CH6_PWR_EN				Y
DMA_READ_CH7_PWR_EN_OFF	DMA_READ_CH7_PWR_EN				Y
DMA_CH_CONTROL1_OFF_WRCH_0	DMA_TC				Y
	DMA_RESERVED5				Y
	DMA_RO				Y
	DMA_NS_DST				Y
	DMA_NS_SRC				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	DMA_ELEMENT_PREFETCH				Y
	DMA_MEM_TYPE				Y
	DMA_FUNC_NUM				Y
	DMA_RESERVED1				Y
	LLE				Y
	CCS				Y
	DMA_RESERVED0				Y
	CS				Y
	RIE				Y
	LIE				Y
	LLP				Y
	TCB				Y
	CB				Y
DMA_CH_CONTROL1_OFF_WRCH_	DMA_AT				Y
	DMA_TC				Y
	DMA_RESERVED5				Y
	DMA_RO				Y
	DMA_NS_DST				Y
	DMA_NS_SRC				Y
	DMA_ELEMENT_PREFETCH				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	DMA_MEM_TYPE				Y
	DMA_FUNC_NUM				Y
	DMA_RESERVED1				Y
	LLE				Y
	CCS				Y
	DMA_RESERVED0				Y
	CS				Y
	RIE				Y
	LIE				Y
	LLP				Y
	TCB				Y
	CB				Y
DMA_CH_CONTROL1_OFF_RDCH_0	DMA_AT				Y
	DMA_TC				Y
	DMA_RESERVED5				Y
	DMA_RO				Y
	DMA_NS_DST				Y
	DMA_NS_SRC				Y
	DMA_ELEMENT_PREFETCH				Y
	DMA_MEM_TYPE				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	DMA_FUNC_NUM				Y
	DMA_RESERVED1				Y
	LLE				Y
	CCS				Y
	DMA_RESERVED0				Y
	CS				Y
	RIE				Y
	LIE				Y
	LLP				Y
	TCB				Y
	CB				Y
DMA_CH_CONTROL1_OFF_RDCH_	DMA_AT				Y
	DMA_TC				Y
	DMA_RESERVED5				Y
	DMA_RO				Y
	DMA_NS_DST				Y
	DMA_NS_SRC				Y
	DMA_ELEMENT_PREFETCH				Y
	DMA_MEM_TYPE				Y
	DMA_FUNC_NUM				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	DMA_RESERVED1				Y
	LLE				Y
	CCS				Y
	DMA_RESERVED0				Y
	CS				Y
	RIE				Y
	LIE				Y
	LLP				Y
	TCB				Y
	CB				Y
DMA_CH_CONTROL2_OFF_WRCH_0	DMA_TH				Y
	DMA_PH				Y
	DMA_RESERVED3				Y
	DMA_ST				Y
	DMA_VF_RESERVED				Y
	DMA_VF				Y
	DMA_VF_EN				Y
DMA_CH_CONTROL2_OFF_WRCH_	DMA_TH				Y
	DMA_PH				Y
	DMA_RESERVED3				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	DMA_ST				Y
	DMA_VF_RESERVED				Y
	DMA_VF				Y
	DMA_VF_EN				Y
DMA_CH_CONTROL2_OFF_RDCH_0	DMA_TH				Y
	DMA_PH				Y
	DMA_RESERVED3				Y
	DMA_ST				Y
	DMA_VF_RESERVED				Y
	DMA_VF				Y
	DMA_VF_EN				Y
DMA_CH_CONTROL2_OFF_RDCH_	DMA_TH				Y
	DMA_PH				Y
	DMA_RESERVED3				Y
	DMA_ST				Y
	DMA_VF_RESERVED				Y
	DMA_VF				Y
	DMA_VF_EN				Y
DMA_TRANSFER_SIZE_OFF_WRCH_0	DMA_TRANSFER_SIZE				Y
DMA_TRANSFER_SIZE_OFF_WRCH_	DMA_TRANSFER_SIZE				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
DMA_TRANSFER_SIZE_OFF_RDCH_0	DMA_TRANSFER_SIZE				Y
DMA_TRANSFER_SIZE_OFF_RDCH_	DMA_TRANSFER_SIZE				Y
DMA_SAR_LOW_OFF_WRCH_0	SRC_ADDR_REG_LOW				Y
DMA_SAR_LOW_OFF_WRCH_	SRC_ADDR_REG_LOW				Y
DMA_SAR_LOW_OFF_RDCH_0	SRC_ADDR_REG_LOW				Y
DMA_SAR_LOW_OFF_RDCH_	SRC_ADDR_REG_LOW				Y
DMA_SAR_HIGH_OFF_WRCH_0	SRC_ADDR_REG_HIGH				Y
DMA_SAR_HIGH_OFF_WRCH_	SRC_ADDR_REG_HIGH				Y
DMA_SAR_HIGH_OFF_RDCH_0	SRC_ADDR_REG_HIGH				Y
DMA_SAR_HIGH_OFF_RDCH_	SRC_ADDR_REG_HIGH				Y
DMA_DAR_LOW_OFF_WRCH_0	DST_ADDR_REG_LOW				Y
DMA_DAR_LOW_OFF_WRCH_	DST_ADDR_REG_LOW				Y
DMA_DAR_LOW_OFF_RDCH_0	DST_ADDR_REG_LOW				Y
DMA_DAR_LOW_OFF_RDCH_	DST_ADDR_REG_LOW				Y
DMA_DAR_HIGH_OFF_WRCH_0	DST_ADDR_REG_HIGH				Y
DMA_DAR_HIGH_OFF_WRCH_	DST_ADDR_REG_HIGH				Y
DMA_DAR_HIGH_OFF_RDCH_0	DST_ADDR_REG_HIGH				Y
DMA_DAR_HIGH_OFF_RDCH_	DST_ADDR_REG_HIGH				Y
DMA_LLP_LOW_OFF_WRCH_0	LLP_LOW				Y
DMA_LLP_LOW_OFF_WRCH_	LLP_LOW				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
DMA_LLP_LOW_OFF_RDCH_0	LLP_LOW				Y
DMA_LLP_LOW_OFF_RDCH_	LLP_LOW				Y
DMA_LLP_HIGH_OFF_WRCH_0	LLP_HIGH				Y
DMA_LLP_HIGH_OFF_WRCH_	LLP_HIGH				Y
DMA_LLP_HIGH_OFF_RDCH_0	LLP_HIGH				Y
DMA_LLP_HIGH_OFF_RDCH_	LLP_HIGH				Y
IATU_REGION_CTRL_1_OFF_OUTBOUND_0	CTRL_1_FUNC_NUM				Y
	PH				Y
	AT				Y
	INCREASE_REGION_SIZE				Y
	TH				Y
	IDO				Y
	ATTR				Y
	TD				Y
	TC				Y
	TYPE				Y
IATU_REGION_CTRL_1_OFF_OUTBOUND_	CTRL_1_FUNC_NUM				Y
	PH				Y
	AT				Y
	INCREASE_REGION_SIZE				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	TH				Y
	IDO				Y
	ATTR				Y
	TD				Y
	TC				Y
	TYPE				Y
IATU_REGION_CTRL_1_OFF_INBOUND_0	CTRL_1_FUNC_NUM				Y
	PH				Y
	AT				Y
	INCREASE_REGION_SIZE				Y
	TH				Y
	IDO				Y
	ATTR				Y
	TD				Y
	TC				Y
	TYPE				Y
IATU_REGION_CTRL_1_OFF_INBOUND_	CTRL_1_FUNC_NUM				Y
	PH				Y
	AT				Y
	INCREASE_REGION_SIZE				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	TH				Y
	IDO				Y
	ATTR				Y
	TD				Y
	TC				Y
	TYPE				Y
IATU_REGION_CTRL_2_OFF_OUTBOUND_0	REGION_EN				Y
	INVERT_MODE				Y
	CFG_SHIFT_MODE				Y
	DMA_BYPASS				Y
	FUNC_BYPASS				Y
	SNP				Y
	HEADER_SUBSTITUTE_EN				Y
	INHIBIT_PAYLOAD				Y
	TLP_HEADER_FIELDS_BYPASS				Y
	MSB2BITS_TAG				Y
	TAG_SUBSTITUTE_EN				Y
	TAG				Y
	MSG_CODE				Y
IATU_REGION_CTRL_2_OFF_OUTBOUND_	REGION_EN				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	INVERT_MODE				Y
	CFG_SHIFT_MODE				Y
	DMA_BYPASS				Y
	FUNC_BYPASS				Y
	SNP				Y
	HEADER_SUBSTITUTE_EN				Y
	INHIBIT_PAYLOAD				Y
	TLP_HEADER_FIELDS_BYPASS				Y
	MSB2BITS_TAG				Y
	TAG_SUBSTITUTE_EN				Y
	TAG				Y
	MSG_CODE				Y
IATU_REGION_CTRL_2_OFF_INBOUND_0	REGION_EN				Y
	INVERT_MODE				Y
	CFG_SHIFT_MODE				Y
	MSG_TYPE_MATCH_MODE				Y
	SINGLE_ADDR_LOC_TRANS_EN				Y
	MATCH_MODE				Y
	FUZZY_TYPE_MATCH_CODE				Y
	VFBAR_MATCH_MODE_EN				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESPONSE_CODE				Y
	PH_MATCH_EN				Y
	MSG_CODE_MATCH_EN				Y
	VF_MATCH_EN				Y
	FUNC_NUM_MATCH_EN				Y
	AT_MATCH_EN				Y
	TH_MATCH_EN				Y
	ATTR_MATCH_EN				Y
	TD_MATCH_EN				Y
	TC_MATCH_EN				Y
	BAR_NUM				Y
	MSG_CODE				Y
IATU_REGION_CTRL_2_OFF_INBOUND_	REGION_EN				Y
	INVERT_MODE				Y
	CFG_SHIFT_MODE				Y
	MSG_TYPE_MATCH_MODE				Y
	SINGLE_ADDR_LOC_TRANS_EN				Y
	MATCH_MODE				Y
	FUZZY_TYPE_MATCH_CODE				Y
	VFBAR_MATCH_MODE_EN				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	RESPONSE_CODE				Y
	PH_MATCH_EN				Y
	MSG_CODE_MATCH_EN				Y
	VF_MATCH_EN				Y
	FUNC_NUM_MATCH_EN				Y
	AT_MATCH_EN				Y
	TH_MATCH_EN				Y
	ATTR_MATCH_EN				Y
	TD_MATCH_EN				Y
	TC_MATCH_EN				Y
	BAR_NUM				Y
	MSG_CODE				Y
IATU_LWR_BASE_ADDR_OFF_OUTBOUND_0	LWR_BASE_RW				Y
	LWR_BASE_HW				Y
IATU_LWR_BASE_ADDR_OFF_OUTBOUND_	LWR_BASE_RW				Y
	LWR_BASE_HW				Y
IATU_LWR_BASE_ADDR_OFF_INBOUND_0	LWR_BASE_RW				Y
	LWR_BASE_HW				Y
IATU_LWR_BASE_ADDR_OFF_INBOUND_	LWR_BASE_RW				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	LWR_BASE_HW				Y
IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_0	UPPER_BASE_RW				Y
IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_	UPPER_BASE_RW				Y
IATU_UPPER_BASE_ADDR_OFF_INBOUND_0	UPPER_BASE_RW				Y
IATU_UPPER_BASE_ADDR_OFF_INBOUND_	UPPER_BASE_RW				Y
IATU_LIMIT_ADDR_OFF_OUTBOUND_0	LIMIT_ADDR_RW				Y
	LIMIT_ADDR_HW				Y
	CBUF_INCR				Y
IATU_LIMIT_ADDR_OFF_OUTBOUND_	LIMIT_ADDR_RW				Y
	LIMIT_ADDR_HW				Y
	CBUF_INCR				Y
IATU_LIMIT_ADDR_OFF_INBOUND_0	LIMIT_ADDR_RW				Y
	LIMIT_ADDR_HW				Y
	CBUF_INCR				Y
IATU_LIMIT_ADDR_OFF_INBOUND_	LIMIT_ADDR_RW				Y
	LIMIT_ADDR_HW				Y
	CBUF_INCR				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_0	LWR_TARGET_RW_OUTBOUND				Y
LWR_TARGET_RW_OUTBOUND	IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_				Y
IATU_LWR_TARGET_ADDR_OFF_INBOUND_0	LWR_TARGET_RW				Y
	LWR_TARGET_HW				Y
IATU_LWR_TARGET_ADDR_OFF_INBOUND_	LWR_TARGET_RW				Y
	LWR_TARGET_HW				Y
IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_0	UPPER_TARGET_RW				Y
IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_	UPPER_TARGET_RW				Y
IATU_UPPER_TARGET_ADDR_OFF_INBOUND_0	UPPER_TARGET_RW				Y
IATU_UPPER_TARGET_ADDR_OFF_INBOUND_	UPPER_TARGET_RW				Y
IATU_REGION_CTRL_3_OFF_OUTBOUND_0	VF_ACTIVE				Y
	RSVDP_VF_NUMBER				Y
	VF_NUMBER				Y
IATU_REGION_CTRL_3_OFF_OUTBOUND_	VF_ACTIVE				Y
	RSVDP_VF_NUMBER				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	VF_NUMBER				Y
IATU_REGION_CTRL_3_OFF_INBOUND_0	VF_ACTIVE				Y
	RSVDP_VF_NUMBER				Y
	VF_NUMBER				Y
IATU_REGION_CTRL_3_OFF_INBOUND_	VF_ACTIVE				Y
	RSVDP_VF_NUMBER				Y
	VF_NUMBER				Y
IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_0	UPPR_LIMIT_ADDR_RW				Y
	UPPR_LIMIT_ADDR_HW				Y
IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_	UPPR_LIMIT_ADDR_RW				Y
	UPPR_LIMIT_ADDR_HW				Y
IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_0	UPPR_LIMIT_ADDR_RW				Y
	UPPR_LIMIT_ADDR_HW				Y
IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_	UPPR_LIMIT_ADDR_RW				Y
	UPPR_LIMIT_ADDR_HW				Y
ACK_F_ASPM_CTRL_OFF	COMMON_CLK_N_FTS	Y			
GEN3_EQ_CONTROL_OFF	GEN3_SUPPORT_FINITE_EQ_REQUEST				Y
	GEN3_EQ_REQ_NUM				Y
	GEN3_EQ_FOM_INC_INITIAL_EVAL				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	GEN3_EQ_PSET_REQ_VEC				Y
	GEN3_EQ_EVAL_2MS_DISABLE				Y
GEN4_LANE_MARGINING_1_OFF	GEN4_MARGINING_MAX_VOLTAGE_OFFSET				Y
	GEN4_MARGINING_NUM_VOLTAGE_STEPS				Y
	GEN4_MARGINING_MAX_TIMING_OFFSET				Y
	GEN4_MARGINING_NUM_TIMING_STEPS				Y
GEN4_LANE_MARGINING_2_OFF	MARGINING_RATE_MODE				Y
	GEN4_MARGINING_IND_ERROR_SAMPLER				Y
	GEN4_MARGINING_SAMPLE_REPORTING_METHOD				Y
	GEN4_MARGINING_IND_LEFT_RIGHT_TIMING				Y
	GEN4_MARGINING_IND_UP_DOWN_VOLTAGE				Y
	GEN4_MARGINING_VOLTAGE_SUPPORTED				Y
	GEN4_MARGINING_MAXLANES				Y
	GEN4_MARGINING_SAMPLE_RATE_TIMING				Y
	GEN4_MARGINING_SAMPLE_RATE_VOLTAGE				Y
CXL_VLSM_CSR_REG_OFF	CXL_VLSM_MC_ALMP_ERROR			Y	
	CXL_VLSM_IO_ALMP_ERROR			Y	

1.1.10 Changes to RAM Sizes

This section details the changes to the default RAM sizes that have occurred since the last production release. It does not detail changes that are associated with new or additional features that you enable on your current configuration

Caution To determine the precise changes to RAM sizes for your actual controller configuration, you can compare the coreConsultant generated RAM sizes for the previous and current releases. For more details, see the "RAM Requirements" section in the Architecture chapter of the *Databook*.

The following changes have occurred for this release.

Table 1-6 RAM Changes

RAM Name	Change
No changes in this release.	

1.1.11 Changes to Configuration Parameters

This section details any changes to the configuration parameters of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the configuration parameters are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

If you intend to source an existing configuration batch file, then you must first convert your configuration file, as described in "Changes from the Last Release" on page 6. If you are not sourcing an existing configuration batch file, then you should be still aware of changes to the default value of some configuration parameters.

Caution	To ensure that your existing configuration absorbs all changes to default parameters updated for this release, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed. Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item. The *Write default Parameter* should only be used for debugging.

Table 1-7 Configuration Parameter Changes

Name	Change
IDE_SIZE	**Default value** changed **from:** 0x58 **to:** 0x0
CX_MAC_PHY_FREQ_VALID	**Default value** changed **from:** function_of (CX_MAX_PCIE_SPEED CX_MAC_SMODE_GEN1 CX_MAC_SMODE_GEN2 CX_MAC_SMODE_GEN3 CX_MAC_SMODE_GEN4 CX_MAC_SMODE_GEN5 CX_PHY_SMODE_GEN1 CX_PHY_SMODE_GEN2 CX_PHY_SMODE_GEN3 CX_PHY_SMODE_GEN4 CX_PHY_SMODE_GEN5) **to:** function_of (CX_MAX_PCIE_SPEED CX_MAC_SMODE_GEN1 CX_MAC_SMODE_GEN2 CX_MAC_SMODE_GEN3 CX_MAC_SMODE_GEN4 CX_MAC_SMODE_GEN5 CX_MAC_SMODE_GEN6 CX_PHY_SMODE_GEN1 CX_PHY_SMODE_GEN2 CX_PHY_SMODE_GEN3 CX_PHY_SMODE_GEN4 CX_PHY_SMODE_GEN5 CX_PHY_SMODE_GEN6)
CX_FREQ_STEP_EN	**Default value** changed **from:** (CX_MAC_SMODE_GEN1 != CX_PHY_SMODE_GEN1) || (CX_MAC_SMODE_GEN2 != CX_PHY_SMODE_GEN2) || (CX_MAC_SMODE_GEN3 != CX_PHY_SMODE_GEN3) || (CX_MAC_SMODE_GEN4 != CX_PHY_SMODE_GEN4) || (CX_MAC_SMODE_GEN5 != CX_PHY_SMODE_GEN5) || (CX_PIPERX_MULTI_BLOCK==1) **to:** (CX_MAC_SMODE_GEN1 != CX_PHY_SMODE_GEN1) || (CX_MAC_SMODE_GEN2 != CX_PHY_SMODE_GEN2) || (CX_MAC_SMODE_GEN3 != CX_PHY_SMODE_GEN3) || (CX_MAC_SMODE_GEN4 != CX_PHY_SMODE_GEN4) || (CX_MAC_SMODE_GEN5 != CX_PHY_SMODE_GEN5) || (CX_MAC_SMODE_GEN6 != CX_PHY_SMODE_GEN6) || (CX_PIPERX_MULTI_BLOCK==1)

Name	Change
CX_RETIMER_LATENCY	**Default Value** changed **from:** [<functionof> CX_MAX_RETIMER CX_SRIS_SUPPORT CX_MAX_ MTU CX_GEN5_SPEED CX_GEN4_SPEED CX_GEN3_SPEED CX_GEN2_ SPEED] **to:** CX_MAX_PCIE_SPEED]
CX_10BITS_TAG	**Default value** changed **from:** (((CX_GEN4_SPEED_VALUE == 1) || (CX_MAX_TAG > 255) || (CX_REMOTE_MAX_TAG > 255)) || ((AMBA_INTERFACE != 1))? 1: 0 **to:** (((CX_GEN4_SPEED_VALUE == 1) || (CX_MAX_TAG > 255) || (CX_REMOTE_MAX_TAG > 255)) || (CX_14BITS_TAG == 1)) && (AMBA_INTERFACE != 1))? 1: 0 **Enabled** changed **from:** ((AMBA_INTERFACE != 1) && (CX_GEN4_SPEED_VALUE == 0) && (CX_MAX_TAG <= 255) && (CX_REMOTE_MAX_TAG <= 255)) **to:** ((AMBA_INTERFACE != 1) && (CX_GEN4_SPEED_VALUE == 0) && (CX_MAX_TAG <= 255) && (CX_14BITS_TAG == 0) && (CX_REMOTE_MAX_TAG <= 255))
CX_MODIFIED_TS_FORMAT_SUPPORT	**Default value** changed **from:** CX_GEN5_SPEED || CX_AP_SUPPORT) **to:** CX_GEN5_SPEED || CX_AP_SUPPORT) && (CX_MAX_PCIE_SPEED < 6
PL_LIMIT	**Value** changed **from:** 2304, ..., 3212 **to:** 2304, ..., 3220 **Default Value** changed **from:** 3212 **to:** 3220
CC_ORDRB_EN	**Enabled** changed **from:** Always **to:** ((AMBA_INTERFACE==2) || (AMBA_INTERFACE==3) || (AMBA_INTERFACE==4))

Name	Change
CC_MSIGIC_EN	**Enabled** changed **from:** C_ORDRB_EN **to:** (CC_DEVICE_TYPE==CC_RC || CC_DEVICE_TYPE==CC_DM) && CC_ORDRB_EN
CX_CPL_TO_RANGES_ENABLE	**Default Value** changed **from:** (CX_PCIE_MODE == PCIE_OVER_CIO) ? 1 : 0 **to:** CC_DEVICE_TYPE!=CC_SW && CX_PCIE_MODE==PCIE_OVER_CIO) ? 1 : 0
FIRST_VF_OFFSET_ARI_CAP_HIER1_n	**Default Value** changed **from:** CX_MAX_PCIE_SPEED >= 5 **to:** (CX_NFUNC>=127) ? 256 : (CX_NFUNC>=65) ? 128 : (CX_NFUNC>=33) ? 64 : (CX_NFUNC>=17) ? 32 : (CX_NFUNC>=9) ? 16 : (CX_NFUNC>=5) ? 8 : (CX_NFUNC>=3) ? 4 : CX_NFUNC

1.2 Converting to the Current Release

Sometimes a new controller release might no longer use a certain configuration parameter, or the meaning of that parameter might have changed. The following process helps you convert your current configuration file so that it creates the same RTL with the new controller.

1. Open coreConsultant and create an unconfigured workspace from the newly installed controller.
2. In the coreConsultant command line, enter the following command:

   `parse_configfile my_configfile.config`

   where `my_configfile.config` is your current configuration file. This command creates an updated configuration file in your working directory as follows:

   `my_configfile.config.new`
3. In the coreConsultant command line, enter the following command:

   `source my_configfile.config.new`
4. Select Apply to generate the new RTL with the updated or translated parameters.
5. From the File Menu, select Write Batch Script and save the configuration file for the new release.
6. When you source the updated configuration file in coreConsultant, you can *ignore any new warnings* about parameter settings that are not relevant to, or not enabled in your configuration.

Attention

Writing Out Your Configuration File

To ensure that your existing configuration absorbs all changes to default parameters updated for this release, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

You must convert your configuration file. Failure to do so, can result in:

- Your configuration file being incompatible with the current release.
- Functional, architectural, RAM, and I/O changes when the default of some configuration parameters change from release to release.

1.3 Fixed Defects and Enhancements (STARs on the Web)

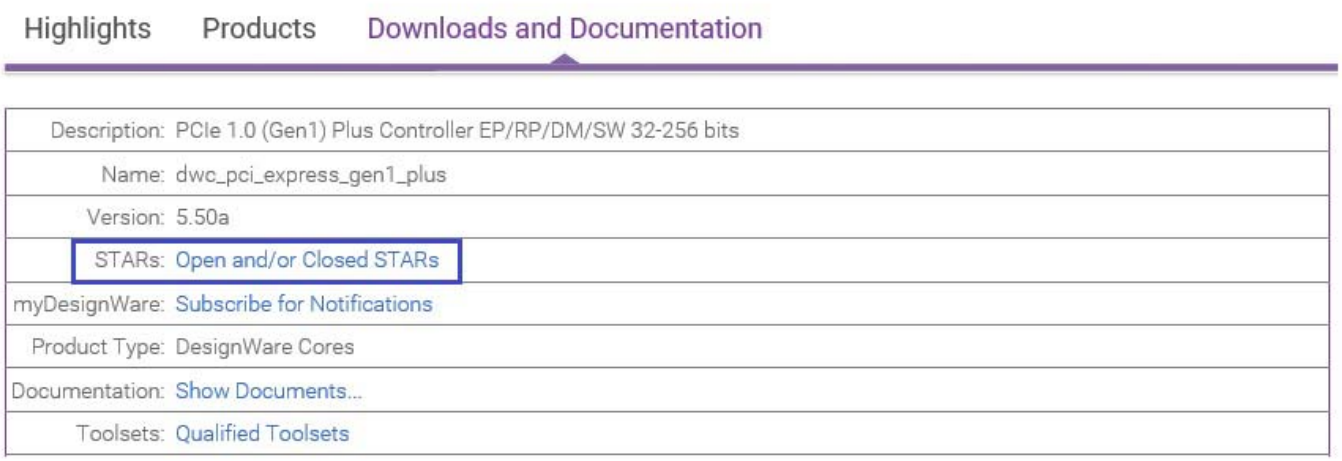
Defects fixed in release 6.00a of the controller are listed in the STAR report for release 6.00a in STARs on the Web.

Table 1-8 Controller STAR Report Location

Controller	Location
PCIe Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_controllers
CXL Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_cxl_controller
CCIX Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_ccix_controller

(A SolvNetPlus ID is required to view STAR reports.)

Figure 1-1 Accessing STARs on the Web through SolvNetPlus



Enhancement STARs are identifiable by the letter “E” in the Severity column, and fixed defect STARs are identifiable by the letter “B.” An E4 or B4 has the highest severity. Clicking on the tab corresponding to 6.00a produces a STAR report of closed STARS for this release. For previous controller versions, click the tab corresponding to the version in question.

1.4 Known Issues and Limitations

You can view a complete list of functional problem reports for this product, including problems identified after product release, by accessing the STAR report on the Web. For more details, see "Fixed Defects and Enhancements (STARs on the Web)" on page 79. You must have a SolvNetPlus ID to view STAR reports. This release has the following known tool and packaging issues at the time of release.

- "Packaged coreConsultant Test Limitations"
- "VTB Limitations"
- "Design Example"
- "Unique Case Violation Simulation Message"
- "coreConsultant Memory Map Limitations"

1.4.1 Packaged coreConsultant Test Limitations

We invite you to submit your coreConsultant configuration for review. Because of the very large configuration space, it is not possible to regress every configuration before a release is made. Synopsys is continually running fixed and randomized configurations, but it is possible that your exact configuration has not been regressed. Test case failures might occur because of improper test bench configuration. In that case open a case through SolvNetPlus.

1.4.2 Unpacking Configurations with CX_NFUNC >32

For configurations with number of Physical Functions greater than 32 (`CX_NFUNC >32`), the controller uses the same structure of IP-XACT for native and AMBA configuration for DBI register accesses.

- In case of native and DBI accesses, there are dedicated pins for PFs and VFs and you must assert as per the scenarios.
- For the `AXI_POPULATED` based configuration, you must configure the dedicated `DBI_FUNCTION_BANK_CTRL_REG` field of `DBI_FUNCTION_BANK_CTRL_REG_OFF` register for `NFUNC > 32`.

1.4.3 VTB Limitations

The following limitations apply to the current release of the VTB:

- Not backward compatible with previous releases
- Not UVM compliant

1.4.4 Design Example

The design example in `<workspace>/examples/DWC_pcie_clkrst.v` has been functionally verified, but has not been explicitly targeted for verification metrics. However, it has been used by Synopsys in the verification and regression environments for all controller configurations; including verification of all power transitions for the controller.

`<workspace>/src/Phy/<arch>/phy_instance.vh` instantiates your Synopsys PHY of choice inside `<workspace>/examples/pcie_iip_device.sv`. These connections between controller and PHY are intended for simulation purposes in the demonstration testbench (VTB) only. You must not reuse `phy_instance.vh` for direct integration within your SoC without reviewing connectivity with Synopsys Support first. The instantiation of the PHY might have ports tie-off or a configuration which might not be optimal or could be even incorrect for your specific use scenario.

1.4.5 Unique Case Violation Simulation Message

The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

There is a known simulator issue with a "Unique case violation" message that occurs sometimes while running simulations with VCS outside of coreConsultant. You can ignore these messages.

To avoid these messages, use the `-xlrm uniq_prior_final` compile option in VCS. The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

1.4.6 coreConsultant Memory Map Limitations

The controller supports the generation of configuration-specific register maps as described in the "Register Configuration Space" chapter in the *Databook*. For SR-IOV configurations (`CX_SRIOV_ENABLE =1`), the following limitations apply.

Table 1-9 coreConsultant Report File Limitations for SR-IOV Configurations

CX_NVFUNC	IP-XACT (IP-XACT XML)	RALF and C Headers (No limitations)	Register Report (DocBook XML) Also applies to Databook
1–256	Defines default #VFs in each PF	Defines default #VFs in each PF	Defines only first VF in each PF
257–4096	Defines only[a] first VF in each PF	Defines default #VFs in each PF	Defines only first VF in each PF

a. For details on how to populate remaining VFs in the IP-XACT file, see "Populating IP-XACT File Manually" in the "Creating Optional Views and Reports" section in the "Configuring the controller" chapter of the User Guide.

1.4.7 Third-party Simulator Limitations

When you are using the QuestaSim 2021.3 simulator, and if you select the HDMA option, compilation failure can occur because the QuestaSim 2021.3 does not support System Verilog IEEE 2012 standard.

1.5 Web Resources

For more information, check the following Synopsys online resources:

- DesignWare IP product information: https://www.synopsys.com/designware-ip.html
- Your custom DesignWare IP page: https://www.synopsys.com/dw/mydesignware.php
- Documentation through SolvNetPlus: https://solvnetplus.synopsys.com (SolvnetID required)
- Synopsys Common Licensing (SCL): https://www.synopsys.com/keys

1.6 Synopsys Statement on Inclusivity and Diversity

Synopsys is committed to creating an inclusive environment where every employee, customer, and partner feels welcomed. We are reviewing and removing exclusionary language from our products and supporting customer-facing collateral. Our effort also includes internal initiatives to remove biased language from our engineering and working environment, including terms that are embedded in our software and IPs. At the same time, we are working to ensure that our web content and software applications are usable to people of varying abilities. You may still find examples of non-inclusive language in our software or documentation as our IPs implement industry-standard specifications that are currently under review to remove exclusionary language.

1.7 Customer Support

To obtain support for your product, prepare the required files and contact the support center using one of the methods described:

- Prepare the following debug information, if applicable:
  - For environment set-up problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, select the following menu:
    - **File > Build Debug Tar-file**

    Check all the boxes in the dialog box that apply to your issue. This option gathers all the Synopsys product data needed to begin debugging an issue and writes it to the <*core tool startup directory*>/debug.tar.gz file.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD).
    - Identify the hierarchy path to the DesignWare instance.
    - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- *For the fastest response*, enter a case through SolvNetPlus:

  a. https://solvnetplus.synopsys.com

Note SolvNetPlus does not support Internet Explorer. Use a supported browser such as Microsoft Edge, Google Chrome, Mozilla Firefox, or Apple Safari.

  b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).

  c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

     Make sure to include the following:

     - **Product L1:** DesignWare Cores
     - **Product L2:** PCI Express

  d. After creating the case, attach any debug files you created.

     For more information about general usage information, refer to the following article in SolvNetPlus:

     https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
  - Attach any debug files you created.
- Or, telephone your local support center:

- North America:
  Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
- All other countries:
  https://www.synopsys.com/support/global-support-centers.html

2

Release Notes: 5.97a

These release notes describe the changes in this release *(5.97a)* relative to the previous production release *(5.96a)*.This release note contains the following sections:

- "Product Updates" on page 88
- "Changes to I/O" on page 91
- "Changes to Software View (Register Map)" on page 103
- "Changes to RAM Sizes" on page 105
- "Changes to Configuration Parameters" on page 106
- "Converting to the Current Release" on page 112
- "Known Issues and Limitations" on page 113
- "Details of Fixed Defects and Enhancements" on page 116
- "Synopsys Statement on Inclusivity and Diversity" on page 117
- "Customer Support" on page 118

2.1 Product Updates

This release contains the following major updates and other minor updates (indicated in "Details of Fixed Defects and Enhancements" on page 116).

Note

In this release,

- CXL controller is available as an LCA (Limited Customer Availability) feature and must not be used for tape out.
- PCIe controller is compatible with the following IDE Security Modules:
  a. DWC_cxl_ide_1.00a-lca03 (for CXL configurations)
  b. DWC_pcie_ide_1.03a-lca02 (for PCIe configurations)

2.1.1 PCIe Configurations Supported for the CXL Controller

Table 2-1 describes the newly added controller support for 128-bit and 256-bit.

Table 2-1 PCIe Configurations Supported for the CXL Controller

core_clk @ Gen{1,2,3,4,5} speed (in MHz)		Max Link Width	
		128-bit	256-bit
Gen5 Configuration	62.5,125,250,500,1000	x4	x8
	125,250,250,500,1000	x4	x8
	62.5,125,125,250,500	N/A	x4

For more information see "Frequency, Speed, and Width Support" section in the "Product Overview" chapter of the *CXL Databook*.

2.1.2 CXL 2.0 Registers

In this enhancement, the following registers are implemented by default in the controller:

- `PF0_CXL_REG_LOCATOR_CAP` - Register Locator DVSEC (in any CXL2.0 configuration),
- `PF0_CXL_GPF_PORT_CAP` - GPF DVSEC for CXL Port (in CXL 2.0 RP and CXL Switch DSP configurations), and
- `PF0_CXL_GPF_DEVICE_CAP` - GPF DVSEC for CXL Device (in CXL2.0 Device configurations)

For more information, see the "Register Descriptions" chapter of the *Reference Manual*.

When moving from prior releases to keep the:

- Register Locator DVSEC implemented externally set the `CX_CXL_REGLOC_INTERNAL` parameter to '0'.
- GPF DVSEC for CXL Port implemented externally set the `CX_CXL_PORT_GPF_INTERNAL` parameter to '0'.
- GPF DVSEC for CXL Device implemented externally set the `CX_CXL_DEVICE_GPF_INTERNAL` parameter to '0'.

2.1.3 CXL IDE Error Injection Support

The CXL controller supports the following IDE Error Injections

- IDE MAC:
  - Insert MAC
  - Delete MAC
  - Delay MAC
- IDE TX Plain and IDE RX Secure Interface:
  - TX CRC Error Injection
  - RX CRC Error Injection

For more information, see `CXL_IDE_EINJ_OFF` register in the "Register Descriptions" chapter in the *Reference Manual*.

2.1.4 CXL 2.0 Component Register Mapping

In this enhancement, the controller diverts the CXL 2.0 Component Registers to RTRGT0 independently from the `MEM_FUNC0_BAR0_TARGET_MAP` setting.

For more information, see "CXL2.0 Component Registers" topic in the "Memory Mapped Space" section in the "Controller Operations" chapter of the *CXL Databook*.

2.1.5 CXL Data Poison Interrupt Signals

In this enhancement, the controller indicates to the application when the CXL controller poisons the data due to RASDP uncorrectable error.

For more information, see "SII: Reset/Status Signals" in Signal Descriptions chapter of the *CXL Databook*.

2.1.6 Wire Write Access Control

In this enhancement the controller provides an option to control the wire write access to the `EINJ_ENABLE_REG` register using the `ERR_INJ_WR_DISABLE` field of the `MISC_CONTROL_1_OFF` register.

For more information, see the "Register Descriptions" chapter of the *Reference Manual.*

2.1.7 LTIM, Order Buffer, and MSI-GIC Interface

LTIM is compliant with AMBA LTI Protocol Specification providing an alternative to interface the SMMU. After SMMU memory translation, the MSI (Message Signal Interrupt) routes to the GIC (Generic Interrupt Controller) taking into account PCIe ordering rules and reduces the latency of the interrupt generation. You can enable the LTIM feature by setting the `CC_LTIM_ENABLE` parameter to '1'.

For more information, see LTIM, Order Buffer, and MSI-GIC Interface section in the "AMBA" chapter of the *PCIe Databook*.

Note In this release, the LTIM, Order Buffer, and MSI-GIC is available as an LCA (Limited Customer Availability) feature and must not be used for tape out. Contact Synopsys Support through SolvNetPlus for an unlocking key for this feature.

2.1.8 Request Handling by LBC

The LBC does not block any pending DBI request while processing a non-posted PCIe wire transaction whose completion is ready in LBC and awaits acceptance from XADM.

For more information, see “Local Bus Controller (LBC)" section in the “Controller Operations” chapter of the *PCIe Databook*.

2.1.9 AXI5 Read Data Chunking

The controller supports AXI5 Read Data Chunking feature for configurations with Master Data Bus up conversion (`MASTER_BUS_DATA_WIDTH <PCIE_CORE_DATA_BUS_WIDTH`).

2.1.10 Flop-Based Clock Divider in PCLK as PHY Input Mode

The controller is enhanced to provide flop-based clock division instead of pulse masking division. You can enable this feature by setting the `CX_PIPE_PCLK_DIV_TYPE` parameter to '1'.

For more information, see “Clock Generation Module” in the “Architecture” chapter of the *PCIe Databook*.

2.1.11 PCIe Integrity and Data Encryption (IDE)

In this enhancement, the controller:

- Supports PCRC
- Supports switch port; Full IDE Flow through is not supported
- Processes inbound IDE traffic, with no performance loss due to the presence of PCRC/MAC

For more information, see “PCIe Integrity and Data Encryption (IDE)” chapter of the *PCIe Databook*.

Note In this release, the IDE feature must not be used for tape out.

2.1.12 Sizing the AXI Outbound Completion Composer RAM

In this documentation enhancement, the “Sizing the AXI Outbound Completion Composer RAM” section is added in the “Advanced Information: Area, Power Estimates, and RAM Sizes” appendix of the *PCIe Databook*.

2.1.13 Documentation Updates

From 5.97a release onwards:

- Power Consumption information is available in *PCIe_Power.pdf*.

  For more information, see “Advanced Information: Area, Power Estimates, and RAM Sizes” appendix of the *PCIe Databook*.
- *PCIe_PHY.pdf* is deprecated.

2.2 Changes to I/O

This section details any changes to the I/O of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the I/O are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

The following table enlists the I/O changes that have occurred for all configurations:

Table 2-2 I/O Signals Added, Removed, or Renamed

Name	Type	Change	Comment
cxl_mst_h2d_req_crd	I	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_CACHE_EN && CX_CXL_IS_EP))
cxl_mst_h2d0_rsp_crd	I		
cxl_mst_h2d1_rsp_crd	I		
cxl_mst_h2d_data_crd	I		
cxl_mst_h2d_req[(CX_CXL_CACHE_H2D_REQ_SIZE-1):0]	O		
cxl_mst_h2d0_rsp[(CX_CXL_CACHE_H2D_RESP_SIZE-1):0]	O		
cxl_mst_h2d1_rsp[(CX_CXL_CACHE_H2D_RESP_SIZE-1):0]	O		
cxl_mst_h2d_data[(CX_CXL_CACHE_H2D_DATA_SIZE-1):0]	O		
cxl_mst_h2d_req_chk[(CX_CXL_CACHE_H2D_REQ_CHK_SIZE-1):0]	O	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_CACHE_EN && CX_CXL_IS_EP))&&((CX_CXL_CHI_DATACHK > 0) ? CX_CXL_ENABLE : 0)
cxl_mst_h2d0_rsp_chk[(CX_CXL_CACHE_H2D_RESP_CHK_SIZE-1):0]	O		
cxl_mst_h2d1_rsp_chk[(CX_CXL_CACHE_H2D_RESP_CHK_SIZE-1):0]	O		
cxl_mst_h2d_data_chk[(CX_CXL_CACHE_H2D_DATA_CHK_SIZE-1):0]	O		

Name	Type	Change	Comment
cxl_slv_d2h0_req_crd	O	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_CACHE_EN && CX_CXL_IS_EP))
cxl_slv_d2h1_req_crd	O		
cxl_slv_d2h_rsp_crd	O		
cxl_slv_d2h_data_crd	O		
cxl_slv_d2h0_req[(CX_CXL_CACHE_D2H_REQ_SIZE-1):0]	I		
cxl_slv_d2h1_req[(CX_CXL_CACHE_D2H_REQ_SIZE-1):0]	I		
cxl_slv_d2h_rsp[(CX_CXL_CACHE_D2H_RESP_SIZE-1):0]	I		
cxl_slv_d2h_data[(CX_CXL_CACHE_D2H_DATA_SIZE-1):0]	I		
cxl_slv_d2h0_req_chk[(CX_CXL_CACHE_D2H_REQ_CHK_SIZE-1):0]	I	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_CACHE_EN && CX_CXL_IS_EP))&&((CX_CXL_CHI_DATACHK > 0) ? CX_CXL_ENABLE : 0)
cxl_slv_d2h1_req_chk[(CX_CXL_CACHE_D2H_REQ_CHK_SIZE-1):0]	I		
cxl_slv_d2h_rsp_chk[(CX_CXL_CACHE_D2H_RESP_CHK_SIZE-1):0]	I		
cxl_slv_d2h_data_chk[(CX_CXL_CACHE_D2H_DATA_CHK_SIZE-1):0]	I		
cxl_slv_h2d_req_crd	O	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_CACHE_EN && CX_CXL_IS_RC))
cxl_slv_h2d0_rsp_crd	O		
cxl_slv_h2d1_rsp_crd	O		
cxl_slv_h2d_data_crd	O		
cxl_slv_h2d_req[(CX_CXL_CACHE_H2D_REQ_SIZE-1):0]	I		
cxl_slv_h2d0_rsp[(CX_CXL_CACHE_H2D_RESP_SIZE-1):0]	I		
cxl_slv_h2d1_rsp[(CX_CXL_CACHE_H2D_RESP_SIZE-1):0]	I		
cxl_slv_h2d_data[(CX_CXL_CACHE_H2D_DATA_SIZE-1):0]	I		

Name	Type	Change	Comment
cxl_slv_h2d_req_chk[(CX_CXL_CACHE_H2D_REQ_CHK_SIZE-1):0]	I	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_CACHE_EN && CX_CXL_IS_RC))&&((CX_CXL_CHI_DATACHK > 0) ? CX_CXL_ENABLE : 0)
cxl_slv_h2d0_rsp_chk[(CX_CXL_CACHE_H2D_RESP_CHK_SIZE-1):0]	I		
cxl_slv_h2d1_rsp_chk[(CX_CXL_CACHE_H2D_RESP_CHK_SIZE-1):0]	I		
cxl_slv_h2d_data_chk[(CX_CXL_CACHE_H2D_DATA_CHK_SIZE-1):0]	I		
cxl_mst_d2h0_req_crd	I	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_CACHE_EN && CX_CXL_IS_RC))
cxl_mst_d2h1_req_crd	I		
cxl_mst_d2h_rsp_crd	I		
cxl_mst_d2h_data_crd	I		
cxl_mst_d2h0_req[(CX_CXL_CACHE_D2H_REQ_SIZE-1):0]	O		
cxl_mst_d2h1_req[(CX_CXL_CACHE_D2H_REQ_SIZE-1):0]	O		
cxl_mst_d2h_rsp[(CX_CXL_CACHE_D2H_RESP_SIZE-1):0]	O		
cxl_mst_d2h_data[(CX_CXL_CACHE_D2H_DATA_SIZE-1):0]	O		
cxl_mst_d2h0_req_chk[(CX_CXL_CACHE_D2H_REQ_CHK_SIZE-1):0]	O	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_CACHE_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_CACHE_EN && CX_CXL_IS_RC))&&((CX_CXL_CHI_DATACHK > 0) ? CX_CXL_ENABLE : 0)
cxl_mst_d2h1_req_chk[(CX_CXL_CACHE_D2H_REQ_CHK_SIZE-1):0]	O		
cxl_mst_d2h_rsp_chk[(CX_CXL_CACHE_D2H_RESP_CHK_SIZE-1):0]	O		
cxl_mst_d2h_data_chk[(CX_CXL_CACHE_D2H_DATA_CHK_SIZE-1):0]	O		

Name	Type	Change	Comment
cxl_mst_m2s_req_crd	I	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_MEM_EN && (CX_CXL_IS_EP || CX_CXL_SYMMEM_SUPPORT)))
cxl_mst_m2s_rwd_crd	I		
cxl_mst_m2s_req[(CX_CXL_MEM_M2S_NDR_SIZE-1):0]	O		
cxl_mst_m2s_rwd[(CX_CXL_MEM_M2S_DATA_SIZE-1):0]	O		
cxl_mst_m2s_req_chk[(CX_CXL_MEM_M2S_NDR_CHK_SIZE-1):0]	O	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_MEM_EN && (CX_CXL_IS_EP || CX_CXL_SYMMEM_SUPPORT))) && ((CX_CXL_CHI_DATACHK > 0)? CX_CXL_ENABLE : 0)
cxl_mst_m2s_rwd_chk[(CX_CXL_MEM_M2S_DATA_CHK_SIZE-1):0]	O		
cxl_slv_s2m_ndr_crd	O	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_MEM_EN && (CX_CXL_IS_EP || CX_CXL_SYMMEM_SUPPORT)))
cxl_slv_s2m_drc_crd	O		
cxl_slv_s2m_ndr[(CX_CXL_MEM_S2M_NDR_SIZE-1):0]	I		
cxl_slv_s2m_drc[(CX_CXL_MEM_S2M_DATA_SIZE-1):0]	I		
cxl_slv_s2m_ndr_chk[(CX_CXL_MEM_S2M_NDR_CHK_SIZE-1):0]	I	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_MEM_EN && (CX_CXL_IS_EP || CX_CXL_SYMMEM_SUPPORT))) && ((CX_CXL_CHI_DATACHK > 0)? CX_CXL_ENABLE : 0)
cxl_slv_s2m_drc_chk[(CX_CXL_MEM_S2M_DATA_CHK_SIZE-1):0]	I		

Name	Type	Change	Comment
cxl_slv_m2s_req_crd	O	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_MEM_EN && (CX_CXL_IS_RC || CX_CXL_SYMMEM_SUPPORT)))
cxl_slv_m2s_rwd_crd	O		
cxl_slv_m2s_req[(CX_CXL_MEM_M2S_NDR_SIZE-1):0]	I		
cxl_slv_m2s_rwd[(CX_CXL_MEM_M2S_DATA_SIZE-1):0]	I		
cxl_slv_m2s_req_chk[(CX_CXL_MEM_M2S_NDR_CHK_SIZE-1):0]	I	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_MEM_EN && (CX_CXL_IS_RC || CX_CXL_SYMMEM_SUPPORT))) && ((CX_CXL_CHI_DATACHK > 0)? CX_CXL_ENABLE : 0)
cxl_slv_m2s_rwd_chk[(CX_CXL_MEM_M2S_DATA_CHK_SIZE-1):0]	I		
cxl_mst_s2m_ndr_crd	I	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_MEM_EN && (CX_CXL_IS_RC || CX_CXL_SYMMEM_SUPPORT)))
cxl_mst_s2m_drc_crd	I		
cxl_mst_s2m_ndr[(CX_CXL_MEM_S2M_NDR_SIZE-1):0]	O		
cxl_mst_s2m_drc[(CX_CXL_MEM_S2M_DATA_SIZE-1):0]	O		
cxl_mst_s2m_ndr_chk[(CX_CXL_MEM_S2M_NDR_CHK_SIZE-1):0]	O	Exists Condition	The exists condition is changed **from:** ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) **to**: ((CX_CXL_ENABLE && !CX_CXL_CXS_ENABLE)) && (CX_CXL_MEM_EN) && ((CX_CXL_CHI_ENABLE && CX_CXL_MEM_EN && (CX_CXL_IS_RC || CX_CXL_SYMMEM_SUPPORT))) && ((CX_CXL_CHI_DATACHK > 0)? CX_CXL_ENABLE : 0)
cxl_mst_s2m_drc_chk[(CX_CXL_MEM_S2M_DATA_CHK_SIZE-1):0]	O		

Name	Type	Change	Comment
cxsrxdata[(CXSDATAFLITWIDTH-1):0]	I	Registered	**From**: Yes **to:** (CX_CXS_DATAFLITWIDTH==CX_CXS_CCIXDATAWIDTH) && ((CX_RASDP==0)&&(CX_RASDP_RAM_PROT==0)) && CX_CXS_RX_INPUT_REG) ? "Yes" : "No"
cxsrxvalidchk[(CXSRXREPWIDTH-1):0]	I	Registered	**From:** Yes **to:** No
cxstxvalid	O	Registered	**From:** Yes **to:** (CX_CXS_TX_OUTPUT_REG || CX_CXS_RAM_PIPELINE_ENABLE) ? "Yes" : "No"
cxstxdata[(CXSDATAFLITWIDTH-1):0]	O	Registered	**From:** Yes **to:**(CX_CXS_TX_OUTPUT_REG || CX_CXS_RAM_PIPELINE_ENABLE) ? "Yes" : "No"
cxstxcntl[(CXSCNTLWIDTH-1):0]	O	Registered	**From**: Yes **to:**(CX_CXS_TX_OUTPUT_REG || CX_CXS_RAM_PIPELINE_ENABLE) ? "Yes" : "No"
cxstxactivereq	O	Registered	**From:** Yes **to:**CX_CXS_SYNCHRONOUS ? "Yes" : "No"
cxstxlast	O	Registered	**From:** Yes **to:**CX_CXS_TX_OUTPUT_REG ? "Yes" : "No"
cxstxdatachk[(CXSDATACHKWIDTH-1):0]	O	Registered	**From:** Yes **to**:CX_CXS_TX_OUTPUT_REG ? "Yes" : "No"
cxstxcntlchk[(CXSCNTLCHKWIDTH-1):0]	O	Registered	**From:** Yes **to:**CX_CXS_TX_OUTPUT_REG ? "Yes" : "No"
cxstxvalidchk[(CXSTXREPWIDTH-1):0]	O	Registered	**From:** Yes **to:**CX_CXS_TX_OUTPUT_REG ? "Yes" : "No"

Name	Type	Change	Comment
cxs_rxram_dina[(CXS_RX_BUFF_DATAW-1):0]	O	Registered	**From:** No **to:** CX_CXS_RX_INPUT_REG ? "Yes" : "No"
cxs_rxram_doutb[(CXS_RX_BUFF_DATAW-1):0]	I	Registered	**From:** Yes **to:**CX_CXS_RAM_PIPELINE_ENABLE ? "Yes" : "No"
cxs_txram_dina[(CXS_TX_BUFF_DATAW-1):0]	O	Registered	**From:** No **to:** (CX_CXL_CXS_ENABLE || CX_RAS_EN) ? "No" : "Yes"
cxs_txram_doutb[(CXS_TX_BUFF_DATAW-1):0]	I	Registered	**From:** Yes **to:**CX_CXS_RAM_PIPELINE_ENABLE ? "Yes" : "No"
cxl_2_0_mbar0_offset[63:0]	I	Registered	**From:** Yes **to:** No
cxl_viral_request	I	Registered	**From:** Yes **to:** CX_CXL_MLD_EN ? "No" : "Yes"
cxl_pm_init_cmpl	I	Registered	**From:** Yes **to:** CX_CXL_RESET_EN ? "No" : "Yes"
mac_phy_messagebus[((NL*8)-1):0]	O	Exists Condition	The exists condition is changed **From:**((CX_CPCIE_ENABLE)) && ((CX_GEN4_SPEED && CX_PIPE44_SUPPORT) || CX_PIPE5_SUPPORT) **to:** ((CX_CPCIE_ENABLE)) && (CX_PIPE_MSGBUS_SUPPORT || CX_PIPE_LEGACY_MSGBUS_SUPPORT)
phy_mac_messagebus[((NL*8)-1):0]	I	Exists Condition	
ide_cfg_flr_rst	O	Exists Condition	The exists condition is changed **From:**(CX_IDE_ENABLE || CX_CXL_IDE_ENABLE) **to:**(CX_IDE_ENABLE_NO_PASSTHROUGH || CX_CXL_IDE_ENABLE)

Name	Type	Change	Comment
ide_msg_grant	O	Exists Condition	The exists condition is changed **From:** CX_IDE_ENABLE **to:** (CX_IDE_ENABLE) && (!(CX_IDE_ENABLE) && (CC_DEVICE_TYPE==CC_SW))
ide_msg_req	I		
ide_msg_sync_fail	I		
ide_msg_selec_link	I		
ide_msg_tc[2:0]	I		
ide_msg_th	I		
ide_msg_td	I		

Name	Type	Change	Comment
ide_msg_ep	I	Exists Condition	The exists condition is changed **From:** CX_IDE_ENABLE **to:** (CX_IDE_ENABLE) && (!(CX_IDE_ENABLE) && (CC_DEVICE_TYPE==CC_SW))
ide_msg_func_num[7:0]	I		
ide_msg_dst_rid[15:0]	I		
ide_msg_stream_id[7:0]	I		
pcie_ide_tx_prefix[((IDE_NPKTS_TX)IDE_PRFX_W_PROT)-1):0]	O		
pcie_ide_tx_local_prefix_size[((IDE_NPKTS_TX*clog2((NW_PRFX+1)))-1):0]	O		
pcie_ide_tx_local_prefix_size[((IDE_NPKTS_TX*clog2((NW_PRFX+1)))-1):0]	O		
pcie_ide_tx_e2e_prefix_size[((IDE_NPKTS_TX*clog2((NW_PRFX+1)))-1):0]	O		
pcie_ide_tx_hdr[(((IDE_NPKTS_TX*IDE_HDR_W_PROT)-1):0]	O		
pcie_ide_tx_hdr_size[((IDE_NPKTS_TX*3)-1):0]	O		
pcie_ide_tx_data[(((IDE_NPKTS_TX*IDE_DATA_W_PROT)-1):0]	O		
pcie_ide_tx_data_size[((IDE_NPKTS_TX*clog2((NW+1)))-1):0]	O		
pcie_ide_tx_sop[(IDE_NPKTS_TX-1):0]	O		
pcie_ide_tx_eop[(IDE_NPKTS_TX-1):0]	O		
pcie_ide_tx_control[((IDE_NPKTS_TX*IDE_CTRLW_TX)-1):0]	O		
pcie_ide_tx_dllp_error[(IDE_NPKTS_TX-1):0]	O		
ide_pcie_tx_halt	I		
ide_pcie_tx_prefix[((IDE_NPKTS_TX*IDE_PRFX_W_PROT)-1):0]	I		
ide_pcie_tx_hdr[((IDE_NPKTS_TX*IDE_HDR_W_PROT)-1):0]	I		
ide_pcie_tx_data[((IDE_NPKTS_TX*IDE_DATA_W_PROT)-1):0]	I		
ide_pcie_tx_data_size[((IDE_NPKTS_TX*clog2((NW+1)))-1):0]	I		

Name	Type	Change	Comment
ide_pcie_tx_sop[(IDE_NPKTS_TX-1):0]	I	Exists Condition	The exists condition is changed **From:** CX_IDE_ENABLE **to:** (CX_IDE_ENABLE) && (!(CX_IDE_ENABLE) && (CC_DEVICE_TYPE==CC_SW))
ide_pcie_tx_eop[(IDE_NPKTS_TX-1):0]	I		
ide_pcie_tx_control[((IDE_NPKTS_TX*IDE_CTRLW_TX)-1):0]	I		
ide_pcie_tx_discard[(IDE_NPKTS_TX-1):0]	I		
ide_pcie_tx_dllp_error[(IDE_NPKTS_TX-1):0]	I		
pcie_ide_tx_halt	O		
pcie_ide_rx_prefix[((IDE_NPKTS_RX*IDE_PRFX_W_PROT)-1):0]	O		
pcie_ide_rx_local_prefix_size[((IDE_NPKTS_RX*clog2((NW_PRFX+1)))-1):0]	O		
pcie_ide_rx_e2e_prefix_size[((IDE_NPKTS_RX*clog2((NW_PRFX+1)))-1):0]	O		
pcie_ide_rx_hdr[((IDE_NPKTS_RX*IDE_HDR_W_PROT)-1):0]	O		
pcie_ide_rx_hdr_size[((IDE_NPKTS_RX*3)-1):0]	O		
pcie_ide_rx_data[((IDE_NPKTS_RX*IDE_DATA_W_PROT)-1):0]	O		
pcie_ide_rx_data_size[((IDE_NPKTS_RX*clog2((NW+1)))-1):0]	O		
pcie_ide_rx_sop[(IDE_NPKTS_RX-1):0]	O		
pcie_ide_rx_eop[(IDE_NPKTS_RX-1):0]	O		
pcie_ide_rx_control[((IDE_NPKTS_RX*IDE_CTRLW_RX)-1):0]	O		
pcie_ide_rx_order	O		
pcie_ide_rx_dllp_error[(IDE_NPKTS_RX-1):0]	O		
ide_pcie_rx_halt	I		
ide_pcie_rx_prefix[((IDE_NPKTS_RX*IDE_PRFX_W_PROT)-1):0]	I		
ide_pcie_rx_hdr[((IDE_NPKTS_RX*IDE_HDR_W_PROT)-1):0]	I		

Name	Type	Change	Comment
ide_pcie_rx_data[((IDE_NPKTS_RX*IDE_DATA_W_PROT)-1):0]	I	Exists Condition	The exists condition is changed **From:** CX_IDE_ENABLE **to:** (CX_IDE_ENABLE) && (!(CX_IDE_ENABLE) && (CC_DEVICE_TYPE==CC_SW))
ide_pcie_rx_data_size[((IDE_NPKTS_RX*clog2((NW+1)))-1):0]	I		
ide_pcie_rx_sop[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_eop[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_control[((IDE_NPKTS_RX*IDE_CTRLW_RX)-1):0]	I		
ide_pcie_rx_ide_check_failed[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_pcrc_check_failed[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_misrouted_ide_tlp[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_report_ide_check_faild[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_dllp_error[(IDE_NPKTS_RX-1):0]	I		
ide_pcie_rx_order	I		
pcie_ide_rx_halt	O		
ide_cfg_device_type[2:0]	O		
ide_cfg_cs	O		
ide_cfg_wr_en[3:0]	O		
ide_cfg_addr[9:0]	O		
ide_cfg_wdata[31:0]	O		
ide_cfg_from_wire	O		
ide_cfg_rdata[31:0]	I		
ide_cfg_ack	I		
ide_cfg_ro_wr_en	O		

Documentation Changes

A number of signals were incorrectly described in the *Databook*. These are also highlighted in the change-tracked version of the *Reference Manual*. These are *not* RTL changes.

The following table enlists the I/O changes that have occurred for all configurations:

Table 2-3 Documentation Changes (Non-RTL)

Name	Type	Change	Comment
For many signals **Synchronous To** is corrected. These corrections are indicated in the change-tracked version of the Databook PDF which can be found at the location identified in the Databook revision history.			

2.3 Changes to Software View (Register Map)

This section discusses changes to the register map of the controller that have occurred in this release.

- It lists renamed registers.
- It lists deleted registers.
- It does *not* list new registers.
- *All* changes to the software map are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

The following changes have occurred for all configurations.

Table 2-4 Register Deletions/Renaming

Register	Nature of Change
No changes in this release.	

Documentation Changes

A number of registers were incorrectly described in the IP-XACT XML, DocBook XML, RAL files, header files, and *Register Descriptions* PDF. These are also highlighted in the change-tracked version of the *Reference Manual* PDF. These are *not* RTL changes.

Table 2-5 Documentation Changes (Non-RTL)

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
EINJ_ENABLE_REG	ERROR_INJECTION6_ENABLE			Y	
	ERROR_INJECTION5_ENABLE			Y	
	ERROR_INJECTION4_ENABLE			Y	
	ERROR_INJECTION3_ENABLE			Y	
	ERROR_INJECTION2_ENABLE			Y	
	ERROR_INJECTION1_ENABLE			Y	

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
	ERROR_INJECTION0_ENABLE			Y	
RASDP_ERROR_INJ_CTRL_OFF	ERROR_INJ_EN		Y		
RASDP_CORR_ERROR_LOCATION_OF	REG_LAST_CORR_ERROR		Y		
	REG_FIRST_CORR_ERROR		Y		
RASDP_UNCORR_ERROR_LOCATION_OF	REG_LAST_UNCORR_ERROR		Y		
	REG_FIRST_UNCORR_ERROR		Y		
CXL_RCIEP_FLEXBUS_R2_SIZE_LOW_OFF	MEMORY_ACTIVE_TIMEOUT_R2		Y		
CXL_RCIEP_FLEXBUS_R1_SIZE_LOW_OFF	MEMORY_ACTIVE_TIMEOUT_R1		Y		
CXL_RCRB_FLEXBUS_CNTRL_STATUS_OFF	CXL_FB_EN_BITS_P2_MISMATCH			Y	
CXL_TEST_CONFIG_BASE_LOW_OFF	CXL_DEVICE_TEST_MEM_SPACE_INDICATOR		Y		
AMBA_ORDERING_CTRL_OFF	AX_MSTR_ORDER_P_EVENT_SEL	Y			
PCIE_VERSION_NUMBER_OFF	VERSION_NUMBER		Y		
	VERSION_TYPE		Y		

2.4 Changes to RAM Sizes

This section details the changes to the default RAM sizes that have occurred since the last production release. It does not detail changes that are associated with new or additional features that you enable on your current configuration

Caution To determine the precise changes to RAM sizes for your actual controller configuration, you can comp RAM sizes for the previous and current releases. For more details, see the “RAM Requirements” sec the *Databook*.

The following changes have occurred for this release.

Table 2-6 RAM Changes

RAM Name	Change
No changes in this release.	

2.5 Changes to Configuration Parameters

This section details any changes to the configuration parameters of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the configuration parameters are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

If you intend to source an existing configuration batch file, then you must first convert your configuration file, as described in "Product Updates" on page 88. If you are not sourcing an existing configuration batch file, then you should be still aware of changes to the default value of some configuration parameters.

Caution

To ensure that your existing configuration absorbs all changes to default parameters updated for this release, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

The *Write default Parameter* should only be used for debugging.

Table 2-7 Configuration Parameter Changes

Name	Change
AMBA_INTERFACE	**Bit** Rsvd(1) removed
CX_IDE_ENABLE	**Enabled from:** CX_CXL_ENABLE==0 **to:** Always
CX_SERDES_ARCH_LANES_TURNOFF	**Default value** changed **from:** Disabled **to:** CX_PIPE_SERDES_ARCH
CX_CPLQ_MANAGEMENT_ENABLE	**Default value** changed **from:** (CC_DEVICE_TYPE!=CC_SW) && !(CX_P2P_ENABLE) && TRGT1_POPULATE && (RADM_CPL_QMODE_VC0<4) **to:** (CC_DEVICE_TYPE!=CC_SW) && !(CX_P2P_ENABLE) && TRGT1_POPULATE && RADM_CPL_QMODE_VC0<4 && (CX_NVC < 2 || RADM_CPL_QMODE_VC1<4) && (CX_NVC < 3 || RADM_CPL_QMODE_VC2<4) && (CX_NVC < 4 || RADM_CPL_QMODE_VC3<4) && (CX_NVC < 5 || RADM_CPL_QMODE_VC4<4) && (CX_NVC < 6 || RADM_CPL_QMODE_VC5<4) && (CX_NVC < 7 || RADM_CPL_QMODE_VC6<4) && (CX_NVC < 8 || RADM_CPL_QMODE_VC7<4) **Enabled** changed **from:** ((CC_DEVICE_TYPE!=CC_SW) && TRGT1_POPULATE && (RADM_CPL_QMODE_VC0<4)) **to:** ((CC_DEVICE_TYPE!=CC_SW) && TRGT1_POPULATE && (RADM_CPL_QMODE_VC0<4) && (CX_NVC<2 || RADM_CPL_QMODE_VC1<4) && (CX_NVC<3 || RADM_CPL_QMODE_VC2<4) && (CX_NVC<4 || RADM_CPL_QMODE_VC3<4) && (CX_NVC<5 || RADM_CPL_QMODE_VC4<4) && (CX_NVC<6 || RADM_CPL_QMODE_VC5<4) && (CX_NVC<7 || RADM_CPL_QMODE_VC6<4) && (CX_NVC<8 || RADM_CPL_QMODE_VC7<4))

Name	Change
MASTER_BUS_ADDR_WIDTH	**Default value** changed **from:** CC_DTIM_ENABLE ? 64 : (AHB_POPULATED ? SLAVE_BUS_ADDR_WIDTH : 32) **to:** CC_DTIM_ENABLE ? 64 : FLT_Q_ADDR_WIDTH > 32 ? 64 : 32 **Enabled** changed **from:** (MASTER_POPULATED && (AXI_POPULATED || AHB_POPULATED)) **to:** MASTER_POPULATED && AXI_POPULATED
SLAVE_BUS_ADDR_WIDTH	**Enabled** changed **from:** (SLAVE_POPULATED && (AXI_POPULATED || AHB_POPULATED)) **to:** SLAVE_POPULATED && AXI_POPULATED
SLV_CLK_DIFF_ENABLE	**Default value** changed **from:** (AXI_POPULATED && SLAVE_POPULATED) || AHB_CLK_DIFF_ENABLE **to:** AXI_POPULATED && SLAVE_POPULATED
MSTR_CLK_DIFF_ENABLE	**Default value** changed **from:** (AXI_POPULATED && MASTER_POPULATED) || AHB_CLK_DIFF_ENABLE **to:** AXI_POPULATED && MASTER_POPULATED
CC_SLV_BURST_LEN	**Default value** changed **from:** (AHB_POPULATED && (SLAVE_BUS_DATA_WIDTH==32))? 32 : 16 **to:** 16
CC_MSTR_BURST_LEN	**Enabled** changed **from:** (MASTER_POPULATED && !(AHB_POPULATED && (CC_MSTR_BURST_TYPE == 0))) **to:** MASTER_POPULATED

Name	Change
CC_MAX_SLV_TAG	**Default value** changed **from:** ((AHB_ENABLED==1) && (CC_AHB_SNUM_MASTERS<=2)) ? 2 : ((AHB_ENABLED==1) && (CC_AHB_SNUM_MASTERS<=4)) ? 4 : ((AHB_ENABLED==1) && (CC_AHB_SNUM_MASTERS<=8)) ? 8 : ((AHB_ENABLED==1) && (CC_AHB_SNUM_MASTERS<=16)) ? 16 : (CC_DMA_ENABLE_VALUE==1) ? ((CX_MAX_TAG==3) ? 2 : (CX_MAX_TAG==7) ? 4 : (CX_MAX_TAG==15) ? 8 : (CX_MAX_TAG==31) ? 16 : (CX_MAX_TAG==63) ? 32: (CX_MAX_TAG==127) ? 64 : (CX_MAX_TAG==255) ? 128 : (CX_MAX_TAG==511) ? 256 : (CX_MAX_TAG>=767) ? 512 : 2) : ((CX_MAX_TAG<=767) ? CX_MAX_TAG +1 : 768) **to:** (CC_DMA_ENABLE_VALUE==1) ? ((CX_MAX_TAG==3) ? 2 : (CX_MAX_TAG==7) ? 4 : (CX_MAX_TAG==15) ? 8 : (CX_MAX_TAG==31) ? 16 :(CX_MAX_TAG==63) ? 32 : (CX_MAX_TAG==127) ? 64 : (CX_MAX_TAG==255) ? 128 : (CX_MAX_TAG==511) ? 256 : (CX_MAX_TAG>=767) ? 512 : 2) : ((CX_MAX_TAG<=767) ? CX_MAX_TAG + 1 : 768) **Enabled** changed **from:** SLAVE_POPULATED && (AHB_ENABLED==0) **to:** SLAVE_POPULATED
CX_REMOTE_MAX_TAG	**Default value** changed **from:** CC_HP_MASTER ? CC_MAX_MSTR_TAGS_AXI-1 :AHB_POPULATED ? 1 : (AXI_POPULATED ? CC_MAX_MSTR_TAGS - 1 : ((CX_MAX_TAG == 767) ? 1023 : CX_MAX_TAG)) **to:** CC_HP_MASTER ? CC_MAX_MSTR_TAGS_AXI-1 :(AXI_POPULATED ? CC_MAX_MSTR_TAGS - 1 : ((CX_MAX_TAG == 767) ? 1023 : CX_MAX_TAG))
CX_ENHANCED_PM_EN	**Enabled** changed **from:** (CX_CPCIE_ENABLE && !(AMBA_INTERFACE==1)) **to:** CX_CXL_ENABLE==0
CX_PHY_ENHANCED_PM_EN	**Enabled** changed **from:** ((CX_S_CPCIE_MODE)) **to:** CX_CXL_ENABLE==0

Name	Change
CX_PSW_EN_ACTIVE_LOW	**Values** changed **from:** ■ LOW (0) ■ HIGH (1) **to:** ■ HIGH (0) ■ LOW (1) **Default value** changed **from:** LOW **to:** HIGH
APP_RETURN_ERR_EN	**Default value** changed **from:** CX_DPC_ENABLE **to:** CX_DPC_ENABLE || CC_LTIM_ENABLE
CC_IB_WREQ_PTRK_EN	**Default value** changed **from:** CC_HP_MASTER **to:** CC_HP_MASTER || CC_ORDRB_EN
CX_AXI_RCHUNK_ENABLE	**Enabled** changed **from:** AMBA_INTERFACE == 4 **to:** (AMBA_INTERFACE == 4 && (CX_GEN4_SPEED_VALUE == 1) || (CX_GEN5_SPEED_VALUE == 1))
CX_AXI_UIDI_ENABLE	**Enabled** changed **from:** AMBA_INTERFACE == 4 **to:** (AMBA_INTERFACE == 4 && (CX_GEN4_SPEED_VALUE == 1) || (CX_GEN5_SPEED_VALUE == 1))
CX_IDO_ENABLE	**Enabled** changed **from:** (CC_DEVICE_TYPE!=CC_SW) && !AHB_POPULATED **to:** CC_DEVICE_TYPE!=CC_SW
CX_L1_SUBSTATES_ENABLE	**Enabled** changed **from:** (CX_PCIE_MODE == PCIE_OVER_CIO) ? 0 : (CX_CPCIE_ENABLE) **to:** (CX_PCIE_MODE == PCIE_OVER_CIO || CX_CXL_ENABLE==1) ? 0 : 1

Name	Change
MEM_FUNCn_BAR0_TARGET_MAP	**Default value** changed **from:** (TRGT1_POPULATE==1 && !(CX_CXL_ENABLE && (CX_CXL_VERSION==2))) ? 1 : 0 **to:** (TRGT1_POPULATE==1 && !(MSIX_TABLE_EN && MSIX_TABLE_BIR_0 == 0)) ? 1 : 0
CX_RTLH_TLP_EXTRACT_REGOUT	**Enabled** changed **from:** CX_RTLH_SIMPLE_EXTRACT && CX_CUSTOM_PIPELINING **to:** CX_NW==16 && CX_CUSTOM_PIPELINING
CX_PIPE_PCLK_MODE	**Default value** changed **from:** CX_CXL_ENABLE==1 && DWC_PCIE_FPGA==0) ? 3 : 0 **to:** ((CX_MAX_PCIE_SPEED == 5 && CX_PIPE_VER == 2) ? 0 : (CX_MAX_PCIE_SPEED == 4 && CX_CXL_ENABLE==1 && DWC_PCIE_FPGA==0) ? 3 : (CX_MAX_PCIE_SPEED == 5 && CX_CXL_ENABLE==1 && CX_PIPE5_SUPPORT==1 && CX_PIPE_SERDES_ARCH && DWC_PCIE_FPGA==0) ? 3 : 0)
DEFAULT_CXL_PORT_USP_CACHE_ENABLE	**Enabled** changed **from:** ((CC_DEVICE_TYPE==CC_EP || CC_DEVICE_TYPE==CC_DM && (CX_CXL_CACHE_EN)) **to:** ((CC_DEVICE_TYPE==CC_EP || CC_DEVICE_TYPE==CC_DM || ((CC_DEVICE_TYPE==CC_SW) && (CX_CXL_VERSION>=2))) && (CX_CXL_CACHE_EN))
DEFAULT_CXL_PORT_USP_MEM_ENABLE	**Enabled** changed **from:** ((CC_DEVICE_TYPE==CC_EP || CC_DEVICE_TYPE==CC_DM && (CX_CXL_CACHE_EN)) **to:** ((CC_DEVICE_TYPE==CC_EP || CC_DEVICE_TYPE==CC_DM || ((CC_DEVICE_TYPE==CC_SW) && (CX_CXL_VERSION>=2))) && (CX_CXL_CACHE_EN))

2.6 Converting to the Current Release

Sometimes a new controller release might no longer use a certain configuration parameter, or the meaning of that parameter might have changed. The following process helps you convert your current configuration file so that it creates the same RTL with the new controller.

1. Open coreConsultant and create an unconfigured workspace from the newly installed controller.
2. In the coreConsultant command line, enter the following command:

   `parse_configfile my_configfile.config`

   where `my_configfile.config` is your current configuration file. This command creates an updated configuration file in your working directory as follows:

   `my_configfile.config.new`
3. In the coreConsultant command line, enter the following command:

   `source my_configfile.config.new`
4. Select Apply to generate the new RTL with the updated or translated parameters.
5. From the File Menu, select Write Batch Script and save the configuration file for the new release.
6. When you source the updated configuration file in coreConsultant, you can *ignore any new warnings* about parameter settings that are not relevant to, or not enabled in your configuration.

Attention

Writing Out Your Configuration File

To ensure that your existing configuration absorbs all changes to default parameters updated for this release, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

You must convert your configuration file. Failure to do so, can result in:

- Your configuration file being incompatible with the current release.
- Functional, architectural, RAM, and I/O changes when the default of some configuration parameters change from release to release.

2.7 Known Issues and Limitations

You can view a complete list of functional problem reports for this product, including problems identified after product release, by accessing the STAR report on the Web. For more details, see "Details of Fixed Defects and Enhancements" on page 116. You must have a SolvNetPlus ID to view STAR reports. This release has the following known tool and packaging issues at the time of release.

- "Packaged coreConsultant Test Limitations"
- "VTB Limitations"
- "Design Example"
- "Unique Case Violation Simulation Message"
- "coreConsultant Memory Map Limitations"

2.7.1 Packaged coreConsultant Test Limitations

We invite you to submit your coreConsultant configuration for review. Because of the very large configuration space, it is not possible to regress every configuration before a release is made. Synopsys is continually running fixed and randomized configurations, but it is possible that your exact configuration has not been regressed. Test case failures might occur because of improper test bench configuration. In that case open a case through SolvNetPlus.

2.7.1.1 Known Test Failures

The following are known testbench issues:

- Viral LD-ID related to MLD and Viral Enable, and status logic update for Switch is not verified.
- LL_Reset functionality for CXL Link Layer Control and Status Register is not verified.
- VTB test might fail due to the following errors:
  - The `pm_*_cxl` might fail with any one error signature due to a design issue while arbitrating between ALMP flit and cxl.io, cxl.mc flit during low power entry, exit scenarios for CXS configurations.
    - Unexpected Data Chunk(G0) when `rx_data_xact_q` is null
    - Invalid slot 1 type: G5 received, when Data chunk slot (G0) is expected
    - Received flit with ReqCrd (2) for Cache.Req when CXL.Cache is disabled
    - Controller must set the `cxs_tx_last` for LLCRD flits
    - Controller must not set the `cxs_tx_last` when pending data rollover>=4
    - cxlE2ESb.MISMATCH

2.7.2 Unpacking Configurations with CX_NFUNC >32

For configurations with number of Physical Functions greater than 32 (`CX_NFUNC >32`), the controller uses the same structure of IP-XACT for native and AMBA configuration for DBI register accesses.

- In case of native and DBI accesses, there are dedicated pins for PFs and VFs and you must assert as per the scenarios.

- For the AXI_POPULATED based configuration, you must configure the dedicated DBI_FUNCTION_BANK_CTRL_REG field of DBI_FUNCTION_BANK_CTRL_REG_OFF register for NFUNC > 32.

2.7.3 VTB Limitations

The following limitations apply to the current release of the VTB:

- Not backward compatible with previous releases
- Not UVM compliant
- No support for big-endian (AHB_ENDIANNESS) configurations

2.7.4 Design Example

The design example in <workspace>/examples/DWC_pcie_clkrst.v has been functionally verified, but has not been explicitly targeted for verification metrics. However, it has been used by Synopsys in the verification and regression environments for all controller configurations; including verification of all power transitions for the controller.

2.7.5 Unique Case Violation Simulation Message

The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

There is a known simulator issue with a "Unique case violation" message that occurs sometimes while running simulations with VCS outside of coreConsultant. You can ignore these messages.

To avoid these messages, use the -xlrm uniq_prior_final compile option in VCS. The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

2.7.6 coreConsultant Memory Map Limitations

The controller supports the generation of configuration-specific register maps as described in the "Register Configuration Space" chapter in the *Databook*. For SR-IOV configurations (CX_SRIOV_ENABLE =1), the following limitations apply.

Table 2-8 coreConsultant Report File Limitations for SR-IOV Configurations

CX_NVFUNC	IP-XACT (IP-XACT XML)	RALF and C Headers (No limitations)	Register Report (DocBook XML) Also applies to Databook
1–256	Defines default #VFs in each PF	Defines default #VFs in each PF	Defines only first VF in each PF
257–4096	Defines only[a] first VF in each PF	Defines default #VFs in each PF	Defines only first VF in each PF

a. For details on how to populate remaining VFs in the IP-XACT file, see "Populating IP-XACT File Manually" in the "Creating Optional Views and Reports" section in the "Configuring the controller" chapter of the User Guide.

2.7.7 VC Spyglass Limitations

- VC Spyglass support is for demonstration purpose only. Spyglass continues to be the used for Linting, CDC, and RDC signoff.
- VC Spyglass CDC has some limitations. For failure cases, contact Synopsys Support through SolvNetPlus for further details.

2.7.8 Third-party Simulator Limitations

When you are using the QuestaSim 2020.4 simulator, and if you select the HDMA option, compilation failure can occur because the QuestaSim 2020.4 does not support System Verilog IEEE 2012 standard.

2.8 Details of Fixed Defects and Enhancements

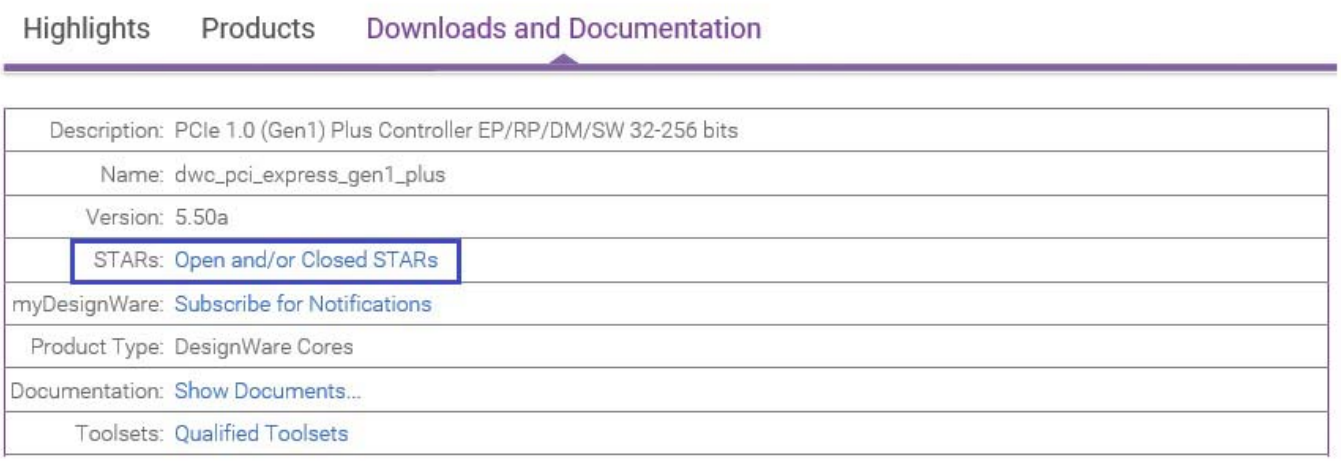
Defects fixed in release 5.97a of the controller are listed in the STAR report for release 5.97a in STARs on the Web.

Table 2-9 Controller STAR Report Location

Controller	Location
PCIe Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_controllers
CXL Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_cxl_controller
CCIX Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_ccix_controller

(A SolvNetPlus ID is required to view STAR reports.)

Figure 2-1 Accessing STARs on the Web through SolvNetPlus



Enhancement STARs are identifiable by the letter “E” in the Severity column, and fixed defect STARs are identifiable by the letter “B.” An E4 or B4 has the highest severity. Clicking on the tab corresponding to 5.97a produces a STAR report of closed STARS for this release. For previous controller versions, click the tab corresponding to the version in question.

2.9 Synopsys Statement on Inclusivity and Diversity

Synopsys is committed to creating an inclusive environment where every employee, customer, and partner feels welcomed. We are reviewing and removing exclusionary language from our products and supporting customer-facing collateral. Our effort also includes internal initiatives to remove biased language from our engineering and working environment, including terms that are embedded in our software and IPs. At the same time, we are working to ensure that our web content and software applications are usable to people of varying abilities. You may still find examples of non-inclusive language in our software or documentation as our IPs implement industry-standard specifications that are currently under review to remove exclusionary language.

2.10 Customer Support

To obtain support for your product, prepare the required files and contact the support center using one of the methods described:

- Prepare the following debug information, if applicable:
  - For environment set-up problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, select the following menu:
    - **File > Build Debug Tar-file**

      Check all the boxes in the dialog box that apply to your issue. This option gathers all the Synopsys product data needed to begin debugging an issue and writes it to the <*core tool startup directory*>/debug.tar.gz file.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD).
    - Identify the hierarchy path to the DesignWare instance.
    - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- *For the fastest response*, enter a case through SolvNetPlus:

  a. https://solvnetplus.synopsys.com

Note SolvNetPlus does not support Internet Explorer. Use a supported browser such as Microsoft Edge, Google Chrome, Mozilla Firefox, or Apple Safari.

  b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).

  c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

     Make sure to include the following:

     - **Product L1:** DesignWare Cores
     - **Product L2:** PCI Express

  d. After creating the case, attach any debug files you created.

     For more information about general usage information, refer to the following article in SolvNetPlus:

     https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
  - Attach any debug files you created.
- Or, telephone your local support center:

- North America:
  Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
- All other countries:
  https://www.synopsys.com/support/global-support-centers.html

3

Release Notes: 5.96a

These release notes describe the changes in this release *(5.96a)* relative to the previous production release *(5.95a)*.This release note contains the following sections:

- "Product Updates" on page 122
- "Changes to I/O" on page 124
- "Changes to Software View (Register Map)" on page 125
- "Changes to RAM Sizes" on page 137
- "Changes to Configuration Parameters" on page 138
- "Converting to the Current Release" on page 140
- "Known Issues and Limitations" on page 141
- "Details of Fixed Defects and Enhancements" on page 144
- "Synopsys Statement on Inclusivity and Diversity" on page 145
- "Customer Support" on page 146

3.1 Product Updates

This release contains the following major updates and other minor updates (indicated in "Details of Fixed Defects and Enhancements" on page 144).

3.1.1 CXL Integrity and Data Encryption (IDE)

This is Synopsys proprietary product. The CXL 2.0 controller supports CXL IDE as defined in CXL 2.0 specification. The CXL controller IDE along with DesignWare® CXL 2.0 Integrity and Data Encryption (IDE) Security IP Module provides Confidentiality, Integrity, and Replay protection for data transiting the CXL link. You can enable this parameter by setting `CX_CXL_IDE_ENABLE` to '1'.

For more information, see "CXL 2.0 Integrity and Data Encryption (IDE)" chapter in the *CXL Databook*.

Note In this release, the CXL IDE is available as an LCA (Limited Customer Availability) feature and must not be used for tape out. Contact Synopsys Support through SolvNetPlus for an unlocking key for this feature.

3.1.2 CXL Power Management

The CXL controller supports Power Management as defined in the *CXL 2.0 Specification* with the following features:

- ASPM L1 support for CXL 1.1 and CXL 2.0 devices
- PCI-PM support for CXL 2.0 device
- Dedicated PM control over CXL.cache/mem via Native Channel Interface

For more information, see the "Power Management Support for CXL" chapter in the *CXL Databook*.

3.1.3 PCIe Integrity and Data Encryption (IDE)

The PCIe Integrity and Data Encryption (IDE) along with the DesignWare® Integrity and Data Encryption (IDE) Security Module provides confidentiality, integrity, and replay protection for TLPs over PCIe interfaces. You can enable this feature by setting `CX_IDE_ENABLE` parameter to '1'.

For more information, see "PCIe Integrity and Data Encryption" chapter in the *PCIe Databook*.

Note In this release, the PCIe IDE is available as an EA (Early Adopter) feature and must not be used for tape out. Contact Synopsys Support through SolvNetPlus for an unlocking key for this feature.

3.1.4 Application Low Power Entering Control

The PCIe controller provides the following parameters and output signal that your application can use for fine grained control of ASPM transitions.

- ASPM top-level control using `CX_ASPM_L1_EN_OUTPUT` internal parameter
- ASPM L1 Link State entry control using the `CX_ASPM_L1_TIMER_ENABLE` internal parameter
- PME_Turn_Off handshake control using the `CX_APP_CTRL_PME_TO_ACK` parameter

- Slot Power Limit indication through the `radm_slot_pwr_payload` signal

For more information, see "Active State Power Management (ASPM)", "Message Reception", and "L2/L3 Entry" sections in the "Controller Operations" chapter of the *PCIe Databook*.

3.1.5 DTI ATS Invalidation Request Filter by BDF

In this enhancement, the PCIe controller DTI Master filters the ATS Invalidation Requests by Root Port ID and Bus Number. The requester must identify the correct Device and Function.

For more information, see "DTIM Support in PCIe Controller with AMBA Bridge" section in the "AMBA" chapter of the *PCIe Databook*.

3.1.6 Non Contiguous Byte Enable (NCBE) Support

In this enhancement, when the AXI slave detects a null write strobe in the middle of an transfer, it decomposes the request into multiple requests.

For more information, see "Non Contiguous Byte Enable (NCBE) Support" section in the "AMBA" chapter of the *PCIe Databook*.

3.1.7 SerDes Architecture Support for Gen5 Controller - PHY Combinations

Table 3-1 describes the new Gen5 Controller - PHY combination support for SerDes architecture (`CX_PIPE_SERDES_ARCH =1`) added in this release.

Table 3-1 Gen5 Controller-PHY Combinations Supported

Controller	PHY g1_2s g2_2s_df g3_4s_dw g4_4s_df g5_4s_df
g1_4s g2_4s_df g3_8s_dw g4_8s_df g5_8s_df	Yes

3.1.8 Posted Queue Bypass

The controller supports Posted Queue Bypass for configurations with 512-bit datapath.

3.2 Changes to I/O

This section details any changes to the I/O of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the I/O are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

The following table enlists the I/O changes that have occurred for all configurations:

Table 3-2 I/O Signals Added, Removed, or Renamed

Name	Type	Change	Comment
cfg_bar[0|1]_[start|limit]	O	Exists condition	The exists condition is changed from !(CX_NFUNC>32) to (!(CX_NFUNC>32)) && (!(CX_IS_SW && !CX_CXL_ENABLE))
CXL Error Status Signals	O	Width	The width of the CXL Error Status Signals are increased.

Documentation Changes

A number of signals were incorrectly described in the *Databook*. These are also highlighted in the change-tracked version of the *Reference Manual*. These are *not* RTL changes.

The following table enlists the I/O changes that have occurred for all configurations:

Table 3-3 Documentation Changes (Non-RTL)

Name	Type	Change	Comment
For many signals **Synchronous To** is corrected. These corrections are indicated in the change-tracked version of the Databook PDF which can be found at the location identified in the Databook revision history.			

3.3 Changes to Software View (Register Map)

This section discusses changes to the register map of the controller that have occurred in this release.

- It lists renamed registers.
- It lists deleted registers.
- It does *not* list new registers.
- *All* changes to the software map are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

The following changes have occurred for all configurations.

Table 3-4 Register Deletions/Renaming

Register	Nature of Change
No changes in this release.	

Documentation Changes

A number of registers were incorrectly described in the IP-XACT XML, DocBook XML, RAL files, header files, and *Register Descriptions* PDF. These are also highlighted in the change-tracked version of the *Reference Manual* PDF. These are *not* RTL changes.

Table 3-5 Documentation Changes (Non-RTL)

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
DEVICE_CAPABILITIES2_REG	PCIE_CAP_EMERGENCY_PWR_RED_REQUEST	Y			
MEMBAR0_HEADER_CAP_REG_OFF	CXL_RCRB_MEMBAR0_CACHE_MEM_SIZE				Y
	CXL_RCRB_MEMBAR0_CACHE_MEM_VER				Y
	CXL_RCRB_MEMBAR0_CAP_VER				Y
	CXL_RCRB_MEMBAR0_CAP_ID				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
MEMBAR0_RAS_CAP_REG_OFF	CXL_RCRB_MEMBAR0_RAS_CAP_PTR				Y
	CXL_RCRB_MEMBAR0_RAS_CAP_VER				Y
	CXL_RCRB_MEMBAR0_RAS_CAP_ID				Y
MEMBAR0_SECURITY_CAP_REG_OFF	CXL_RCRB_MEMBAR0_SEC_CAP_PTR				Y
	CXL_RCRB_MEMBAR0_SEC_CAP_VER				Y
	CXL_RCRB_MEMBAR0_SEC_CAP_ID				Y
MEMBAR0_LINK_CAP_REG_OFF	CXL_RCRB_MEMBAR0_LINK_CAP_PTR				Y
	CXL_RCRB_MEMBAR0_LINK_CAP_VER				Y
	CXL_RCRB_MEMBAR0_LINK_CAP_ID				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
MEMBAR0_RAS_UNCOR_ERROR_STATUS_REG_OFF	CXL_RCRB_MEMBAR0_CXL_IDE_RX_ER				Y
	CXL_RCRB_MEMBAR0_CXL_IDE_TX_ER				Y
	CXL_RCRB_MEMBAR0_CXL_INTERNAL_ERR				Y
	CXL_RCRB_MEMBAR0_RCVR_OVERFLOW				Y
	CXL_RCRB_MEMBAR0_POISON_RVD				Y
	CXL_RCRB_MEMBAR0_ENCOD_VIOLATION				Y
	CXL_RCRB_MEMBAR0_REINIT_THRESHOLD				Y
	CXL_RCRB_MEMBAR0_MEM_DATA_ECC				Y
	CXL_RCRB_MEMBAR0_MEM_BE_PAR				Y
	CXL_RCRB_MEMBAR0_MEM_ADD_PAR				Y
	CXL_RCRB_MEMBAR0_MEM_DATA_PAR				Y
	CXL_RCRB_MEMBAR0_CACHE_DATA_ECC				Y
	CXL_RCRB_MEMBAR0_CACHE_BE_PAR				Y
	CXL_RCRB_MEMBAR0_CACHE_ADD_PAR				Y
	CXL_RCRB_MEMBAR0_CACHE_DATA_PAR				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
MEMBAR0_RAS_UNCOR_ERROR_MASK_REG_OFF	CXL_RCRB_MEMBAR0_CXL_IDE_RX_MASK				Y
	CXL_RCRB_MEMBAR0_CXL_IDE_TX_MASK				Y
	CXL_RCRB_MEMBAR0_CXL_INTERNAL_ER_MASK				Y
	CXL_RCRB_MEMBAR0_RCVR_OVERFLOW_MASK				Y
	CXL_RCRB_MEMBAR0_POISON_RVD_MASK				Y
	CXL_RCRB_MEMBAR0_ENCOD_VIOLATION_MASK				Y
	CXL_RCRB_MEMBAR0_REINIT_THRESHOLD_MASK				Y
	CXL_RCRB_MEMBAR0_MEM_DATA_ECC_MASK				Y
	CXL_RCRB_MEMBAR0_MEM_BE_PAR_MASK				Y
	CXL_RCRB_MEMBAR0_MEM_ADD_PAR_MASK				Y
	CXL_RCRB_MEMBAR0_MEM_DATA_PAR_MASK				Y
	CXL_RCRB_MEMBAR0_CACHE_DATA_ECC_MASK				Y
	CXL_RCRB_MEMBAR0_CACHE_BE_PAR_MASK				Y
	CXL_RCRB_MEMBAR0_CACHE_ADD_PAR_MASK				Y
	CXL_RCRB_MEMBAR0_CACHE_DATA_PAR_MASK				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
MEMBAR0_RAS_UNCOR_ERROR_SEVERITY_REG_OFF	CXL_RCRB_MEMBAR0_CXL_IDE_RX_SEV				Y
	CXL_RCRB_MEMBAR0_CXL_IDE_TX_SEV				Y
	CXL_RCRB_MEMBAR0_CXL_INTERNAL_ER_SEV				Y
	CXL_RCRB_MEMBAR0_RCVR_OVERFLOW_SEV				Y
	CXL_RCRB_MEMBAR0_POISON_RVD_SEV				Y
	CXL_RCRB_MEMBAR0_ENCOD_VIOLATION_SEV				Y
	CXL_RCRB_MEMBAR0_REINIT_THRESHOLD_SEV				Y
	CXL_RCRB_MEMBAR0_MEM_DATA_ECC_SEV				Y
	CXL_RCRB_MEMBAR0_MEM_BE_PAR_SEV				Y
	CXL_RCRB_MEMBAR0_MEM_ADD_PAR_SEV				Y
	CXL_RCRB_MEMBAR0_MEM_DATA_PAR_SEV				Y
	CXL_RCRB_MEMBAR0_CACHE_DATA_ECC_SEV				Y
	CXL_RCRB_MEMBAR0_CACHE_BE_PAR_SEV				Y
	CXL_RCRB_MEMBAR0_CACHE_ADD_PAR_SEV				Y
	CXL_RCRB_MEMBAR0_CACHE_DATA_PAR_SEV				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
MEMBAR0_RAS_CORR_ERROR_STATUS_REG_OFF	CXL_RCRB_MEMBAR0_PHY_LAYER_ERR				Y
	CXL_RCRB_MEMBAR0_MEM_POISON_RVD				Y
	CXL_RCRB_MEMBAR0_CACHE_POISON_RVD				Y
	CXL_RCRB_MEMBAR0_CORR_RETRY_THRESHOLD				Y
	CXL_RCRB_MEMBAR0_CORR_CRC_THRESHOLD				Y
	CXL_RCRB_MEMBAR0_CORR_MEM_DATA_ECC				Y
	CXL_RCRB_MEMBAR0_CORR_CACHE_DATA_ECC				Y
MEMBAR0_RAS_CORR_ERROR_MASK_REG_OFF	CXL_RCRB_MEMBAR0_PHY_LAYER_ERR_MASK				Y
	CXL_RCRB_MEMBAR0_MEM_POISON_RVD_MASK				Y
	CXL_RCRB_MEMBAR0_CACHE_POISON_RVD_MASK				Y
	CXL_RCRB_MEMBAR0_CORR_RETRY_THRESHOLD_MASK				Y
	CXL_RCRB_MEMBAR0_CORR_CRC_THRESHOLD_MASK				Y
	CXL_RCRB_MEMBAR0_CORR_MEM_DATA_ECC_MASK				Y
	CXL_RCRB_MEMBAR0_CORR_CACHE_DATA_ECC_MASK				Y
MEMBAR0_RAS_ERR_CAP_CNTRL_REG_OFF	CXL_RCRB_MEMBAR0_POISON_END				Y
	CXL_RCRB_MEMBAR0_MUL_HDR_RECORDING_CAP				Y
	CXL_RCRB_MEMBAR0_ERR_PTR				Y
MEMBAR0_RAS_HEADER_LOG_REG_00_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_00				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
MEMBAR0_RAS_HEADER_LOG_REG_01_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_01				Y
MEMBAR0_RAS_HEADER_LOG_REG_02_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_02				Y
MEMBAR0_RAS_HEADER_LOG_REG_03_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_03				Y
MEMBAR0_RAS_HEADER_LOG_REG_04_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_04				Y
MEMBAR0_RAS_HEADER_LOG_REG_05_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_05				Y
MEMBAR0_RAS_HEADER_LOG_REG_06_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_06				Y
MEMBAR0_RAS_HEADER_LOG_REG_07_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_07				Y
MEMBAR0_RAS_HEADER_LOG_REG_08_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_08				Y
MEMBAR0_RAS_HEADER_LOG_REG_09_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_09				Y
MEMBAR0_RAS_HEADER_LOG_REG_10_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_10				Y
MEMBAR0_RAS_HEADER_LOG_REG_11_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_11				Y
MEMBAR0_RAS_HEADER_LOG_REG_12_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_12				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
MEMBAR0_RAS_HEADER_LOG_REG_13_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_13				Y
MEMBAR0_RAS_HEADER_LOG_REG_14_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_14				Y
MEMBAR0_RAS_HEADER_LOG_REG_15_OFF	CXL_RCRB_MEMBAR0_HDR_LOG_15				Y
MEMBAR0_SEC_POLICY_REG_OFF	CXL_RCRB_MEMBAR0_SEC_DEVICE_TEST_LVL				Y
MEMBAR0_LINK_LAYER_CAP_REG_OFF	CXL_RCRB_MEMBAR0_NUM_PHY_REINIT_RCVD				Y
	CXL_RCRB_MEMBAR0_NUM_RETRY_RCVD				Y
	CXL_RCRB_MEMBAR0_LLR_VAL_RCVD				Y
	CXL_RCRB_MEMBAR0_LLR_VAL_SUPP		Y		Y
	CXL_RCRB_MEMBAR0_LNK_VER_RCVD				Y
	CXL_RCRB_MEMBAR0_LNK_VER_SUPP				Y
MEMBAR0_LINK_LAYER_CAP_2_REG_OFF	CXL_RCRB_MEMBAR0_NO_LL_RESET_SUPPORT				Y
	CXL_RCRB_MEMBAR0_NUM_FREE_BUF_RCVD				Y
	CXL_RCRB_MEMBAR0_ECHO_ESEQ_RCVD				Y
	CXL_RCRB_MEMBAR0_WR_PTR_RCVD				Y
	CXL_RCRB_MEMBAR0_NUM_PHY_REINIT_RCVD_2				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
MEMBAR0_LINK_CNTRL_STATUS_REG_OFF	CXL_RCRB_MEMBAR0_LINK_LL_RETRY_BUF_CONSUME				Y
	CXL_RCRB_MEMBAR0_LINK_INIT_STATE				Y
	CXL_RCRB_MEMBAR0_LINK_LL_CRD_STALL				Y
	CXL_RCRB_MEMBAR0_LINK_LL_INIT_STALL				Y
	CXL_RCRB_MEMBAR0_LINK_LL_RST				Y
MEMBAR0_LINK_RX_CR_CNTRL_REG_OFF	CXL_RCRB_MEMBAR0_LINK_CTL_MEM_REQ_RSP_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_CTL_CACHE_DATA_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_CTL_CACHE_RSP_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_CTL_CACHE_REQ_CRD				Y
MEMBAR0_LINK_RX_CR_CNTRL_2_REG_OFF	CXL_RCRB_MEMBAR0_LINK_CTL_MEM_DATA_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_CTL_MEM_REQ_RSP_CRD_2				Y
MEMBAR0_LINK_RX_CR_RTN_STATUS_REG_OFF	CXL_RCRB_MEMBAR0_LINK_ST_MEM_REQ_RSP_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_ST_CACHE_DATA_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_ST_CACHE_RSP_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_ST_CACHE_REQ_CRD				Y
MEMBAR0_LINK_RX_CR_RTN_STATUS_2_REG_OFF	CXL_RCRB_MEMBAR0_LINK_ST_MEM_DATA_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_ST_MEM_REQ_RSP_CRD_2				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
MEMBAR0_LINK_TX_CR_STATUS_REG_OFF	CXL_RCRB_MEMBAR0_LINK_TX_MEM_REQ_RSP_CR				Y
	CXL_RCRB_MEMBAR0_LINK_TX_CACHE_DATA_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_TX_CACHE_RSP_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_TX_CACHE_REQ_CRD				Y
MEMBAR0_LINK_TX_CR_STATUS_2_REG_OFF	CXL_RCRB_MEMBAR0_LINK_TX_MEM_DATA_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_TX_MEM_REQ_RSP_CRD_2				Y
MEMBAR0_LINK_ACK_TMR_CNTRL_REG_OFF	CXL_RCRB_MEMBAR0_LINK_ACK_FLUSH_RETIMER				Y
	CXL_RCRB_MEMBAR0_LINK_ACK_FRC_THRESHOLD				Y
MEMBAR0_LINK_DEFEATURE_REG_OFF	CXL_RCRB_MEMBAR0_LINK_MDH_DISABLE				Y
MEMBAR0_ARB_MUX_CXL_IO_REG_OFF	CXL_RCRB_MEMBAR0_ARB_MUX_CXL_IO_RND_ROBIN				Y
MEMBAR0_ARB_MUX_CXL_CACHE_MEM_REG_OFF	CXL_RCRB_MEMBAR0_ARB_MUX_CXL_CACHE_MEM_RND_ROBIN				Y
SHADOW_PCI_MSIX_CAP_ID_NEXT_CTRL_REG	PCI_MSIX_RESERVED1				Y
	PCI_MSIX_TABLE_SIZE				Y
	PCI_MSIX_RESERVED0		Y		Y
SHADOW_MSIX_TABLE_OFFSET_REG	PCI_MSIX_TABLE_OFFSET				Y
	PCI_MSIX_BIR				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
SHADOW_MSIX_PBA_OFFSET_REG	PCI_MSIX_PBA_OFFSET				Y
	PCI_MSIX_PBA_BIR				Y
ACK_F_ASPM_CTRL_OFF	ASPM_L1_TIMER_ENABLE		Y		
CXL_VLSM_CR_REG_OFF	CXL_VLSM_IO_ALMP_ERROR			Y	
CXL_FATAL_ERR_CR_REG_OFF	CXL_IDE_RX_PLAIN_IF_ERR	Y			
	CXL_IDE_RX_SECURE_IF_ERR	Y			
	CXL_IDE_TX_PLAIN_IF_ERR	Y			
	CXL_IDE_TX_SECURE_IF_ERR	Y			
	CXL_MDH_ERR	Y			
	CXL_MEM_DATA_VD_ERR	Y			
	CXL_CACHE_DATA_VD_ERR	Y			
	CXL_H2D_ORD_VIOLATION	Y			
	CXL_AP_VIRAL_REQ	Y			
	CXL_CXS_TX_END_ERR	Y			
	CXL_ULL_CXS_END_ERR	Y			
	CXL_LL_RX_FLOW_CTRL_ERR	Y			
	CXL_RETRY_CRC_ERR	Y			

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
CXL_FATAL_ERR_CR_REG_OFF	CXL_RETRY_ESEQ_OVERFLOW	Y			
	CXL_LL_MULTI_INIT_PARAM	Y			
	CXL_LL_INIT_PARAM_ERR	Y			
	CXL_LL_TC_FLOW_CTRL_ERR	Y			
	CXL_LRSM_ACK_ERROR	Y			
	CXL_LRSM_ABORT	Y			
	CXL_LL_STATIC_BIT_ERR	Y			
	CXL_RAS_ERROR	Y			
	CXL_FATAL_ERR_RETRY_ACK_VIRAL	Y			

3.4 Changes to RAM Sizes

This section details the changes to the default RAM sizes that have occurred since the last production release. It does not detail changes that are associated with new or additional features that you enable on your current configuration

Caution To determine the precise changes to RAM sizes for your actual controller configuration, you can compare the coreConsultant generated RAM sizes for the previous and current releases. For more details, see the “RAM Requirements” section in the Architecture chapter of the *Databook*.

The following changes have occurred for this release.

Table 3-6 RAM Changes

RAM Name	Change
No changes in this release.	

3.5 Changes to Configuration Parameters

This section details any changes to the configuration parameters of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the configuration parameters are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

If you intend to source an existing configuration batch file, then you must first convert your configuration file, as described in "Product Updates" on page 122. If you are not sourcing an existing configuration batch file, then you should be still aware of changes to the default value of some configuration parameters.

Caution

To ensure that your existing configuration absorbs all changes to default parameters updated for this release, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

The *Write default Parameter* should only be used for debugging.

Table 3-7 Configuration Parameter Changes

Name	Change
PL_LIMIT	**Default value** changed **from:** 3208 **to:** 3212
CX_CONFIG_INTERCEPT_ENABLE	**Default value** changed **from:** false **to:** (CC_DEVICE_TYPE!=CC_RC) && CX_IDE_ENABLE
DEFAULT_NO_SOFT_RESET_n	**Default value** changed **from:** Always **to:** CX_IDE_ENABLE==0
BAR[0|1]_ENABLED_n	**Default value** changed **from:** (CC_DEVICE_TYPE==CC_RC || CC_DEVICE_TYPE==CC_SW) ? 0 : 1 **to:** ((CC_DEVICE_TYPE==CC_RC || CC_DEVICE_TYPE==CC_SW) &&!(CX_CXL_ENABLE && (CX_CXL_VERSION==2))) ? 0 : 1
CX_RADM_LUT_TO_FETCH_PIPE	**Default value** changed **from:** 1 **to:** (CX_CCIX_ENABLE) ? 0 : 1 **Enabled** changed **from:** CX_CUSTOM_PIPELINING **to:** CX_CUSTOM_PIPELINING && !CX_CCIX_ENABLE

Name	Change
CX_CXL_MBAR0_CAP_ARRAY_SIZE	**Default value** changed **from:** 0x4 **to:** 0x3

3.6 Converting to the Current Release

Sometimes a new controller release might no longer use a certain configuration parameter, or the meaning of that parameter might have changed. The following process helps you convert your current configuration file so that it creates the same RTL with the new controller.

1. Open coreConsultant and create an unconfigured workspace from the newly installed controller.
2. In the coreConsultant command line, enter the following command:

   `parse_configfile my_configfile.config`

   where `my_configfile.config` is your current configuration file. This command creates an updated configuration file in your working directory as follows:

   `my_configfile.config.new`
3. In the coreConsultant command line, enter the following command:

   `source my_configfile.config.new`
4. Select Apply to generate the new RTL with the updated or translated parameters.
5. From the File Menu, select Write Batch Script and save the configuration file for the new release.
6. When you source the updated configuration file in coreConsultant, you can *ignore any new warnings* about parameter settings that are not relevant to, or not enabled in your configuration.

Attention

Writing Out Your Configuration File

To ensure that your existing configuration absorbs all changes to default parameters updated for this release, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

You must convert your configuration file. Failure to do so, can result in:

- Your configuration file being incompatible with the current release.
- Functional, architectural, RAM, and I/O changes when the default of some configuration parameters change from release to release.

3.7 Known Issues and Limitations

You can view a complete list of functional problem reports for this product, including problems identified after product release, by accessing the STAR report on the Web. For more details, see "Details of Fixed Defects and Enhancements" on page 144. You must have a SolvNetPlus ID to view STAR reports. This release has the following known tool and packaging issues at the time of release.

- "Packaged coreConsultant Test Limitations"
- "VTB Limitations"
- "Design Example"
- "Unique Case Violation Simulation Message"
- "coreConsultant Memory Map Limitations"

3.7.1 Packaged coreConsultant Test Limitations

We invite you to submit your coreConsultant configuration for review. Because of the very large configuration space, it is not possible to regress every configuration before a release is made. Synopsys is continually running fixed and randomized configurations, but it is possible that your exact configuration has not been regressed. Test case failures might occur because of improper testbench configuration. In that case open a case through SolvNetPlus.

3.7.1.1 Known Test Failures

The following are known testbench issues:

- The AXI5 configuration cannot use the ARM AXI4 assertions.
- Viral LD-ID related to MLD and Viral Enable, and status logic update for Switch is not verified.
- LL_Reset functionality for CXL Link Layer Control and Status Register is not verified.
- The `tl_ptm_scaled_clk` test might fail with the error:

  ```
  Clk correction is too big - TB issue
  ```
- The following corner case scenarios for CXL Power Management are not fully validated at the time of the release:
  - PERST# applied after DUT transmits ALMP L1_1 Request
  - PERST# applied after link partner transmits ALMP L1_1 Status
  - Link retrain triggered after DUT transmits ALMP L1_1 Request
  - Link retrain triggered after link partner transmits ALMP L1_1 Status
- The AXI Stream or DTI feature requires AMBA SVT VIP S-2021.06-1. The tests might fail for this feature if you use AMBA SVT VIP S-2021.06.
- The `tl_cxl_channel_io_traffic*_cxl_vtb` test might fail with the following errors:
  - VIP to DUT scoreboard detected * TLPs reported as transmitted, but not received.
  - `ERROR: AER PF0: UNCORR_ERR_STATUS - UNSUPPORTED_REQUEST_ERR_POS` is set.

    This is due to a lack of support in this testbench for Alternate Memory Ranges.

    Note: Alternate Memory Ranges are verified separately.

- VTB test might fail due to the following errors:
  - For `Pm_l*_transition` tests, the test limitation cannot complete the transition. It gives the message as "Transition from `ENTER_LS -> IDLE` was not reached"
  - For `Pm_direct*` on CXS configurations, the following test issue is caused by AXI VIP when the application sends too many TLPs before exiting low power

    "`uvm_test_top.env.m_vtb_device_env[].dut_axi_sys.env.master[] [track_timeout] {OBJECT_NUM('d) PORT_ID('d) PORT_NAME() TYPE(READ) COHERENT_XACT_TYPE() ATOMIC_XACT_OP_TYPE() WRITE_WITH_CMO_XACT_TYPE() ID('h) SECURE('d) ADDR('h) CACHE_TYPE('d) START_TIME(.ns)}` Timed out"

3.7.2 Unpacking Configurations with CX_NFUNC >32

For configurations with number of Physical Functions greater than 32 (`CX_NFUNC >32`), the controller uses the same structure of IP-XACT for native and AMBA configuration for DBI register accesses.

- In case of native and DBI accesses, there are dedicated pins for PFs and VFs and you must assert as per the scenarios.
- For the `AXI_POPULATED` based configuration, you must configure the dedicated `DBI_FUNCTION_BANK_CTRL_REG` field of `DBI_FUNCTION_BANK_CTRL_REG_OFF` register for `NFUNC > 32`.

3.7.3 VTB Limitations

The following limitations apply to the current release of the VTB:

- Not backward compatible with previous releases
- Not UVM compliant
- No support for big-endian (`AHB_ENDIANNESS`) configurations

3.7.4 Design Example

The design example in `<workspace>/examples/DWC_pcie_clkrst.v` has been functionally verified, but has not been explicitly targeted for verification metrics. However, it has been used by Synopsys in the verification and regression environments for all controller configurations; including verification of all power transitions for the controller.

3.7.5 Unique Case Violation Simulation Message

The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

There is a known simulator issue with a "Unique case violation" message that occurs sometimes while running simulations with VCS outside of coreConsultant. You can ignore these messages.

To avoid these messages, use the `-xlrm uniq_prior_final` compile option in VCS. The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

3.7.6 coreConsultant Memory Map Limitations

The controller supports the generation of configuration-specific register maps as described in the "Register Configuration Space" chapter in the *Databook*. For SR-IOV configurations (`CX_SRIOV_ENABLE =1`), the following limitations apply.

Table 3-8 coreConsultant Report File Limitations for SR-IOV Configurations

CX_NVFUNC	IP-XACT (IP-XACT XML)	RALF and C Headers (No limitations)	Register Report (DocBook XML) Also applies to Databook
1–256	Defines default #VFs in each PF	Defines default #VFs in each PF	Defines only first VF in each PF
257–4096	Defines only[a] first VF in each PF	Defines default #VFs in each PF	Defines only first VF in each PF

a. For details on how to populate remaining VFs in the IP-XACT file, see "Populating IP-XACT File Manually" in the "Creating Optional Views and Reports" section in the "Configuring the controller" chapter of the User Guide.

3.7.7 VC Spyglass Limitations

- VC Spyglass support is for demonstration purpose only. Spyglass continues to be the used for Linting, CDC, and RDC signoff.
- VC Spyglass CDC has some limitations. For failure cases, contact Synopsys Support through SolvNet-Plus for further details.

3.7.8 Third-party Simulator Limitations

When you are using the QuestaSim 2020.4 simulator, and if you select the HDMA option, compilation failure can occur because the QuestaSim 2020.4 does not support System Verilog IEEE 2012 standard.

3.8 Details of Fixed Defects and Enhancements

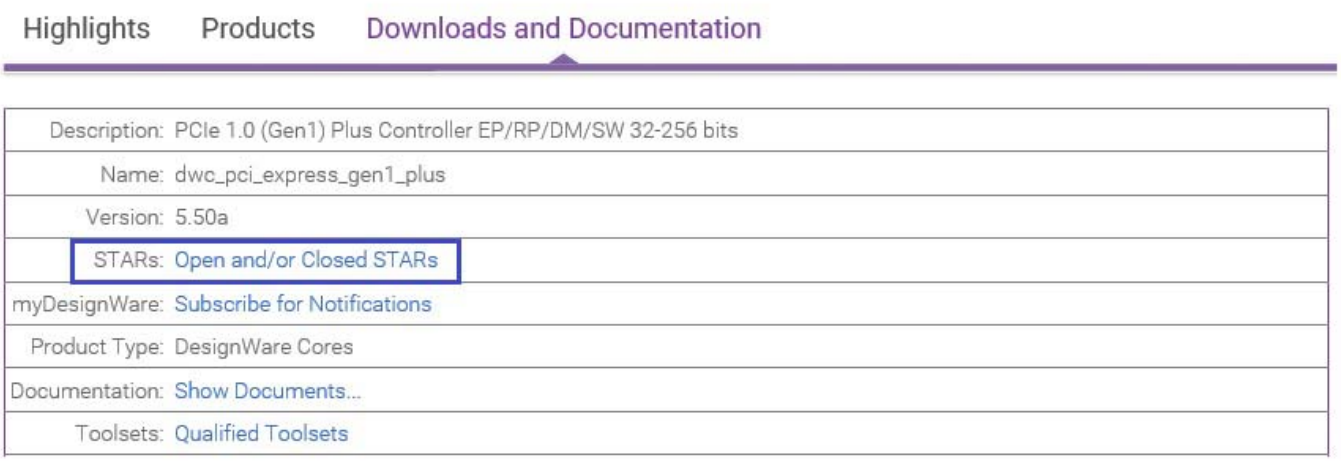
Defects fixed in release 5.96a of the controller are listed in the STAR report for release 5.96a in STARs on the Web.

Table 3-9 Controller STAR Report Location

Controller	Location
PCIe Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_controllers
CXL Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_cxl_controller
CCIX Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_ccix_controller

(A SolvNetPlus ID is required to view STAR reports.)

Figure 3-1 Accessing STARs on the Web through SolvNetPlus



Enhancement STARs are identifiable by the letter “E” in the Severity column, and fixed defect STARs are identifiable by the letter “B.” An E4 or B4 has the highest severity. Clicking on the tab corresponding to 5.96a produces a STAR report of closed STARS for this release. For previous controller versions, click the tab corresponding to the version in question.

3.9 Synopsys Statement on Inclusivity and Diversity

Synopsys is committed to creating an inclusive environment where every employee, customer, and partner feels welcomed. We are reviewing and removing exclusionary language from our products and supporting customer-facing collateral. Our effort also includes internal initiatives to remove biased language from our engineering and working environment, including terms that are embedded in our software and IPs. At the same time, we are working to ensure that our web content and software applications are usable to people of varying abilities. You may still find examples of non-inclusive language in our software or documentation as our IPs implement industry-standard specifications that are currently under review to remove exclusionary language.

3.10 Customer Support

To obtain support for your product, prepare the required files and contact the support center using one of the methods described:

- Prepare the following debug information, if applicable:
  - For environment set-up problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, select the following menu:
    - **File > Build Debug Tar-file**

    Check all the boxes in the dialog box that apply to your issue. This option gathers all the Synopsys product data needed to begin debugging an issue and writes it to the <*core tool startup directory*>/debug.tar.gz file.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD).
    - Identify the hierarchy path to the DesignWare instance.
    - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- *For the fastest response*, enter a case through SolvNetPlus:

  a. https://solvnetplus.synopsys.com

Note SolvNetPlus does not support Internet Explorer. Use a supported browser such as Microsoft Edge, Google Chrome, Mozilla Firefox, or Apple Safari.

  b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).

  c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

     Make sure to include the following:
     - **Product L1:** DesignWare Cores
     - **Product L2:** PCI Express

  d. After creating the case, attach any debug files you created.

     For more information about general usage information, refer to the following article in SolvNetPlus:

     https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources
- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
  - Attach any debug files you created.
- Or, telephone your local support center:

- North America:
  Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
- All other countries:
  https://www.synopsys.com/support/global-support-centers.html

4

Release Notes: 5.95a

These release notes describe the changes in this release *(5.95a)* relative to the previous production release *(5.90a)*.This release note contains the following sections:

- "Product Updates" on page 150
- "Changes to I/O" on page 152
- "Changes to Software View (Register Map)" on page 157
- "Changes to RAM Sizes" on page 169
- "Changes to Configuration Parameters" on page 170
- "Converting to the Current Release" on page 172
- "Known Issues and Limitations" on page 173
- "Details of Fixed Defects and Enhancements" on page 175
- "Synopsys Statement on Inclusivity and Diversity" on page 176
- "Customer Support" on page 177

4.1 Product Updates

This release contains the following major updates and other minor updates (indicated in "Details of Fixed Defects and Enhancements" on page 175).

4.1.1 CXL Updates

The CXL updates are as follows:

- CXL 2.0 Switch configuration support.
- Precision Time Management (PTM) support when the controller operates in PCIe mode.
- New ELBI2 DBI mechanism to access the 512K region of any BAR mapped to RTRGT0 for CXL 2.0 controller AXI bridge configuration.
- CXL Reset enhancement to reset the non-sticky fields of all the CXL DVSECs and CXL MEMBAR0 while sticky registers retain their value, as per CXL 2.0 specification.
- Drift Buffer and Sync Header Bypass support.
- CXL Viral handling enhancements. The CXL Viral handling now depends on the CXL controller configuration as a Device, Host, or Switch port.

For more information, see the *CXL Databook*.

Table 4-1 shows the Parameter Descriptions for `DEFAULT_CXL_PORT_USP_SYNC_HDR_BYPASS_ENABLE` and `DEFAULT_CXL_PORT_USP_DRIFT_BUFFER_ENABLE`.

Table 4-1 CXL Configuration Parameters

Label	Description
CXL Sync Header Bypass Enable bit default value	Default value for CXL Sync Header Bypass Enable bit in CXL Port DVSEC for Upstream port **Values:** 0, 1 **Default Value:** 0 **Enabled:** CC_DEVICE_TYPE==CC_EP || CC_DEVICE_TYPE==CC_DM **Parameter Type:** Register Default Value **Parameter Name:** DEFAULT_CXL_PORT_USP_SYNC_HDR_BYPASS_ENABLE
CXL Drift Buffer Enable bit default value	Default value for CXL Drift Buffer Enable bit in CXL Port DVSEC for Upstream port **Values:** 0, 1 **Default Value:** 0 **Enabled:** CC_DEVICE_TYPE==CC_EP || CC_DEVICE_TYPE==CC_DM **Parameter Type:** Register Default Value **Parameter Name:** DEFAULT_CXL_PORT_USP_DRIFT_BUFFER_ENABLE

Note In this release, CXL controller is available as an LCA (Limited Customer Availability) product.

4.1.2 AXI Updates

The PCIe controller is enhanced to support the following AXI5 features:

- AXI5 Unique ID Indicator
- AXI5 Read Data Chunking

For more information, see "AXI5 Read Data Chunking" section in the "AMBA" chapter of the *PCIe Databook*.

Note In this release, the AXI5 is available as an EA (Early Adopter) feature and must not be used for tape out. Contact Synopsys Support through SolvNetPlus for an unlocking key for this feature.

4.1.3 DOE Poisoned CfgWr Support

The PCIe controller informs the user application (DOE) if it has received poisoned CfgWr by asserting the `radm_rcvd_cfg[0|1]wr_poisoned` signals to '1'. You can enable this feature by setting the `CX_DETECT_POISONED_CFGWR` parameter to '1'.

For more information, see "SII: Detect Poisoned CfgWr Signals" section in the "Signal Descriptions" chapter of the *Reference Manual*.

4.1.4 SerDes Architecture Support for Gen5 Controller - PHY Combinations

Table 4-2 describes the new PCIe Gen5 Controller - PHY combination support for SerDes architecture (`CX_PIPE_SERDES_ARCH =1`) added in 5.96a.

Table 4-2 Gen5 Controller-PHY Combinations Supported

Controller	PHY g1_4s g2_4s_df g3_4s_df g4_4s_df g5_4s_df
g1_4s g2_4s_df g3_8s_dw g4_8s_df g5_8s_df	Yes

4.1.5 Gen4/5 Lane Margining Parameters

The PCIe controller provides additional lane margining parameters for Gen4 and Gen5 configurations.

For more information, see "Advanced PHY Config/Gen4 PHY Lane Margining Config Parameters" and "Advanced PHY Config/Gen5 PHY Lane Margining Config Parameters" sections in the "Parameter Descriptions" chapter of the *Reference Manual*.

4.2 Changes to I/O

This section details any changes to the I/O of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the I/O are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

The following table enlists the I/O changes that have occurred for all configurations:

Table 4-3 I/O Signals Added, Removed, or Renamed

Name	Type	Change	Comment
slv_armisc_info[(SLV_MISC_INFO_PW-1):0]	I	Re-purposed	Bit[6] changed **from:** TLP's EP bit **to:** Reserved
lbc_ext_rd[((4*CX_LBC_NW)-1):0]	O	Added	Indicates valid byte lanes for ELBI read.
ibh_mcpl_sb_ram_addrb	O	Signal width	Changed **from:** ibh_mcpl_sb_ram_addra[(CC_IB_MCPL_SEG_BUF_RAM_ADDR_WD-1):0] **to:** ibh_mcpl_sb_ram_addra[((CC_MSTR_CPL_SEG_N_SLICES*CC_IB_MCPL_SEG_BUF_RAM_ADDR_WD)-1):0]
ibh_mcpl_sb_ram_addra_par	O	Signal width	Changed **from:** ibh_mcpl_sb_ram_addra_par[(CC_IB_MCPL_SEG_BUF_RAM_ADDRP_WD-1):0] **to:** ibh_mcpl_sb_ram_addra_par[((CC_MSTR_CPL_SEG_N_SLICES*CC_IB_MCPL_SEG_BUF_RAM_ADDRP_WD)-1):0]
ibh_mcpl_sb_ram_addrb	O	Signal width	Changed **from:** ibh_mcpl_sb_ram_addrb[(CC_IB_MCPL_SEG_BUF_RAM_ADDR_WD-1):0] **to:**ibh_mcpl_sb_ram_addrb[((CC_MSTR_CPL_SEG_N_SLICES*CC_IB_MCPL_SEG_BUF_RAM_ADDR_WD)-1):0]
ibh_mcpl_sb_ram_addrb_par	O	Signal width	Changed **from:** ibh_mcpl_sb_ram_addrb_par[(CC_IB_MCPL_SEG_BUF_RAM_ADDRP_WD-1):0] **to:** ibh_mcpl_sb_ram_addrb_par[((CC_MSTR_CPL_SEG_N_SLICES*CC_IB_MCPL_SEG_BUF_RAM_ADDRP_WD)-1):0]

Name	Type	Change	Comment
ibh_mcpl_sb_ram_dina	O	Signal width	Changed **from:** ibh_mcpl_sb_ram_dina[(CC_IB_MCPL_SEG_BUF_RAM_DATA_WD-1):0] **to:** ibh_mcpl_sb_ram_dina[((CC_MSTR_CPL_SEG_N_SLICES*CC_MSTR_CPL_SEG_BUF_SLICE_WD)-1):0]
ibh_mcpl_sb_ram_doutb	I	Signal width	Changed **from:** ibh_mcpl_sb_ram_doutb[(CC_IB_MCPL_SEG_BUF_RAM_DATA_WD-1):0] **to:** ibh_mcpl_sb_ram_doutb[((CC_MSTR_CPL_SEG_N_SLICES*CC_MSTR_CPL_SEG_BUF_SLICE_WD)-1):0]
ibh_mcpl_sb_ram_dina	O	Signal width	Changed **from:** ibh_mcpl_sb_ram_enb **to:** ibh_mcpl_sb_ram_enb[(CC_MSTR_CPL_SEG_N_SLICES-1):0]
ibh_mcpl_sb_ram_wea	O	Signal width	Changed **from:** ibh_mcpl_sb_ram_wea **to:** ibh_mcpl_sb_ram_wea[(CC_MSTR_CPL_SEG_N_SLICES-1):0]
ibh_mcpl_sb_ram_addra	O	Signal width	Changed **from:** ib_mcpl_sb_ram_addra[(CC_IB_MCPL_SEG_BUF_RAM_ADDR_WD-1):0] **to:** ib_mcpl_sb_ram_addra[((CC_MSTR_CPL_SEG_N_SLICES*CC_IB_MCPL_SEG_BUF_RAM_ADDR_WD)-1):0]
ib_mcpl_sb_ram_addrb	O	Signal width	Changed **from:** ib_mcpl_sb_ram_addra[(CC_IB_MCPL_SEG_BUF_RAM_ADDR_WD-1):0] **to:** ib_mcpl_sb_ram_addra[((CC_MSTR_CPL_SEG_N_SLICES*CC_IB_MCPL_SEG_BUF_RAM_ADDR_WD)-1):0]

Name	Type	Change	Comment
ib_mcpl_sb_ram_addra_par	O	Signal width	Changed **from:** ib_mcpl_sb_ram_addra_par[(CC_IB_MCPL_SEG_BUF_RAM_ADDRP_WD-1):0] **to:** ib_mcpl_sb_ram_addra_par[((CC_MSTR_CPL_SEG_N_SLICES*CC_IB_MCPL_SEG_BUF_RAM_ADDRP_WD)-1):0]
ib_mcpl_sb_ram_addrb	O	Signal width	Changed **from:** ib_mcpl_sb_ram_addrb[(CC_IB_MCPL_SEG_BUF_RAM_ADDR_WD-1):0] **to:**ib_mcpl_sb_ram_addrb[((CC_MSTR_CPL_SEG_N_SLICES*CC_IB_MCPL_SEG_BUF_RAM_ADDR_WD)-1):0]
ib_mcpl_sb_ram_addrb_par	O	Signal width	Changed **from:** ib_mcpl_sb_ram_addrb_par[(CC_IB_MCPL_SEG_BUF_RAM_ADDRP_WD-1):0] **to:** ib_mcpl_sb_ram_addrb_par[((CC_MSTR_CPL_SEG_N_SLICES*CC_IB_MCPL_SEG_BUF_RAM_ADDRP_WD)-1):0]
ib_mcpl_sb_ram_dina	O	Signal width	Changed **from:** ib_mcpl_sb_ram_dina[(CC_IB_MCPL_SEG_BUF_RAM_DATA_WD-1):0] **to:** ib_mcpl_sb_ram_dina[((CC_MSTR_CPL_SEG_N_SLICES*CC_MSTR_CPL_SEG_BUF_SLICE_WD)-1):0]
ib_mcpl_sb_ram_doutb	I	Signal width	Changed **from:** ib_mcpl_sb_ram_doutb[(CC_IB_MCPL_SEG_BUF_RAM_DATA_WD-1):0] **to:** ib_mcpl_sb_ram_doutb[((CC_MSTR_CPL_SEG_N_SLICES*CC_MSTR_CPL_SEG_BUF_SLICE_WD)-1):0]
ib_mcpl_sb_ram_dina	O	Signal width	Changed **from:** ib_mcpl_sb_ram_enb **to:** ib_mcpl_sb_ram_enb[(CC_MSTR_CPL_SEG_N_SLICES-1):0]

Name	Type	Change	Comment
ib_mcpl_sb_ram_wea	O	Signal width	Changed **from:** ib_mcpl_sb_ram_wea **to:** ib_mcpl_sb_ram_wea[(CC_MSTR_CPL_SEG_N_SLICES-1):0]
ib_mcpl_sb_ram_addra	O	Signal width	Changed **from:** ib_mcpl_sb_ram_addra[(CC_IB_MCPL_SEG_BUF_RAM_ADDR_WD-1):0] **to:** ib_mcpl_sb_ram_addra[((CC_MSTR_CPL_SEG_N_SLICES*CC_IB_MCPL_SEG_BUF_RAM_ADDR_WD)-1):0]
cfg_bar[0|2|4]_[start|limit][((64*NF)-1):0] cfg_bar[1|3|5]_[start|limit][((32*NF)-1):0] cfg_exp_rom_[start|limit][((32*NF)-1):0]	O	Exists	Condition changed **from:** Always **to:** !(CX_NFUNC>32)
cfg_cxl_mbar0_corr_err[4:0] cfg_cxl_mbar0_uncorr_err[3:0] cfg_cxl_pl_reg_fatal_err[20:0]	O	Added	CXL error status signals.
cxl_viral_ldid_request[15:0]	I	Added	CX Viral mode LD-ID request signal.
cxl_viral_ldid[15:0]	O	Changed	The signal is not validated by cxl_viral_status.
cfg_cxl_dev_disable_caching cfg_cxl_dev_initiate_cache_wr_invld cxl_dev_cache_invalid cxl_dev_cache_wr_invld_cmpl	O	Changed	Exists condition **from:** (CX_CXL_ENABLE) && (CX_CXL_2_0_ENABLE) **to:** (CX_CXL_ENABLE) && (CX_CXL_2_0_ENABLE) &&(CX_CXL_CACHE_EN)
cii_lbc_cpl_status[2:0]	I	Added	Override completion status signal.

Documentation Changes

A number of signals were incorrectly described in the *Databook*. These are also highlighted in the change-tracked version of the *Reference Manual*. These are *not* RTL changes.

The following table enlists the I/O changes that have occurred for all configurations:

Table 4-4 Documentation Changes (Non-RTL)

Name	Type	Change	Comment
For many signals **Synchronous To** is corrected. These corrections are indicated in the change-tracked version of the Databook PDF which can be found at the location identified in the Databook revision history.			
cxpl_debug_info[63:0]	O	Re-purposed	■ Bit[25] is re-purposed as rplh_rcvd_idle[0],and ■ Bit[24] is re-purposed as rplh_rcvd_idle[1]
diag_status_bus[CX_DIAG_STATUS_BUS_WD-1:0]	O	Re-purposed	■ xmlh_xdlh_halt is re-purposed as xplh_xdlh_halt ■ xdlh_xmlh_sdp is re-purposed as xdlh_xplh_sdp ■ xdlh_xmlh_eot is re-purposed as xdlh_xplh_eot ■ rmlh_rdlh_pkt_data is re-purposed as rplh_rdlh_pkt_data ■ rmlh_rdlh_pkt_err is re-purposed as rplh_rdlh_pkt_err ■ rmlh_rdlh_pkt_dv is re-purposed as rplh_rdlh_pkt_dv ■ rmlh_rdlh_pkt_edb is re-purposed as rplh_rdlh_pkt_edb ■ rmlh_rdlh_pkt_end is re-purposed as rplh_rdlh_pkt_end ■ rmlh_rdlh_tlp_start is re-purposed as rplh_rdlh_tlp_start ■ rmlh_rdlh_dllp_start is re-purposed as rplh_rdlh_dllp_start ■ rmlh_rdlh_nak is re-purposed as rplh_rdlh_nak ■ rmlh_rcvd_idle1 is re-purposed as rplh_rcvd_idle1 ■ rmlh_rcvd_idle0 is re-purposed as rplh_rcvd_idle0 ■ xadm_notlp_pending is re-purposed as xadm_tlp_pending

4.3 Changes to Software View (Register Map)

This section discusses changes to the register map of the controller that have occurred in this release.

- It lists renamed registers.
- It lists deleted registers.
- It does *not* list new registers.
- *All* changes to the software map are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

The following changes have occurred for all configurations.

Table 4-5 Register Deletions/Renaming

Register	Nature of Change
SPCIE_CAP_OFF_20H_REG SPCIE_CAP_OFF_28H_REG SPCIE_CAP_OFF_24H_REG SPCIE_CAP_OFF_2CH_REG SPCIE_CAP_OFF_30H_REG SPCIE_CAP_OFF_34H_REG SPCIE_CAP_OFF_38H_REG SPCIE_CAP_OFF_3CH_REG SPCIE_CAP_OFF_40H_REG	Removed

Documentation Changes

A number of registers were incorrectly described in the IP-XACT XML, DocBook XML, RAL files, header files, and *Register Descriptions* PDF. These are also highlighted in the change-tracked version of the *Reference Manual* PDF. These are *not* RTL changes.

Table 4-6 Documentation Changes (Non-RTL)

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
STATUS_COMMAND_REG	PCI_TYPE0_IO_EN	Y			
BAR0_REG	BAR0_PREFETCH	Y			
	BAR0_MEM_IO	Y			
BAR1_REG	BAR1_PREFETCH	Y			
	BAR1_TYPE	Y			
	BAR1_MEM_IO	Y			
BAR2_REG	BAR2_PREFETCH	Y			
	BAR2_MEM_IO	Y			
BAR3_REG	BAR3_PREFETCH	Y			
	BAR3_TYPE	Y			
	BAR3_MEM_IO	Y			
BAR4_REG	BAR4_PREFETCH	Y			
	BAR4_MEM_IO	Y			
BAR5_REG	BAR5_PREFETCH	Y			
	BAR5_TYPE	Y			
	BAR5_MEM_IO	Y			

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
SPCIE_CAP_OFF_20H_REG	USP_RX_PRESET_HINT11	Y			Y
	USP_TX_PRESET11	Y			Y
	USP_RX_PRESET_HINT10	Y			Y
	USP_TX_PRESET10	Y			Y
	DSP_RX_PRESET_HINT11	Y			Y
	DSP_TX_PRESET11	Y			Y
	DSP_RX_PRESET_HINT10	Y			Y
	DSP_TX_PRESET10	Y			Y
SPCIE_CAP_OFF_24H_REG	USP_RX_PRESET_HINT13	Y			Y
	USP_TX_PRESET13	Y			Y
	USP_RX_PRESET_HINT12	Y			Y
	USP_TX_PRESET12	Y			Y
	DSP_RX_PRESET_HINT13	Y			Y
	DSP_TX_PRESET13	Y			Y
	DSP_RX_PRESET_HINT12	Y			Y
	DSP_TX_PRESET12	Y			Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
SPCIE_CAP_OFF_28H_REG	USP_RX_PRESET_HINT15	Y			Y
	USP_TX_PRESET15	Y			Y
	USP_RX_PRESET_HINT14	Y			Y
	USP_TX_PRESET14	Y			Y
	DSP_RX_PRESET_HINT15	Y			Y
	DSP_TX_PRESET15	Y			Y
	DSP_RX_PRESET_HINT14	Y			Y
	DSP_TX_PRESET14	Y			Y
CXL_RCRB_FLEXBUS_CNTRL_STATUS_OFF	CXL_RETIMER_PSNT_MISMATCH			Y	
MEMBAR0_LINK_RX_CR_CNTRL_REG_OFF	CXL_RCRB_MEMBAR0_LINK_CTL_MEM_REQ_RSP_CRD	Y			Y
	CXL_RCRB_MEMBAR0_LINK_CTL_CACHE_DATA_CRD	Y			Y
	CXL_RCRB_MEMBAR0_LINK_CTL_CACHE_RSP_CRD	Y			Y
	CXL_RCRB_MEMBAR0_LINK_CTL_CACHE_REQ_CRD	Y			Y
MEMBAR0_LINK_RX_CR_CNTRL_2_REG_OFF	CXL_RCRB_MEMBAR0_LINK_CTL_MEM_DATA_CRD	Y			Y
	CXL_RCRB_MEMBAR0_LINK_CTL_MEM_REQ_RSP_CRD_2	Y			Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
MEMBAR0_LINK_RX_CR_RTN_STATUS_REG_OFF	CXL_RCRB_MEMBAR0_LINK_ST_MEM_REQ_RSP_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_ST_CACHE_DATA_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_ST_CACHE_RSP_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_ST_CACHE_REQ_CRD	Y			Y
MEMBAR0_LINK_RX_CR_RTN_STATUS_2_REG_OFF	CXL_RCRB_MEMBAR0_LINK_ST_MEM_DATA_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_ST_MEM_REQ_RSP_CRD_2				Y
MEMBAR0_LINK_TX_CR_STATUS_REG_OFF	CXL_RCRB_MEMBAR0_LINK_TX_MEM_REQ_RSP_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_TX_CACHE_DATA_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_TX_CACHE_RSP_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_TX_CACHE_REQ_CRD				Y
MEMBAR0_LINK_TX_CR_STATUS_2_REG_OFF	CXL_RCRB_MEMBAR0_LINK_TX_MEM_DATA_CRD				Y
	CXL_RCRB_MEMBAR0_LINK_TX_MEM_REQ_RSP_CRD_2				Y
MEMBAR0_LINK_DEFEATURE_REG_OFF	CXL_RCRB_MEMBAR0_LINK_MDH_DISABLE	Y			Y
PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG	PCIE_INT_MSG_NUM	Y	Y		
	PCIE_SLOT_IMP	Y	Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
DEVICE_CAPABILITIES_REG	PCIE_CAP_FLR_CAP	Y	Y		
	PCIE_CAP_ROLE_BASED_ERR_REPORT	Y	Y		
	PCIE_CAP_EP_L1_ACCPT_LATENCY	Y	Y		
	PCIE_CAP_EP_L0S_ACCPT_LATENCY	Y	Y		
	PCIE_CAP_EXT_TAG_SUPP	Y	Y		
	PCIE_CAP_PHANTOM_FUNC_SUPPORT	Y	Y		
	PCIE_CAP_MAX_PAYLOAD_SIZE	Y	Y		
DEVICE_CONTROL_DEVICE_STATUS	PCIE_CAP_INITIATE_FLR	Y		Y	
	PCIE_CAP_MAX_READ_REQ_SIZE	Y	Y		
	PCIE_CAP_EN_NO_SNOOP	Y	Y		
	PCIE_CAP_EXT_TAG_EN	Y	Y		
	PCIE_CAP_MAX_PAYLOAD_SIZE_CS	Y			
	PCIE_CAP_EN_REL_ORDER	Y	Y		
	PCIE_CAP_UNSUPPORT_REQ_REP_EN	Y			
	PCIE_CAP_FATAL_ERR_REPORT_EN	Y			
	PCIE_CAP_NON_FATAL_ERR_REPORT_EN	Y			
	PCIE_CAP_CORR_ERR_REPORT_EN	Y			
LINK_CONTROL_LINK_STATUS_REG	PCIE_CAP_DLL_ACTIVE				Y
	PCIE_CAP_NEGO_LINK_WIDTH				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
DEVICE_CAPABILITIES2_REG	PCIE_CAP_FRS_SUPPORTED	Y	Y		
	PCIE_CAP_DMWR_LEN_SUPP		Y		
	PCIE_CAP_DMWR_CPL_SUPP		Y		
	PCIE_CAP2_CFG_MAX_END2END_TLP_PRFXS	Y	Y		
	PCIE_CAP2_CFG_END2END_TLP_PRFX_SUPPORT	Y	Y		
	PCIE_CAP2_CFG_EXTND_FMT_SUPPORT	Y	Y		
	PCIE_CAP_OBFF_SUPPORT	Y	Y		
	PCIE_CAP2_10_BIT_TAG_REQ_SUPPORT		Y		
	PCIE_CAP2_10_BIT_TAG_COMP_SUPPORT		Y		
	PCIE_CAP_TPH_CMPLT_SUPPORT_0		Y		
	PCIE_CAP_LTR_SUPP	Y	Y		
	PCIE_CAP_NO_RO_EN_PR2PR_PAR		Y		
	PCIE_CAP_128_CAS_CPL_SUPP		Y		
	PCIE_CAP_64_ATOMIC_CPL_SUPP		Y		
	PCIE_CAP_32_ATOMIC_CPL_SUPP		Y		
	PCIE_CAP_CPL_TIMEOUT_DISABLE_SUPPORT		Y		
	PCIE_CAP_CPL_TIMEOUT_RANGE		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
DEVICE_CONTROL2_DEVICE_STATUS2_REG	PCIE_CAP_OBFF_EN	Y			
	PCIE_CAP_EMERGENCY_PWR_RED_REQUEST	Y			
	PCIE_CAP_10BITS_TAG_REQ_EN	Y	Y		
	PCIE_CAP_IDO_CPL_EN	Y			
	PCIE_CAP_IDO_REQ_EN	Y			
	PCIE_CAP_ATOMIC_EGRESS_BLK				Y
	PCIE_CAP_ATOMIC_REQ_EN	Y			
	PCIE_CAP_CPL_TIMEOUT_DISABLE	Y	Y		
	PCIE_CAP_CPL_TIMEOUT_VALUE	Y			
	PCIE_CTRL2_CFG_END2END_TLP_PFX_BLCK				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
SHADOW_LINK_CAPABILITIES_REG	SHADOW_PCIE_CAP_L0S_EXIT_LATENCY				Y
	SHADOW_PCIE_CAP_L1_EXIT_LATENCY				Y
	PCIE_CAP_PORT_NUM				Y
	PCIE_CAP_ASPM_OPT_COMPLIANCE				Y
	PCIE_CAP_LINK_BW_NOT_CAP				Y
	PCIE_CAP_DLL_ACTIVE_REP_CAP				Y
	PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP				Y
	PCIE_CAP_CLOCK_POWER_MAN				Y
	PCIE_CAP_ACTIVE_STATE_LINK_PM_SUPPORT				Y
	PCIE_CAP_MAX_LINK_WIDTH				Y
	PCIE_CAP_MAX_LINK_SPEED				Y
NPEM_STATUS_OFF	NPEM_CMD_COMPLETE	Y			
VF_PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG	PCIE_INT_MSG_NUM		Y		
	PCIE_SLOT_IMP		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
VF_DEVICE_CAPABILITIES_REG	PCIE_CAP_FLR_CAP		Y		
	PCIE_CAP_ROLE_BASED_ERR_REPORT		Y		
	PCIE_CAP_EP_L1_ACCPT_LATENCY		Y		
	PCIE_CAP_EP_L0S_ACCPT_LATENCY		Y		
	PCIE_CAP_PHANTOM_FUNC_SUPPORT		Y		
	PCIE_CAP_MAX_PAYLOAD_SIZE		Y		
VF_DEVICE_CONTROL_DEVICE_STATUS	PCIE_CAP_INITIATE_FLR	Y			
VF_LINK_CONTROL_LINK_STATUS_REG	PCIE_CAP_DLL_ACTIVE				Y
	PCIE_CAP_NEGO_LINK_WIDTH				Y

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
VF_DEVICE_CAPABILITIES2_REG	PCIE_CAP_FRS_SUPPORTED	Y	Y		
	PCIE_CAP_DMWR_LEN_SUPP		Y		
	PCIE_CAP_DMWR_CPL_SUPP		Y		
	PCIE_CAP2_CFG_EXTND_FMT_SUPPORT		Y		
	PCIE_CAP_OBFF_SUPPORT		Y		
	PCIE_CAP2_10_BIT_TAG_REQ_SUPPORT		Y		
	PCIE_CAP2_10_BIT_TAG_COMP_SUPPORT		Y		
	PCIE_CAP_TPH_CMPLT_SUPPORT_0		Y		
	PCIE_CAP_LTR_SUPP		Y		
	PCIE_CAP_128_CAS_CPL_SUPP		Y		
	PCIE_CAP_64_ATOMIC_CPL_SUPP		Y		
	PCIE_CAP_32_ATOMIC_CPL_SUPP		Y		
	PCIE_CAP_CPL_TIMEOUT_DISABLE_SUPPORT		Y		
	PCIE_CAP_CPL_TIMEOUT_RANGE		Y		
VF_DEVICE_CONTROL2_DEVICE_STATUS2_REG	PCIE_CAP_EMERGENCY_PWR_RED_REQUEST	Y			
	PCIE_CAP_10BITS_TAG_REQ_EN		Y		
	PCIE_CAP_ATOMIC_EGRESS_BLK				Y
	PCIE_CAP_CPL_TIMEOUT_DISABLE		Y		
	PCIE_CTRL2_CFG_END2END_TLP_PFX_BLCK				Y
	PCIE_CAP_SUPPORT_LINK_SPEED_VECTOR		Y		

Register	Register Field	Memory Access is Corrected	Value After Reset is Corrected	Testable is Corrected	Fields are Made Visible
VF_LINK_CONTROL2_LINK_STATUS2_REG	PCIE_CAP_CROSSLINK_RESOLUTION		Y		

4.4 Changes to RAM Sizes

This section details the changes to the default RAM sizes that have occurred since the last production release. It does not detail changes that are associated with new or additional features that you enable on your current configuration

Caution To determine the precise changes to RAM sizes for your actual controller configuration, you can compare the coreConsultant generated RAM sizes for the previous and current releases. For more details, see the “RAM Requirements” section in the Architecture chapter of the *Databook*.

The following changes have occurred for this release.

Table 4-7 RAM Changes

RAM Name	Change
AXI Slave Non-Posted Set-Aside Buffer RAM	The internal width of the slv_awlen and slv_arlen is reduced from 8 to log2(CC_SLV_BURST_LEN). The RAM has a four bit reduction in width.
AXI Master Non-Posted Read Request Buffer RAM AXI Master Read Queue Request Formation CDC Buffer RAM AXI Master Write Queue Request Formation CDC Buffer RAM	The RAM width is increased by one bit.
Depth calculation for P tracker data and header buffers are updated. The P tracker is not enabled by default.	

4.5 Changes to Configuration Parameters

This section details any changes to the configuration parameters of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the configuration parameters are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

If you intend to source an existing configuration batch file, then you must first convert your configuration file, as described in "Product Updates" on page 150. If you are not sourcing an existing configuration batch file, then you should be still aware of changes to the default value of some configuration parameters.

Caution

To ensure that your existing configuration absorbs all changes to default parameters updated for this release, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

The *Write default Parameter* should only be used for debugging.

Table 4-8 Configuration Parameter Changes

Name	Change
CC_LEGACY_DMA_MAP	Default value changed **from:** CC_DMA_ENABLE_VALUE == 1 && CC_NUM_DMA_WR_CHAN < 9&& CC_NUM_DMA_RD_CHAN < 9) ? 1 : (!CX_DMA_PF_ENABLE **to:** !CX_DMA_PF_ENABLE
PL_LIMIT	Default value changed **from:** 3172 **to** 3208
FIRST_VF_OFFSET_ARI_CAP_HIER1_n	Default Value changed **from:** (CX_NFUNC>=17) ? 32 : (CX_NFUNC>=9) ? 16 : (CX_NFUNC>=5) ?8 : (CX_NFUNC>=3) ? 4 : CX_NFUNC **to:** (CX_NFUNC>=33) ? 64 : (CX_NFUNC>=17) ? 32 : (CX_NFUNC>=9)? 16 : (CX_NFUNC>=5) ? 8 : (CX_NFUNC>=3) ? 4 : CX_NFUNC
VFINDEX_CALC_REGOUT	Default value changed **from:** (CX_NFUNC>=17) ? 32 : (CX_NFUNC>=9) ? 16 : (CX_NFUNC>=5) ? 8 : (CX_NFUNC>=3) ? 4 : CX_NFUNC **to:** CX_SRIOV_ENABLE && (CX_NVFUNC>32 || CX_NFUNC>32) Enabled changed **from:** CX_SRIOV_ENABLE && !CX_VF_STRIDE_ALWAYS_ONE **to:** CX_SRIOV_ENABLE==1

Name	Change
CX_RADM_LUT_TO_FETCH_PIPE	Default Value changed **from:** 0 **to:** 1 Enabled changed **from:** CX_CUSTOM_PIPELINING && CX_RADM_LUT_TO_FETCH_PIPE_LOCK **to:** CX_CUSTOM_PIPELINING
RADM_CPLQ_HDP_VC0	Enabled changed **from:** (AMBA_INTERFACE == 0 && CC_DMA_ENABLE == 0) &&CX_RADMQ_MODE!=0 && RADM_CPL_QMODE_VC0!=4 &&(RADM_DEPTH_DECOUPLE_VC0==1 || RADM_CPLQ_HCRD_VC0 == 0) **to:** ((AMBA_INTERFACE == 0 && CC_DMA_ENABLE == 0) ||CX_CPLQ_MANAGEMENT_ENABLE) && CX_RADMQ_MODE!=0 &&RADM_CPL_QMODE_VC0!=4 && (RADM_DEPTH_DECOUPLE_VC0==1 ||RADM_CPLQ_HCRD_VC0 == 0)
RADM_CPLQ_DDP_VC0	Enabled changed **from:** (AMBA_INTERFACE == 0 && CC_DMA_ENABLE == 0) &&CX_RADMQ_MODE!=0 && RADM_CPL_QMODE_VC0!=4 &&(RADM_DEPTH_DECOUPLE_VC0==1 || RADM_CPLQ_DCRD_VC0 == 0) **to:** ((AMBA_INTERFACE == 0 && CC_DMA_ENABLE == 0) ||CX_CPLQ_MANAGEMENT_ENABLE) && CX_RADMQ_MODE!=0 &&RADM_CPL_QMODE_VC0!=4 && (RADM_DEPTH_DECOUPLE_VC0==1 ||RADM_CPLQ_DCRD_VC0 == 0)
RADM_CPLQ_DDP_VCn	Enabled changed **from:** (AMBA_INTERFACE == 0 && CC_DMA_ENABLE == 0) && CX_NVC>1 &&CX_RADMQ_MODE==2 && RADM_CPL_QMODE_VC1!=4 &&(RADM_DEPTH_DECOUPLE_VC1==1 || RADM_CPLQ_DCRD_VC1 == 0) **to:** ((AMBA_INTERFACE == 0 && CC_DMA_ENABLE == 0) ||CX_CPLQ_MANAGEMENT_ENABLE) && CX_NVC>1 && CX_RADMQ_MODE==2&& RADM_CPL_QMODE_VC1!=4 && (RADM_DEPTH_DECOUPLE_VC1==1 ||RADM_CPLQ_DCRD_VC1 == 0)
Advanced PHY Config / Gen4 PHY Lane Margining Config Parameters	‘Advanced PHY Config / PHY Lane Margining Config Parameters’ are renamed as ‘Advanced PHY Config / Gen4 PHY Lane Margining Config Parameters’

4.6 Converting to the Current Release

Sometimes a new controller release might no longer use a certain configuration parameter, or the meaning of that parameter might have changed. The following process helps you convert your current configuration file so that it creates the same RTL with the new controller.

1. Open coreConsultant and create an unconfigured workspace from the newly installed controller.
2. In the coreConsultant command line, enter the following command:

   ```
   parse_configfile my_configfile.config
   ```

   where `my_configfile.config` is your current configuration file. This command creates an updated configuration file in your working directory as follows:

   ```
   my_configfile.config.new
   ```
3. In the coreConsultant command line, enter the following command:

   ```
   source my_configfile.config.new
   ```
4. Select Apply to generate the new RTL with the updated or translated parameters.
5. From the File Menu, select Write Batch Script and save the configuration file for the new release.
6. When you source the updated configuration file in coreConsultant, you can *ignore any new warnings* about parameter settings that are not relevant to, or not enabled in your configuration.

Attention

Writing Out Your Configuration File

To ensure that your existing configuration absorbs all changes to default parameters updated for this release, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

You must convert your configuration file. Failure to do so, can result in:

- Your configuration file being incompatible with the current release.
- Functional, architectural, RAM, and I/O changes when the default of some configuration parameters change from release to release.

4.7 Known Issues and Limitations

You can view a complete list of functional problem reports for this product, including problems identified after product release, by accessing the STAR report on the Web. For more details, see "Details of Fixed Defects and Enhancements" on page 175. You must have a SolvNet ID to view STAR reports. This release has the following known tool and packaging issues at the time of release.

- "Packaged coreConsultant Test Limitations"
- "VTB Limitations"
- "Design Example"
- "Unique Case Violation Simulation Message"
- "coreConsultant Memory Map Limitations"

4.7.1 Packaged coreConsultant Test Limitations

We invite you to submit your coreConsultant configuration for review. Because of the very large configuration space, it is not possible to regress every configuration before a release is made. Synopsys is continually running fixed and randomized configurations, but it is possible that your exact configuration has not been regressed. Test case failures might occur because of improper testbench configuration. In that case open a case through SolvNetPlus.

4.7.1.1 Known Test Failures

The following are known testbench issues:

- The AXI5 configuration cannot use the ARM AXI4 assertions.
- Viral LD-ID related to MLD and Viral Enable, and status logic update for Switch is not verified.
- LL_Reset functionality for CXL Link Layer Control and Status Register is not verified.
- ALMP Status resolution related to CXL PM is not verified.
- Alternate Memory Ranges are not fully verified.
- The `tl_ptm_scaled_clk` test might fail with the error:

  ```
  Clk correction is too big - TB issue
  ```

- The `pm_direct_up_vdut_cpcie_l1_pcipm_msg_req_exit_turnoff` tests might fail in CXL configurations. PM is not fully supported by CXL configurations.
- The `pm_l1_transitions_dw_vdut_cpcie_l1_link_entr_l1_idle` test might fail with error:

  ```
  vm_test_top [] Transition from S_LINK_ENT_L -> S_IDLE was not reached
  ```

  The test fails when `pclk` and `aux_clk` frequencies are almost the same.

4.7.2 VTB Limitations

The following limitations apply to the current release of the VTB:

- Not backward compatible with previous releases
- Not UVM compliant
- No support for big-endian (`AHB_ENDIANNESS`) configurations

4.7.3 Design Example

The design example in `<workspace>/examples/DWC_pcie_clkrst.v` has been functionally verified, but has not been explicitly targeted for verification metrics. However, it has been used by Synopsys in the verification and regression environments for all controller configurations; including verification of all power transitions for the controller.

4.7.4 Unique Case Violation Simulation Message

The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

There is a known simulator issue with a "Unique case violation" message that occurs sometimes while running simulations with VCS outside of coreConsultant. You can ignore these messages.

To avoid these messages, use the `-xlrm uniq_prior_final` compile option in VCS. The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

4.7.5 coreConsultant Memory Map Limitations

The controller supports the generation of configuration-specific register maps as described in the "Register Configuration Space" chapter in the *Databook*. For SR-IOV configurations (`CX_SRIOV_ENABLE =1`), the following limitations apply.

Table 4-9 coreConsultant Report File Limitations for SR-IOV Configurations

CX_NVFUNC	IP-XACT (IP-XACT XML)	RALF and C Headers (No limitations)	Register Report (DocBook XML) Also applies to Databook
1–256	Defines default #VFs in each PF	Defines default #VFs in each PF	Defines only first VF in each PF
257–4096	Defines only[a] first VF in each PF	Defines default #VFs in each PF	Defines only first VF in each PF

a. For details on how to populate remaining VFs in the IP-XACT file, see "Populating IP-XACT File Manually" in the "Creating Optional Views and Reports" section in the "Configuring the controller" chapter of the User Guide.

4.7.6 VC Spyglass Limitations

VC Spyglass support is used for demonstration only while Spyglass continues to be the used for Linting, CDC and RDC signoff.

4.7.7 Third-party Simulator Limitations

When you are using the QuestaSim 2019.4 simulator, and if you select the HDMA option, compilation failure can occur because the QuestaSim 2019.4 does not support System Verilog IEEE 2012 standard.

4.8 Details of Fixed Defects and Enhancements

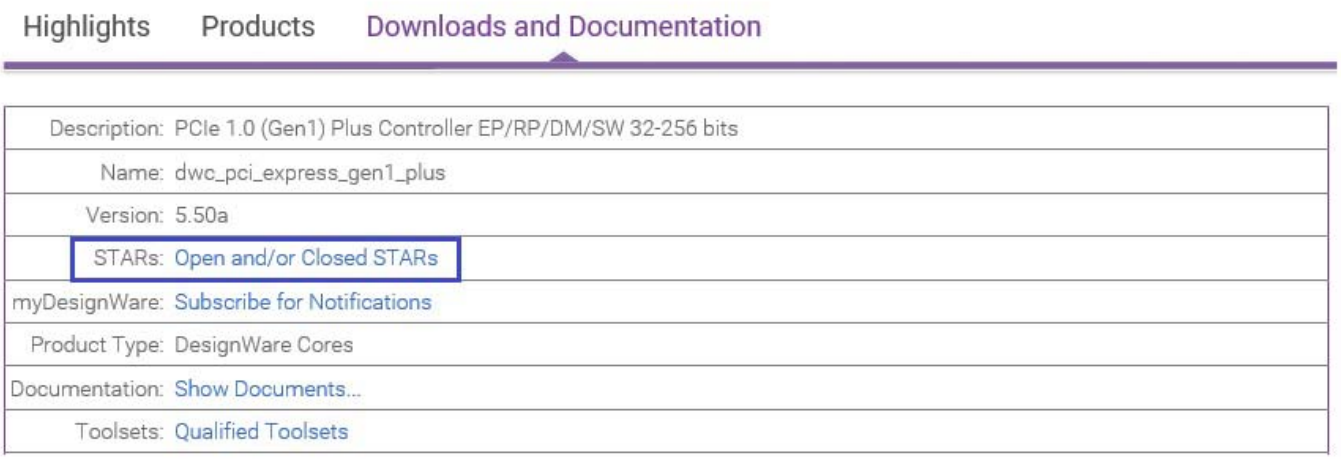
Defects fixed in release 5.95a of the controller are listed in the STAR report for release 5.95a in STARs on the Web.

Table 4-10 Controller STAR Report Location

Controller	Location
PCIe Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_controllers
CXL Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_cxl_controller
CCIX Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_ccix_controller

(A SolvNetPlus ID is required to view STAR reports.)

Figure 4-1 Accessing STARs on the Web through SolvNetPlus



Enhancement STARs are identifiable by the letter “E” in the Severity column, and fixed defect STARs are identifiable by the letter “B.” An E4 or B4 has the highest severity. Clicking on the tab corresponding to 5.95a produces a STAR report of closed STARS for this release. For previous controller versions, click the tab corresponding to the version in question.

4.9 Synopsys Statement on Inclusivity and Diversity

Synopsys is committed to creating an inclusive environment where every employee, customer, and partner feels welcomed. We are reviewing and removing exclusionary language from our products and supporting customer-facing collateral. Our effort also includes internal initiatives to remove biased language from our engineering and working environment, including terms that are embedded in our software and IPs. At the same time, we are working to ensure that our web content and software applications are usable to people of varying abilities. You may still find examples of non-inclusive language in our software or documentation as our IPs implement industry-standard specifications that are currently under review to remove exclusionary language.

4.10 Customer Support

To obtain support for your product, prepare the required files and contact the support center using one of the methods described:

- Prepare the following debug information, if applicable:
  - For environment set-up problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, select the following menu:
    - **File > Build Debug Tar-file**

    Check all the boxes in the dialog box that apply to your issue. This option gathers all the Synopsys product data needed to begin debugging an issue and writes it to the <*core tool startup directory*>/debug.tar.gz file.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD).
    - Identify the hierarchy path to the DesignWare instance.
    - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- *For the fastest response*, enter a case through SolvNetPlus:

  a. https://solvnetplus.synopsys.com

Note SolvNetPlus does not support Internet Explorer. Use a supported browser such as Microsoft Edge, Google Chrome, Mozilla Firefox, or Apple Safari.

  b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).

  c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

     Make sure to include the following:

     - **Product L1:** DesignWare Cores
     - **Product L2:** PCI Express

  d. After creating the case, attach any debug files you created.

     For more information about general usage information, refer to the following article in SolvNetPlus:

     https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
  - Attach any debug files you created.
- Or, telephone your local support center:

- North America:
  Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
- All other countries:
  https://www.synopsys.com/support/global-support-centers.html

5

Release Notes: 5.90a

These release notes describe the changes in this release *(5.90a)* relative to the previous production release *(5.80a)*.

This release note contains the following sections:

- "Product Updates" on page 180
- "Changes to I/O" on page 183
- "Changes to Software View (Register Map)" on page 185
- "Changes to RAM Sizes" on page 196
- "Changes to Configuration Parameters" on page 197
- "Converting to the Current Release" on page 200
- "Known Issues and Limitations" on page 201
- "Details of Fixed Defects and Enhancements" on page 204
- "Customer Support" on page 205

5.1 Product Updates

This release contains the following major updates and other minor updates (indicated in "Details of Fixed Defects and Enhancements" on page 204).

5.1.1 CXL Updates

The following CXL updates are done in this release:

- CXL 2.0 support, as defined in the *Compute Express Link Specification Revision 2 Version 0.9*. The CXL controller provides support for the following CXL 2.0 features also:
  - Multi-Logical Device (MLD)
  - CXL Reset (Enhanced FLR)
  - Cache Management
    - Device Disable Caching
    - Device Cache Writeback and Invalidate Cache
  - Device PM Initialization Completion reporting
  - DevLoad Field support in S2M NDR Message
  - Viral LD-ID Field support in Retry.Ack Payload
  - Backward compatibility with CXL 1.1 (Option to linkup in CXL 1.1 mode)
- ELBI support for CXL Host
- Relaxed ordering between M2S Req and M2S RwD messages channels to align with the clarification provided in *Compute Express Link Specification Revision 2 Version 0.9*
- Poison Bit support
- Application Viral interface
- Header Log for Uncorrectable Errors
- Multi-Data Header check
- CXS data protection for CXS.B CXL controller
- CCIX over 64B Flits support for CXS.B CXL controller

Attention Configurations with application interface running at 2 GHz, needs an update in Multi-Cycle Path RTL and related constraints.

Note In this release, CXL controller is available as an LCA (Limited Customer Availability) feature.

5.1.2 Enhanced Configuration Access Mechanism (ECAM)

The controller supports the optional Enhanced Configuration Access Mechanism (ECAM) feature of a Downstream port as defined in *PCI Express Base Specification Revision 5.0, Version 1.0*. To enable ECAM feature you must set the parameter `CX_SBSA_ECAM` to '1'.

For more information on ECAM, see "Enhanced Configuration Access Mechanism" section in the "Controller Operations" chapter of the *Databook*.

Note In this release, the ECAM is available as an EA (Early Adopter) feature and must not be used for tape out. Contact Synopsys Support through SolvNetPlus for an unlocking key for this feature.

5.1.3 Data Throttling

In this enhancement Dynamic Pacing is renamed as Data Throttling as per the *PIPE Specification for PCI Express, Version 4.4.1, Version 5.1.1*.

For more information, see "Gen2/Gen3/Gen4/Gen5 Modes" topic in "Frequency, Speed, and Width Support" section in the "Product Overview" chapter of the *Databook*.

5.1.4 Support for Additional Gen5 Controller-PHY Combinations

Table 5-1 describes the new Gen5 controller-PHY combinations.

Table 5-1 Gen5 Configurations

Rate	Controller	PHY
Gen1	4s (62.5 MHz)	4s (62.5 MHz)
Gen2	4s (125 MHz)	4s (125 MHz)
Gen3	4s (250 MHz)	4s (250 MHz)
Gen4	8s (250 MHz)	8s (250 MHz)
Gen5	8s (500 MHz)	8s (500 MHz)

5.1.5 EQ Bypass Redo from Lower Rate

The controller can redo equalization for Gen3 and Gen4 rate after performing equalization for Gen5. To enable this feature set the `EQ_BYPASS_HIGHEST_RATE_SUPPORT` field of the `PL32G_CAPABILITY_REG` register to '1'.

For more information see the "Gen5 and Above" topic in the "Equalization Overview and Synopsys-Specific Features" topic of the "Advanced Information: Gen3/4/5 Equalization Details and Example" chapter in the *Databook*.

5.1.6 Fine-Grained Reset Generation for PHYs

The controller supports an improved reset sequence that offers fine-tuned control to meet your PHY requirements. The features of this enhancements are as follows:

- The application access to the controller register space no longer depends on the readiness of the PHY. It can be performed as soon as a cold or warm reset completes.
- A new reset request signal (pm_req_phy_perst) and a corresponding reset signal in the clk/rst (phy_perst_n) have been added. These can be used to separately reset a PHY hard macro during a warm reset.

- This new behaviour is controllable through a design parameter and a register.
- You can use the `DEFAULT_PHY_PERST_ON_WARM_RESET` parameter and `PHY_PERST_ON_WARM_RESET` register to control the behaviour of the new reset signal.
- You can control the separation between the `phy_perst_n` and the `phy_rst_n` (used for PIPE reset) signals using the `CX_PMA_PIPE_RST_DELAY_TIMER` internal parameter and the `PMA_PIPE_RST_DELAY_TIMER` register.
- The application can still use the `app_hold_phy_rst` to maintain the PIPE reset asserted for an arbitrary amount of time.

5.2 Changes to I/O

This section details any changes to the I/O of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the I/O are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

The following table enlists the I/O changes that have occurred for all configurations:

Table 5-2 I/O Signals Added, Removed, or Renamed

Name	Type	Change	Comment
lbc_ext_cxl_mbar0_access	O	Added	Indicates that the current ELBI access is for CXL MEMBAR0.
cfg_cxl_dev_range1_* cfg_cxl_dev_range2_*	O	Added	Flex Bus range 1 and range2 related information
cfg_cxl_dev_range2_mem_*	O	Added	CXL Viral Mode Request
cxl_viral_request	O	Added	Flex Bus range 2 related information that you can use
cxl_ras_stat_rx_uncorr[7:0]	I	Exists	Condition changed **from**: (CX_CXL_CHI_ENABLE) && ((CX_CXL_CHI_DATACHK > 0) ? CX_CXL_ENABLE : 0) **to**: (CX_CXL_ENABLE &&!CX_CXL_CXS_ENABLE)) && ((CX_CXL_CHI_DATACHK > 0) ? CX_CXL_ENABLE : 0)
All the ELBI Interface Signals	*	Exists	Condition changed **from**: Always **to**: !(CX_IS_RC && !CX_CXL_ENABLE)
smlh_cxl_enabled[5:0]	O	Signal Width	The signal width is changed **from**: [3:0] **to**: [5:0]. Provides additional information corresponding to CXL 2.0 support and Multi Logic Device.
pm_req_phy_perst	O	Added	Request from controller's PMC to the DWC_pcie_clkrst.v to assert the phy_perst_n output
lbc_ext_dbi_access	O	Added	Indicates that the current ELBI access is initiated using DBI.
vlsm_mc_state	O	Added	CXL.cache/mem vLSM state
vlsm_io_state	O	Added	CXL.io vLSM state
mstr_a*len	O	Signal Width	The minimum width is set as 4 bits for AXI3 (AMBA_INTERFACE==2) configurations and 8 bits for AXI4 and AXI5 (AMBA_INTERFACE==3 || 4)configurations

Note The following signals were not described in the “Changes to I/O” section of the PCIe 5.80a Release Notes.

- mstr_bmisc_info_cpl_stat/mstr_rmisc_info_cpl_stat- Signal width changed to 3 bits
- app_err_bus[(ERR_BUS_WD-1):0]- Signal width changed to 15 bits

Documentation Changes

A number of signals were incorrectly described in the *Databook*. These are also highlighted in the change-tracked version of the *Reference Manual*. These are *not* RTL changes.

The following table enlists the I/O changes that have occurred for all configurations:

Table 5-3 Documentation Changes (Non-RTL)

Name	Type	Change	Comment
For many signals **Synchronous To** is corrected. These corrections are indicated in the change-tracked version of the Databook PDF which can be found at the location identified in the Databook revision history.			

5.3 Changes to Software View (Register Map)

This section discusses changes to the register map of the controller that have occurred in this release.

- It lists renamed registers.
- It lists deleted registers.
- It does *not* list new registers.
- *All* changes to the software map are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

The following changes have occurred for all configurations.

Table 5-4 Register Deletions/Renaming

Register	Field	Nature of Change
TYPE1_DEV_ID_VEND_ID_REG	RCRB_NEXT_OFFSET_PTR RCRB_VERSION	Removed
BAR0_REG	MEMBAR0	Removed
BAR1_REG	MEMBAR1	Removed
IATU_REGION_CTRL_2_VIEWPORT_OFF_INBOUND_i	LWR_BASE_RW LWR_BASE_HW	Removed
CXL_LL_CTRL_CR_REG_OFF	RSVDP_26 CXL_CRC_THRESHOLD CXL_LRSM_TIMEOUT_THRESHOLD	Removed
DEVICE_ID_VENDOR_ID_REG	PCI_TYPE0_RCRB_NEXT_OFFSET_PTR PCI_TYPE0_RCRB_VERSION PCI_TYPE0_VENDOR_ID	Removed

Documentation Changes

A number of registers were incorrectly described in the IP-XACT XML, DocBook XML, RAL files, header files, and *Register Descriptions* PDF. These are also highlighted in the change-tracked version of the *Reference Manual* PDF. These are *not* RTL changes.

Table 5-5 Documentation Changes (Non-RTL)

Register	Field	Nature of Change
DEVICE_ID_VENDOR_ID_REG	PCI_TYPE0_DEVICE_ID	**Memory Access** Corrected
CAP_REG	ARI_NEXT_FUN_NUM	**Value after reset** **Memory Access** **Testable** Corrected Fields are visible

Register	Field	Nature of Change
CXL_RCIEP_DVSEC_HDR_2_FLEXBUS_CAP_OFF	PM_INIT_CMPL_RPT_CAP CXL_LOGICAL_DEV CXL_RST_MEM_CLR_CAP CXL_RST_TIMEOUT CXL_RST_CAP CACHE_WB_INVALID_CAP	**Value after reset** **Memory Access** Corrected Fields are visible
	MEM_CAP CACHE_CAP	**Value after reset** Corrected
CXL_RCIEP_FLEXBUS_CNTRL_2_STATUS_2_OFF	PWR_INIT_CMPL CXL_RST_ERROR CXL_RST_CMPL CACHE_INVALID CXL_RST_MEM_CLR_EN INIT_CXL_RST INIT_CACHE_WR_INVALID DISABLE_CACHE	**Value after reset** **Memory Access** Corrected Fields are visible
CXL_RCIEP_FLEX_BUS_LOCK_OFF	CACHE_SIZE CACHE_SIZE_UNIT	**Value after reset** **Memory Access** Corrected Fields are visible
CXL_RCRB_PCIE_EXT_CAP_HDR_OFF	FLEX_BUS_PORT_NXT_OFFSET	**Value after reset** Corrected Fields are visible
	FLEX_BUS_PORT_CAP_VERSION FLEX_BUS_PORT_CAP_ID	Fields are visible
CXL_RCRB_DVSEC_PORT_HDR_1_OFF	CXL_RCRB_DVSEC_LEN CXL_RCRB_DVSEC_REV	**Value after reset** Corrected Fields are visible
	CXL_RCRB_DVSEC_VNDR_ID	Fields are visible
CXL_RCRB_DVSEC_HDR_2_FLEXBUS_CAP_OFF	CXL_MUL_LOG_DEV_CAP CXL2P0_CAP	**Value after reset** **Memory Access** Corrected Fields are visible
	MEM_CAP CACHE_CAP	**Value after reset** Corrected Fields are visible
	IO_CAP CXL_RCRB_DVSEC_ID	Fields are visible

Register	Field	Nature of Change
CXL_RCRB_FLEXBUS_CNTRL_STATUS_OFF	CXL_FB_EN_BITS_P2_MISMATCH CXL_RETIMER_PSNT_MISMATCH CXL_MLD_END CXL2P0_ENABLED DISABLE_CXL_L1P1_TRAINING CXL_MLD_EN CXL2P0_ENABLE DRIFT_BUF_EN CXL_SYNC_HDR_BYPASS_EN	**Value after reset** **Memory Access** Corrected Fields are visible
	DRIFT_BUF_END CXL_SYNC_HDR_BYPASS_END MEM_END IO_END CACHE_END IO_EN	Fields are visible
	CACHE_EN MEM_EN	**Value after reset** **Memory Access** **Testable** Corrected Fields are visible
	RETIMER_2_PRESENT RETIMER_1_PRESENT	**Memory Access** **Testable** Corrected Fields are visible
CXL_RCRB_FLEXBUS_RCVD_MOD_TS_PH1_OFF	RCVD_FB_DATA_PH_1	**Value after reset** **Memory Access** Corrected Fields are visible
CXL_2_0_EXT_DVSEC_CAP_HDR_OFF	CXL_2_0_EXT_NEXT_OFFSET CXL_2_0_EXT_CAP_VERSION CXL_2_0_EXT_CAP_ID	**Value after reset** **Memory Access** Corrected Fields are visible
CXL_2_0_EXT_DVSEC_HDR_1_OFF	CXL_2_0_EXT_DVSEC_LEN CXL_2_0_EXT_DVSEC_REV CXL_2_0_EXT_DVSEC_VNDR_ID	**Value after reset** **Memory Access** Corrected Fields are visible
CXL_2_0_EXT_DVSEC_HDR_2_OFF	CXL_2_0_PM_INIT_CMPL CXL_2_0_EXT_DVSEC_ID	**Value after reset** **Memory Access** Corrected Fields are visible

Register	Field	Nature of Change
CXL_2_0_CTRL_ALT_BUS_BASE_LIMIT_OFF	ALT_BUS_LIMIT ALT_BUS_BASE ALT_BME ALT_MEM_ID_SPACE_EN UNMASK_LINK_DISABLE UNMASK_SBR	**Value after reset** **Memory Access** Corrected Fields are visible
CXL_2_0_ALT_MEM_BASE_LIMIT_OFF	ALT_MEM_LIMIT ALT_MEM_BASE	**Value after reset** **Memory Access** Corrected Fields are visible
CXL_2_0_ALT_PREFETCH_MEM_BASE_LIMIT_OFF	ALT_PREF_MEM_LIMIT ALT_PREF_MEM_BASE	**Value after reset** **Memory Access** Corrected Fields are visible
CXL_2_0_ALT_PREFETCH_MEM_BASE_HIGH_OFF	ALT_PREF_MEM_BASE_HIGH	**Value after reset** **Memory Access** Corrected Fields are visible
CXL_2_0_ALT_PREFETCH_MEM_LIMIT_HIGH_OFF	ALT_PREF_MEM_LIMIT_HIGH	**Value after reset** **Memory Access** Corrected Fields are visible
CXL_2_0_CXL_RCRB_BASE_OFF	CXL_RCRB_BASE_ADDR_LOW CXL_RCRB_EN	**Value after reset** **Memory Access** Corrected Fields are visible
CXL_2_0_CXL_RCRB_BASE_HIGH_OFF	CXL_RCRB_BASE_ADDR_HIGH	**Value after reset** **Memory Access** Corrected Fields are visible
MEMBAR0_HEADER_CAP_REG_OFF	CXL_RCRB_MEMBAR0_CACHE_MEM_SIZE	**Value after reset** Corrected
MEMBAR0_RAS_CAP_REG_OFF	CXL_RCRB_MEMBAR0_RAS_CAP_VER	**Value after reset** Corrected
MEMBAR0_SECURITY_CAP_REG_OFF	CXL_RCRB_MEMBAR0_SEC_CAP_PTR CXL_RCRB_MEMBAR0_SEC_CAP_VER CXL_RCRB_MEMBAR0_SEC_CAP_ID	**Value after reset** Corrected Fields are visible
MEMBAR0_LINK_CAP_REG_OFF	CXL_RCRB_MEMBAR0_LINK_CAP_PTR CXL_RCRB_MEMBAR0_LINK_CAP_VER	**Value after reset** Corrected

Register	Field	Nature of Change
MEMBAR0_RAS_UNCOR_ERROR_STATUS_REG_OFF	CXL_RCRB_MEMBAR0_CXL_IDE_RX_ER CXL_RCRB_MEMBAR0_CXL_IDE_TX_ER CXL_RCRB_MEMBAR0_CXL_INTERNAL_ERR	**Value after reset** **Memory Access** Corrected Fields are visible
MEMBAR0_RAS_UNCOR_ERROR_MASK_REG_OFF	CXL_RCRB_MEMBAR0_CXL_IDE_RX_MASK CXL_RCRB_MEMBAR0_CXL_IDE_TX_MASK CXL_RCRB_MEMBAR0_CXL_INTERNAL_ER_MASK	**Value after reset** **Memory Access** Corrected Fields are visible
	CXL_RCRB_MEMBAR0_RCVR_OVERFLOW_MASK CXL_RCRB_MEMBAR0_POISON_RVD_MASK CXL_RCRB_MEMBAR0_ENCOD_VIOLATION_MASK CXL_RCRB_MEMBAR0_REINIT_THRESHOLD_MASK CXL_RCRB_MEMBAR0_MEM_DATA_ECC_MASK CXL_RCRB_MEMBAR0_MEM_BE_PAR_MASK CXL_RCRB_MEMBAR0_MEM_ADD_PAR_MASK CXL_RCRB_MEMBAR0_MEM_DATA_PAR_MASK CXL_RCRB_MEMBAR0_CACHE_DATA_ECC_MASK CXL_RCRB_MEMBAR0_CACHE_BE_PAR_MASK CXL_RCRB_MEMBAR0_CACHE_ADD_PAR_MASK CXL_RCRB_MEMBAR0_CACHE_DATA_PAR_MASK	**Value after reset** Corrected
MEMBAR0_RAS_UNCOR_ERROR_SEVERITY_REG_OFF	CXL_RCRB_MEMBAR0_CXL_IDE_RX_SEV CXL_RCRB_MEMBAR0_CXL_IDE_TX_SEV CXL_RCRB_MEMBAR0_CXL_INTERNAL_ER_SEV	**Value after reset** **Memory Access** Corrected Fields are visible
	CXL_RCRB_MEMBAR0_RCVR_OVERFLOW_SEV CXL_RCRB_MEMBAR0_POISON_RVD_SEV CXL_RCRB_MEMBAR0_ENCOD_VIOLATION_SEV CXL_RCRB_MEMBAR0_REINIT_THRESHOLD_SEV CXL_RCRB_MEMBAR0_MEM_DATA_ECC_SEV CXL_RCRB_MEMBAR0_MEM_BE_PAR_SEV CXL_RCRB_MEMBAR0_MEM_ADD_PAR_SEV CXL_RCRB_MEMBAR0_MEM_DATA_PAR_SEV CXL_RCRB_MEMBAR0_CACHE_DATA_ECC_SEV CXL_RCRB_MEMBAR0_CACHE_BE_PAR_SEV CXL_RCRB_MEMBAR0_CACHE_ADD_PAR_SEV CXL_RCRB_MEMBAR0_CACHE_DATA_PAR_SEV	**Value after reset** Corrected

Register	Field	Nature of Change
MEMBAR0_RAS_CORR_ERROR_MASK_REG_OFF	CXL_RCRB_MEMBAR0_PHY_LAYER_ERR_MASK CXL_RCRB_MEMBAR0_MEM_POISON_RVD_MASK CXL_RCRB_MEMBAR0_CACHE_POISON_RVD_MASK CXL_RCRB_MEMBAR0_CORR_RETRY_THRESHOLD_MASK CXL_RCRB_MEMBAR0_CORR_CRC_THRESHOLD_MASK CXL_RCRB_MEMBAR0_CORR_MEM_DATA_ECC_MASK CXL_RCRB_MEMBAR0_CORR_CACHE_DATA_ECC_MASK	**Value after reset** Corrected
MEMBAR0_RAS_ERR_CAP_CNTRL_REG_OFF	CXL_RCRB_MEMBAR0_POISON_END CXL_RCRB_MEMBAR0_ERR_PTR	**Value after reset** Corrected
MEMBAR0_LINK_LAYER_CAP_REG_OFF	CXL_RCRB_MEMBAR0_LNK_VER_SUPP	**Value after reset** Corrected
PCIE_CAP_ID	PCIE_CAP_FLR_CAP	**Value after reset** **Memory Access** Corrected Fields are visible
	PCIE_CAP_CAP_SLOT_PWR_LMT_SCALE PCIE_CAP_ROLE_BASED_ERR_REPORT	**Memory Access** Corrected Fields are visible
	PCIE_CAP_EP_L1_ACCPT_LATENCY PCIE_CAP_EP_L0S_ACCPT_LATENCY PCIE_CAP_EXT_TAG_SUPP PCIE_CAP_PHANTOM_FUNC_SUPPORT PCIE_CAP_MAX_PAYLOAD_SIZE	**Memory Access** Corrected

Register	Field	Nature of Change
MAX_4096B_SIZE	PCIE_CAP_EMERGENCY_PWR_RED_DETECTED PCIE_CAP_TRANS_PENDING PCIE_CAP_AUX_POWER_DETECTED PCIE_CAP_UNSUPPORTED_REQ_DETECTED PCIE_CAP_FATAL_ERR_DETECTED PCIE_CAP_NON_FATAL_ERR_DETECTED PCIE_CAP_CORR_ERR_DETECTED PCIE_CAP_INITIATE_FLR PCIE_CAP_MAX_READ_REQ_SIZE PCIE_CAP_EN_NO_SNOOP PCIE_CAP_AUX_POWER_PM_EN PCIE_CAP_PHANTOM_FUNC_EN PCIE_CAP_EXT_TAG_EN PCIE_CAP_MAX_PAYLOAD_SIZE_CS PCIE_CAP_EN_REL_ORDER PCIE_CAP_UNSUPPORT_REQ_REP_EN PCIE_CAP_FATAL_ERR_REPORT_EN PCIE_CAP_NON_FATAL_ERR_REPORT_EN PCIE_CAP_CORR_ERR_REPORT_EN	**Memory Access** Corrected
DEVICE_CAPABILITIES2_REG	PCIE_CAP_FRS_SUPPORTED PCIE_CAP_DMWR_LEN_SUPP PCIE_CAP_DMWR_CPL_SUPP PCIE_CAP2_CFG_MAX_END2END_TLP_PRFXS PCIE_CAP2_CFG_END2END_TLP_PRFX_SUPPORT PCIE_CAP2_CFG_EXTND_FMT_SUPPORT PCIE_CAP_OBFF_SUPPORT PCIE_CAP2_10_BIT_TAG_REQ_SUPPORT PCIE_CAP2_10_BIT_TAG_COMP_SUPPORT PCIE_CAP_TPH_CMPLT_SUPPORT_1 PCIE_CAP_TPH_CMPLT_SUPPORT_0 PCIE_CAP_LTR_SUPP PCIE_CAP_NO_RO_EN_PR2PR_PAR PCIE_CAP_128_CAS_CPL_SUPP PCIE_CAP_64_ATOMIC_CPL_SUPP PCIE_CAP_32_ATOMIC_CPL_SUPP PCIE_CAP_ATOMIC_ROUTING_SUPP PCIE_CAP_ARI_FORWARD_SUPPORT PCIE_CAP_CPL_TIMEOUT_DISABLE_SUPPORT PCIE_CAP_CPL_TIMEOUT_RANGE	**Memory Access** Corrected

Register	Field	Nature of Change
DEVICE_CONTROL2_DEVICE_STATUS2_REG	PCIE_CAP_OBFF_EN PCIE_CAP_10BITS_TAG_REQ_EN PCIE_CAP_EMERGENCY_PWR_RED_REQUEST PCIE_CAP_LTR_EN PCIE_CAP_IDO_CPL_EN PCIE_CAP_IDO_REQ_EN PCIE_CAP_ATOMIC_EGRESS_BLK PCIE_CAP_ATOMIC_REQ_EN PCIE_CAP_ARI_FORWARD_SUPPORT_CS PCIE_CAP_CPL_TIMEOUT_DISABLE PCIE_CAP_CPL_TIMEOUT_VALUE PCIE_CTRL2_CFG_END2END_TLP_PFX_BLCK	**Memory Access** Corrected
ACS_CAP_HDR_REG	NEXT_OFFSET CAP_VERSION CAP_ID	**Memory Access** Corrected
ACS_CAPABILITIES_CTRL_REG	ACS_DIRECT_TRANSLATED_P2P_EN ACS_P2P_EGRESS_CONTROL_EN ACS_USP_FORWARDING_EN ACS_P2P_CPL_REDIRECT_EN ACS_P2P_REQ_REDIRECT_EN ACS_AT_BLOCK_EN ACS_SRC_VALID_EN ACS_EGRESS_CTRL_SIZE ACS_DIRECT_TRANSLATED_P2P ACS_P2P_EGRESS_CONTROL ACS_USP_FORWARDING ACS_P2P_CPL_REDIRECT ACS_P2P_REQ_REDIRECT ACS_AT_BLOCK ACS_SRC_VALID	**Memory Access** Corrected
ACS_EGRESS_CTRL_VECTOR_REG0	ACS_EGRESS_CTRL_VECTOR_REG0 ACS_EGRESS_CTRL_VECTOR_REG1	**Memory Access** Corrected
ACS_EGRESS_CTRL_VECTOR_REG2	ACS_EGRESS_CTRL_VECTOR_REG2	**Memory Access** Corrected
ACS_EGRESS_CTRL_VECTOR_REG3	ACS_EGRESS_CTRL_VECTOR_REG3	**Memory Access** Corrected
ACS_EGRESS_CTRL_VECTOR_REG4	ACS_EGRESS_CTRL_VECTOR_REG4	**Memory Access** Corrected
ACS_EGRESS_CTRL_VECTOR_REG5	ACS_EGRESS_CTRL_VECTOR_REG5	**Memory Access** Corrected
ACS_EGRESS_CTRL_VECTOR_REG6	ACS_EGRESS_CTRL_VECTOR_REG6	**Memory Access** Corrected

Register	Field	Nature of Change
ACS_EGRESS_CTRL_VECTOR_REG7	ACS_EGRESS_CTRL_VECTOR_REG7	**Memory Access** Corrected
VF_DEVICE_ID_VENDOR_ID_REG	PCI_TYPE0_DEVICE_ID	**Memory Access** Corrected
VF_LINK_CAPABILITIES_REG	PCIE_CAP_ASPM_OPT_COMPLIANCE	**Testable** Corrected Fields are visible
MISC_CONTROL_1_OFF	RASDES_REG_PF0_ONLY	**Memory Access** Corrected Fields are visible
	RAS_REG_PF0_ONLY	**Value after reset** **Memory Access** Corrected Fields are visible
PHY_INTEROP_CTRL_OFF	PHY_PERST_ON_WARM_RESET	**Value after reset** **Memory Access** **Testable** Corrected Fields are visible
DMA_VIEWPORT_SEL_OFF	PMA_PIPE_RST_DELAY_TIMER	**Value after reset** Corrected
CXL_LL_CTRL_CR_REG_OFF	CXL_AP_PROT_ENA CXL_AP_PROT_TYPE	**Memory Access** Corrected
CXL_FATAL_ERR_CR_REG_OFF	CXL_MDH_ERR CXL_MEM_DATA_VD_ERR CXL_CACHE_DATA_VD_ERR CXL_H2D_ORD_VIOLATION CXL_AP_VIRAL_REQ CXL_CXS_TX_END_ERR CXL_ULL_CXS_END_ERR CXL_LL_RX_FLOW_CTRL_ERR CXL_RETRY_CRC_ERR CXL_RETRY_ESEQ_OVERFLOW CXL_LL_MULTI_INIT_PARAM CXL_LL_INIT_PARAM_ERR CXL_LL_TC_FLOW_CTRL_ERR CXL_LRSM_ACK_ERROR CXL_LRSM_ABORT CXL_LL_STATIC_BIT_ERR CXL_RAS_ERROR CXL_FATAL_ERR_RETRY_ACK_VIRAL	**Memory Access** Corrected

Register	Field	Nature of Change
CXL_PORT_LOGIC_VIRAL_STS_OFF	CXL_PL_VIRAL_LDID_STS CXL_PL_VIRAL_STATUS	**Value after reset** **Memory Access** **Testable** Corrected Fields are visible
ECAM_BASE_ADDR_LWR_OFF	ECAM_BASE_ADDR_LWR	**Value after reset** **Memory Access** Corrected Fields are visible
ECAM_BASE_ADDR_UPPER_OFF	ECAM_BASE_ADDR_UPPER	**Value after reset** **Memory Access** Corrected Fields are visible
ECAM_CTRL_OFF	ECAM_CTRL_TYPE1_TO_TYPE0_DISABLE ECAM_CTRL_DSP_ECAM_EN	**Value after reset** **Memory Access** Corrected Fields are visible
CXL_TEST_DVSEC_CAPABILITY_OFF	CXL_DEVICE_TEST_CONFIG_SIZE CXL_DEVICE_TEST_COMP_TIMEOUT_INJECT CXL_DEVICE_TEST_UNEXPECTED_COMP CXL_DEVICE_TEST_CACHE_FLUSHED CXL_DEVICE_TEST_WR_INV CXL_DEVICE_TEST_WO_WR_INV_F CXL_DEVICE_TEST_WO_WR_INV CXL_DEVICE_TEST_CLEAN_EVC_NO_DATA CXL_DEVICE_TEST_DIRTY_EVICT CXL_DEVICE_TEST_CLEAN_EVICT CXL_DEVICE_TEST_CL_FLUSH CXL_DEVICE_TEST_MEM_WR CXL_DEVICE_TEST_ITOM_WR CXL_DEVICE_TEST_RD_OWN_NO_DATA CXL_DEVICE_TEST_RD_ANY CXL_DEVICE_TEST_RD_SHARED CXL_DEVICE_TEST_RD_OWN CXL_DEVICE_TEST_RD_CURR CXL_DEVICE_TEST_ALGO_2 CXL_DEVICE_TEST_ALGO_1B CXL_DEVICE_TEST_ALGO_1A CXL_DEVICE_TEST_SELF_CHECK	**Value after reset** Corrected

Register	Field	Nature of Change
ACS_CAP_HDR_REG	NEXT_OFFSET CAP_VERSION CAP_ID	Fields are visible
ACS_CAPABILITIES_CTRL_REG	ACS_DIRECT_TRANSLATED_P2P_EN ACS_P2P_EGRESS_CONTROL_EN ACS_USP_FORWARDING_EN ACS_P2P_CPL_REDIRECT_EN ACS_P2P_REQ_REDIRECT_EN ACS_AT_BLOCK_EN ACS_SRC_VALID_EN ACS_EGRESS_CTRL_SIZE ACS_DIRECT_TRANSLATED_P2P ACS_P2P_EGRESS_CONTROL ACS_USP_FORWARDING ACS_P2P_CPL_REDIRECT ACS_P2P_REQ_REDIRECT ACS_AT_BLOCK ACS_SRC_VALID	Fields are visible
ACS_EGRESS_CTRL_VECTOR_REG0	ACS_EGRESS_CTRL_VECTOR_REG0	Fields are visible
ACS_EGRESS_CTRL_VECTOR_REG1	ACS_EGRESS_CTRL_VECTOR_REG1	Fields are visible
ACS_EGRESS_CTRL_VECTOR_REG2	ACS_EGRESS_CTRL_VECTOR_REG2	Fields are visible
ACS_EGRESS_CTRL_VECTOR_REG3	ACS_EGRESS_CTRL_VECTOR_REG3	Fields are visible
ACS_EGRESS_CTRL_VECTOR_REG4	ACS_EGRESS_CTRL_VECTOR_REG4	Fields are visible
ACS_EGRESS_CTRL_VECTOR_REG5	ACS_EGRESS_CTRL_VECTOR_REG5	Fields are visible
ACS_EGRESS_CTRL_VECTOR_REG6	ACS_EGRESS_CTRL_VECTOR_REG6	Fields are visible
ACS_EGRESS_CTRL_VECTOR_REG7	ACS_EGRESS_CTRL_VECTOR_REG7	Fields are visible

5.4 Changes to RAM Sizes

This section details the changes to the default RAM sizes that have occurred since the last production release. It does not detail changes that are associated with new or additional features that you enable on your current configuration

Caution To determine the precise changes to RAM sizes for your actual controller configuration, you can compare the coreConsultant generated RAM sizes for the previous and current releases. For more details, see the “RAM Requirements” section in the Architecture chapter of the *Databook*.

The following changes have occurred for this release.

RAM Name	Change
Native CXL Interface RAMs	The CXL controller is updated to calculate the exact RAM sizes based on the CXL controller configuration.

5.5 Changes to Configuration Parameters

This section details any changes to the configuration parameters of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the configuration parameters are indicated in the change-tracked version of the *Reference Manual* PDF which can be found at the location identified in the *Reference Manual* revision history.

If you intend to source an existing configuration batch file, then you must first convert your configuration file, as described in "Product Updates" on page 180. If you are not sourcing an existing configuration batch file, then you should be still aware of changes to the default value of some configuration parameters.

Caution

To ensure that your existing configuration absorbs all changes to default parameters updated for this release, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

The *Write default Parameter* should only be used for debugging.

Table 5-6 Configuration Parameter Changes

Name	Change
CX_CXL_MEM_REQ_DP CX_CXL_MEM_RSP_DP	These parameters are invisible in coreConsultant now. A new parameter (CX_CXL_MEM_NDR_DP) sets these parameters now.
CX_CXL_CHI_MAXCREDITS CX_CXL_CHI_DATACHK	**Enabled** value changed **from**: CX_CXL_CHI_ENABLE **to**: CX_CXL_ENABLE && CX_CXL_CHI_ENABLE
CC_ACELITE_ENABLE	**Enabled**: value changed **from**: AMBA_INTERFACE==3 **to**: AMBA_INTERFACE>=3
CX_PIPERX_MULTI_BLOCK	**Default Value**: changed **from**: ((SNPS_RSVDPARAM_67==1) || (CX_PIPE_SERDES_ARCH && CX_MAX_PCIE_SPEED>=3 && (CX_PHY_SMODE_GEN3>=8 || CX_PHY_SMODE_GEN4>=8 || CX_PHY_SMODE_GEN5>=8)))? 1 : 0 **to**: (SNPS_RSVDPARAM_67==1) || (CX_PIPE_SERDES_ARCH && CX_MAX_PCIE_SPEED>=3 && (CX_PHY_NB_GEN3>=8 || CX_PHY_NB_GEN4>=8 || CX_PHY_NB_GEN5>=8)))? 1 : 0
CX_PIPE_PCLK_MODE	**Enabled**: changed **from**: CX_PIPE_VER>=3 || SNPS_RSVDPARAM_14==1 **to**: CX_PIPE_VER>=2

Name	Change
CX_10BITS_TAG	**Default Value**: changed **from**: (((CX_GEN4_SPEED_VALUE == 1) || (CX_MAX_TAG > 255) || (CX_REMOTE_MAX_TAG > 255)) && (AMBA_INTERFACE != 1) && (CC_DTIM_ENABLE != 1))? 1: 0 **to**: (((CX_GEN4_SPEED_VALUE == 1) || (CX_MAX_TAG > 255) || (CX_REMOTE_MAX_TAG > 255)) && (AMBA_INTERFACE != 1))? 1: 0
DBI_MULTI_FUNC_BAR_EN	**Default Value**: changed **from**: MSIX_TABLE_EN || (CX_CXL_ENABLE && ((CC_DEVICE_TYPE==CC_EP) || (CC_DEVICE_TYPE==CC_DM))) **to**: MSIX_TABLE_EN || CX_CXL_ENABLE
PL_LIMIT	**Default Value**: changed **from**: 3104 **to**: 3172 Values: changed **from**: 2304,..., 3104 **to**: 2304, ..., 3172
RADM_NPQ_DSCALE_VC0 RADM_NPQ_DSCALE_VCn	**Default Value**: changed **from**: (CX_NP_DSCALE == 16) ? 3 : (CX_NP_DSCALE == 4) ? 2 : 1 **to**: 1
CX_DISABLE_ECC_XTLH_MERGE	**Enabled**: changed **from**: Always **to**: CX_RASDP != 0 && ARC_WIDTH > 64
CX_MEMBAR0_VIEW	**Default Value** changed **from**: Always **to**: CX_CXL_ENABLE
DPC_RPPIO_HDR_RAM_DATA_WDTH DPC_RPPIO_RAM_ADDR_WDTH DPC_RPPIO_PRFX_RAM_DATA_WDTH CX_CXL_RAM_READ_LATENCY DEFAULT_CXL_IO_ENABLE	These parameters are invisible in coreConsultant now.
CX_DEF_MEM_WR_REQ_EN CX_PIPE_OPTIONAL_PCLKCHANGE_HS	Location of these parameters in the coreConsultant has changed.
USE_1PSRAM_MODEL	Parameter removed
CX_CXL_RANGE_1_DESIRED_INTERLEAVE	Additional options available **Enabled** changed **from**: CX_CXL_MEM_EN **to**: (CX_CXL_MEM_EN && (CX_IS_EP || CX_IS_DM))

Name	Change
CX_CXL_DEVICE_CTS_EN	**Default Value** changed **from**: CX_CXL_ENABLE **to**: 0 **Enabled** changed **from**: CX_CXL_ENABLE **to**: (CX_CXL_ENABLE && (CX_IS_EP || CX_IS_DM))
CX_CXL_CACHE_SIZE CX_CXL_CACHE_SIZE_UNITS	**Enabled** changed **from**: CX_CXL_DEVICE_CTS_EN **to**: (CX_CXL_DEVICE_CTS_EN && (CX_IS_EP || CX_IS_DM))
CX_CXL_MEM_HWINIT_MODE CX_CXL_HDM_COUNT	**Enabled** changed **from**: CX_CXL_MEM_EN **to**: (CX_CXL_MEM_EN && (CX_IS_EP || CX_IS_DM))
CX_CXL_RANGE_1_MEM_SIZE_HIGH CX_CXL_RANGE_1_MEM_INFO_VALID CX_CXL_RANGE_1_MEM_ACTIVE CX_CXL_RANGE_1_MEDIA_TYPE CX_CXL_RANGE_1_MEM_CLASS CX_CXL_RANGE_1_MEM_SIZE_LOW	**Enabled** changed **from**: CX_CXL_MEM_EN **to**: (CX_CXL_MEM_EN && (CX_IS_EP || CX_IS_DM))
CX_CXL_RANGE_2_MEDIA_TYPE	Additional options available **Default Value** changed **from**: Volatile Memory **to**: CX_CXL_2_0_ENABLE ? 2 : 0 **Enabled** changed **from**: CX_CXL_MEM_EN && (CX_CXL_HDM_COUNT == 2)) **to**: CX_CXL_MEM_EN && !CX_CXL_2_0_ENABLE && (CX_CXL_HDM_COUNT == 2))
CX_CXL_RANGE_2_MEM_CLASS	Additional options available **Default Value** changed **from**: Memory Class **to**: CX_CXL_2_0_ENABLE ? 2 : 0 **Enabled** changed **from**: CX_CXL_MEM_EN && (CX_CXL_HDM_COUNT == 2)) **to**: CX_CXL_MEM_EN && !CX_CXL_2_0_ENABLE && (CX_CXL_HDM_COUNT == 2))
CX_CXL_RANGE_2_DESIRED_INTERLEAVE	Additional options available

5.6 Converting to the Current Release

Sometimes a new controller release might no longer use a certain configuration parameter, or the meaning of that parameter might have changed. The following process helps you convert your current configuration file so that it creates the same RTL with the new controller.

1. Open coreConsultant and create an unconfigured workspace from the newly installed controller.
2. In the coreConsultant command line, enter the following command:

   ```
   parse_configfile my_configfile.config
   ```

   where `my_configfile.config` is your current configuration file. This command creates an updated configuration file in your working directory as follows:

   ```
   my_configfile.config.new
   ```
3. In the coreConsultant command line, enter the following command:

   ```
   source my_configfile.config.new
   ```
4. Select Apply to generate the new RTL with the updated or translated parameters.
5. From the File Menu, select Write Batch Script and save the configuration file for the new release.
6. When you source the updated configuration file in coreConsultant, you can *ignore any new warnings* about parameter settings that are not relevant to, or not enabled in your configuration.

Attention

Writing Out Your Configuration File

To ensure that your existing configuration absorbs all changes to default parameters updated for this release, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

You must convert your configuration file. Failure to do so, can result in:

- Your configuration file being incompatible with the current release.
- Functional, architectural, RAM, and I/O changes when the default of some configuration parameters change from release to release.

5.7 Known Issues and Limitations

You can view a complete list of functional problem reports for this product, including problems identified after product release, by accessing the STAR report on the Web. For more details, see "Details of Fixed Defects and Enhancements" on page 204. You must have a SolvNet ID to view STAR reports. This release has the following known tool and packaging issues at the time of release.

- "Packaged coreConsultant Test Limitations"
- "VTB Limitations"
- "Design Example"
- "Unique Case Violation Simulation Message"
- "coreConsultant Memory Map Limitations"

5.7.1 Packaged coreConsultant Test Limitations

We invite you to submit your coreConsultant configuration for review. Because of the very large configuration space, it is not possible to regress every configuration before a release is made. Synopsys is continually running fixed and randomized configurations, but it is possible that your exact configuration has not been regressed. Test case failures might occur because of improper testbench configuration. In that case open a case through SolvNetPlus.

5.7.1.1 Known Test Failures

The following are known testbench issues:

- The AXI5 configuration cannot use the ARM AXI4 assertions.
- LD-ID feature is partially verified.
- DL Layer recovery and link is partially verified.
- The CXL RAS feature is not verified.
- LL_Reset functionality for CXL Link Layer Control and Status Register is not verified.
- ALMP Status Resolution Table is not fully verified.
- Hiding recovery scenarios of ARB/MUX are partially verified.
- Alternate Memory Ranges are not verified.
- The AXI configuration `pl_skew_dw_vdut_cpcie_phy_skew_only_vtb` test might fail with the error:

  ```
  Timed out waiting for bvalid
  ```

- The `pm_basic_l2` test might fail on AXI configurations with L2 power gating due to test issue in the AXI power isolation.
- The `tl_esm` test might fail on CCIX configurations with the error:

  ```
  Unexpected Message Bus command
  ```

- The `VTB RAL` tests might fail for PF>0 on configurations with resizable BARs – RAL model error.
- The `tl_ptm_scaled_clk` test might fail with the error:

  ```
  test scenario diverges from optimal scaled clock values when re-iterating the
  calibration leading to increased clock correction values
  ```

- The `pl_cdm_access_while_speed_change` test might fail on configurations with CXS interface.
- The `pm_direct_up_vdut_cpcie_l1_pcipm_msg_req_exit_turnoff` tests might fail in configurations that support `max_pclk` with the error:

  ```
  Timeout waiting for a smlh_ltssm_state change on clock aux_clk
  ```
- The `pm_l1_transitions_dw_vdut_cpcie_l1_link_entr_l1_idle` test might fail with error:

  ```
  vm_test_top [] Transition from S_LINK_ENT_L -> S_IDLE was not reached
  ```

  The test fails when `pclk` and `aux_clk` frequencies are almost the same.
- The `pm_l1_transitions_up_vdut_cpcie_l1_wakeup_mpf_ob_pwrup_cmd` test might fail for configurations with 16 lanes due to a testbench call back error:

  ```
  Timeout waiting for PM_PME message(s) to be received. Expected count, received count
  ```
- The `pm_l2_transitions` tests might fail due to monitor reset error with the error:

  ```
  monitorSubPhaseThread - Monitored Header is larger than dwords
  ```
- The `tl_mem_access_native_rbuff` test might fail due to known error in the VIP.
- The `pl_disable` test might fail on the CXL configurations with the error:

  ```
  ASSERT_RDPTR_INCREMENT_WITH_WRPTR_REPLAY: ERROR: RdPtr is matching WrPtr during replay!
  ```

5.7.2 VTB Limitations

The following limitations apply to the current release of the VTB:

- Not backward compatible with previous releases
- Not UVM compliant
- No support for big-endian (`AHB_ENDIANNESS`) configurations

5.7.3 Design Example

The design example in `<workspace>/examples/DWC_pcie_clkrst.v` has been functionally verified, but has not been explicitly targeted for verification metrics. However, it has been used by Synopsys in the verification and regression environments for all controller configurations; including verification of all power transitions for the controller.

5.7.4 Unique Case Violation Simulation Message

The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

There is a known simulator issue with a “Unique case violation” message that occurs sometimes while running simulations with VCS outside of coreConsultant. You can ignore these messages.

To avoid these messages, use the `-xlrm uniq_prior_final` compile option in VCS. The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

5.7.5 coreConsultant Memory Map Limitations

The controller supports the generation of configuration-specific register maps as described in the "Register Configuration Space" chapter in the *Databook*. For SR-IOV configurations (`CX_SRIOV_ENABLE =1`), the following limitations apply.

Table 5-7 coreConsultant Report File Limitations for SR-IOV Configurations

CX_NVFUNC	IP-XACT (IP-XACT XML)	RALF and C Headers (No limitations)	Register Report (DocBook XML) Also applies to Databook
1–256	Defines default #VFs in each PF	Defines default #VFs in each PF	Defines only first VF in each PF
257–4096	Defines only[a] first VF in each PF	Defines default #VFs in each PF	Defines only first VF in each PF

a. For details on how to populate remaining VFs in the IP-XACT file, see "Populating IP-XACT File Manually" in the "Creating Optional Views and Reports" section in the "Configuring the controller" chapter of the User Guide.

5.7.6 VC Spyglass Limitations

VC Spyglass support is used for demonstration only while Spyglass continues to be the used for Linting, CDC and RDC signoff. Expect the following limitation:

- `SET_SDC_*`, `SETUP_CLOCK_*` and `CDC_GLITCH_DATAPATH` are expected to fail but they do not compromise the design

5.7.7 Third-party Simulator Limitations

When you are using the QuestaSim 2019.4 simulator, and if you select the HDMA option, compilation failure can occur because the QuestaSim 2019.4 does not support System Verilog IEEE 2012 standard.

5.8 Details of Fixed Defects and Enhancements

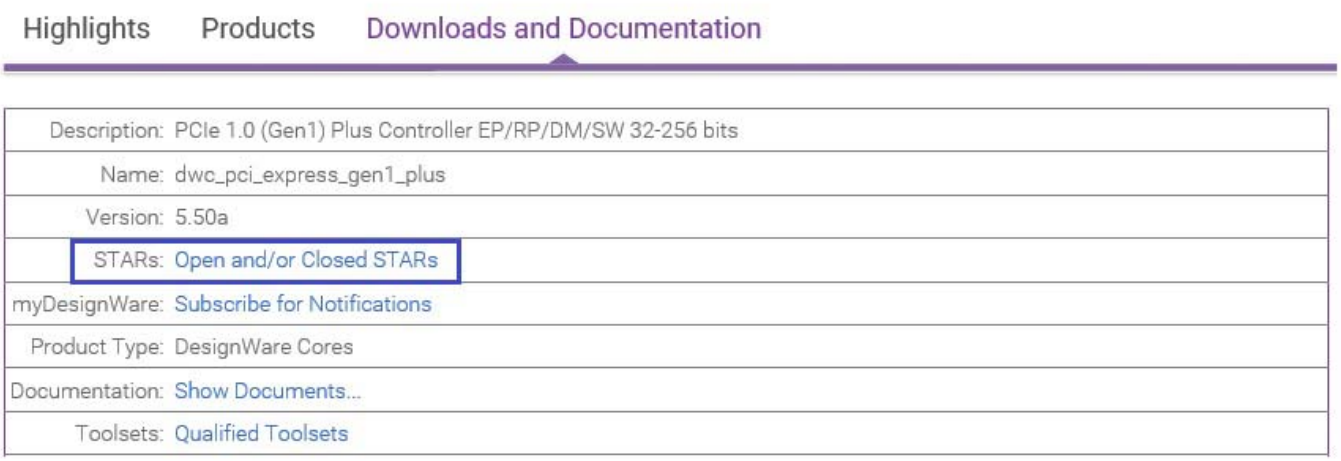
Defects fixed in release 5.90a of the controller are listed in the STAR report for release 5.90a in STARs on the Web.

Table 5-8 Controller STAR Report Location

Controller	Location
PCIe Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_controllers
CXL Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_cxl_controller
CCIX Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_ccix_controller

(A SolvNetPlus ID is required to view STAR reports.)

Figure 5-1 Accessing STARs on the Web through SolvNetPlus



Enhancement STARs are identifiable by the letter “E” in the Severity column, and fixed defect STARs are identifiable by the letter “B.” An E4 or B4 has the highest severity. Clicking on the tab corresponding to 5.90a produces a STAR report of closed STARS for this release. For previous controller versions, click the tab corresponding to the version in question.

5.9 Customer Support

Synopsys provides various methods for contacting Customer Support, as follows:

- Prepare the following debug information, if applicable:
  - For environment set-up problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, select the following menu:
    - **File > Build Debug Tar-file**

    Check all the boxes in the dialog box that apply to your issue. This option gathers all the Synopsys product data needed to begin debugging an issue and writes it to the <*core tool startup directory*>/debug.tar.gz file.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD).
    - Identify the hierarchy path to the DesignWare instance.
    - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- *For the fastest response*, enter a case through SolvNetPlus:

  a. https://solvnetplus.synopsys.com

Note SolvNetPlus does not support Internet Explorer. Use a supported browser such as Microsoft Edge, Google Chrome, Mozilla Firefox, or Apple Safari.

  b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).

  c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

     Make sure to include the following:
     - **Product L1:** DesignWare Cores
     - **Product L2:** PCI Express

  d. After creating the case, attach any debug files you created.

     For more information about general usage information, refer to the following article in SolvNetPlus:

     https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
  - Attach any debug files you created.
- Or, telephone your local support center:
  - North America:

    Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.

- All other countries:
  https://www.synopsys.com/support/global-support-centers.html

6

Release Notes: 5.80a

These release notes describe the changes in this release *(5.80a)* relative to the previous production release *(5.71a)*. This release note contains the following sections:

- "Product Updates" on page 208
- "Changes to I/O" on page 210
- "Changes to Software View (Register Map)" on page 211
- "Changes to RAM Sizes" on page 213
- "Changes to Configuration Parameters" on page 214
- "Converting to the Current Release" on page 217
- "Known Issues and Limitations" on page 218
- "Details of Fixed Defects and Enhancements" on page 220
- "Customer Support" on page 221

6.1 Product Updates

This release contains the following major updates and other minor updates (indicated in "Details of Fixed Defects and Enhancements" on page 220).

6.1.1 Complute Express Link (CXL) Controller

The CXL controller provides a solution for the implementation of CXL Host and/or Device, which supports CXL.io, CXL.cache, and CXL.mem protocols. The CXL controller supports all the required features of the *Compute Express Link Specification Revision 1.1*, as well as *PCI Express 5.0, 4.0, and 3.1 Specifications*. The CXL controller is compliant with CXS Issue B Interface to support the CXL protocol over 512b CXS flits.

For more information on CXL controller, see *"Compute Express Link (CXL)" Databook*.

Note The CXL controller is available as an LCA (Limited Customer Availability) release.

6.1.2 Enhanced Downstream Port Containment (eDPC)

The controller supports RP PIO error controls as described in *PCI Express Base Specification, Revision 5.0, Version 1.0*. RP PIO error control mechanism includes fine-grained controls for managing Programmed I/O (PIO) errors, and Completion synthesis to avoid Completion Timeouts for outstanding Non-Posted Requests. You can enable eDPC by setting the parameter `CX_DPC_RP_PIO_EXTNS` to '1'.

For more information, see the *"DPC"* section in the *"Controller Operations"* chapter of the *Databook*.

6.1.3 Deferrable Memory Write (DMWr)

The controller supports Deferrable Memory Write and Device 3 Extended Capability as described in *Deferrable Memory Write (DMWr) and Device 3 Extended Capability ECN*. You can enable Deferrable Memory Write (DMWr) by setting the parameter `CX_DEF_MEM_WR_ENABLE` to '1'.

For more information, see the *"Deferrable Memory Write (DMWr)"* section in the *"Controller Operations"* chapter of the *Databook*.

6.1.4 Emergency Power Reduction

The controller supports Emergency Power Reduction mechanism as described in *PCI Express Base Specification, Revision 5.0, Version 1.0*. You can enable this optional mechanism by setting the parameter `EMERGENCY_POWER_REDUCTION_ENABLE` to '1'.

For more information, see *"Emergency Power Reduction"* topic in the *"Power Management"* section in the *"Controller Operations"* chapter of the *Databook*.

6.1.5 Equalization Redo Updates

The USP controller is enhanced to generate equalization (EQ) redo interrupt and perform a finite number of equalization redo requests.

The USP performs the maximum number of EQ redo requests set in the `GEN3_EQ_REQ_NUM` field of the `GEN3_EQ_CONTROL_OFF` register, when the `GEN3_SUPPORT_FINITE_EQ_REQUEST` field of the `GEN3_EQ_CONTROL_OFF` register is set to '1'. The USP stops the EQ redo requests for the current data rate to

avoid the endless EQ redo requests from the USP when the EQ redo requests are equal or above the number set in the `GEN3_EQ_REQ_NUM` field.

For more information, see *"Equalization Overview and Synopsys-Specific Features"* section in the *"Advanced Information: Gen3/4/5 Equalization Details and Example"* appendix of the *Databook*.

6.2 Changes to I/O

This section details any changes to the I/O of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the I/O are indicated in the change-tracked version of the *Databook* PDF which can be found at the location identified in the *Databook* revision history.

The following I/O changes have occurred for all configurations:

Table 6-1 I/O Signals Added, Removed, or Renamed

Name	Type	Change	Comment
No changes in this release.			

Documentation Changes

A number of signals were incorrectly described in the *Databook*. These are also highlighted in the change-tracked version of the *Databook*. These are *not* RTL changes.

The following I/O changes have occurred for all configurations:

Table 6-2 Documentation Changes (Non-RTL)

Name	Type	Change	Comment
For many signals **Synchronous To** is corrected. These corrections are indicated in the change-tracked version of the Databook PDF which can be found at the location identified in the Databook revision history.			

6.3 Changes to Software View (Register Map)

This section discusses changes to the register map of the controller that have occurred in this release.

- It lists renamed registers.
- It lists deleted registers.
- It does *not* list new registers.
- *All* changes to the software map are indicated in the change-tracked version of the *Register Descriptions* PDF which can be found at the location identified in the *Register Descriptions* revision history.

The following changes have occurred for all configurations.

Table 6-3 Register Deletions/Renaming

Register	Field	Nature of Change
No changes in this release.		

Documentation Changes

A number of registers were incorrectly described in the IP-XACT XML, DocBook XML, RAL files, header files, and *Databook*. These are also highlighted in the change-tracked version of the *Register Descriptions* PDF. These are *not* RTL changes.

Table 6-4 Documentation Changes (Non-RTL)

Register	Field	Nature of Change
STATUS_COMMAND_REG	PCI_TYPE0_BUS_MASTER_EN	**Memory Access** Corrected
CLASS_CODE_REVISION_ID	BASE_CLASS_CODE SUBCLASS_CODE PROGRAM_INTERFACE	**Memory Access** Corrected
BIST_HEADER_TYPE_LATENCY_CACHE_LINE_SIZE_REG	MULTI_FUNC	**Memory Access** Corrected
PL32G_CAPABILITY_REG	MOD_TS_ALT_PROTOCOL_SUPPORT	**Memory Access** **Value after reset** **Testable** Corrected Fields are visible
PL32G_CONTROL_REG	MOD_TS_USAGE_MODE_SELECT	**Testable** Corrected
PL32G_RCVD_MOD_TS_DATA2_REG	RCVD_ALT_PROTOCOL_NEGO_STATUS	**Testable** Corrected
PL32G_TX_MOD_TS_DATA2_REG	TX_ALT_PROTOCOL_NEGO_STATUS	**Testable** Corrected

Register	Field	Nature of Change
PL32G_CAP_OFF_iH_REG	USP_32G_TX_PRESET[15-0] DSP_32G_TX_PRESET[15-0]	**Value after reset** Corrected Fields are visible
PL32G_CAP_OFF_2CH_REG	[USP|DSP]_32G_TX_PRESET[12-15]	**Value after reset** Corrected Fields are Visible
RASDP_[CORR|UNCORR]_ERROR_LOCATION_OFF	REG_[FIRST|LAST]_CORR_ERROR	**Value after reset** Corrected
VF_RESBAR_CTRL_REG_[0-5]_REG	VF_RESBAR_CTRL_REG_NUM_BARS	**Value after reset** Corrected
PCI_MSI_CAP_ID_NEXT_CTRL_REG	PCI_MSI_MULTIPLE_MSG_CAP	**Value after reset** Corrected Fields are visible

6.4 Changes to RAM Sizes

This section details the changes to the default RAM sizes that have occurred since the last production release. It does not detail changes that are associated with new or additional features that you enable on your current configuration

Caution To determine the precise changes to RAM sizes for your actual controller configuration, you can compare the coreConsultant generated RAM sizes for the previous and current releases. For more details, see the “RAM Requirements” section in the Architecture chapter of the *Databook*.

The following changes have occurred for this release.

RAM Name	Change
AXI Master Completion Asynchronous Clock Crossing FIFO RAM	The width of some of the RAM signals has changed. Therefore, there is a change in the total width of the RAMs. **Note:** The RAM changes apply to legacy DMA only
AXI Slave Non-Posted TLP Decomposer Header/Data FIFO RAM	
AXI Slave Non-Posted Write Set-Aside Buffer RAM	
AXI Slave Posted TLP Decomposer Header FIFO RAM	

6.5 Changes to Configuration Parameters

This section details any changes to the configuration parameters of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the configuration parameters are indicated in the change-tracked version of the *Databook* PDF which can be found at the location identified in the *Databook* revision history.

If you intend to source an existing configuration batch file, then you must first convert your configuration file, as described in "Product Updates" on page 208. If you are not sourcing an existing configuration batch file, then you should be still aware of changes to the default value of some configuration parameters.

Caution To ensure that your existing configuration absorbs all changes to default parameters that the PCIe R&D team makes, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

Table 6-5 Configuration Parameter Changes

Name	Change
PL_LIMIT	**Values:** changed **from:** 2304,...,3104 **to:**2304,..... 3168 **Default Value:** changed **from:** 3104 **to:** 3168
Phy Selection	**Enabled:** changed **from:** (!(CX_PCIE_MODE == SINGLE_MPCIE)) **to:** Always
Maximum Link Width	**Default:** changed **from:** (CX_PCIE_MODE == PCIE_OVER_CIO) ? 16 :(CX_S_CPCIE_MODE) ? 4 : (CM_TXNL_GUI > CM_RXNL_GUI) ? CM_TXNL_GUI : CM_RXNL_GUI **to:** (CX_PCIE_MODE == PCIE_OVER_CIO) ? 16 : 4
Deskew Fifo Depth for C-PCIe	**Enabled:** changed **from:** (!(CX_PCIE_MODE == SINGLE_MPCIE)) **to:** Always
CX_WIRE_SKEW_GEN2_NS	**Default:** changed **from:** ((CX_SEL_PHY_MODE ? (CX_MAX_CPCIE_SPEED >= 2) :CX_S_CPCIE_MODE ? (CX_GEN2_MODE != GEN2_DISABLED) : 0)==1) ? 8 : 0 **to:**((CX_GEN2_MODE != GEN2_DISABLED)==1) ? 8 : 0

Name	Change
CX_WIRE_SKEW_GEN3_NS	**Default:** changed **from:** ((CX_SEL_PHY_MODE ? (CX_MAX_CPCIE_SPEED >= 3) :CX_S_CPCIE_MODE ? (CX_GEN3_MODE != GEN3_DISABLED) : 0)==1) ? 6 : 0 **to:** ((CX_GEN3_MODE != GEN3_DISABLED)==1) ? 6 : 0
DEFAULT_REPLAY_ADJ	**Enabled:** changed **from:** ((CX_S_CPCIE_MODE || CX_SEL_PHY_MODE)) **to:** CX_S_CPCIE_MODE
DEFAULT_GEN2_SPEED_CHANGE	**Enabled:** changed **from:** ((CX_S_MPCIE_MODE) ? 0 : CX_GEN2_SPEED) **to:** CX_GEN2_MODE !=GEN2_DISABLED
CX_ENHANCED_PM_EN	**Enabled:** changed **from:** ((CX_CPCIE_ENABLE || SNPS_RSVDPARAM_10 ||!CM_SNPS_MPHY_ENABLE) && !(AMBA_INTERFACE==1)) **to:** (CX_CPCIE_ENABLE && !(AMBA_INTERFACE==1))
CX_PHY_ENHANCED_PM_EN	**Enabled:** changed **from:** ((CX_S_CPCIE_MODE || CX_SEL_PHY_MODE)) **to:** CX_S_CPCIE_MODE
CX_L12_PG_EN	**Enabled:** changed **from:** ((CX_ENHANCED_PM_EN) && (CX_L1_SUBSTATES_ENABLE || CX_MPCIE_ENABLE)) **to:** ((CX_ENHANCED_PM_EN) && (CX_L1_SUBSTATES_ENABLE))
CX_L1_RETENTION	**Enabled:** changed **from:**((CX_L12_PG_EN) && (CX_L1_SUBSTATES_ENABLE ||CX_MPCIE_ENABLE)) **to:**((CX_L12_PG_EN) && (CX_L1_SUBSTATES_ENABLE))
DEFAULT_L0S_EXIT_LATENCY DEFAULT_L1_EXIT_LATENCY	**Enabled:** changed **from:** ((CX_S_CPCIE_MODE || CX_SEL_PHY_MODE)) **to:** CX_S_CPCIE_MODE
PWR_BUDGET_CAP_ENABLE	**Enabled:** changed **from:** Always **to:** !EMERGENCY_POWER_REDUCTION_ENABLE **Default value:** changed **from:** false **to:** EMERGENCY_POWER_REDUCTION_ENABLE ? 1 : 0
CX_SRIS_SUPPORT	**Enabled:** changed **from:** (!(CX_PCIE_MODE == SINGLE_MPCIE)) **to:** Always

Name	Change
CC_OB_PDCMP_RAM_RD_LATENCY CC_OB_NPDCMP_RAM_RD_LATENCY CC_SLV_NPW_SAB_RAM_RD_LATENCY	**Enabled:** changed **from:** MASTER_POPULATED **to:** SLAVE_POPULATED && AXI_POPULATED
CX_SMLH_PIPELINE_LTSSM	**Default value:**changed **from:** (CX_TECHNOLOGY == 0) && !CX_MPCIE_ENABLE **to:** (CX_TECHNOLOGY == 0) Enabled value changed **from:** CX_CUSTOM_PIPELINING && !CX_MPCIE_ENABLE **to:** CX_CUSTOM_PIPELINING
CX_RMLH_PIPE_REGOUT	**Default value:** changed **from:** (CX_MPCIE_ENABLE) ? 1 : (CX_TECHNOLOGY == 2) ? ((((CX_NB== 1) || (CX_GEN2_SPEED)) & (CX_NL > 1)) ? 1:0) : 1 **to:** (CX_TECHNOLOGY == 2) ? ((CX_CXL_ENABLE) ? 0 : (((CX_NB ==1) || (CX_GEN2_SPEED)) & (CX_NL > 1)) ? 1:0) : 1 **Enabled:** changed **from:** CX_CUSTOM_PIPELINING && !CX_MPCIE_ENABLE **to:** CX_CUSTOM_PIPELINING

6.6 Converting to the Current Release

Sometimes a new controller release might no longer use a certain configuration parameter, or the meaning of that parameter might have changed. The following process helps you convert your current configuration file so that it creates the same RTL with the new controller.

1. Open coreConsultant and create an unconfigured workspace from the newly installed controller.
2. In the coreConsultant command line, enter the following command:

   `parse_configfile my_configfile.config`

   where `my_configfile.config` is your current configuration file. This command creates an updated configuration file in your working directory as follows:

   `my_configfile.config.new`
3. In the coreConsultant command line, enter the following command:

   `source my_configfile.config.new`
4. Select Apply to generate the new RTL with the updated or translated parameters.
5. From the File Menu, select Write Batch Script and save the configuration file for the new release.
6. When you source the updated configuration file in coreConsultant, you can *ignore any new warnings* about parameter settings that are not relevant to, or not enabled in your configuration.

Attention

Writing Out Your Configuration File

To ensure that your existing configuration absorbs all changes to default parameters that the PCIe R&D team makes, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

You must convert your configuration file. Failure to do so, can result in:

- Your configuration file being incompatible with the current release.
- Functional, architectural, RAM, and I/O changes when the default of some configuration parameters change from release to release.

6.7 Known Issues and Limitations

You can view a complete list of functional problem reports for this product, including problems identified after product release, by accessing the STAR report on the Web. For more details, see "Details of Fixed Defects and Enhancements" on page 220. You must have a SolvNet ID to view STAR reports. This release has the following known tool and packaging issues at the time of release.

- "Packaged coreConsultant Test Limitations"
- "VTB Limitations"
- "Design Example"
- "Unique Case Violation Simulation Message"
- "coreConsultant Memory Map Limitations"

6.7.1 Packaged coreConsultant Test Limitations

We invite you to submit your coreConsultant configuration for review. Because of the very large configuration space, it is not possible to regress every configuration before a release is made. Synopsys is continually running fixed and randomized configurations, but it is possible that your exact configuration has not been regressed. Test case failures might occur because of improper testbench configuration. In that case open a case through SolvNetPlus.

6.7.1.1 Known Test Failures

The following are known testbench issues:

- AXI5 configuration cannot use the ARM AXI assertions.
- The `ft_ras_des_einj` test might fail for CXL with CXS.B interface configuration because of a testbench issue on assertions hdl path.
- The `pm_l1_transitions_dw_vdut_cpcie_l1_link_entr_l1_idle_vtb` test might fail with assertion error

  ```
  ERROR {CPCIE_CLKRST}
  muxd_aux_clk and core_clk are not synchronous on entering P1.CPM
  ```

  The test fails because two assertions must be updated to take PERST# into consideration.
- The `pl_disable_dw_vip_cpcie_vtb` test might fail to linkup in CXL mode on tests with VIP.
- The `vtb_ral_custom_test` might fail in CXL configurations with `CX_ACS_ENABLE =1` and `CX_N-FUNC =1`.

6.7.2 VTB Limitations

The following limitations apply to the current release of the VTB:

- Not backward compatible with previous releases
- Not UVM compliant
- No support for big-endian (`AHB_ENDIANNESS`) configurations

6.7.3 Design Example

The design example in `<workspace>/examples/DWC_pcie_clkrst.v` has been functionally verified, but has not been explicitly targeted for verification metrics. However, it has been used by Synopsys in the verification and regression environments for all controller configurations; including verification of all power transitions for the controller.

6.7.4 Unique Case Violation Simulation Message

The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

There is a known simulator issue with a "Unique case violation" message that occurs sometimes while running simulations with VCS outside of coreConsultant. You can ignore these messages.

To avoid these messages, use the `-xlrm uniq_prior_final` compile option in VCS. The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

6.7.5 coreConsultant Memory Map Limitations

The controller supports the generation of configuration-specific register maps as described in the "Register Configuration Space" chapter in the *Databook*. For SR-IOV configurations (`CX_SRIOV_ENABLE =1`), the following limitations apply.

Table 6-6 coreConsultant Report File Limitations for SR-IOV Configurations

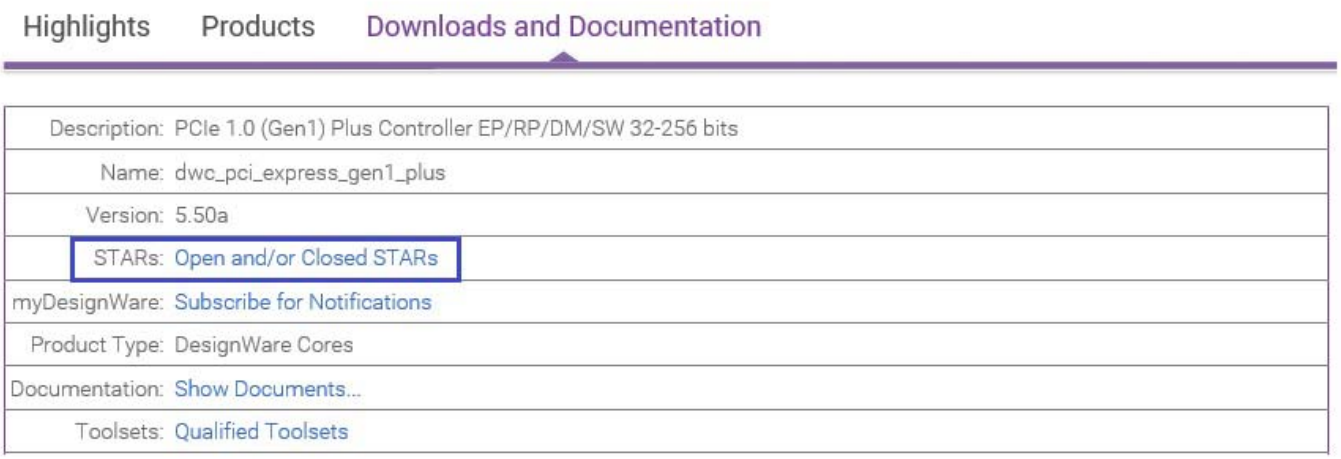
CX_NVFUNC	IP-XACT (IP-XACT XML)	RALF and C Headers (No limitations)	Register Report (DocBook XML) Also applies to Databook
1 - 256	Defines default #VFs in each PF	Defines default #VFs in each PF	Defines only first VF in each PF
257.. 4096	Defines only[a] first VF in each PF	Defines default #VFs in each PF	Defines only first VF in each PF

a. For details on how to populate remaining VFs in the IP-XACT file, see "Populating IP-XACT File Manually" in the "Creating Optional Views and Reports" section in the "Configuring the controller" chapter of the User Guide.

6.8 Details of Fixed Defects and Enhancements

Defects fixed in release 5.80a of the DesignWare Cores PCI Express Controller are listed in the STAR report for release 5.80a in STARs on the Web. You must have a SolvNet ID to view STAR reports at https://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_controllers.

Figure 6-1 Accessing STARs on the Web through SolvNet



Enhancement STARs are identifiable by the letter “E” in the Severity column, and fixed defect STARs are identifiable by the letter “B.” An E4 or B4 has the highest severity. Clicking on the tab corresponding to 5.80a produces a STAR report of closed STARS for this release. For previous controller versions, click the tab corresponding to the version in question.

6.9 Customer Support

Synopsys provides various methods for contacting Customer Support, as follows:

- Prepare the following debug information, if applicable:
  - For environment set-up problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, select the following menu:

    File > Build Debug Tar-file

    Check all the boxes in the dialog box that apply to your issue. This option gathers all the Synopsys product data needed to begin debugging an issue and writes it to the <*core tool startup directory*>/debug.tar.gz file.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD).
    - Identify the hierarchy path to the DesignWare instance.
    - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- *For the fastest response*, enter a case through SolvNetPlus:

  a. https://solvnetplus.synopsys.com

Note SolvNetPlus does not support Internet Explorer. Use a supported browser such as Microsoft Edge, Google Chrome, Mozilla Firefox, or Apple Safari.

  b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).

  c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

     Make sure to include the following:

     Product L1: DesignWare Cores

     Product L2: PCI Express

  d. After creating the case, attach any debug files you created.

     For more information about general usage information, refer to the following article in SolvNetPlus:

     https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
  - Attach any debug files you created.
- Or, telephone your local support center:
  - North America:

    Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.

- All other countries:
  https://www.synopsys.com/support/global-support-centers.html

7

Release Notes: 5.71a

These release notes describe the changes in this release *(5.71a)* relative to the previous production release *(5.70a)*. This release note contains the following sections:

- "Product Updates" on page 224
- "Changes to I/O" on page 226
- "Changes to Software View (Register Map)" on page 227
- "Changes to RAM Sizes" on page 228
- "Changes to Configuration Parameters" on page 229
- "Converting to the Current Release" on page 230
- "Known Issues and Limitations" on page 231
- "Details of Fixed Defects and Enhancements" on page 233
- "Customer Support" on page 234

7.1 Product Updates

This release contains the following major updates and other minor updates (indicated in "Details of Fixed Defects and Enhancements" on page 233).

7.1.1 ECC Protection to the AXI Interface

The controller optionally supports ECC protection in the AXI interface, as an alternate to parity protection. You can use the `CX_AXI_IF_TYPE_OF_PROT` parameter to configure the AXI interface protection. The Interface Safety Block (ISB) handles the parity and ECC protection generation and monitoring in the AXI interface. To enable ARC mode ECC computation, set the parameter `CX_AXI_IF_ECC_MODE` to '1'. The ARC mode supports only 32-bits ECC granularity. Table 7-1 shows the AXI Interface Protection parameter descriptions.

Table 7-1 AXI Interface Protection

Label	Description
AXI Interface Protection Enable (ECC/Parity)	Select AXI Interface protection features. ■ Legacy Mode (0) ■ Parity in data, address and control (1) ■ ECC in data, Parity in address and control (2) **Default Value:** Legacy Mode **Enabled:** ((CX_RASDP==0)? 0: 1) **Parameter Name:** CX_AXI_IF_TYPE_OF_PROT
ECC granularity for AXI Interface	Select the ECC Granularity for the AXI Interface. **Values:** ■ Full Width (0) ■ 32-bits (1) ■ 64-bits (2) **Default Value:** Full Width **Enabled:** (((CX_AXI_IF_TYPE_OF_PROT == 2) && CX_RASDP_EN)==1) **Parameter Name:** CX_AXI_IF_ECC_GRAN
ECC 32-bit Encoding	Select the AXI Interface ECC 32-bit Encoding: ■ 0: Standard ECC Computation ■ 1: ARC Mode ECC Computation **Values:** ■ Standard(0) ■ ARC Mode (1) **Default Value:** Standard **Enabled:** (((CX_AXI_IF_TYPE_OF_PROT == 2) &&CX_RASDP_EN)==1) **Parameter Name:** CX_AXI_IF_ECC_MODE

For more information, see "RAS Data Protection" section in the "Controller Operations" chapter of the *Databook*.

7.1.2 Updated Automotive Safety Package

The automotive safety package for 5.71a includes an updated automotive reference for FMEDA, Safety manual, and DFMEA.

For more information, see "Automotive Safety Package" section in the "Automotive" chapter of the Databook.

7.2 Changes to I/O

This section details any changes to the I/O of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the I/O are indicated in the change-tracked version of the *Databook* PDF which can be found at the location identified in the *Databook* revision history.

The following I/O changes have occurred for all configurations:

Table 7-2 I/O Signals Added, Removed, or Renamed

Name	Type	Change	Comment
*misc_info_tlpprfx	I/O	Signal Width	The signal width is changed from [(PRFX_W_PAR-1):0] to [(PRFX_WIDTH-1):0]
*_[aw|ar]addrp	I/O	Renamed	Renamed and re-purposed as *_[ar|aw]user
*_[w|r]datap	I/O		Renamed and re-purposed as *_[r|w]user

Documentation Changes

A number of signals were incorrectly described in the *Databook*. These are also highlighted in the change-tracked version of the *Databook*. These are *not* RTL changes.

The following I/O changes have occurred for all configurations:

Table 7-3 Documentation Changes (Non-RTL)

Name	Type	Change	Comment
For many signals **Synchronous To** is corrected. These corrections are indicated in the change-tracked version of the Databook PDF which can be found at the location identified in the Databook revision history.			

7.3 Changes to Software View (Register Map)

This section discusses changes to the register map of the controller that have occurred in this release.

- It lists renamed registers.
- It lists deleted registers.
- It does *not* list new registers.
- *All* changes to the software map are indicated in the change-tracked version of the *Register Descriptions* PDF which can be found at the location identified in the *Register Descriptions* revision history.

The following changes have occurred for all configurations.

Table 7-4 Register Deletions/Renaming

Register	Field	Nature of Change
No changes in this release.		

Table 7-5 Documentation Changes (Non-RTL)

Register	Field	Nature of Change
No changes in this release.		

7.4 Changes to RAM Sizes

This section details the changes to the default RAM sizes that have occurred since the last production release. It does not detail changes that are associated with new or additional features that you enable on your current configuration

Caution To determine the precise changes to RAM sizes for your actual controller configuration, you can compare the coreConsultant generated RAM sizes for the previous and current releases. For more details, see the “RAM Requirements” section in the Architecture chapter of the *Databook*.

The following changes have occurred for this release.

RAM Name	Change
No changes in this release.	

7.5 Changes to Configuration Parameters

This section details any changes to the configuration parameters of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the configuration parameters are indicated in the change-tracked version of the *Databook* PDF which can be found at the location identified in the *Databook* revision history.

If you intend to source an existing configuration batch file, then you must first convert your configuration file, as described in "Product Updates" on page 224. If you are not sourcing an existing configuration batch file, then you should be still aware of changes to the default value of some configuration parameters.

Caution To ensure that your existing configuration absorbs all changes to default parameters that the PCIe R&D team makes, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

Table 7-6 Configuration Parameter Changes

Name	Change
CX_APP_FLR_PIPE_EN	**Default Value** changed **from** CX_CUSTOM_PIPELINING &&CX_FLR_ENABLE && (CX_MAX_CORECLK_FREQ >=500) **to** CX_FLR_ENABLE && (CX_MAX_CORECLK_FREQ >=500)

7.6 Converting to the Current Release

Sometimes a new controller release might no longer use a certain configuration parameter, or the meaning of that parameter might have changed. The following process helps you convert your current configuration file so that it creates the same RTL with the new controller.

1. Open coreConsultant and create an unconfigured workspace from the newly installed controller.
2. In the coreConsultant command line, enter the following command:

   ```
   parse_configfile my_configfile.config
   ```

   where `my_configfile.config` is your current configuration file. This command creates an updated configuration file in your working directory as follows:

   ```
   my_configfile.config.new
   ```
3. In the coreConsultant command line, enter the following command:

   ```
   source my_configfile.config.new
   ```
4. Select Apply to generate the new RTL with the updated or translated parameters.
5. From the File Menu, select Write Batch Script and save the configuration file for the new release.
6. When you source the updated configuration file in coreConsultant, you can *ignore any new warnings* about parameter settings that are not relevant to, or not enabled in your configuration.

Attention

Writing Out Your Configuration File

To ensure that your existing configuration absorbs all changes to default parameters that the PCIe R&D team makes, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

You must convert your configuration file. Failure to do so, can result in:

- Your configuration file being incompatible with the current release.
- Functional, architectural, RAM, and I/O changes when the default of some configuration parameters change from release to release.

7.7 Known Issues and Limitations

You can view a complete list of functional problem reports for this product, including problems identified after product release, by accessing the STAR report on the Web. For more details, see "Details of Fixed Defects and Enhancements" on page 233. You must have a SolvNet ID to view STAR reports. This release has the following known tool and packaging issues at the time of release.

- "Packaged coreConsultant Test Limitations"
- "VTB Limitations"
- "Design Example"
- "Unique Case Violation Simulation Message"
- "coreConsultant Memory Map Limitations"

7.7.1 Packaged coreConsultant Test Limitations

We invite you to submit your coreConsultant configuration for review. Because of the very large configuration space, it is not possible to regress every configuration before a release is made. Synopsys is continually running fixed and randomized configurations, but it is possible that your exact configuration has not been regressed. Test case failures might occur because of improper test bench configuration. In that case open a case through SolvNet.

7.7.2 VTB Limitations

The following limitations apply to the current release of the VTB:

- Not backward compatible with previous releases
- Not UVM compliant
- No support for big-endian (`AHB_ENDIANNESS`) configurations

7.7.3 Design Example

The design example in `<workspace>/examples/DWC_pcie_clkrst.v` has been functionally verified, but has not been explicitly targeted for verification metrics. However, it has been used by Synopsys in the verification and regression environments for all controller configurations; including verification of all power transitions for the controller.

7.7.3.1 Unique Case Violation Simulation Message

The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

There is a known simulator issue with a "Unique case violation" message that occurs sometimes while running simulations with VCS outside of coreConsultant. You can ignore these messages.

To avoid these messages, use the `-xlrm uniq_prior_final` compile option in VCS. The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

7.7.3.2 coreConsultant Memory Map Limitations

The controller supports the generation of configuration-specific register maps as described in the "Register Configuration Space" chapter in the *Databook*. For SR-IOV configurations (`CX_SRIOV_ENABLE =1`), the following limitations apply.

Table 7-7 coreConsultant Report File Limitations for SR-IOV Configurations

CX_NVFUNC	IP-XACT (IP-XACT XML)	RALF and C Headers (No limitations.)	Register Report (DocBook XML). Also applies to Databook.
1 - 256	Defines default #VFs in each PF	Defines default #VFs in each PF	Defines only first VF in each PF
257 .. 4096	Defines only[a] first VF in each PF	Defines default #VFs in each PF	Defines only first VF in each PF

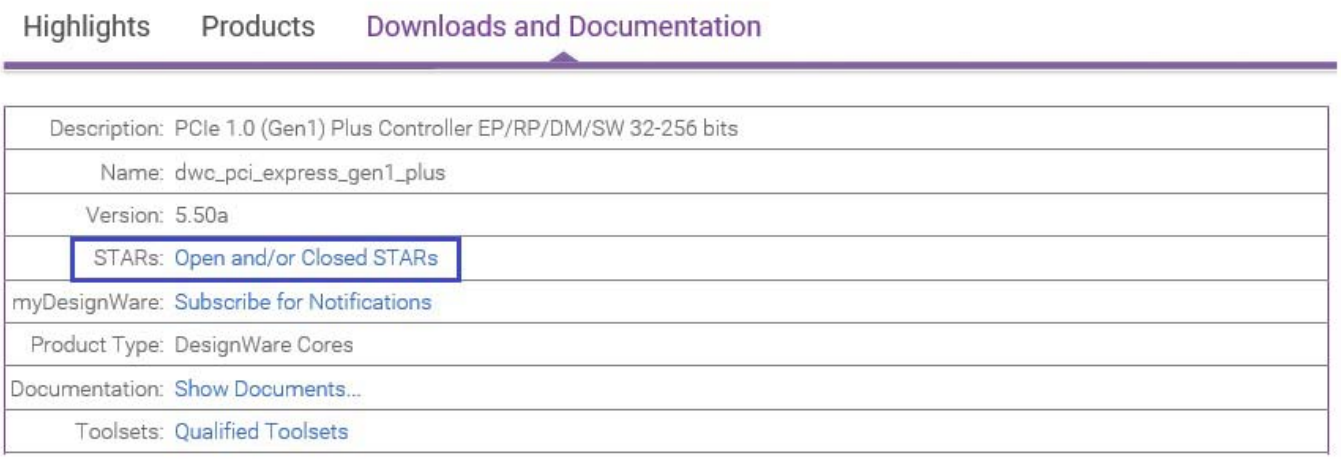
a. For details on how to populate remaining VFs in the IP-XACT file, see "Populating IP-XACT File Manually" in the "Creating Optional Views and Reports" section in the "Configuring the controller" chapter of the User Guide.

7.8 Details of Fixed Defects and Enhancements

Defects fixed in release 5.71a of the DesignWare Cores PCI Express Controller are listed in the STAR report for release 5.71a in STARs on the Web. You must have a SolvNet ID to view STAR reports at https://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_controllers.

http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_ep#tab2

Figure 7-1 Accessing STARs on the Web through SolvNet



Enhancement STARs are identifiable by the letter “E” in the Severity column, and fixed defect STARs are identifiable by the letter “B.” An E4 or B4 has the highest severity. Clicking on the tab corresponding to 5.71a produces a STAR report of closed STARS for this release. For previous controller versions, click the tab corresponding to the version in question.

7.9 Customer Support

Synopsys provides various methods for contacting Customer Support, as follows:

- Prepare the following debug information, if applicable:
  - For environment set-up problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, select the following menu:

    File > Build Debug Tar-file

    Check all the boxes in the dialog box that apply to your issue. This option gathers all the Synopsys product data needed to begin debugging an issue and writes it to the <*core tool startup directory*>/debug.tar.gz file.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD).
    - Identify the hierarchy path to the DesignWare instance.
    - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- *For the fastest response*, enter a case through SolvNetPlus:

  a. https://solvnetplus.synopsys.com

Note SolvNetPlus does not support Internet Explorer. Use a supported browser such as Microsoft Edge, Google Chrome, Mozilla Firefox, or Apple Safari.

  b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).

  c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

     Make sure to include the following:

     Product L1: DesignWare Cores

     Product L2: PCI Express

  d. After creating the case, attach any debug files you created.

     For more information about general usage information, refer to the following article in SolvNetPlus:

     https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
  - Attach any debug files you created.
- Or, telephone your local support center:
  - North America:

    Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.

- All other countries:
  https://www.synopsys.com/support/global-support-centers.html

8

Release Notes: 5.70a

These release notes describe the changes in this release *(5.70a)* relative to the previous production release *(5.60a)*. This release note contains the following sections:

- "Product Updates" on page 238
- "Changes to I/O" on page 241
- "Changes to Software View (Register Map)" on page 242
- "Changes to RAM Sizes" on page 249
- "Changes to Configuration Parameters" on page 250
- "Converting to the Current Release" on page 251
- "Known Issues and Limitations" on page 252
- "Details of Fixed Defects and Enhancements" on page 254
- "Customer Support" on page 255

8.1 Product Updates

This release contains the following major updates and other minor updates (indicated in "Details of Fixed Defects and Enhancements" on page 254).

8.1.1 HDMA Channel Separation

The controller supports per-channel register address segments separation. By default, each channel's register address segment is separated by 256. You can configure the per-channel register address segment separation using the internal parameter `CX_DMAREG_CHADDR_SPACE` or `CHANNEL_SEPARATION` field of `VSECDMA_DEVICE_INFORMATION_OFF` register.

For more information, see the *Registers and Context Memory* topic in *HDMA Architecture* section in the *HDMA* chapter of the *Databook*.

8.1.2 Atomic Operations for AXI5

The controller supports PCIe AtomicOps transactions for AMBA AXI5 configuration, in addition to the native PCIe controller configuration. For AMBA AXI5 configurations (`AMBA_INTERFACE =AXI5`), the AXI bridge module seamlessly transports the PCIe AtomicOp transactions to the AXI interconnect, and vice-versa when you enable AtomicOps (`CX_ATOMIC_ENABLE =1`).

For more information on AtomicOps support for AXI5 configuration, see *"Atomic Operations"* section in the *"Controller Operations"* chapter of the *Databook*.

Note: In this release, Atomic Operations for AXI5 is an Early Adopter (EA) feature and must not be used for tape out. Contact Synopsys support through SolvNetPlus for an unlocking key for this feature.

8.1.3 EQ Coefficient Request in FOM Mode (FCOEF)

The controller supports EQ Coefficient Request in Figure Of Merit (FOM) mode when you set the parameter `CX_EQ_MASTER_COEF_REQ_FOR_FOM_ENABLE` to '1'.

- The EQ master requests for coefficients from the programmed port logic registers `GEN3_FCO-EF_LANE*_[PRE|POST]_CURSOR` in Recovery.Equalization Phase2 for USP or Recovery.Equalization Phase 3 for DSP in EQ master phases.
- The EQ master informs the PHY of performing FOM evaluation for the coefficients requested and sends the coefficients through TS1s to the remote partner. The coefficients received by the remote partner are applied to its transmitter.

For more information, see *EQ Coefficient Request in FOM Mode (FCOEF)* topic in *Advanced Information: Gen3/4/5 Equalization Details and Example* appendix of the *Databook*.

8.1.4 SerDes Architecture Support for Controller - PHY Combination

Table 8-1 describes the new Gen5 controller - PHY combination support for SerDes architecture (`CX_PIPE_SERDES_ARCH =1`) added in 5.70a.

Table 8-1 Gen5 Controller-PHY Combinations Supported

		PHY
		g1_4s **g2_4s_df** **g3_8s_dw** **g4_8s_df** **g5_8s_df**
Controller	g1_4s g2_4s_df g3_8s_dw g4_8s_df g5_8s_df	Yes

Table 8-2 describes the new Gen4 controller - PHY combination support for SerDes architecture (`CX_PIPE_SERDES_ARCH =1`) added in 5.70a.

Table 8-2 Gen4 Controller-PHY Combinations Supported

		PHY
		g1_4s **g2_4s_df** **g3_8s_dw** **g4_8s_df**
Controller	g1_4s g2_4s_df g3_8s_dw g4_8s_df	Yes

Table 8-3 describes the new Gen3 controller - PHY combination support for SerDes architecture (`CX_PIPE_SERDES_ARCH =1`) added in 5.70a.

Table 8-3 Gen3 Controller-PHY Combinations Supported

		PHY
		g1_2s **g2_4s_dw** **g3_8s_dw**
Controller	g1_2s g2_4s_dw g3_8s_dw	Yes

For more information, see *Controller-PHY Compatibility* topic in *Frequency, Speed, and Width Support* section in *Product Overview* chapter of the *Databook*.

8.1.5 Data Link Feature Exchange

For Gen4 and above, the controller is enhanced to facilitate link up with legacy endpoint devices that do not support Scaled Flow Control. To enable this link up, you must set `DL_FEATURE_EXCHANGE_EN` field of `DATA_LINK_FEATURE_CAP_OFF` register to '0'.

For more information, see the *Scaled Flow Control* topic in *Flow Control* section in the *Controller Operations* chapter of the *Databook* and `DATA_LINK_FEATURE_CAP_OFF` register in the *Register Descriptions*.

8.1.6 AXI Bridge Buffering

The controller is enhanced to allow AXI slave to read from 'Slave Completion Composer Segmented Buffer'. The 'Slave Completion Composer Segmented Buffer RAM' and 'Slave Completion CDC FIFO RAM' are merged into 'Slave Completion Composer Segmented Buffer'.This improves the throughput and latency on the AXI bridge, when the outbound slave completion reads the slave frequency higher than the controller frequency.

For more information see, *Bridge Buffering* topic in the *AXI Bridge Architecture* section in *AMBA* chapter of the *Databook*.

8.2 Changes to I/O

This section details any changes to the I/O of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the I/O are indicated in the change-tracked version of the *Databook* PDF which can be found at the location identified in the *Databook* revision history.

The following I/O changes have occurred for all configurations:

Table 8-4 I/O Signals Added, Removed, or Renamed

Name	Type	Change	Comment
mstr_*	O	Signal Width	The signal width is changed from [(MSTR_ID_WD-1):0] to [MSTR_ID_WD_ATOP-1):0]
mstrh_*			
mstr_*_info_tlpprfx	I	Added	Signal Description added in the *Databook*.
slv_*_info_tlpprfx	O		

Documentation Changes

A number of signals were incorrectly described in the *Databook*. These are also highlighted in the change-tracked version of the *Databook*. These are *not* RTL changes.

The following I/O changes have occurred for all configurations:

Table 8-5 Documentation Changes (Non-RTL)

Name	Type	Change	Comment
For many signals **Synchronous To** is corrected. These corrections are indicated in the change-tracked version of the Databook PDF which can be found at the location identified in the Databook revision history.			

8.3 Changes to Software View (Register Map)

This section discusses changes to the register map of the controller that have occurred in this release.

- It lists renamed registers.
- It lists deleted registers.
- It does *not* list new registers.
- *All* changes to the software map are indicated in the change-tracked version of the *Register Descriptions* PDF which can be found at the location identified in the *Register Descriptions* revision history.

The following changes have occurred for all configurations.

Table 8-6 Register Deletions/Renaming

Register	Field	Nature of Change
No changes in this release.		

Documentation Changes

A number of registers were incorrectly described in the IP-XACT XML, DocBook XML, RAL files, header files, and *Databook*. These are also highlighted in the change-tracked version of the *Register Descriptions* PDF. These are *not* RTL changes.

Table 8-7 Documentation Changes (Non-RTL)

Register	Field	Nature of Change
MSI_CAP_OFF_08H_REG	PCI_MSI_CAP_OFF_08H	**Memory Access** Corrected
NPEM_CTRL_OFF	NPEM_CRITICAL_ARRAY_CONTROL NPEM_DISABLED_CONTROL NPEM_ENCLOSURE_SPECIFIC_CONTROL NPEM_FAILED_ARRAY_CONTROL NPEM_FAIL_CONTROL NPEM_HOT_SPARE_CONTROL NPEM_INVALID_DEVICE_TYPE_CONTROL NPEM_LOCATE_CONTROL NPEM_OK_CONTROL NPEM_PFA_CONTROL NPEM_REBUILD_CONTROL	**Memory Access** Corrected
PCI_MSI_CAP_ID_NEXT_CTRL_REG	PCI_MSI_ENABLE PCI_MSI_MULTIPLE_MSG_EN	**Memory Access** Corrected
VF_MSI_CAP_OFF_04H_REG	PCI_MSI_CAP_OFF_04H	**Memory Access** Corrected
VF_MSI_CAP_OFF_08H_REG	PCI_MSI_CAP_OFF_08H	**Memory Access** Corrected

Register	Field	Nature of Change
VF_PCI_MSI_CAP_ID_NEXT_CTRL_REG	PCI_MSI_ENABLE PCI_MSI_MULTIPLE_MSG_EN	**Memory Access** Corrected
DATA_LINK_FEATURE_CAP_OFF	DL_FEATURE_EXCHANGE_EN	**Value After Reset** Corrected
GEN3_RELATED_OFF	EQ_EIEOS_CNT	**Value After Reset** Corrected
PL16G_CAP_OFF_[20|24|28|2C]H_REG	DSP_16G_TX_PRESET[0-15]	**Value After Reset** Corrected
SYMBOL_TIMER_FILTER_1_OFF	SKP_INT_VAL	**Value After Reset** Corrected
NPEM_CTRL_OFF	NPEM_INITIATE_RESET	**Testable** Corrected
DMA_CH_CONTROL1_OFF_[RD|WR]CH_0	CB CCS CS DMA_AT DMA_ELEMETNT _PREFETCH DMA_FUNC_NUM DMA_MEM_TYPE DMA_NS_DST DMA_NS_SRC DMA_RESERVED[0|1|5] DMA_RO DMA_TC LIE LLE LLP RIE TCB	Field Made Visible
DMA_CH_CONTROL2_OFF_[RD|WR]CH_0	DMA_PH DMA_RESERVED3 DMA_ST DMA_TH DMA_VF DMA_VF_EN DMA_VF_RESERVED	Field Made Visible
DMA_DAR_[LOW|HIGH]_OFF_[RD|WR]CH_0	DST_ADDR_REG_[LOW|HIGH]	Field Made Visible
DMA_LLP_[LOW|HIGH]_OFF_[RDWR]CH_0	LLP_[LOW|HIGH]	Field Made Visible

Register	Field	Nature of Change
DMA_READ_CH[0-7]_PWR_EN_OFF	DMA_READ_CH[0-7]_PWR_EN RSVDP_1	Field Made Visible
DMA_READ_CH[01|23|45|67]_IMWR_DATA_OFF	RD_CHANNEL_[0-7]_DATA	Field Made Visible
DMA_[READ|WRITE]_CHANNEL_ARB_WEIGHT_[LOW|HIGH]_OFF	READ_CHANNEL[0-7]_WEIGHT RSVDP_20	Field Made Visible
DMA_SAR_[LOW|HIGH]_OFF_[RD|WR]CH_0	SRC_ADDR_REG_[LOW|HIGH]	Field Made Visible
DMA_TRANSFER_SIZE_OFF_[RD|WR]CH_0	DMA_TRANSFER_SIZE	Field Made Visible
DMA_WRITE_CH[01|23|45|67]_IMWR_DATA_OFF	WR_CHANNEL_[0-7]_DATA	Field Made Visible
DMA_WRITE_CH[0-7]_PWR_EN_OFF	DMA_WRITE_CH[0-7]_PWR_EN RSVDP_1	Field Made Visible
HDMA_CONTROL1_OFF_[RDCH|WRCH_0	AT DST_SNOOP LLEN MEM_TYPE PH RO SRC_SNOOP ST TH	Field Made Visible
HDMA_CYCLE_OFF_[RD|WR]CH_0	CYCLE_[BIT|STATE]	Field Made Visible
HDMA_DAR_[LOW|HIGH]_OFF_[RD|WR]CH_0	DAR_PTR_[LOW|HIGH]	Field Made Visible
HDMA_DOORBELL_OFF_[RD|WR]CH_0	DB_[START|STOP]	Field Made Visible
HDMA_ELEM_PF_OFF_[RD|WR]CH_0	PREFETCH	Field Made Visible
HDMA_EN_OFF_[RD|WR]CH_0	ENABLE	Field Made Visible
HDMA_FUNC_NUM_OFF_[RD|WR]CH_0	PF VF VF_EN	Field Made Visible
HDMA_HANDSHAKE_OFF_[RD|WR]CH_0	HANDSHAKE_COUNT HS_EN	Field Made Visible

Register	Field	Nature of Change
HDMA_INT_CLEAR_OFF_[RD|WR]CH_0	ABORT_CLEAR STOP_CLEAR WATERMARK_CLEAR	Field Made Visible
HDMA_INT_SETUP_OFF_[RD|WR]CH_0	ABORT_MASK LAIE LSIE RAIE RSIE STOP_MASK WATERMARK_MASK	Field Made Visible
HDMA_INT_STATUS_OFF_[RD|WR]CH]]_0	ABORT ERROR STOP WATERMARK	Field Made Visible
HDMA_LLP_[LOW|HIGH]_OFF_[RD|WR]CH_0	ELEMENT_LIST_PTR_[LOW|HIGH]	Field Made Visible
HDMA_MSI_ABORT_[LOW|HIGH]_OFF_[RD|WR]CH_0	MSI_ABORT_ADDR_[LOW|HIGH]	Field Made Visible
HDMA_MSI_MSGD_OFF_[RD|WR]CH_0	MSI_MESSAGE	Field Made Visible
HDMA_MSI_STOP_[LOW|HIGH]_OFF_[RD|WR]CH_0	MSI_STOP_ADDR_[LOW|HIGH]	Field Made Visible
HDMA_MSI_WATERMARK_[LOW|HIGH]_OFF_[RD|WR]CH_0	MSI_WATERMARK_ADDR_[LOW|HIGH]	Field Made Visible
HDMA_QOS_OFF_[RD|WR]CH_0	PF_DEPTH TC WEIGHT	Field Made Visible
HDMA_SAR_[LOW|HIGH]_OFF_[RD|WR]CH_0	SAR_PTR_[LOW|HIGH]	Field Made Visible
HDMA_STATUS_OFF_[RD|WR]CH_0	STATUS	Field Made Visible
HDMA_WATERMARK_EN_OFF_[RD|WR]CH_0	LWIE RWIE	Field Made Visible
HDMA_XFERSIZE_OFF_[RD|WR]CH_0	XFERSIZE	Field Made Visible
IATU_LIMIT_ADDR_OFF_[INBOUND|OUTBOUND]_0	CBUF_INCR LIMIT_ADDR_[H|R]W	Field Made Visible
IATU_LWR_[BASE|TARGET]_ADDR_OFF_[INBOUND|OUTBOUND]_0	LWR_[BASE|TARGET]_[H|R]W LWR_TARGET_RW_OUTBOUND	Field Made Visible

Register	Field	Nature of Change
IATU_REGION_CTRL_1_OFF_[INBOUND|OUTBOUND]_0	AT ATTR CTRL_1_FUNC_NUM IDO INCREASE_REGION_SIZE PH TC TD TH TYPE	Field Made Visible
IATU_REGION_CTRL_2_OFF_INBOUND_0	ATTR_MATCH_EN AT_MATCH_EN BAR_NUM CFG_SHIFT_MODE FUNC_NUM_MATCH_EN FUZZY_TYPE_MATCH_CODE INVERT_MODE MATCH_MODE MSG_CODE MSG_CODE_MATCH_EN MSG_TYPE_MATCH_MODE PH_MATCH_EN REGION_EN RESPONSE_CODE SINGLE_ADDR_LOC_TRANS_EN TC_MATCH_EN TD_MATCH_EN TH_MATCH_EN VFBAR_MATCH_MODE_EN VF_MATCH_EN	Field Made Visible

Register	Field	Nature of Change
IATU_REGION_CTRL_2_OFF_OUTBOUND_0	CFG_SHIFT_MODE DMA_BYPASS FUNC_BYPASS HEADER_SUBSTITUTE_EN INHIBIT_PAYLOAD INVERT_MODE MSB2BITS_TAG MSG_CODE REGION_EN SNP TAG TAG_SUBSTITUTE_EN TLP_HEADER_FIELDS_BYPASS	Field Made Visible
IATU_REGION_CTRL_3_OFF_[INBOUND|OUTBOUND]_0	RSVDP_VF_NUMBER VF_ACTIVE VF_NUMBER	Field Made Visible
IATU_UPPER_BASE_ADDR_OFF_[INBOUND|OUTBOUND]_0	UPPER_[BASE|TARGET]_RW	Field Made Visible
IATU_UPPR_LIMIT_ADDR_OFF_[INBOUND|OUTBOUND_0	UPPR_LIMIT_ADDR_[H|R]W	Field Made Visible
NPEM_CAP_OFF	NPEM_CAPABLE NPEM_CRITICAL_ARRAY_CAPABLE NPEM_DISABLED_CAPABLE NPEM_ENCLOSURE_SPECIFIC_CAPABILITIES NPEM_FAILED_ARRAY_CAPABLE NPEM_FAIL_CAPABLE NPEM_HOT_SPARE_CAPABLE NPEM_INVALID_DEVICE_TYPE_CAPABLE NPEM_LOCATE_CAPABLE NPEM_PFA_CAPABLE NPEM_REBUILD_CAPABLE NPEM_RESET_CAPABLE RESVDP12	Field Made Visible

Register	Field	Nature of Change
NPEM_CTRL_OFF	NPEM_ENABLE NPEM_CRITICAL_ARRAY_CONTROL NPEM_DISABLED_CONTROL NPEM_ENCLOSURE_SPECIFIC_CONTROL NPEM_FAILED_ARRAY_CONTROL NPEM_FAIL_CONTROL NPEM_HOT_SPARE_CONTROL NPEM_INITIATE_RESET NPEM_INVALID_DEVICE_TYPE_CCONTROL NPEM_LOCATE_CONTROL NPEM_OK_CONTROL NPEM_REBUILD_CONTROL RSVDP12	Field Made Visible
NPEM_EXT_CAP_HDR_OFF	NPEM_CAP_VERSION NPEM_EXT_CAP_ID NPEM_NEXT_OFFSET	Field Made Visible
NPEM_STATUS_OFF	NPEM_CMD_COMPLETE NPEM_ENCLOSURE_SPECIFIC_STATUS	Field Made Visible
VF_CORR_ERR_STATUS_OFF	HEADER_LOG_OVERFLOW_STATUS	Field Made Visible

8.4 Changes to RAM Sizes

This section details the changes to the default RAM sizes that have occurred since the last production release. It does not detail changes that are associated with new or additional features that you enable on your current configuration

Caution To determine the precise changes to RAM sizes for your actual controller configuration, you can compare the coreConsultant generated RAM sizes for the previous and current releases. For more details, see the "RAM Requirements" section in the Architecture chapter of the *Databook*.

The following changes have occurred for this release.

RAM Name	Change
Slave Completion CDC FIFO RAM	The RAM instance 'u_ob_cpl_c2a_cdc_ram' has been removed. For more information, see "AXI Bridge Buffering" on page 240.

8.5 Changes to Configuration Parameters

This section details any changes to the configuration parameters of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the configuration parameters are indicated in the change-tracked version of the *Databook* PDF which can be found at the location identified in the *Databook* revision history.

If you intend to source an existing configuration batch file, then you must first convert your configuration file, as described in "Product Updates" on page 238. If you are not sourcing an existing configuration batch file, then you should be still aware of changes to the default value of some configuration parameters.

Caution To ensure that your existing configuration absorbs all changes to default parameters that the PCIe R&D team makes, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

Table 8-8 Configuration Parameter Changes

Name	Change
CX_10BITS_TAG	**Enabled**: changed **from:** ((AMBA_INTERFACE != 1) && (CX_GEN4_SPEED_VALUE == 0)) **to:** ((AMBA_INTERFACE != 1) && (CX_GEN4_SPEED_VALUE == 0) && (CX_MAX_TAG <= 255) && (CX_REMOTE_MAX_TAG <= 255))
1-Port SRAMs only	**Enabled:** changed **from:** CX_RAM_AT_TOP_IF && CX_MAX_PCLK_EXISTS **to:** ((CX_PHY_MAX_PCLK_FREQ_MHZ > 0 || CX_PIPE_PCLK_MODE > 0))
CX_RTLH_FC_CHECK_REGOUT	Enabled: changed 1 **from:** CX_RTLH_SIMPLE_EXTRACT && CX_CUSTOM_PIPELINING **to:** CX_CUSTOM_PIPELINING

8.6 Converting to the Current Release

Sometimes a new controller release might no longer use a certain configuration parameter, or the meaning of that parameter might have changed. The following process helps you convert your current configuration file so that it creates the same RTL with the new controller.

1. Open coreConsultant and create an unconfigured workspace from the newly installed controller.
2. In the coreConsultant command line, enter the following command:

   ```
   parse_configfile my_configfile.config
   ```

   where `my_configfile.config` is your current configuration file. This command creates an updated configuration file in your working directory as follows:

   ```
   my_configfile.config.new
   ```
3. In the coreConsultant command line, enter the following command:

   ```
   source my_configfile.config.new
   ```
4. Select Apply to generate the new RTL with the updated or translated parameters.
5. From the File Menu, select Write Batch Script and save the configuration file for the new release.
6. When you source the updated configuration file in coreConsultant, you can *ignore any new warnings* about parameter settings that are not relevant to, or not enabled in your configuration.

Attention

Writing Out Your Configuration File

To ensure that your existing configuration absorbs all changes to default parameters that the PCIe R&D team makes, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

You must convert your configuration file. Failure to do so, can result in:

- Your configuration file being incompatible with the current release.
- Functional, architectural, RAM, and I/O changes when the default of some configuration parameters change from release to release.

8.7 Known Issues and Limitations

You can view a complete list of functional problem reports for this product, including problems identified after product release, by accessing the STAR report on the Web. For more details, see "Details of Fixed Defects and Enhancements" on page 254. You must have a SolvNet ID to view STAR reports. This release has the following known tool and packaging issues at the time of release.

- "Packaged coreConsultant Test Limitations"
- "VTB Limitations"
- "Design Example"
- "Unique Case Violation Simulation Message"
- "coreConsultant Memory Map Limitations"

8.7.1 Packaged coreConsultant Test Limitations

We invite you to submit your coreConsultant configuration, so that Synopsys can run the full range of testing on your configuration. Because of the very large configuration space, it is not possible to regress every configuration before a release is made. Synopsys is continually running fixed and randomized configurations, but it is possible that your exact configuration has not been regressed. Test case failures might occur because of improper test bench configuration. In that case open a case through SolvNet.

8.7.2 VTB Limitations

The following limitations apply to the current release of the VTB:

- Not backward compatible with previous releases
- Not UVM compliant
- No support for big-endian (`AHB_ENDIANNESS`) configurations

8.7.3 Design Example

The design example in `<workspace>/examples/DWC_pcie_clkrst.v` has been functionally verified, but has not been explicitly targeted for verification metrics. However, it has been used by Synopsys in the verification and regression environments for all controller configurations; including verification of all power transitions for the controller.

8.7.3.1 Unique Case Violation Simulation Message

The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

There is a known simulator issue with a "Unique case violation" message that occurs sometimes while running simulations with VCS outside of coreConsultant. You can ignore these messages.

To avoid these messages, use the `-xlrm uniq_prior_final` compile option in VCS. The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

8.7.3.2 coreConsultant Memory Map Limitations

The controller supports the generation of configuration-specific register maps as described in the "Register Configuration Space" chapter in the *Databook*. For SR-IOV configurations (`CX_SRIOV_ENABLE =1`), the following limitations apply.

Table 8-9 coreConsultant Report File Limitations for SR-IOV Configurations

CX_NVFUNC	IP-XACT (IP-XACT XML)	RALF and C Headers (No limitations.)	Register Report (DocBook XML). Also applies to Databook.
1 - 256	Defines default #VFs in each PF	Defines default #VFs in each PF	Defines only first VF in each PF
257 .. 4096	Defines only[a] first VF in each PF	Defines default #VFs in each PF	Defines only first VF in each PF

a. For details on how to populate remaining VFs in the IP-XACT file, see "Populating IP-XACT File Manually" in the "Creating Optional Views and Reports" section in the "Configuring the controller" chapter of the User Guide.

8.8 Details of Fixed Defects and Enhancements

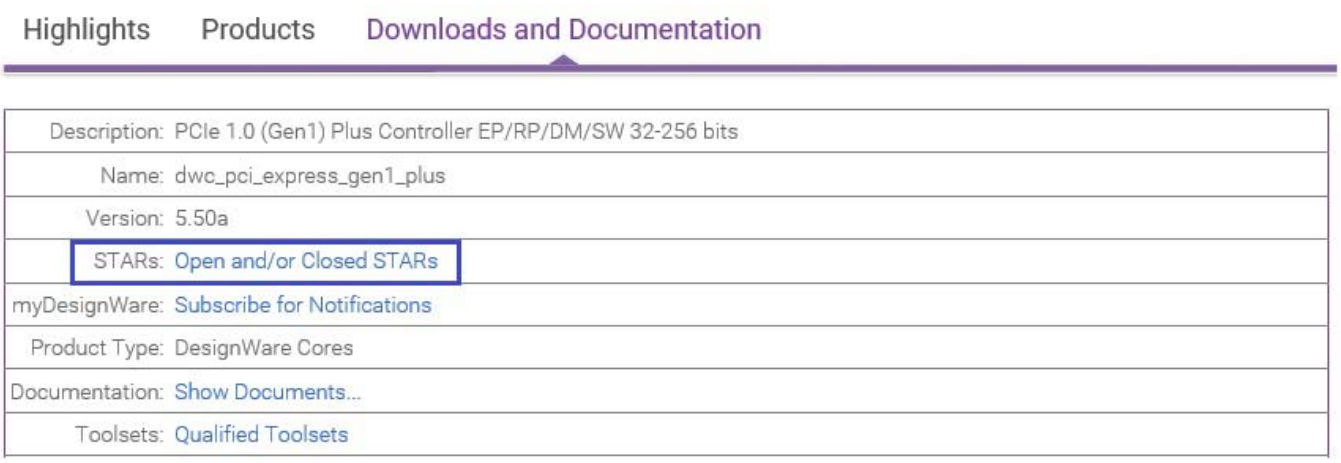
Defects fixed in release 5.70a of the DesignWare Cores PCI Express Controllerare listed in the STAR report for release 5.70a in STARs on the Web. You must have a SolvNet ID to view STAR reports as shown in Table 8-10.

http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_ep#tab2

Table 8-10 Accessing STARs on the Web through SolvNet

Controller	Web Address
DM	http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_dm#tab2
EP	http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_ep#tab2
RC	http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_rc#tab2
SW	http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_sw#tab2

Figure 8-1 Accessing STARs on the Web through SolvNet



Enhancement STARs are identifiable by the letter “E” in the Severity column, and fixed defect STARs are identifiable by the letter “B.” An E4 or B4 has the highest severity. Clicking on the tab corresponding to 5.70a produces a STAR report of closed STARS for this release. For previous controller versions, click the tab corresponding to the version in question.

8.9 Customer Support

Synopsys provides various methods for contacting Customer Support, as follows:

- Prepare the following debug information, if applicable:
  - For environment set-up problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, select the following menu:

    File > Build Debug Tar-file

    Check all the boxes in the dialog box that apply to your issue. This option gathers all the Synopsys product data needed to begin debugging an issue and writes it to the <*core tool startup directory*>/debug.tar.gz file.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD).
    - Identify the hierarchy path to the DesignWare instance.
    - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- *For the fastest response*, enter a case through SolvNetPlus:

  a. https://solvnetplus.synopsys.com

Note SolvNetPlus does not support Internet Explorer. Use a supported browser such as Microsoft Edge, Google Chrome, Mozilla Firefox, or Apple Safari.

  b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).

  c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

     Make sure to include the following:

     Product L1: DesignWare Cores

     Product L2: PCI Express

  d. After creating the case, attach any debug files you created.

     For more information about general usage information, refer to the following article in SolvNetPlus:

     https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
  - Attach any debug files you created.
- Or, telephone your local support center:
  - North America:

    Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.

- All other countries:
  https://www.synopsys.com/support/global-support-centers.html

9

Release Notes: 5.60a

These release notes describe the changes in this release *(5.60a)* relative to the previous production release *(5.50a)*. This release note contains the following sections:

- "Product Updates" on page 258
- "Changes to I/O" on page 261
- "Changes to Software View (Register Map)" on page 262
- "Changes to RAM Sizes" on page 278
- "Changes to Configuration Parameters" on page 279
- "Converting to the Current Release" on page 281
- "Known Issues and Limitations" on page 282
- "Details of Fixed Defects and Enhancements" on page 284
- "Customer Support" on page 285

9.1 Product Updates

This release contains the following major updates and other minor updates (indicated in "Details of Fixed Defects and Enhancements" on page 284).

9.1.1 Multistream Transmission

The Multistream transmission provides multiple independent transmit interfaces. Each interface is capable of accepting traffic for transmission regardless of the state of other interface. To enable MultiStream transmission set the parameter `CX_MULTISTREAM` to '1'.

For more information on Multistream Transmission, see *"Transmit TLP Processing"* section in *"Controller Operations"* chapter of the *Databook*. For example transactions, see *"Transmit Interfaces (XALI0/1/2)"* section in the *"Signal Interfaces"* chapter of the *Databook*.

9.1.2 Native PCIe Enclosure Management (NPEM)

The controller supports Native PCIe Enclosure Management (NPEM) feature as defined in the *PCI Express Base Specification, Revision 5.0, Version 1.0*. To enable this feature set the parameter `NPEM_ENABLE` to '1'. For more information on NPEM, see *"Native PCIe Enclosure Management (NPEM)"* section in the *"Controller Operations"* chapter of the *Databook*.

9.1.3 Enhanced Precision Time Management

Enhanced Precision Time Management (ePTM) is supported for all modes of the controller. An ePTM capable bit is added to the PTM capability register. The PTM requester invalidates PTM context on detection of replay and duplicate TLPs. The PTM responder invalidates historical timestamps (t3-t2) on detection of replay and duplicate TLPs.

For more information, see *"Precision Time Management"* section in the *"Controller Operations"* chapter of the *Databook*.

9.1.4 SR-IOV without MSIX

As per *PCI Express Base Specification, Revision 5.0, Version 1.0* when SR-IOV is enabled, either MSI or MSI-X capability must be enabled.

Prior to this release, the controller allowed only MSIX capability to be enabled for SR-IOV configurations (`CC_DEVICE_TYPE =0 or 2 && CX_SRIOV_ENABLE =1`). In this release, the controller is enhanced to remove this restriction. The controller now allows MSI-X capability to be turned-off for SR-IOV configurations.

For more information on SR-IOV, see *"Single Root I/O Virtualization"* section in the *"Controller Operations"* chapter of the *Databook*.

9.1.5 Synthesis Constraint Improvements

Virtual clocks are added to the synthesis constraints. Each physical clock is assigned a corresponding equivalent virtual clock. This allows a more accurate measurement of the timing paths without the need to factor in additional clock tree timing logic.

For more information, see *"Synthesis Troubleshooting Guide"* Appendix of the *User Guide*.

The synthesis constraints applied to the design follows a specific CDC Methodology. Adding timing exceptions, overrides the default flop-to-flop timing paths that are defined for each individual clock domain. **set_max_delay** can be set according to the specific CDC type.

For more information, see *"Clock Domain Crossing Methodology"* Appendix of the *User Guide*.

9.1.6 Lane Turn off in SerDes PIPE Architecture

For SerDes PIPE architecture, lane turn off functionality is available when the parameter `CX_SERDES_ARCH_LANES_TURNOFF` is set to '1'.This feature is Synopsys defined and provides the same functionality as lane 'turn off' method described in *PIPE Specification for PCI Express Version 5.1.1*.

For more information on lane turn off, see *SerDes Architecture* in *"PIPE Interface"* section of the *"Signal Interfaces"* chapter of the *Databook*.

9.1.7 PCLK as PHY Input

The controller supports PCLK as PHY input for PIPE 5.0 and above according to the *PIPE Specification 5.1.1*. In PCLK as PHY input, the clock reset module generates PCLK based on MAXPCLK provided by the PHY, and drives it to the PHY. To enable this feature set the parameter `CX_PIPE_PCLK_MODE` to a value greater than '0'.

For more information, see *"Reference Clock Removal"* section of the *Architecture* chapter and *"L1 Substrates"* topic in the *"Power Management"* section of the *"Controller Operations"* chapter of the *Databook*.

9.1.8 Downstream Port Containment (DPC)

The controller supports DPC Extended Capability feature as defined in the *PCI Express Base Specification, Revision 5.0, Version 1.0*. To enable this feature set the parameter `CX_DPC_ENABLE` to '1'. For more information on DPC, see *"Downstream Port Containment"* section in the *"Controller Operations"* chapter of the *Databook*.

Note: In this release, DPC is a Limited Customer Availability (LCA) feature and must not be used for tape out. Contact Synopsys support through Solvnet for an unlocking key for this feature.

Note

In this release, the following are Early Adopter (EA) features and must not be used for tape out. Contact Synopsys support through Solvnet for an unlocking key.

- PCIe for USB4
- Atomic Operations for AXI5
- 10 Bit TAG
- Linked List Descriptor Pre-fetch
- AXI Ordering DMA

9.1.9 PCIe for USB4

The PCIe controller implementation is extended to support USB4 functionality. The PCIe controller for USB4 connects to USB4 PCIe UP/DN adapter through an enhanced PIPE interface. To enable this feature set the parameter `CX_PCIE_MODE` to '3'.

For more information, see *"PCIe for USB4"* chapter of the *Databook*.

9.1.10 Atomic Operations for AXI5

The controller now supports PCIe AtomicOps transactions for AMBA AXI5 configuration, in addition to the native PCIe controller configuration. For AMBA AXI5 configurations (`AMBA_INTERFACE =AXI5`), the AXI bridge module seamlessly transports the PCIe AtomicOp transactions to the AXI interconnect, and vice-versa when AtomicOps is enabled (`CX_ATOMIC_ENABLE =1`).

For more information on AtomicOps support for AXI5 configuration, see *"Atomic Operations"* section in the *"Controller Operations"* chapter of the *Databook*.

9.1.11 10-Bit Tag

The controller is now enhanced to support up to 768 Tags on the transmit path and 1024 Tags on the receive path when AXI bridge is enabled. However, the number of tags remains limited to 256 in the transmit and receive path if the embedded DMA controller and/or the Distributed Translation Interface Master is enabled.

9.1.12 Linked List Descriptor Pre-fetch

The DMA is now enhanced to pre-fetch DMA linked list descriptors to improve DMA data throughput. For more information, see `DMA_LLP_*` registers in the *Register Descriptions*.

9.1.13 AXI Ordering DMA

In earlier releases, the write channel used an unique AXI ID (per channel) for all DMA non-posted requests sent to the AXI master.

From 5.60a release onwards, the write channel uses random AXI ID (per channel) for all DMA non-posted requests sent to the AXI master. The AXI bridge maintains the order of CPLs returned to DMA within each channel.

For more information, see *"DMA Ordering"* topic in the *"Advanced DMA Information and Operation"* section in the *"Legacy DMA Controller"* chapter of the *Databook*.

9.2 Changes to I/O

This section details any changes to the I/O of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the I/O are indicated in the change-tracked version of the *Databook* PDF which can be found at the location identified in the *Databook* revision history.

The following I/O changes have occurred for all configurations:

Table 9-1 I/O Signals Added, Removed, or Renamed

Name	Type	Change	Comment
No I/O changes has occurred for all configurations in this release.			

Documentation Changes

A number of signals were incorrectly described in the *Databook*. These are also highlighted in the change-tracked version of the *Databook*. These are *not* RTL changes.

The following I/O changes have occurred for all configurations:

Table 9-2 Documentation Changes (Non-RTL)

Name	Type	Change	Comment
For many signals **Synchronous To** is corrected. These corrections are indicated in the change-tracked version of the Databook PDF which can be found at the location identified in the Databook revision history.			

9.3 Changes to Software View (Register Map)

This section discusses changes to the register map of the controller that have occurred in this release.

- It lists renamed registers.
- It lists deleted registers.
- It does *not* list new registers.
- *All* changes to the software map are indicated in the change-tracked version of the *Register Descriptions* PDF which can be found at the location identified in the *Register Descriptions* revision history.

The following changes have occurred for all configurations.

Table 9-3 Register Deletions/Renaming

Register	Field	Nature of Change
VF_UNCORR_ERR_MASK_OFF	PSND_TLP_EGRSS_BLOCKED_ERR_MASK	Removed

Documentation Changes

A number of registers were incorrectly described in the IP-XACT XML, DocBook XML, RAL files, header files, and *Databook*. These are also highlighted in the change-tracked version of the *Register Descriptions* PDF. These are *not* RTL changes.

Table 9-4 Documentation Changes (Non-RTL)

Register	Field	Nature of Change
ESM_LN_EQ_CNTL_20G_0_OFF	ESM_DSP_TX_PRESET_20G_[0-3]	**Memory Access** corrected **Testable** corrected
	ESM_USP_TX_PRESET_20G_[0-3]	**Memory Access** corrected
ESM_LN_EQ_CNTL_20G_12_OFF	ESM_DSP_TX_PRESET_20G_[12-15]	**Memory Access** corrected **Testable** corrected
	ESM_USP_TX_PRESET_20G_[12-15]	**Memory Access** corrected

Register	Field	Nature of Change
ESM_LN_EQ_CNTL_20G_4_OFF	ESM_DSP_TX_PRESET_20G_[4-7]	**Memory Access** corrected **Testable** corrected
	ESM_USP_TX_PRESET_20G_[4-7]	**Memory Access** corrected
ESM_LN_EQ_CNTL_20G_8_OFF	ESM_DSP_TX_PRESET_20G_[8-11]	**Memory Access** corrected **Testable** corrected
	ESM_USP_TX_PRESET_20G_[8-11]	**Memory Access** corrected
ESM_LN_EQ_CNTL_25G_0_OFF	ESM_DSP_TX_PRESET_25G_[0-3]	**Memory Access** corrected **Testable** corrected
	ESM_USP_TX_PRESET_25G_[0-3]	**Memory Access** corrected
ESM_LN_EQ_CNTL_25G_4_OFF	ESM_DSP_TX_PRESET_25G_[4-7]	**Memory Access** corrected **Testable** corrected
	ESM_USP_TX_PRESET_25G_[4-7]	**Memory Access** corrected

Register	Field	Nature of Change
ESM_LN_EQ_CNTL_25G_12_OFF	ESM_DSP_TX_PRESET_25G_[12-15]	**Memory Access** corrected **Testable** corrected
	ESM_USP_TX_PRESET_25G_[12-15]	**Memory Access** corrected
ESM_LN_EQ_CNTL_25G_8_OFF	ESM_DSP_TX_PRESET_25G_[8-11]	**Memory Access** corrected **Testable** corrected
	ESM_USP_TX_PRESET_25G_[8-11]	**Memory Access** corrected
MSI_CAP_OFF_08H_REG	PCI_MSI_CAP_OFF_[08|0A]H	**Memory Access** corrected
PL16G_CAP_OFF_20H_REG	DSP_16G_TX_PRESET[0-3]	**Memory Access** corrected **Testable** corrected
	USP_16G_TX_PRESET[0-3]	**Memory Access** corrected
PL16G_CAP_OFF_24H_REG	DSP_16G_TX_PRESET[4-7]	**Memory Access** corrected **Testable** corrected
	USP_16G_TX_PRESET[4-7]	**Memory Access** corrected

Register	Field	Nature of Change
PL16G_CAP_OFF_28H_REG	DSP_16G_TX_PRESET[8-11]	**Memory Access** corrected **Testable** corrected
	USP_16G_TX_PRESET[8-11]	**Memory Access** corrected
PL16G_CAP_OFF_2CH_REG	DSP_16G_TX_PRESET[12-15]	**Memory Access** corrected **Testable** corrected
	USP_16G_TX_PRESET[12-15]	**Memory Access** corrected
PTM_REQ_SCALED_CLOCK_T_OFF	PTM_REQ_SCALED_CLOCK_T_[FRAC|INT]	**Testable** corrected
RESBAR_CAP_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_128[GB | MB | TB]	**Memory Access** corrected
RESBAR_CAP_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_16[GB | MB | TB]	**Memory Access** corrected
RESBAR_CAP_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_1[GB | MB | TB]	**Memory Access** corrected
RESBAR_CAP_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_256[GB | MB]	**Memory Access** corrected
RESBAR_CAP_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_2[GB | MB | TB]	**Memory Access** corrected
RESBAR_CAP_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_32[GB | MB | TB]	**Memory Access** corrected
RESBAR_CAP_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_4[GB | MB | TB]	**Memory Access** corrected
RESBAR_CAP_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_512[GB | MB]	**Memory Access** corrected
RESBAR_CAP_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_64[GB | MB | TB]	**Memory Access** corrected

Register	Field	Nature of Change
RESBAR_CAP_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_8[GB | MB | TB]	**Memory Access** corrected
RESBAR_CTRL_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_[128 | 16 | 1 | 2 | 256 | 32 | 4 | 512 | 64 | 8]PB	**Memory Access** corrected
RESBAR_CTRL_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_[1 | 2 | 4 | 8]EB	**Memory Access** corrected
RESBAR_CTRL_REG_[0-5]_REG	RESBAR_CAP_REG_[0-5]_[256 | 512]TB	**Memory Access** corrected
SPCIE_CAP_OFF_0CH_REG	DSP_RX_PRESET_HINT[0-1] DSP_TX_PRESET[0-1]	**Memory Access** corrected
	USP_RX_PRESET_HINT[0-1] USP_TX_PRESET[0-1]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_10H_REG	DSP_RX_PRESET_HINT[2-3] DSP_TX_PRESET[2-3]	**Memory Access** corrected
	USP_RX_PRESET_HINT[2-3] USP_TX_PRESET[2-3]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_14H_REG	DSP_RX_PRESET_HINT[4-5] DSP_TX_PRESET[4-5]	**Memory Access** corrected
	USP_RX_PRESET_HINT[4-5] USP_TX_PRESET[4-5]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_18H_REG	DSP_RX_PRESET_HINT[6-7] DSP_TX_PRESET[6-7]	**Memory Access** corrected
	USP_RX_PRESET_HINT[6-7] USP_TX_PRESET[6-7]	**Memory Access** corrected **Testable** corrected

Register	Field	Nature of Change
SPCIE_CAP_OFF_1CH_REG	DSP_RX_PRESET_HINT[8-9] DSP_TX_PRESET[8-9]	**Memory Access** corrected
	USP_RX_PRESET_HINT[8-9] USP_TX_PRESET[8-9]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_20H_REG	DSP_RX_PRESET_HINT[10-11] DSP_TX_PRESET[10-11]	**Memory Access** corrected
	USP_RX_PRESET_HINT[10-11] USP_TX_PRESET[10-11]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_24H_REG	DSP_RX_PRESET_HINT[12-13] DSP_TX_PRESET[12-13]	**Memory Access** corrected
	USP_RX_PRESET_HINT[12-13] USP_TX_PRESET[12-13]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_28H_REG	DSP_RX_PRESET_HINT[14-15] DSP_TX_PRESET[14-15]	**Memory Access** corrected
	USP_RX_PRESET_HINT[14-15] USP_TX_PRESET[14-15]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_2CH_REG	DSP_16G_RX_PRESET_HINT[0-1] DSP_16G_TX_PRESET[0-1]	**Memory Access** corrected
	USP_16G_RX_PRESET_HINT[0-1] USP_16G_TX_PRESET[0-1]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_30H_REG	DSP_16G_RX_PRESET_HINT[2-3] DSP_16G_TX_PRESET[2-3]	**Memory Access** corrected
	USP_16G_RX_PRESET_HINT[2-3] USP_16G_TX_PRESET[2-3]	**Memory Access** corrected **Testable** corrected

Register	Field	Nature of Change
SPCIE_CAP_OFF_34H_REG	DSP_16G_RX_PRESET_HINT[4-5] DSP_16G_TX_PRESET[4-5]	**Memory Access** corrected
	USP_16G_RX_PRESET_HINT[4-5] USP_16G_TX_PRESET[4-5]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_38H_REG	DSP_16G_RX_PRESET_HINT[6-7] DSP_16G_TX_PRESET[6-7]	**Memory Access** corrected
	USP_16G_RX_PRESET_HINT[6-7] USP_16G_TX_PRESET[6-7]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_3CH_REG	DSP_16G_RX_PRESET_HINT[8-9] DSP_16G_TX_PRESET[8-9]	**Memory Access** corrected
	USP_16G_RX_PRESET_HINT[8-9] USP_16G_TX_PRESET[8-9]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_40H_REG	DSP_16G_RX_PRESET_HINT[10-11] DSP_16G_TX_PRESET[10-11]	**Memory Access** corrected
	USP_16G_RX_PRESET_HINT[10-11] USP_16G_TX_PRESET[10-11]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_44H_REG	DSP_16G_RX_PRESET_HINT[12-13] DSP_16G_TX_PRESET[12-13]	**Memory Access** corrected
	USP_16G_RX_PRESET_HINT[12-13] USP_16G_TX_PRESET[12-13]	**Memory Access** corrected **Testable** corrected
SPCIE_CAP_OFF_48H_REG	DSP_16G_RX_PRESET_HINT[14-15] DSP_16G_TX_PRESET[14-15]	**Memory Access** corrected
	USP_16G_RX_PRESET_HINT[14-15] USP_16G_TX_PRESET[14-15]	**Memory Access** corrected **Testable** corrected

Register	Field	Nature of Change
TPH_ST_TABLE_REG_0	TPH_REQ_ST_TABLE_LOWER_[0-1]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[0-1]	Field made visible
TPH_ST_TABLE_REG_1	TPH_REQ_ST_TABLE_LOWER_[2-3]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[2-3]	Field made visible
TPH_ST_TABLE_REG_10	TPH_REQ_ST_TABLE_LOWER_[20-21]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[20-21]	Field made visible
TPH_ST_TABLE_REG_11	TPH_REQ_ST_TABLE_LOWER_[22-23]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[22-23]	Field made visible
TPH_ST_TABLE_REG_12	TPH_REQ_ST_TABLE_LOWER_[24-25]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[24-25]	Field made visible
TPH_ST_TABLE_REG_13	TPH_REQ_ST_TABLE_LOWER_[26-27]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[26-27]	Field made visible
TPH_ST_TABLE_REG_14	TPH_REQ_ST_TABLE_LOWER_[28-29]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[28-29]	Field made visible
TPH_ST_TABLE_REG_15	TPH_REQ_ST_TABLE_LOWER_[30-31]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[30-31]	Field made visible

Register	Field	Nature of Change
TPH_ST_TABLE_REG_16	TPH_REQ_ST_TABLE_LOWER_[32-33]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[32-33]	Field made visible
TPH_ST_TABLE_REG_17	TPH_REQ_ST_TABLE_LOWER_[34-35]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[34-35]	Field made visible
TPH_ST_TABLE_REG_18	TPH_REQ_ST_TABLE_LOWER_[36-37]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[36-37]	Field made visible
TPH_ST_TABLE_REG_19	TPH_REQ_ST_TABLE_LOWER_[38-39]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[38-39]	Field made visible
TPH_ST_TABLE_REG_2	TPH_REQ_ST_TABLE_LOWER_[4-5]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[4-5]	Field made visible
TPH_ST_TABLE_REG_20	TPH_REQ_ST_TABLE_LOWER_[40-41]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[40-41]	Field made visible
TPH_ST_TABLE_REG_21	TPH_REQ_ST_TABLE_LOWER_[42-43]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[42-43]	Field made visible
TPH_ST_TABLE_REG_22	TPH_REQ_ST_TABLE_LOWER_[44-45]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[44-45]	Field made visible

Register	Field	Nature of Change
TPH_ST_TABLE_REG_23	TPH_REQ_ST_TABLE_LOWER_[46-47]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[46-47]	Field made visible
TPH_ST_TABLE_REG_24	TPH_REQ_ST_TABLE_LOWER_[48-49]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[48-49]	Field made visible
TPH_ST_TABLE_REG_25	TPH_REQ_ST_TABLE_LOWER_[50-51]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[50-51]	Field made visible
TPH_ST_TABLE_REG_26	TPH_REQ_ST_TABLE_LOWER_[52-53]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[52-53]	Field made visible
TPH_ST_TABLE_REG_27	TPH_REQ_ST_TABLE_LOWER_[54-55]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[54-55]	Field made visible
TPH_ST_TABLE_REG_28	TPH_REQ_ST_TABLE_LOWER_[56-57]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[56-57]	Field made visible
TPH_ST_TABLE_REG_29	TPH_REQ_ST_TABLE_LOWER_[58-59]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[58-59]	Field made visible
TPH_ST_TABLE_REG_3	TPH_REQ_ST_TABLE_LOWER_[6-7]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[6-7]	Field made visible

Register	Field	Nature of Change
TPH_ST_TABLE_REG_30	TPH_REQ_ST_TABLE_LOWER_[60-61]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[60-61]	Field made visible
TPH_ST_TABLE_REG_31	TPH_REQ_ST_TABLE_LOWER_[62-63]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[62-63]	Field made visible
TPH_ST_TABLE_REG_4	TPH_REQ_ST_TABLE_LOWER_[8-9]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[8-9]	Field made visible
TPH_ST_TABLE_REG_5	TPH_REQ_ST_TABLE_LOWER_[10-11]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[10-11]	Field made visible
TPH_ST_TABLE_REG_6	TPH_REQ_ST_TABLE_LOWER_[12-13]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[12-13]	Field made visible
TPH_ST_TABLE_REG_7	TPH_REQ_ST_TABLE_LOWER_[14-15]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[14-15]	Field made visible
TPH_ST_TABLE_REG_8	TPH_REQ_ST_TABLE_LOWER_[16-17]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[16-17]	Field made visible
TPH_ST_TABLE_REG_9	TPH_REQ_ST_TABLE_LOWER_[18-19]	**Memory Access** corrected Field made visible
	TPH_REQ_ST_TABLE_HIGHER_[18-19]	Field made visible
UNCORR_ERR_MASK_OFF	ACS_VIOLATION_MASK	Field made visible
UNCORR_ERR_SEV_OFF	ATOMIC_EGRESS_BLOCKED_ERR_SEVERITY	Field made visible

Register	Field	Nature of Change
VF_MSI_CAP_OFF_08H_REG	PCI_MSI_CAP_OFF_[08|0A]H	**Memory Access** corrected
VF_MSIX_PBA_OFFSET_REG	PCI_MSIX_PBA_[BIR | OFFSET]	**Testable** corrected
VF_PCI_MSIX_CAP_ID_NEXT_CTRL_REG	PCI_MSIX_FUNCTION_MASK	**Memory Access** corrected
VF_RESBAR_CAP_REG_[0-5]_REG	VF_RESBAR_CAP_REG_[0-5]_128[GB | MB | TB]	**Memory Access** corrected
VF_RESBAR_CAP_REG_[0-5]_REG	VF_RESBAR_CAP_REG_[0-5]_16[GB | MB | TB]	**Memory Access** corrected
VF_RESBAR_CAP_REG_[0-5]_REG	VF_RESBAR_CAP_REG_[0-5]_1[GB | MB | TB]	**Memory Access** corrected
VF_RESBAR_CAP_REG_[0-5]_REG	VF_RESBAR_CAP_REG_[0-5]_256[GB | MB]	**Memory Access** corrected
VF_RESBAR_CAP_REG_[0-5]_REG	VF_RESBAR_CAP_REG_[0-5]_2[GB | MB | TB]	**Memory Access** corrected
VF_RESBAR_CAP_REG_[0-5]_REG	VF_RESBAR_CAP_REG_[0-5]_32[GB | MB | TB]	**Memory Access** corrected
VF_RESBAR_CAP_REG_[0-5]_REG	VF_RESBAR_CAP_REG_[0-5]_4[GB | MB | TB]	**Memory Access** corrected
VF_RESBAR_CAP_REG_[0-5]_REG	VF_RESBAR_CAP_REG_[0-5]_512[GB | MB]	**Memory Access** corrected
VF_RESBAR_CAP_REG_[0-5]_REG	VF_RESBAR_CAP_REG_[0-5]_64[GB | MB | TB]	**Memory Access** corrected
VF_RESBAR_CAP_REG_[0-5]_REG	VF_RESBAR_CAP_REG_[0-5]_8[GB | MB | TB]	**Memory Access** corrected
VF_RESBAR_CTRL_REG_[0-5]_REG	VF_RESBAR_CTRL_REG_[0-5]_[1 | 128 | 16 | 256 | 2 | 32 | 4 | 512 | 64 | 8]PB	**Memory Access** corrected
VF_RESBAR_CTRL_REG_[0-5]_REG	VF_RESBAR_CTRL_REG_[0-5]_[256 | 512]EB	**Memory Access** corrected
VF_RESBAR_CTRL_REG_[0-5]_REG	VF_RESBAR_CTRL_REG_[0-5]_[1 | 2 | 4 | 8]EB	**Memory Access** corrected

Register	Field	Nature of Change
VF_TPH_ST_TABLE_REG_0	TPH_REQ_ST_TABLE_LOWER_[0-1]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[0-1]	Field is visible
VF_TPH_ST_TABLE_REG_1	TPH_REQ_ST_TABLE_LOWER_[2-3]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[2-3]	Field is visible
VF_TPH_ST_TABLE_REG_10	TPH_REQ_ST_TABLE_LOWER_[20-21]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[20-21]	Field is visible
VF_TPH_ST_TABLE_REG_11	TPH_REQ_ST_TABLE_LOWER_[22-23]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[22-23]	Field is visible
VF_TPH_ST_TABLE_REG_12	TPH_REQ_ST_TABLE_LOWER_[24-25]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[24-25]	Field is visible
VF_TPH_ST_TABLE_REG_13	TPH_REQ_ST_TABLE_LOWER_[26-27]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[26-27]	Field is visible
VF_TPH_ST_TABLE_REG_14	TPH_REQ_ST_TABLE_LOWER_[28-29]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[28-29]	Field is visible
VF_TPH_ST_TABLE_REG_15	TPH_REQ_ST_TABLE_LOWER_[30-31]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[30-31]	Field is visible

Register	Field	Nature of Change
VF_TPH_ST_TABLE_REG_16	TPH_REQ_ST_TABLE_LOWER_[32-33]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[32-33]	Field is visible
VF_TPH_ST_TABLE_REG_17	TPH_REQ_ST_TABLE_LOWER_[34-35]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[34-35]	Field is visible
VF_TPH_ST_TABLE_REG_18	TPH_REQ_ST_TABLE_LOWER_[36-37]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[36-37]	Field is visible
VF_TPH_ST_TABLE_REG_19	TPH_REQ_ST_TABLE_LOWER_[38-39]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[38-39]	Field is visible
VF_TPH_ST_TABLE_REG_2	TPH_REQ_ST_TABLE_LOWER_[4-5]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[4-5]	Field is visible
VF_TPH_ST_TABLE_REG_20	TPH_REQ_ST_TABLE_LOWER_[40-41]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[40-41]	Field is visible
VF_TPH_ST_TABLE_REG_21	TPH_REQ_ST_TABLE_LOWER_[42-43]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[42-43]	Field is visible
VF_TPH_ST_TABLE_REG_22	TPH_REQ_ST_TABLE_LOWER_[44-45]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[44-45]	Field is visible

Register	Field	Nature of Change
VF_TPH_ST_TABLE_REG_23	TPH_REQ_ST_TABLE_LOWER_[46-47]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[46-47]	Field is visible
VF_TPH_ST_TABLE_REG_24	TPH_REQ_ST_TABLE_LOWER_[48-49]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[48-49]	Field is visible
VF_TPH_ST_TABLE_REG_25	TPH_REQ_ST_TABLE_LOWER_[50-51]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[50-51]	Field is visible
VF_TPH_ST_TABLE_REG_26	TPH_REQ_ST_TABLE_LOWER_[52-53]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[52-53]	Field is visible
VF_TPH_ST_TABLE_REG_27	TPH_REQ_ST_TABLE_LOWER_[54-55]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[54-55]	Field is visible
VF_TPH_ST_TABLE_REG_28	TPH_REQ_ST_TABLE_LOWER_[56-57]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[56-57]	Field is visible
VF_TPH_ST_TABLE_REG_29	TPH_REQ_ST_TABLE_LOWER_[58-59]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[58-59]	Field is visible
VF_TPH_ST_TABLE_REG_3	TPH_REQ_ST_TABLE_LOWER_[6-7]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[6-7]	Field is visible

Register	Field	Nature of Change
VF_TPH_ST_TABLE_REG_30	TPH_REQ_ST_TABLE_LOWER_[60-61]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[60-61]	Field is visible
VF_TPH_ST_TABLE_REG_31	TPH_REQ_ST_TABLE_LOWER_[62-63]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[62-63]	Field is visible
VF_TPH_ST_TABLE_REG_4	TPH_REQ_ST_TABLE_LOWER_[8-9]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[8-9]	Field is visible
VF_TPH_ST_TABLE_REG_5	TPH_REQ_ST_TABLE_LOWER_[10-11]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[10-11]	Field is visible
VF_TPH_ST_TABLE_REG_6	TPH_REQ_ST_TABLE_LOWER_[12-13]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[12-13]	Field is visible
VF_TPH_ST_TABLE_REG_7	TPH_REQ_ST_TABLE_LOWER_[14-15]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[14-15]	Field is visible
VF_TPH_ST_TABLE_REG_8	TPH_REQ_ST_TABLE_LOWER_[16-17]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[16-17]	Field is visible
VF_TPH_ST_TABLE_REG_9	TPH_REQ_ST_TABLE_LOWER_[18-19]	**Memory Access** corrected Field is visible
	TPH_REQ_ST_TABLE_HIGHER_[18-19]	Field is visible
VF_UNCORR_ERR_MASK_OFF	ACS_VIOLATION_MASK	Field is visible
VF_UNCORR_ERR_SEV_OFF	ATOMIC_EGRESS_BLOCKED_ERR_SEVERITY	Field is visible

9.4 Changes to RAM Sizes

This section details the changes to the default RAM sizes that have occurred since the last production release. It does not detail changes that are associated with new or additional features that you enable on your current configuration

Caution To determine the precise changes to RAM sizes for your actual controller configuration, you can compare the coreConsultant generated RAM sizes for the previous and current releases. For more details, see the “RAM Requirements” section in the Architecture chapter of the *Databook*.

No changes have occurred for this release.

9.5 Changes to Configuration Parameters

This section details any changes to the configuration parameters of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the configuration parameters are indicated in the change-tracked version of the *Databook* PDF which can be found at the location identified in the *Databook* revision history.

If you intend to source an existing configuration batch file, then you must first convert your configuration file, as described in "Product Updates" on page 258. If you are not sourcing an existing configuration batch file, then you should be still aware of changes to the default value of some configuration parameters.

Caution To ensure that your existing configuration absorbs all changes to default parameters that the PCIe R&D team makes, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.
Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

Table 9-5 Configuration Parameter Changes

Name	Change
Transmit MAC Layer (XML) Precoding Output	**Default Value:** changed **from:** CX_TECHNOLOGY == 0)) ? 0 : 0 **to:** ((SNPS_RSVDPARAM_37 == 1) ? 1 : ((CX_TECHNOLOGY == 0)) ? 0: 0
CLIENT2_POPULATED	**Default Value:** changed from: AXI_POPULATED ? 1 : (CX_XADM_CLI_INTF_DEDICATED? 1: 0) to:
MSIX_CAP_ENABLE	**Default Value:** changed **from:** false **to:** CX_SRIOV_ENABLE ? 1 : 0
VF_MSIX_PBA_OFFSET_n	**Default Value:** changed **from:** 0x0 **to:** VF_MSIX_PBA_OFFSET_0_BASELINE >> 3) + ((VF_MSIX_PBA_OFFSET_0_BASELINE & 0b111) != 0
MSIX_PBA_OFFSET_n	**Default Value:** changed **from:** 0x0 **to:** MSIX_PBA_OFFSET_0_BASELINE >> 3) +((MSIX_PBA_OFFSET_0_BASELINE & 0b111) != 0
EXT_VF_MSIX_CAP_ENABLE	**Default Value:** changed **from:** CX_SRIOV_ENABLE && CX_EXTENSIBLE_VFUNC **to:** CX_EXTENSIBLE_VFUNC

Name	Change
CX_XMLH_PRECODING_REGOUT	**Default Value:** changed **from:** (SNPS_RSVDPARAM_37 == 1) ? 1 : ((CX_TECHNOLOGY == 0)) ? 0 : 0 **to:** (CX_TECHNOLOGY == 0) ? 0: 0
CX_GEN4_SPEC07	Parameter Invisible Mandatory Parameter for Gen4 devices.
CX_GEN4_SPEC07_RM	Parameter Invisible Mandatory Parameter for Gen4 devices.

9.6 Converting to the Current Release

Sometimes a new controller release might no longer use a certain configuration parameter, or the meaning of that parameter might have changed. The following process helps you convert your current configuration file so that it creates the same RTL with the new controller.

1. Open coreConsultant and create an unconfigured workspace from the newly installed controller.
2. In the coreConsultant command line, enter the following command:

   `parse_configfile my_configfile.config`

   where `my_configfile.config` is your current configuration file. This command creates an updated configuration file in your working directory as follows:

   `my_configfile.config.new`
3. In the coreConsultant command line, enter the following command:

   `source my_configfile.config.new`
4. Select Apply to generate the new RTL with the updated or translated parameters.
5. From the File Menu, select Write Batch Script and save the configuration file for the new release.
6. When you source the updated configuration file in coreConsultant, you can *ignore any new warnings* about parameter settings that are not relevant to, or not enabled in your configuration.

Attention

Writing Out Your Configuration File

To ensure that your existing configuration absorbs all changes to default parameters that the PCIe R&D team makes, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File->Write Batch Script* menu item.

You must convert your configuration file. Failure to do so, can result in:

- Your configuration file being incompatible with the current release.
- Functional, architectural, RAM, and I/O changes when the default of some configuration parameters change from release to release.

9.7 Known Issues and Limitations

You can view a complete list of functional problem reports for this product, including problems identified after product release, by accessing the STAR report on the Web. For more details, see "Details of Fixed Defects and Enhancements" on page 284. You must have a SolvNet ID to view STAR reports. This release has the following known tool and packaging issues at the time of release.

- "Packaged coreConsultant Test Limitations"
- "VTB Limitations"
- "Design Example"
- "Unique Case Violation Simulation Message"
- "coreConsultant Memory Map Limitations"

9.7.1 Packaged coreConsultant Test Limitations

We invite you to submit your coreConsultant configuration, so that Synopsys can run the full range of testing on your configuration. Because of the very large configuration space, it is not possible to regress every configuration before a release is made. Synopsys is continually running fixed and randomized configurations, but it is possible that your exact configuration has not been regressed. Test case failures might occur because of improper test bench configuration. In that case open a case through SolvNet.

9.7.2 VTB Limitations

The following limitations apply to the current release of the VTB:

- Not backward compatible with previous releases
- Not UVM compliant
- No support for big-endian (`AHB_ENDIANNESS`) configurations

9.7.3 Design Example

The design example in `<workspace>/examples/DWC_pcie_clkrst.v` has been functionally verified, but has not been explicitly targeted for verification metrics. However, it has been used by Synopsys in the verification and regression environments for all controller configurations; including verification of all power transitions for the controller.

9.7.3.1 Unique Case Violation Simulation Message

The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

There is a known simulator issue with a "Unique case violation" message that occurs sometimes while running simulations with VCS outside of coreConsultant. You can ignore these messages.

To avoid these messages, use the `-xlrm uniq_prior_final` compile option in VCS. The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

9.7.3.2 coreConsultant Memory Map Limitations

The controller supports the generation of configuration-specific register maps as described in the "Register Configuration Space" chapter in the *Databook*. For SR-IOV configurations (`CX_SRIOV_ENABLE =1`), the following limitations apply.

Table 9-6 Coreconsultant Report File Limitations for SR-IOV Configurations

CX_NVFUNC	IP-XACT (IP-XACT XML)	RALF and C Headers (No limitations.)	Register Report (DocBook XML). Also applies to Databook.
1 - 256	Defines default #VFs in each PF	Defines default #VFs in each PF	Defines only first VF in each PF
257 .. 4096	Defines only[a] first VF in each PF	Defines default #VFs in each PF	Defines only first VF in each PF

a. For details on how to populate remaining VFs in the IP-XACT file, see "Populating IP-XACT File Manually" in the "Creating Optional Views and Reports" section in the "Configuring the controller" chapter of the User Guide.

9.8 Details of Fixed Defects and Enhancements

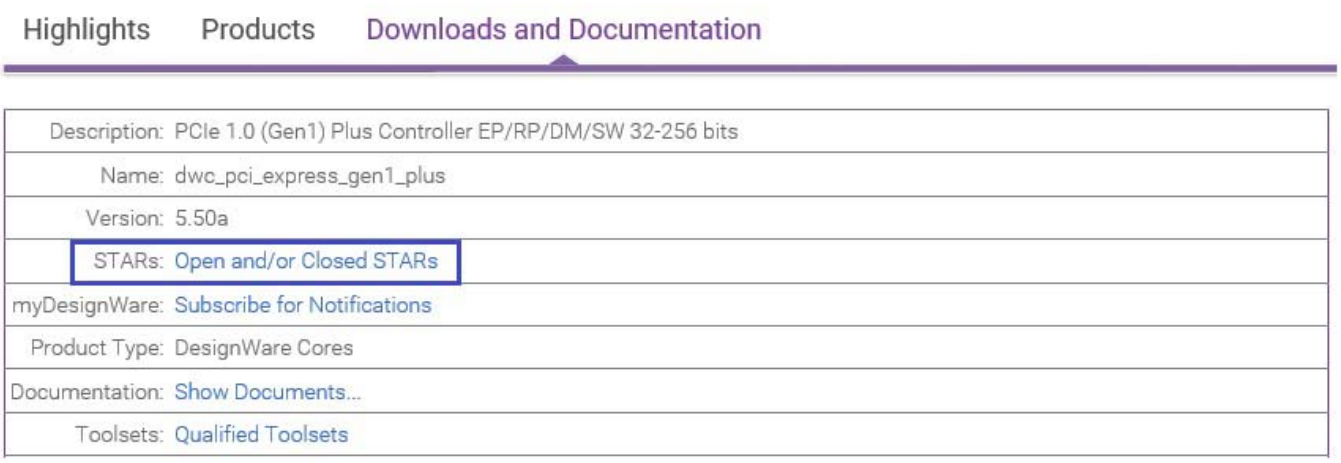
Defects fixed in release 5.60a of the DesignWare Cores PCI Express Controllerare listed in the STAR report for release 5.60a in STARs on the Web. You must have a SolvNet ID to view STAR reports as shown in Table 9-7.

http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_ep#tab2

Table 9-7 Accessing STARs on the Web through SolvNet

Controller	Web Address
DM	http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_dm#tab2
EP	http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_ep#tab2
RC	http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_rc#tab2
SW	http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_sw#tab2

Figure 9-1 Accessing STARs on the Web through SolvNet



Enhancement STARs are identifiable by the letter “E” in the Severity column, and fixed defect STARs are identifiable by the letter “B.” An E4 or B4 has the highest severity. Clicking on the tab corresponding to 5.60a produces a STAR report of closed STARS for this release. For previous controller versions, click the tab corresponding to the version in question.

9.9 Customer Support

To obtain support for your product:

- First, prepare the following debug information, if applicable:
  - For environment setup problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, use the following menu entry:

    File > Build Debug Tar-file

    Check all the boxes in the dialog box that apply to your issue. This menu entry gathers all the Synopsys product data needed to begin debugging an issue and writes it to the file `<core tool startup directory>/debug.tar.gz`.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD)
    - Identify the hierarchy path to the DesignWare instance
    - Identify the timestamp of any signals or locations in the waveforms that are not understood
- Then, contact Support Center, with a description of your question and supplying the above information, using one of the following methods:
  - *For fastest response*, use the SolvNet website. When you fill in your information as explained later, your issue is automatically routed to a support engineer who is experienced with your product. The **Sub Product 1** entry is critical for correct routing.

    Go to http://solvnet.synopsys.com/EnterACalland click on the link to enter a call. Provide the requested information, including:
    - **Customer Tracking Number:** Enter your project name. Use the same name for cases related to the same project.
    - **Product:** DesignWare Cores
    - **Sub Product 1:** PCI Express
    - **Product Version:** 5.60a (for example)
    - **Problem Type:**
    - **Issue Severity:**
    - **Problem Title:** Provide a brief summary of the issue or list the error message you have encountered
    - **Problem Description:** For simulation issues, include the hierarchy path to the DesignWare instance and the timestamp of any signals or locations in waveforms that are not understood.

      After creating the case, attach any debug files you created in the previous step.
  - Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
    - Include the Product name, Sub Product name and Tool Version number in your e-mail (as identified above) so it can be routed correctly.
    - For simulation issues, include the hierarchy path to the DesignWare instance and the timestamp of any signals in waveforms for reference
    - Attach any debug files you created in the previous step.
  - Or, telephone your local support center:

- North America: Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
- All other countries: https://www.synopsys.com/support/global-support-centers.html

Release Notes: 5.50a

These release notes describe the changes in this release `(5.50a)` relative to the previous production release `(5.50a)`. This is the `5.50a` early adopter (EA) release of the PCI Express core. This release note contains the following sections:

- "Product Updates" on page 288
- "Changes to I/O" on page 291
- "Changes to Software View (Register Map)" on page 292
- "Changes to RAM Sizes" on page 314
- "Changes to Configuration Parameters" on page 315
- "Converting to the Current Release" on page 318
- "Known Issues and Limitations" on page 319
- "Details of Fixed Defects and Enhancements" on page 321
- "Customer Support" on page 322

10.1 Product Updates

This release contains the following major updates and other minor updates (indicated in "Details of Fixed Defects and Enhancements" on page 321).

10.1.1 Gen5 Feature

The controller now supports the *PCI Express Base Specification Revision 5.0, Version 1.0* with the following qualifications.

Table 10-1 Gen5 Specification Compliance

Feature	Description
PIPE Spec version	■ PIPE 4.4.1 + 3-bit rate signal ■ PIPE 5.1.1 - Supported for LPC Interface - Supported for SERDES IF for Gen5 4s configuration - PCLK as PHY input is available as Early Adopter[a]
Frequency and width configuration	See "*Frequency, Speed, and Width Support*" section in the "*Product Overview*" chapter of the *Databook*.
TS1/TS2 Symbol 4 bit 5 for Gen5 Data rate	Supported
EIEOS Format change - 32 0b and 32 1b	Supported
Lane Margining at Gen5 Speed	Supported
Initial Link Up sequence	Supported: Gen1 - Gen3 EQ - Gen4 EQ - Gen5 EQ - Gen5 L0 Supported: EQ bypass to highest rate Supported: Non EQ needed
Speed Change	Supported
Physical Layer 32.0GT/s Extended Capability	Supported
Compliance Pattern at Gen5 Speed	Supported
Modified TS1/TS2 Ordered Set	Supported (Disabled by default)
SKP OS encoding change for 32GT/s (AAh->99h)	Supported
Body of SDS OS encoding change for 32GT/s (55h->87h)	Supported
Increased the number of EIEOS Blocks for Gen5	Supported
LTSSM: From Loopback to Recovery.EQ and back to Loopback	Supported
Precoding	Supported
Alternate Protocol Extended Capability	Not Supported

a. Contact Synopsys support through SolvNet for an unlocking key for this feature.

10.1.2 New Controller-PHY Combinations

Table 10-2 describes the new Gen5 controller-PHY combinations added in 5.50a.

Table 10-2 Gen5 Controller-PHY Combinations Supported

		PHY	
		g1_2s g2_2s_df g3_2s_df g4_2s_df g5_4s_dw	g1_4s g2_4s_df g3_4s_df g4_4s_df g5_4s_df
CONTROLLER	g1_2s g2_2s_df g3_2s_df g4_2s_df g5_4s_dw	✓	✗
	g1_4s g2_4s_df g3_8s_dw g4_8s_df g5_8s_df	✗	✓

10.1.3 Hyper DMA (HDMA)

A new modular embedded DMA architecture (HDMA) capable of processing multiple descriptors simultaneously, is supported in this release. To enable this feature, set `CX_DMA_PF_ENABLE` (in addition to `CC_DMA_ENABLE`) configuration parameter. HDMA provides the following advantages over the legacy DMA:

- More number of channels (up to 64 read and 64 write channels)
- Programmable descriptor prefetch depth
- Multiple descriptor fetch in one clock cycle
- Full bandwidth utilization for small transfer blocks (1TLP per descriptor)
- Backward compatibility with legacy DMA
- DMA registers DBI channel separation for better SRIOV support
- DMA stop doorbell support for SRIOV
- Synthesis QoR for 1GHz or above

For more information, see "*HDMA Controller*" chapter of the *Databook*.

Note: In this release, HDMA is an Early Adopter (EA) feature and must not be used for tape out. Contact Synopsys support through SolvNet for an unlocking key for this feature.

10.1.4 PIPE 5.1.1 SerDes Architecture Support

The controller supports SerDes architecture as defined in *PIPE Specification for PCI Express, Version 5.1.1* for Gen5 4s configuration with the following features and limitations:

- 8b/10b encode/decode and error indication
- 128b/130b encode/decode and error indication
- Symbol lock
- Block alignment
- Elastic buffer (data synchronization between the recovered clock and PCLK)
  - Support Nominal Half Full Buffer mode and Nominal Empty Buffer mode
  - Support SRIS and SRNS
- Polarity
- Loopback Slave (remote digital loopback)

To enable this feature set `CX_PIPE_SERDES_ARCH =1`. A new output signal `mac_phy_serdes_arch` indicates whether SerDes architecture is enabled.

10.1.5 Expansion ROM Validation

The controller supports expansion ROM validation feature as defined in *PCI Express Base Specification, Revision 5.0, Version 1.0*. Expansion ROM validation is an optional mechanism to indicate to software the results of a hardware validation of Expansion ROM contents. For more information, see *"Expansion ROM Validation Status Signals"* in the *"Signal Descriptions"* chapter of the *Databook* and expansion ROM registers in the *"Register Descriptions"*.

10.2 Changes to I/O

This section details any changes to the I/O of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the I/O are indicated in the change-tracked version of the *Databook* PDF which can be found at the location identified in the *Databook* revision history.

The following I/O changes have occurred for all configurations:

Table 10-3 I/O Signals Added, Removed, or Renamed

Name	Type	Change	Comment
adm_adaptor_powerdown	O	Added	This signal emulates the completion of PHY functions for encapsulated end point solution.

Documentation Changes

A number of signals were incorrectly described in the *Databook*. These are also highlighted in the change-tracked version of the *Databook*. These are *not* RTL changes.

The following I/O changes have occurred for all configurations:

Table 10-4 Documentation Changes (Non-RTL)

Name	Type	Change	Comment
For many signals **Synchronous To** is corrected. These corrections are indicated in the change-tracked version of the Databook PDF which can be found at the location identified in the Databook revision history.			
pm_current_data_rate	O	Signal moved to Common PIPE Signals	This signal was in the wrong signal group
cdm_ras_des_ec_info_li	O	Signal name changed from cdm_ras_des_ec_info_i to cdm_ras_des_ec_info_li	Correction
cdm_ras_des_sd_info_li	O	Signal name changed from cdm_ras_des_sd_info_i to cdm_ras_des_sd_info_li	Correction

10.3 Changes to Software View (Register Map)

This section discusses changes to the register map of the controller that have occurred in this release.

- It lists renamed registers.
- It lists deleted registers.
- It does *not* list new registers.
- *All* changes to the software map are indicated in the change-tracked version of the *Register Descriptions* PDF which can be found at the location identified in the *Register Descriptions* revision history.

The following changes have occurred for all configurations.

Table 10-5 Register Deletions/Renaming

Register	Field	Nature of Change
No changes have occurred in this release.		

Documentation Changes

A number of registers were incorrectly described in the IP-XACT XML, DocBook XML, RAL files, header files, and *Databook*. These are also highlighted in the change-tracked version of the *Register Descriptions* PDF. These are *not* RTL changes.

Table 10-6 Documentation Changes (Non-RTL)

Register	Field	Nature of Change
ACK_LATENCY_TIMER_OFF	REPLAY_TIME_LIMIT	**Testable** corrected
	ROUND_TRIP_LATENCY_TIME_LIMIT	
AMBA_ERROR_RESPONSE_DEFAULT_OFF	AMBA_ERROR_RESPONSE_CRS	Fields made visible
	AMBA_ERROR_RESPONSE_MAP	
CAP_ID_NXT_PTR_REG	PME_SUPPORT	**Value After Reset** corrected **Testable** corrected
CON_STATUS_REG	PME_ENABLE	**Testable** corrected
	POWER_STATE	
DEVICE_CAPABILITIES_REG	PCIE_CAP_CAP_SLOT_PWR_LMT_SCALE	**Testable** corrected
	PCIE_CAP_CAP_SLOT_PWR_LMT_VALUE	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
DEVICE_CONTROL_DEVICE_STATUS	PCIE_CAP_AUX_POWER_DETECTED	**Testable** corrected
	PCIE_CAP_AUX_POWER_PM_EN	
	PCIE_CAP_EXT_TAG_EN	
	PCIE_CAP_PHANTOM_FUNC_EN	
	PCIE_CAP_TRANS_PENDING	
	PCIE_CAP_AUX_POWER_DETECTED	
DMA_CH_CONTROL1_OFF_[RD|WR]CH_0	CB	Fields made visible
	CCS	
	CS	
	DMA_AT	
	DMA_ELEMENT_PREFETCH	
	DMA_FUNC_NUM	
	DMA_MEM_TYPE	
	DMA_NS_DST	
	DMA_NS_SRC	
	DMA_RESERVED0	
	DMA_RESERVED1	
	DMA_RESERVED5	
	DMA_RO	
	DMA_TC	
	LIE	
	LLE	
	LLP	
	RIE	
	TCB	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
DMA_CH_CONTROL2_OFF_[WR|RD]CH_0	DMA_PH	Fields made visible
	DMA_RESERVED3	
	DMA_ST	
	DMA_TH	
	DMA_VF	
	DMA_VF_EN	
	DMA_VF_RESERVED	
DMA_CTRL_OFF	NUM_DMA_[RD|WR]_CHAN	Fields made visible
	RSVDP_[20|26|4]	
DMA_DAR_HIGH_OFF_[RD|WR]CH_0	DST_ADDR_REG_HIGH	Fields made visible
DMA_DAR_LOW_OFF_[RD|WR]CH_0	DST_ADDR_REG_LOW	Fields made visible
DMA_LLP_HIGH_OFF_[RD|WR]CH_0	LLP_HIGH	Fields made visible
DMA_LLP_LOW_OFF_[RD|WR]CH_0	LLP_LOW	Fields made visible
DMA_READ_ABORT_IMWR_HIGH_OFF	DMA_READ_ABORT_HIGH_REG	Fields made visible
DMA_READ_ABORT_IMWR_LOW_OFF	DMA_READ_ABORT_LOW_REG	Fields made visible
DMA_READ_CH01_IMWR_DATA_OFF	RD_CHANNEL_[0|1]_DATA	Fields made visible
DMA_READ_CH0_PWR_EN_OFF	DMA_READ_CH0_PWR_EN	Fields made visible
	RSVDP_1	
DMA_READ_CH1_PWR_EN_OFF	DMA_READ_CH1_PWR_EN	Fields made visible
	RSVDP_1	Fields made visible
DMA_READ_CH23_IMWR_DATA_OFF	RD_CHANNEL_[2|3]_DATA	Fields made visible
DMA_READ_CH2_PWR_EN_OFF	DMA_READ_CH2_PWR_EN	Fields made visible
	RSVDP_1	
DMA_READ_CH3_PWR_EN_OFF	DMA_READ_CH3_PWR_EN	Fields made visible
	RSVDP_1	
DMA_READ_CH45_IMWR_DATA_OFF	RD_CHANNEL_[4|5]_DATA	Fields made visible
DMA_READ_CH4_PWR_EN_OFF	DMA_READ_CH4_PWR_EN	Fields made visible
	RSVDP_1	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
DMA_READ_CH5_PWR_EN_OFF	DMA_READ_CH5_PWR_EN	Fields made visible
	RSVDP_1	
DMA_READ_ENGINE_EN_OFF	DMA_READ_ENGINE	**Testable** corrected Fields made visible
	DMA_READ_ENGINE_EN_HSHAKE_CH[0-7]	Fields made visible
	RSVDP_[1|24]	
DMA_READ_CH67_IMWR_DATA_OFF	RD_CHANNEL_[6|7]_DATA	Fields made visible
DMA_READ_CH6_PWR_EN_OFF	DMA_READ_CH6_PWR_EN	Fields made visible
	RSVDP_1	
DMA_READ_CH7_PWR_EN_OFF	DMA_READ_CH7_PWR_EN	Fields made visible
	RSVDP_[1|24]	
DMA_READ_CHANNEL_ARB_WEIGHT_HIGH_OFF	READ_CHANNEL[4|5|6|7]_WEIGHT	Fields made visible
DMA_READ_CHANNEL_ARB_WEIGHT_LOW_OFF	READ_CHANNEL[0|1|2|3]_WEIGHT	Fields made visible
DMA_READ_DONE_IMWR_HIGH_OFF	DMA_READ_DONE_HIGH_REG	Fields made visible
DMA_READ_DONE_IMWR_LOW_OFF	DMA_READ_DONE_LOW_REG	Fields made visible
DMA_READ_DOORBELL_OFF	RD_DOORBELL_NUM	Fields made visible
	RD_STOP	
DMA_READ_ENGINE_CHGROUP_OFF	DMA_READ_ENGINE_CHGROUP_ENABLE	Fields made visible
	DMA_READ_ENGINE_CHGROUP_END	
	DMA_READ_ENGINE_CHGROUP_START	
DMA_READ_ENGINE_HSHAKE_CNT_HIGH_OFF	DMA_READ_ENGINE_HSHAKE_CNT_CH[4|5|6|7]	Fields made visible
DMA_READ_ENGINE_HSHAKE_CNT_LOW_OFF	DMA_READ_ENGINE_HSHAKE_CNT_CH[0|1|2|3]	Fields made visible
	RSVDP_[13|21|29|5]	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
DMA_READ_ENGINE_PF_OFF	DMA_READ_ENGINE_MAX_PRE_FETCH	**Value After Reset** corrected Fields made visible
	RSVDP_READ_ENGINE_PF	Fields made visible
DMA_READ_ERR_STATUS_HIGH_OFF	CPL_ABORT	Fields made visible
	CPL_TIMEOUT	
	DATA_POISIONING	
	UNSUPPORTED_REQ	
DMA_READ_ERR_STATUS_LOW_OFF	APP_WR_ERR_DETECT	Fields made visible
	LINK_LIST_ELEMENT_FETCH_ERR_DETECT	
	RSVDP_[24|8]	
DMA_READ_INT_CLEAR_OFF	RD_ABORT_INT_CLEAR	Fields made visible
	RD_DONE_INT_CLEAR	
	RSVDP_[24|8]	
DMA_READ_INT_MASK_OFF	RD_ABORT_INT_MASK	Fields made visible
	RD_DONE_INT_MASK	
	RSVDP_[24|8]	
DMA_READ_INT_STATUS_OFF	RD_ABORT_INT_STATUS	Fields made visible
	RD_DONE_INT_STATUS	
	RSVDP_[24|8]	
DMA_READ_LINKED_LIST_ERR_EN_OFF	RD_CHANNEL_LLLAIE	Fields made visible
	RD_CHANNEL_LLRAIE	
	RSVDP_[24|8]	
DMA_SAR_HIGH_OFF_[RD|WR]CH_0	SRC_ADDR_REG_HIGH	Fields made visible
DMA_SAR_LOW_OFF_[RD|WR]CH_0	SRC_ADDR_REG_LOW	Fields made visible
DMA_TRANSFER_SIZE_OFF_[WR|RD]CH_0	DMA_TRANSFER_SIZE	Fields made visible
DMA_WRITE_ABORT_IMWR_HIGH_OFF	DMA_WRITE_ABORT_HIGH_REG	Fields made visible
DMA_WRITE_ABORT_IMWR_LOW_OFF	DMA_WRITE_ABORT_LOW_REG	Fields made visible

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
DMA_WRITE_CH0_PWR_EN_OFF	DMA_WRITE_CH0_PWR_EN	Fields made visible
	RSVDP_1	
DMA_WRITE_CH01_IMWR_DATA_OFF	WR_CHANNEL_[0|1]_DATA	Fields made visible
DMA_WRITE_CH1_PWR_EN_OFF	DMA_WRITE_CH1_PWR_EN	Fields made visible
	RSVDP_1	
DMA_WRITE_CH23_IMWR_DATA_OFF	WR_CHANNEL_[2|3]_DATA	Fields made visible
DMA_WRITE_CH2_PWR_EN_OFF	DMA_WRITE_CH2_PWR_EN	Fields made visible
	RSVDP_1	
DMA_WRITE_CH3_PWR_EN_OFF	DMA_WRITE_CH3_PWR_EN	Fields made visible
	RSVDP_1	
DMA_WRITE_CH45_IMWR_DATA_OFF	WR_CHANNEL_[4|5]_DATA	Fields made visible
DMA_WRITE_CH4_PWR_EN_OFF	DMA_WRITE_CH4_PWR_EN	Fields made visible
	RSVDP_1	
DMA_WRITE_CH5_PWR_EN_OFF	DMA_WRITE_CH5_PWR_EN	Fields made visible
	RSVDP_1	
DMA_WRITE_CH6_PWR_EN_OFF	DMA_WRITE_CH6_PWR_EN	Fields made visible
	RSVDP_1	
DMA_WRITE_CH67_IMWR_DATA_OFF	WR_CHANNEL_[6|7]_DATA	Fields made visible
DMA_WRITE_CH7_PWR_EN_OFF	DMA_WRITE_CH7_PWR_EN	Fields made visible
	RSVDP_1	
DMA_WRITE_CHANNEL_ARB_WEIGHT_HIGH_OFF	WRITE_CHANNEL[4|5|6|7]_WEIGHT	Fields made visible
	RSVDP_20	
DMA_WRITE_CHANNEL_ARB_WEIGHT_LOW_OFF	WRITE_CHANNEL[0|1|2|3]_WEIGHT	Fields made visible
	RSVDP_20	
DMA_WRITE_DONE_IMWR_HIGH_OFF	DMA_WRITE_DONE_HIGH_REG	Fields made visible
DMA_WRITE_DONE_IMWR_LOW_OFF	DMA_WRITE_DONE_LOW_REG	Fields made visible

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
DMA_WRITE_DOORBELL_OFF	RSVDP_3	Fields made visible
	WR_DOORBELL_NUM	
	WR_STOP	
DMA_WRITE_ENGINE_EN_OFF	DMA_WRITE_ENGINE	**Testable** corrected Fields made visible
	DMA_WRITE_ENGINE_EN_HSHAKE_CH[0-7]	Fields made visible
	RSVDP_[1|24]	
DMA_WRITE_ENGINE_CHGROUP_OFF	DMA_WRITE_ENGINE_CHGROUP_[ENABLE|END|START]	Fields made visible
	RSVDP_17	
DMA_WRITE_ENGINE_HSHAKE_CNT_HIGH_OFF	DMA_WRITE_ENGINE_HSHAKE_CNT_CH[4-7]	Fields made visible
	RSVDP_[13|21|29|5]	
DMA_WRITE_ENGINE_PF_OFF	DMA_WRITE_ENGINE_MAX_PRE_FETCH	**Value After Reset** corrected Fields made visible
	RSVDP_WRITE_ENGINE_PF	Fields made visible
DMA_WRITE_ERR_STATUS_OFF	APP_READ_ERR_DETECT	Fields made visible
	LINKLIST_ELEMENT_FETCH_ERR_DETECT	
	RSVDP_[8|24]	
DMA_WRITE_INT_CLEAR_OFF	WR_ABORT_INT_CLEAR	Fields made visible
	WR_DONE_INT_CLEAR	
	RSVDP_[8|24]	
DMA_WRITE_INT_MASK_OFF	WR_ABORT_INT_MASK	Fields made visible
	WR_DONE_INT_MASK	
	RSVDP_[8|24]	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
DMA_WRITE_INT_STATUS_OFF	WR_ABORT_INT_STATUS	Fields made visible
	WR_DONE_INT_STATUS	
	RSVDP_[8|24]	
DMA_WRITE_LINKED_LIST_ERR_EN_OFF	WR_CHANNEL_LLRAIE	Fields made visible
	WR_CHANNEL_LLLAIE	
	RSVDP_[8|24]	
ESM_CNTL_OFF	ESM_DATA_RATE[0|1]	**Testable** corrected
	ESM_ENABLE	
	ESM_PERFORM_CAL	
	LINK_REACH_TARGET	
ESM_LN_EQ_CNTL_20G_0_OFF	ESM_USP_TX_PRESET_20G_[0-3]	**Value After Reset** corrected
ESM_LN_EQ_CNTL_20G_12_OFF	ESM_USP_TX_PRESET_20G_[12-15]	**Value After Reset** corrected
ESM_LN_EQ_CNTL_20G_4_OFF	ESM_USP_TX_PRESET_20G_[4-7]	**Value After Reset** corrected
ESM_LN_EQ_CNTL_20G_8_OFF	ESM_USP_TX_PRESET_20G_[8-11]	**Value After Reset** corrected
ESM_LN_EQ_CNTL_25G_0_OFF	ESM_USP_TX_PRESET_25G_[0-3]	**Value After Reset** corrected
ESM_LN_EQ_CNTL_25G_12_OFF	ESM_USP_TX_PRESET_25G_[12-15]	**Value After Reset** corrected
ESM_LN_EQ_CNTL_25G_4_OFF	ESM_USP_TX_PRESET_25G_[4-7]	**Value After Reset** corrected
ESM_LN_EQ_CNTL_25G_8_OFF	ESM_USP_TX_PRESET_25G_[8-11]	**Value After Reset** corrected
ESM_STAT_OFF	ESM_CALIB_CMPLT	**Testable** corrected
	ESM_CURNT_DATA_RATE	
EXP_ROM_BAR_MASK_REG	ROM_MASK	**Memory Access** corrected
GEN3_EQ_COEFF_LEGALITY_STATUS_OFF	GEN3_EQ_VIOLATE_COEF_RULES	**Testable** corrected

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
GEN3_EQ_PSET_COEF_MAP__0	GEN3_EQ_POST_CURSOR_PSET	**Value After Reset** corrected
GEN3_RELATED_OFF	USP_SEND_8GT_EQ_TS2_DISABLE	**Testable** corrected
IATU_LIMIT_ADDR_VIEWPORT_OFF_OUTBOUND_0	CBUF_INCR	**Testable** corrected
LINK_CAPABILITIES_REG	PCIE_CAP_L0S_EXIT_LATENCY	**Memory Access** corrected **Value After Reset** corrected **Testable** corrected
	PCIE_CAP_L1_EXIT_LATENCY	
LINK_CAPABILITIES2_REG	PCIE_CAP_SUPPORT_LINK_SPEED_VECTOR	**Testable** corrected
LINK_CONTROL_LINK_STATUS_REG	PCIE_CAP_EN_CLK_POWER_MAN	**Testable** corrected
	PCIE_CAP_LINK_AUTO_BW_INT_EN	
	PCIE_CAP_LINK_BW_MAN_INT_EN	
	PCIE_CAP_LINK_DISABLE	
	PCIE_CAP_LINK_SPEED	
	PCIE_CAP_LINK_TRAINING	
	PCIE_CAP_NEGO_LINK_WIDTH	
	PCIE_CAP_RETRAIN_LINK	
LINK_CONTROL2_LINK_STATUS2_REG	PCIE_CAP_TARGET_LINK_SPEED	**Memory Access** corrected **Value After Reset** corrected **Testable** corrected
	PCIE_CAP_CROSSLINK_RESOLUTION	**Value After Reset** corrected
	DOWNSTREAM_COMPO_PRESENCE	Fields made visible
	PCIE_CAP_CURR_DEEMPHASIS	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
PCIE_VERSION_NUMBER_OFF	VERSION_NUMBER	**Value After Reset** corrected
PCIE_VERSION_TYPE_OFF	VERSION_TYPE	**Value After Reset** corrected
LINK_CONTROL3_REG	PERFORM_EQ	**Testable** corrected
MARGIN_PORT_CAPABILITIES_STATUS_REG	MARGINING_READY	**Testable** corrected
	MARGINING_SOFTWARE_READY	
PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG	PCIE_DEV_PORT_TYPE	**Testable** corrected
PHY_CONTROL_OFF	PHY_CONTROL	**Value After Reset** corrected
PHY_STATUS_OFF	PHY_STATUS	**Testable** corrected
PIPE_LOOPBACK_CONTROL_OFF	RXSTATUS_VALUE	**Testable** corrected
PL_DEBUG0_OFF	DEB_REG_0	**Testable** corrected
PL_DEBUG1_OFF	DEB_REG_1	**Testable** corrected
PL16G_CAP_OFF_20H_REG	USP_16G_TX_PRESET[0-3]	**Value After Reset** corrected
PL16G_CAP_OFF_24H_REG	USP_16G_TX_PRESET[4-7]	**Value After Reset** corrected
PL16G_CAP_OFF_28H_REG	USP_16G_TX_PRESET[8-11]	**Value After Reset** corrected
PL16G_CAP_OFF_2CH_REG	USP_16G_TX_PRESET[12-15]	**Value After Reset** corrected
PL32G_CAP_OFF_20H_REG	USP_32G_TX_PRESET[0-3]	**Value After Reset** corrected
PL32G_CAP_OFF_24H_REG	USP_32G_TX_PRESET[4-7]	**Value After Reset** corrected
PL32G_CAP_OFF_28H_REG	USP_32G_TX_PRESET[8-11]	**Value After Reset** corrected

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
PL32G_CAP_OFF_2CH_REG	USP_32G_TX_PRESET[12-15]	**Value After Reset** corrected
PL32G_STATUS_REG	TX_PRECODE_REQ	**Value After Reset** corrected
	TX_PRECODING_ON	
PORT_LINK_CTRL_OFF	LINK_CAPABLE	**Testable** corrected
PTM_REQ_LOCAL_LSB_OFF	PTM_REQ_LOCAL_LSB	**Testable** corrected
PTM_REQ_NOM_CLOCK_T_OFF	PTM_REQ_NOM_CLOCK_T_INT	**Testable** corrected
RESOURCE_STATUS_REG_VC0	VC_NEGO_PENDING_VC0	**Testable** corrected
RESOURCE_STATUS_REG_VC[1-7]	VC_NEGO_PENDING_VC[1-7]	**Value After Reset** corrected **Testable** corrected
SHADOW_SRIOV_VF_OFFSET_POSITION	SHADOW_SRIOV_VF_OFFSET	**Value After Reset** corrected **Testable** corrected
	SHADOW_SRIOV_VF_STRIDE	
RX_SERIALIZATION_Q_CTRL_OFF	ALMOST_FULL_THRESHOLD	**Testable** corrected
SD_STATUS_L1LTSSM_REG	LTSSM_VARIABLE	**Testable** corrected
SD_STATUS_L3FC_REG	CREDIT_DATA1	**Testable** corrected
SHADOW_MSIX_PBA_OFFSET_REG	PCI_MSIX_PBA_BIR	**Testable** corrected
	PCI_MSIX_PBA_OFFSET	
SHADOW_MSIX_TABLE_OFFSET_REG	PCI_MSIX_BIR	**Testable** corrected
	PCI_MSIX_TABLE_OFFSET	
SHADOW_PCI_MSIX_CAP_ID_NEXT_CTRL_REG	PCI_MSIX_TABLE_SIZE	**Testable** corrected

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
SHADOW_READI_TIME_REPORTING1_OFF	RESET_TIME	**Testable** corrected
	RTR_TIME_VALID	
SHADOW_READI_TIME_REPORTING2_OFF	D3HOT_D0_TIME	**Testable** corrected
	FLR_TIME	
SPCIE_CAP_OFF_0CH_REG	USP_RX_PRESET_HINT[0|1]	**Value After Reset** corrected **Testable** corrected
	USP_TX_PRESET[0|1]	
SPCIE_CAP_OFF_10H_REG	USP_RX_PRESET_HINT[2|3]	**Value After Reset** corrected **Testable** corrected
	USP_TX_PRESET[2|3]	
SPCIE_CAP_OFF_14H_REG	USP_RX_PRESET_HINT[4|5]	**Value After Reset** corrected **Testable** corrected
	USP_TX_PRESET[4|5]	
SPCIE_CAP_OFF_18H_REG	USP_RX_PRESET_HINT[6|7]	**Value After Reset** corrected **Testable** corrected
	USP_TX_PRESET[6|7]	
SPCIE_CAP_OFF_1CH_REG	USP_RX_PRESET_HINT[8|9]	**Value After Reset** corrected **Testable** corrected
	USP_TX_PRESET[8|9]	
SPCIE_CAP_OFF_20H_REG	USP_RX_PRESET_HINT10	**Value After Reset** corrected **Testable** corrected
	USP_TX_PRESET10	
SPCIE_CAP_OFF_24H_REG	USP_RX_PRESET_HINT[12|13]	**Value After Reset** corrected **Testable** corrected
	USP_TX_PRESET[12|13]	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
SPCIE_CAP_OFF_28H_REG	USP_RX_PRESET_HINT[14-15] USP_TX_PRESET[14-15]	**Value After Reset** corrected **Testable** corrected
SPCIE_CAP_OFF_2CH_REG	USP_16G_RX_PRESET_HINT[0|1] USP_16G_TX_PRESET[0|1]	**Value After Reset** corrected **Testable** corrected
SPCIE_CAP_OFF_30H_REG	USP_16G_RX_PRESET_HINT[2|3] USP_16G_TX_PRESET[2|3]	**Value After Reset** corrected **Testable** corrected
SPCIE_CAP_OFF_34H_REG	USP_16G_RX_PRESET_HINT[4|5] USP_16G_TX_PRESET[4|5]	**Value After Reset** corrected **Testable** corrected
SPCIE_CAP_OFF_38H_REG	USP_16G_RX_PRESET_HINT[6|7] USP_16G_TX_PRESET[6|7]	**Value After Reset** corrected **Testable** corrected
SPCIE_CAP_OFF_3CH_REG	USP_16G_RX_PRESET_HINT[8|9] USP_16G_TX_PRESET[8|9]	**Value After Reset** corrected **Testable** corrected
SPCIE_CAP_OFF_40H_REG	USP_16G_RX_PRESET_HINT[10|11] USP_16G_TX_PRESET[10|11]	**Value After Reset** corrected **Testable** corrected
SPCIE_CAP_OFF_44H_REG	USP_16G_RX_PRESET_HINT[12|13] USP_16G_TX_PRESET[12|13]	**Value After Reset** corrected **Testable** corrected
SPCIE_CAP_OFF_48H_REG	USP_16G_RX_PRESET_HINT[14|15] USP_16G_TX_PRESET[14|15]	**Value After Reset** corrected **Testable** corrected
SRIOV_BAR1_REG	RSVDP_SRIOV_VF_BAR1	**Memory Access** corrected

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
SRIOV_BAR3_REG	RSVDP_SRIOV_VF_BAR3	**Memory Access** corrected **Testable** corrected
SRIOV_BAR5_REG	RSVDP_SRIOV_VF_BAR5	**Memory Access** corrected **Testable** corrected
SRIOV_VF_OFFSET_POSITION	SRIOV_VF_OFFSET	**Testable** corrected
	SRIOV_VF_STRIDE	
STATUS_COMMAND_REG	INT_STATUS	**Testable** corrected
TIME_BASED_ANALYSIS_DATA_REG	TIME_BASED_ANALYSIS_DATA	**Testable** corrected
TIMER_CTRL_MAX_FUNC_NUM_OFF	TIMER_MOD_REPLAY_TIMER	**Testable** corrected
TOTAL_VFS_INITIAL_VFS_REG	SRIOV_INITIAL_VFS	**Testable** corrected
	SRIOV_TOTAL_VFS	
TPH_ST_TABLE_REG_0	TPH_REQ_ST_TABLE_HIGHER_[0|1]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[0|1]	
TPH_ST_TABLE_REG_1	TPH_REQ_ST_TABLE_HIGHER_[2|3]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[2|3]	
TPH_ST_TABLE_REG_10	TPH_REQ_ST_TABLE_HIGHER_[20|21]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[20|21]	
TPH_ST_TABLE_REG_11	TPH_REQ_ST_TABLE_HIGHER_[22|23]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[22|23]	
TPH_ST_TABLE_REG_12	TPH_REQ_ST_TABLE_HIGHER_[24|25]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[24|25]	
TPH_ST_TABLE_REG_13	TPH_REQ_ST_TABLE_HIGHER_[26|27]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[26|27]	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
TPH_ST_TABLE_REG_14	TPH_REQ_ST_TABLE_HIGHER_[28|29]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[28|29]	
TPH_ST_TABLE_REG_15	TPH_REQ_ST_TABLE_HIGHER_[30|31]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[30|31]	
TPH_ST_TABLE_REG_16	TPH_REQ_ST_TABLE_HIGHER_[32|33]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[32|33]	
TPH_ST_TABLE_REG_17	TPH_REQ_ST_TABLE_HIGHER_[34|35]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[34|35]	
TPH_ST_TABLE_REG_18	TPH_REQ_ST_TABLE_HIGHER_[36|37]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[36|37]	
TPH_ST_TABLE_REG_19	TPH_REQ_ST_TABLE_HIGHER_[38|39]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[38|39]	
TPH_ST_TABLE_REG_2	TPH_REQ_ST_TABLE_HIGHER_[4|5]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[4|5]	
TPH_ST_TABLE_REG_20	TPH_REQ_ST_TABLE_HIGHER_[40|41]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[40|41]	
TPH_ST_TABLE_REG_21	TPH_REQ_ST_TABLE_HIGHER_[42|43]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[42|43]	
TPH_ST_TABLE_REG_22	TPH_REQ_ST_TABLE_HIGHER_[44|45]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[44|45]	
TPH_ST_TABLE_REG_23	TPH_REQ_ST_TABLE_HIGHER_[46|47]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[46|47]	
TPH_ST_TABLE_REG_24	TPH_REQ_ST_TABLE_HIGHER_[48|49]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[48|49]	
TPH_ST_TABLE_REG_25	TPH_REQ_ST_TABLE_HIGHER_50	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_50	
TPH_ST_TABLE_REG_26	TPH_REQ_ST_TABLE_HIGHER_[52|53]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[52|53]	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
TPH_ST_TABLE_REG_27	TPH_REQ_ST_TABLE_HIGHER_[54|55]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[54|55]	
TPH_ST_TABLE_REG_28	TPH_REQ_ST_TABLE_HIGHER_[56|57]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[56|57]	
TPH_ST_TABLE_REG_29	TPH_REQ_ST_TABLE_HIGHER_[58|59]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[58|59]	
TPH_ST_TABLE_REG_3	TPH_REQ_ST_TABLE_HIGHER_[6|7]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[6|7]	
TPH_ST_TABLE_REG_30	TPH_REQ_ST_TABLE_HIGHER_[60|61]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[60|61]	
TPH_ST_TABLE_REG_31	TPH_REQ_ST_TABLE_HIGHER_[62|63]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[62|63]	
TPH_ST_TABLE_REG_4	TPH_REQ_ST_TABLE_HIGHER_[8|9]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[8|9]	
TPH_ST_TABLE_REG_5	TPH_REQ_ST_TABLE_HIGHER_[10|11]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[10|11]	
TPH_ST_TABLE_REG_6	TPH_REQ_ST_TABLE_HIGHER_[12|13]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[12|13]	
TPH_ST_TABLE_REG_7	TPH_REQ_ST_TABLE_HIGHER_[14|15]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[14|15]	
TPH_ST_TABLE_REG_8	TPH_REQ_ST_TABLE_HIGHER_[16|17]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[16|17]	
TPH_ST_TABLE_REG_9	TPH_REQ_ST_TABLE_HIGHER_[18|19]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[18|19]	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
UNCORR_ERR_STATUS_OFF	ATOMIC_EGRESS_BLOCKED_ERR_STATUS	**Testable** corrected
	DL_PROTOCOL_ERR_STATUS	
	FC_PROTOCOL_ERR_STATUS	
	MALF_TLP_ERR_STATUS	
	REC_OVERFLOW_ERR_STATUS	
	SURPRISE_DOWN_ERR_STATUS	
VC_CAPABILITIES_REG_2	VC_ARBI_TABLE_OFFSET	**Value After Reset** corrected
VF_CAP_ID_NXT_PTR_REG	AUX_CURR	**Value After Reset** corrected
	PME_SUPPORT	**Value After Reset** corrected **Testable** corrected
VF_CON_STATUS_REG	PME_ENABLE	**Testable** corrected
	POWER_STATE	
VF_DEVICE_CAPABILITIES_REG	PCIE_CAP_CAP_SLOT_PWR_LMT_SCALE	**Testable** corrected
	PCIE_CAP_CAP_SLOT_PWR_LMT_VALUE	
VF_DEVICE_CONTROL_DEVICE_STATUS	PCIE_CAP_AUX_POWER_DETECTED	**Testable** corrected
	PCIE_CAP_TRANS_PENDING	
VF_LINK_CAPABILITIES_REG	PCIE_CAP_CLOCK_POWER_MAN	**Value After Reset** corrected **Testable** corrected
	PCIE_CAP_L0S_EXIT_LATENCY	
	PCIE_CAP_L1_EXIT_LATENCY	
VF_LINK_CAPABILITIES2_REG	PCIE_CAP_SUPPORT_LINK_SPEED_VECTOR	**Testable** corrected
	PCIE_CAP_RETIMER_PRE_DET_SUPPORT	Fields made visible

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
VF_LINK_CONTROL_LINK_STATUS_REG	PCIE_CAP_SLOT_CLK_CONFIG	**Value After Reset** corrected **Testable** corrected
	PCIE_CAP_EN_CLK_POWER_MAN	**Testable** corrected
	PCIE_CAP_LINK_AUTO_BW_INT_EN	
	PCIE_CAP_LINK_BW_MAN_INT_EN	
	PCIE_CAP_LINK_DISABLE	
	PCIE_CAP_LINK_SPEED	
	PCIE_CAP_LINK_TRAINING	
	PCIE_CAP_NEGO_LINK_WIDTH	
	PCIE_CAP_RETRAIN_LINK	
VF_LINK_CONTROL2_LINK_STATUS2_REG	PCIE_CAP_TARGET_LINK_SPEED	**Memory Access** corrected **Value After Reset** corrected Fields made visible
	PCIE_CAP_CROSSLINK_RESOLUTION	**Value After Reset** corrected
	PCIE_CAP_CURR_DEEMPHASIS	**Value After Reset** corrected Fields made visible
	DOWNSTREAM_COMPO_PRESENCE	Fields made visible
	RSVDP_26	
VF_MSIX_PBA_OFFSET_REG	PCI_MSIX_PBA_BIR	**Value After Reset** corrected **Testable** corrected
	PCI_MSIX_PBA_OFFSET	
VF_MSIX_TABLE_OFFSET_REG	PCI_MSIX_PBA_BIR	**Value After Reset** corrected **Testable** corrected
	PCI_MSIX_PBA_OFFSET	
VF_PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG	PCIE_DEV_PORT_TYPE	**Testable** corrected

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
VF_PCI_MSIX_CAP_ID_NEXT_CTRL_REG	PCI_MSIX_TABLE_SIZE	**Testable** corrected
VF_READI_TIME_REPORTING1_OFF	DL_UP_TIME	**Testable** corrected
	RESET_TIME	
	RTR_TIME_VALID	
VF_READI_TIME_REPORTING2_OFF	D3HOT_D0_TIME	**Testable** corrected
	FLR_TIME	
VF_STATUS_COMMAND_REG	INT_STATUS	**Testable** corrected
VF_SUBSYSTEM_ID_SUBSYSTEM_VENDOR_ID_REG	SUBSYS_DEV_ID	**Value After Reset** corrected
	SUBSYS_VENDOR_ID	
VF_TPH_REQ_CAP_REG_REG	TPH_REQ_CAP_INT_VEC	**Testable** corrected
	TPH_REQ_CAP_ST_TABLE_LOC_[0|1]	
	TPH_REQ_CAP_ST_TABLE_SIZE	
	TPH_REQ_DEVICE_SPEC	
	TPH_REQ_EXTENDED_TPH	
	TPH_REQ_NO_ST_MODE	
VF_TPH_ST_TABLE_REG_0	TPH_REQ_ST_TABLE_HIGHER_[0|1]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[0|1]	
VF_TPH_ST_TABLE_REG_1	TPH_REQ_ST_TABLE_HIGHER_[2|3]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[2|3]	
VF_TPH_ST_TABLE_REG_10	TPH_REQ_ST_TABLE_HIGHER_[20|21]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[20|21]	
VF_TPH_ST_TABLE_REG_11	TPH_REQ_ST_TABLE_HIGHER_[22|23]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[22|23]	
VF_TPH_ST_TABLE_REG_12	TPH_REQ_ST_TABLE_HIGHER_[24|25]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[24|25]	
VF_TPH_ST_TABLE_REG_13	TPH_REQ_ST_TABLE_HIGHER_[26|27]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[26|27]	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
VF_TPH_ST_TABLE_REG_14	TPH_REQ_ST_TABLE_HIGHER_[28|29]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[28|29]	
VF_TPH_ST_TABLE_REG_15	TPH_REQ_ST_TABLE_HIGHER_[30|31]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[30|31]	
VF_TPH_ST_TABLE_REG_16	TPH_REQ_ST_TABLE_HIGHER_[32|33]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[32|33]	
VF_TPH_ST_TABLE_REG_17	TPH_REQ_ST_TABLE_HIGHER_[34|35]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[34|35]	
VF_TPH_ST_TABLE_REG_18	TPH_REQ_ST_TABLE_HIGHER_[36|37]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[36|37]	
VF_TPH_ST_TABLE_REG_19	TPH_REQ_ST_TABLE_HIGHER_[38|39]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[38|39]	
VF_TPH_ST_TABLE_REG_2	TPH_REQ_ST_TABLE_HIGHER_[4|5]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[4|5]	
VF_TPH_ST_TABLE_REG_20	TPH_REQ_ST_TABLE_HIGHER_[40|41]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[40|41]	
VF_TPH_ST_TABLE_REG_21	TPH_REQ_ST_TABLE_HIGHER_[42|43]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[42|43]	
VF_TPH_ST_TABLE_REG_22	TPH_REQ_ST_TABLE_HIGHER_[44|45]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[44|45]	
VF_TPH_ST_TABLE_REG_23	TPH_REQ_ST_TABLE_HIGHER_[46|47]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[46|47]	
VF_TPH_ST_TABLE_REG_24	TPH_REQ_ST_TABLE_HIGHER_[48|49]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[48|49]	
VF_TPH_ST_TABLE_REG_25	TPH_REQ_ST_TABLE_HIGHER_[50|51]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[50|51]	
VF_TPH_ST_TABLE_REG_26	TPH_REQ_ST_TABLE_HIGHER_[52|53]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[52|53]	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
VF_TPH_ST_TABLE_REG_27	TPH_REQ_ST_TABLE_HIGHER_[54|55]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[54|55]	
VF_TPH_ST_TABLE_REG_28	TPH_REQ_ST_TABLE_HIGHER_[56|57]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[56|57]	
VF_TPH_ST_TABLE_REG_29	TPH_REQ_ST_TABLE_HIGHER_[58|59]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[58|59]	
VF_TPH_ST_TABLE_REG_3	TPH_REQ_ST_TABLE_HIGHER_[6|7]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[6|7]	
VF_TPH_ST_TABLE_REG_30	TPH_REQ_ST_TABLE_HIGHER_[60|61]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[60|61]	
VF_TPH_ST_TABLE_REG_31	TPH_REQ_ST_TABLE_HIGHER_[62|63]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[62|63]	
VF_TPH_ST_TABLE_REG_4	TPH_REQ_ST_TABLE_HIGHER_[8|9]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[8|9]	
VF_TPH_ST_TABLE_REG_5	TPH_REQ_ST_TABLE_HIGHER_[10|11]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[10|11]	
VF_TPH_ST_TABLE_REG_6	TPH_REQ_ST_TABLE_HIGHER_[12|13]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[12|13]	
VF_TPH_ST_TABLE_REG_7	TPH_REQ_ST_TABLE_HIGHER_[14|15]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[14|15]	
VF_TPH_ST_TABLE_REG_8	TPH_REQ_ST_TABLE_HIGHER_[16|17]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[16|17]	
VF_TPH_ST_TABLE_REG_9	TPH_REQ_ST_TABLE_HIGHER_[18|19]	Fields made visible
	TPH_REQ_ST_TABLE_LOWER_[18|19]	

Table 10-6 Documentation Changes (Non-RTL) (Continued)

Register	Field	Nature of Change
VF_UNCORR_ERR_STATUS_OFF	ATOMIC_EGRESS_BLOCKED_ERR_STATUS	**Testable** corrected
	DL_PROTOCOL_ERR_STATUS	
	FC_PROTOCOL_ERR_STATUS	
	MALF_TLP_ERR_STATUS	
	REC_OVERFLOW_ERR_STATUS	
	SURPRISE_DOWN_ERR_STATUS	

10.4 Changes to RAM Sizes

This section details the changes to the default RAM sizes that have occurred since the last production release. It does not detail changes that are associated with new or additional features that you enable on your current configuration

Caution To determine the precise changes to RAM sizes for your actual controller configuration, you should compare the simulation-reported RAM sizes for the previous and current releases. For more details, see the “RAM Requirements” section in the Architecture chapter of the *Databook*.

The following changes have occurred for this release.

No changes have occurred for this release.

Table 10-7 RAM Changes

RAM Name	Change
AXI Master Read Queue Request Formation CDC Buffer RAM	These RAMs hold request header/data specific signals. The width of some of these signals has changed. Therefore, changing the total width of the RAMs. ***Note:*** The RAM changes apply to legacy DMA only.
AXI Master Write Queue Request Formation CDC Buffer RAM	
AXI Master Non-posted Request Buffer RAM	

10.5 Changes to Configuration Parameters

This section details any changes to the configuration parameters of the controller that have occurred since the last production release. It does *not* detail changes that are associated with new or additional features that you enable on your current configuration.

All changes to the configuration parameters are indicated in the change-tracked version of the *Databook* PDF which can be found at the location identified in the *Databook* revision history.

If you intend to source an existing configuration batch file, then you must first convert your configuration file, as described in "Known Issues and Limitations" on page 319. If you are not sourcing an existing configuration batch file, then you should be still aware of changes to the default value of some configuration parameters.

Caution

To ensure that your existing configuration absorbs all changes to default parameters that the PCIe R&D team makes, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File*->Write *Batch Script* menu item.

Table 10-8 Configuration Parameter Changes

Name	Change
CX_PIPERX_MULTI_BLOCK	**Default value:** changed **from:** (((CX_PHY_FREQ == FREQ_125) && (CX_PHY_GEN2_MODE == GEN2_DF) && (CX_PHY_GEN3_MODE == GEN3_DW) && (CX_PHY_GEN4_MODE == GEN4_DW) && (CX_PHY_INTERFACE == V7_INTERFACE)) ? 1 : 0==1) ? 1 : 0 **to:** ((SNPS_RSVDPARAM_39==1) || (CX_PIPE_SERDES_ARCH && CX_MAX_PCIE_SPEED>=3 && (CX_PHY_SMODE_GEN3>=8 || CX_PHY_SMODE_GEN4>=8 || CX_PHY_SMODE_GEN5>=8)))? 1 : 0
CX_ATOMIC_ENABLE	**Enabled:** changed **from:** !AMBA_POPULATED && !CC_DMA_ENABLE **to:** !(AMBA_INTERFACE!=0)

Table 10-8 Configuration Parameter Changes

Name	Change
1-Port SRAMs only	**Label:** changed **from:** CX_RAM_TYPE **to:** 1-Port SRAMs only **Values:** changed **from:** Simple(0), DesignWare(1), and FPGA RAM (2) **to:** 0,1 **Default Value:** changed **from:** DWC_PCIE_FPGA ? 2 : 0 **to:** 0 **Enabled:** changed **from:** !DWC_PCIE_FPGA && !CX_RAM_AT_TOP_IF **to:** CX_RAM_AT_TOP_IF && CX_MAX_PCLK_EXISTS
DEFAULT_AUX_CLK_FREQ	**Enabled:** changed **from:** CX_L1_SUBSTATES_ENABLE **to:** Always
CC_IB_RD_REQ_ORDR_RAM_RD_LATENCY	**Name:** changed **from:** CC_IB_RD_REQ_CDC_RAM_RD_LATENCY **to:** CC_IB_RD_REQ_ORDR_RAM_RD_LATENCY **Enabled:** changed **from:** SLV_CLK_DIFF_ENABLE && SLAVE_POPULATED **to:** ((AMBA_INTERFACE==2) || (AMBA_INTERFACE==3))
CC_IB_WR_REQ_CDC_RAM_RD_LATENCY	**Name:** changed **from:** CC_IB_WR_REQ_CDC_RAM_RD_LATENCY **to:** CC_IB_RD_ORDR_CDC_RAM_RD_LATENCY **Enabled:** changed **from:** ((AMBA_INTERFACE==2) || (AMBA_INTERFACE==3)) **to:** SLV_CLK_DIFF_ENABLE && SLAVE_POPULATED
CC_DTIM_REQQ_RAM_RD_LATENCY	**Name:** changed **from:** CC_IF_WRCTX_LLQ_OVERLAY_RAM_LATENCY **to:** CC_DTIM_REQQ_RAM_RD_LATENCY **Enabled:** changed **from:** CX_DMA_PF_ENABLE **to:** CC_DTIM_ENABLE
CX_MSIX_TABLE_RAM_RD_LATENCY	**Name:** changed **from:** CC_IF_RD_CTXC2W_RAM_LATENCY **to:** CX_MSIX_TABLE_RAM_RD_LATENCY **Enabled:** changed **from:** CX_DMA_PF_ENABLE **to:** MSIX_TABLE_EN==1

Table 10-8 Configuration Parameter Changes

Name	Change
CX_BLOCK_VDM_TLP	**Label:** changed **from:** CX_BLOCK_VDM_TLP **to:** Block VDMs in Non-D0 State
CPLQ_MNG_HDP	**Default value:** changed **from:** 2*(CX_MAX_TAG+1) **to:** MIN_RD_REQ_SIZE > 2*CX_RCB) ? (1+MIN_RD_REQ_SIZE/CX_RCB)*(CX_MAX_TAG+1) : 2*(CX_MAX_TAG+1
CX_CXS_SYNCHRONOUS	**Enabled:** changed **from:** CX_CXS_ENABLE **to:** (CX_CXS_ENABLE && (CX_CXS_DATAFLITWIDTH!=CX_CXS_CCIXDATAWIDTH))
RAM1P_ARCH	**Enabled:** changed **from:** !(CX_RAM_TYPE==1) **to:** Always

10.6 Converting to the Current Release

Sometimes a new controller release might no longer use a certain configuration parameter, or the meaning of that parameter might have changed. The following process helps you convert your current configuration file so that it creates the same RTL with the new controller.

1. Open coreConsultant and create an unconfigured workspace from the newly installed controller.
2. In the coreConsultant command line, enter the following command:

   ```
   parse_configfile my_configfile.config
   ```

   where `my_configfile.config` is your current configuration file. This command creates an updated configuration file in your working directory as follows:

   ```
   my_configfile.config.new
   ```

3. In the coreConsultant command line, enter the following command:

   ```
   source my_configfile.config.new
   ```

4. Select Apply to generate the new RTL with the updated or translated parameters.
5. From the File Menu, select Write Batch Script and save the configuration file for the new release.
6. When you source the updated configuration file in coreConsultant, you can *ignore any new warnings* about parameter settings that are not relevant to, or not enabled in your configuration.

Caution

Writing Out Your Configuration File

To ensure that your existing configuration absorbs all changes to default parameters that the PCIe R&D team makes, you should never configure coreConsultant to write out the configuration settings for parameters that you have not set/changed.

Therefore, you must never select the *Write default parameter values* option in the *File*->Write *Batch Script* menu item.

You must convert your configuration file. Failure to do so, can result in:

- Your configuration file being incompatible with the current release.
- Functional, architectural, RAM, and I/O changes when the default of some configuration parameters change from release to release.

10.7 Known Issues and Limitations

You can view a complete list of functional problem reports for this product, including problems identified after product release, by accessing the STAR report on the Web. For more details, see "Details of Fixed Defects and Enhancements" on page 321. You must have a SolvNet ID to view STAR reports. This release has the following known tool and packaging issues at the time of release.

- "Packaged coreConsultant Test Limitations"
- "VTB Limitations"
- "Design Example"
- "Unique Case Violation Simulation Message""coreConsultant Memory Map Limitations"

10.7.1 Packaged coreConsultant Test Limitations

We invite you to submit your coreConsultant configuration, so that Synopsys can run the full range of testing on your configuration. Because of the very large configuration space, it is not possible to regress every configuration before a release is made. Synopsys is continually running fixed and randomized configurations, but it is possible that your exact configuration has not been regressed. Test case failures might occur because of improper test bench configuration. In that case open a case through SolvNet.

10.7.2 VTB Limitations

The following limitations apply to the current release of the VTB:

- Not backward compatible with previous releases
- Not UVM compliantNo support for big-endian (`AHB_ENDIANNESS`) configurations.

10.7.3 Design Example

The design example in `<workspace>/examples/DWC_pcie_clkrst.v` has been functionally verified, but has not been explicitly targeted for verification metrics. However, it has been used by Synopsys in the verification and regression environments for all controller configurations; including verification of all power transitions for the controller.

Synopsys has only processed a small number of reference configurations of `DWC_pcie_clkrst.v` through the Synthesis and Spyglass CDC flows. Therefore, your configuration of `DWC_pcie_clkrst.v` might not have been processed through these flows. The design example is shipped as example code. For that reason, it is not qualified for tape-out release. You must prove it in your SoC flow.

10.7.4 Unique Case Violation Simulation Message

The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

There is a known simulator issue with a "Unique case violation" message that occurs sometimes while running simulations with VCS outside of coreConsultant. You can ignore these messages.

To avoid these messages, use the `-xlrm uniq_prior_final` compile option in VCS. The simulator is reporting the violation when considering transient values of the input signals instead of considering only the stable values for these inputs. Therefore, there is no functional issue.

10.7.5 coreConsultant Memory Map Limitations

The controller supports the generation of configuration-specific register maps as described in the "Register Configuration Space" chapter in the *Databook*. For SR-IOV configurations (`CX_SRIOV_ENABLE =1`), the following limitations apply.

Coreconsultant Report File Limitations for SR-IOV Configurations

CX_NVFUNC	IP-XACT (IP-XACT XML)	RALF and C Headers (No limitations.)	Register Report (DocBook XML). Also applies to *Databook*.
1 - 256	Defines default #VFs in each PF	Defines default #VFs in each PF	Defines *only* first VF in each PF
257 .. 4096	Defines *only*[a] first VF in each PF	Defines default #VFs in each PF	Defines *only* first VF in each PF

a. For details on how to populate remaining VFs in the IP-XACT file, see "Populating IP-XACT File Manually" in the "Creating Optional Views and Reports" section in the "Configuring the controller" chapter of the *User Guide*.

10.8 Details of Fixed Defects and Enhancements

Defects fixed in release 5.50a of the DesignWare Cores PCI Express Controllers are listed in the STAR report for release 5.50a in STARs on the Web. You must have a SolvNet ID to view STAR reports at:

http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_ep#tab2

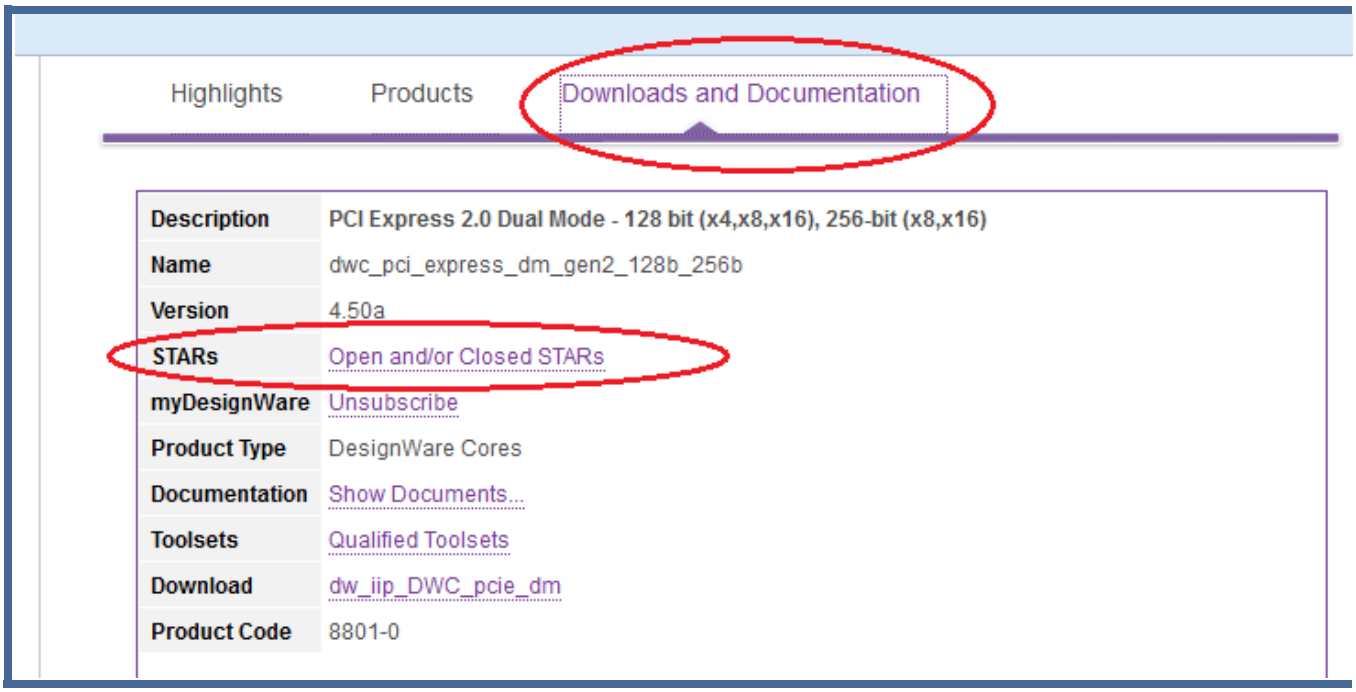
http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_dm#tab2

http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_rc#tab2

http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_sw#tab2

Attention For EA releases, consult Synopsys for a list of STARs fixed.

Figure 10-1 Accessing STARs on the Web through SolvNet.



Enhancement STARs are identifiable by the letter “E” in the Severity column, and fixed defect STARs are identifiable by the letter “B.” **An E1 or B1 has the lowest severity.** Clicking on the tab corresponding to 5.50a produces a STAR report of closed STARS for this release. For previous controller versions, click the tab corresponding to the version in question.

10.9 Customer Support

To obtain support for your product:

- First, prepare the following debug information, if applicable:
  - For environment setup problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, use the following menu entry:

    File > Build Debug Tar-file

    Check all the boxes in the dialog box that apply to your issue. This menu entry gathers all the Synopsys product data needed to begin debugging an issue and writes it to the file <*core tool startup directory*>/debug.tar.gz.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD)
    - Identify the hierarchy path to the DesignWare instance
    - Identify the timestamp of any signals or locations in the waveforms that are not understood
- Then, contact Support Center, with a description of your question and supplying the above information, using one of the following methods:
  - *For fastest response*, use the SolvNet website. When you fill in your information as explained later, your issue is automatically routed to a support engineer who is experienced with your product. The **Sub Product 1** entry is critical for correct routing.

    Go to http://solvnet.synopsys.com/EnterACall and click on the link to enter a call. Provide the requested information, including:
    - **Customer Tracking Number:** Enter your project name. Use the same name for cases related to the same project.
    - **Product:** DesignWare Cores
    - **Sub Product 1:** PCI Express
    - **Product Version:** 5.50a (for example)
    - **Problem Type:**
    - **Issue Severity:**
    - **Problem Title:** Provide a brief summary of the issue or list the error message you have encountered
    - **Problem Description:** For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood

    After creating the case, attach any debug files you created in the previous step.
  - Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
    - Include the Product name, Sub Product name and Tool Version number in your e-mail (as identified above) so it can be routed correctly.
    - For simulation issues, include the timestamp of any signals in waveforms for reference
    - Attach any debug files you created in the previous step.

- Or, telephone your local support center:
  - North America: Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
  - All other countries: https://www.synopsys.com/support/global-support-centers.html