SYNOPSYS®

DesignWare® Cores PCI Express Controller

Install Guide

Version 6.00a
June 2022

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Contents

Revision History

The following table provides the history of changes to this installation guide.

Version	Date	Description
6.00a	June 2022	Release update.

1 Installation and Setup

This guide provides information on how to install and set up the DesignWare PCIe controller. After you complete the installation procedure, you work primarily with the Synopsys coreConsultant tool to configure and synthesize the controller, and simulate it in the provided verification environment.

Attention If your controller is already installed and you are performing only the setup procedures, check the “Downloads and Documentation” tab on the corresponding component summary page to confirm that you have the latest version.“Accessing Product Documentation” on page 8 shows the location of the documents.

1.1 Accessing Product Documentation

Before you install the controller, you can download the full document set, including this document, the Databook, User Guide, and Release Notes for PCIe Controller, CXL Controller, or CCIX Controller at:

Table 1-1 Controller Document Location

Controller	Location
PCIe Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_express_controllers
CXL Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_cxl_controller
CCIX Controller	https://www.synopsys.com/dw/ipdir.php?ds=dwc_ccix_controller

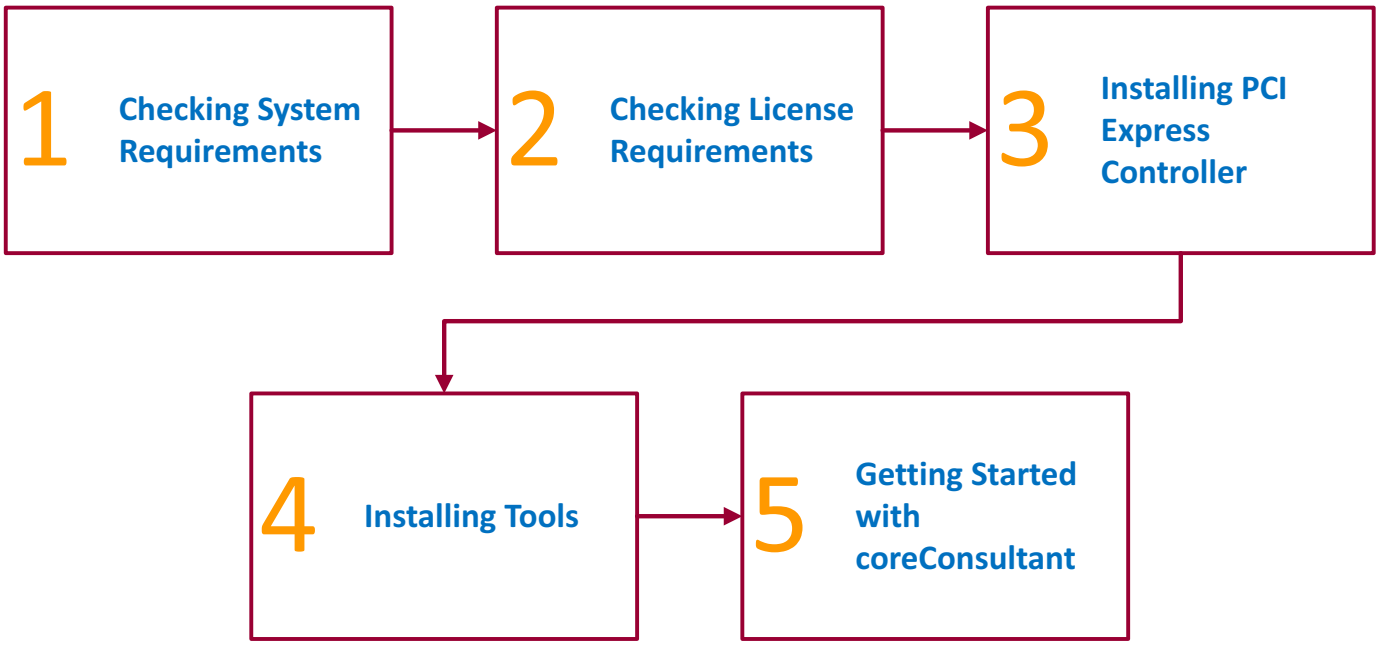
(A SolvNetPlus ID and a valid license are required to download these documents.)

You can access the full document set, including this document, the Databook, User guide, and Release notes, in your installation and workspace directories at *$DESIGNWARE_HOME/iip/DWC_pcie_ctl/latest/doc* and <*workspace*>*/doc* respectively.

Instructions for creating a workspace are provided in "Next Steps" on page 25.

1.2 Process Overview

To use the controller, you must follow the steps in this installation guide.



1.3 Checking System Requirements

Table 1-2 describes the system requirements for the controller.

Table 1-2 System Requirements

Element	Requirement
Operating System	Current information about supported operating system configurations and required patches is at the “Release Specific Support” page at: https://www.synopsys.com/support/licensing-installation-computeplatforms/compute-platforms/release-specific-support.html
Minimum Disk Space	■ 150 MB available hard disk space for coreConsultant installation ■ 400 MB available hard disk space for PCI Express Controller installation
Memory	■ 1,024 MB available swap space ■ 1,024 MB RAM

Note You must have access to https://www.synopsys.com/designware-ip.html to download the release image. You can sign up to receive updates for any designware component through this web site as well.

1.4 Checking License Requirements

This section provides the required license information needed to use the controller. The PCI Express (PCIe) controller licensing scheme is modified in release version 5.10a. The legacy licensing scheme (prior to release version 5.10a) is still supported by the PCIe controller. If the new licenses and legacy licenses are detected simultaneously, the new licenses suppress the legacy licenses.

1.4.1 PCI Express Controller Licenses (Release Version 5.10a Onwards)

Table 1-3 lists the licenses needed for a regular configuration of the PCI Express (PCIe) controller. Figure 1-1 and Figure 1-2 list the features included in each PCIe controller license.

Table 1-3 PCIe Controller Regular Licenses

Conventional PCIe Gen Mode X is 2,3,4, 5[a], or 6[b]	Support Type	AMBA Bridge	License X is 2,3,4,5, or 6
Gen**X**	Standard	No	DWC-PCIE-G**X**-STND-N-SRC
Gen**X**	Plus	No	DWC-PCIE-G**X**-PLUS-N-SRC
Gen**X**	Premium	No	DWC-PCIE-G**X**-PREM-N-SRC
Gen**X**	Premium II	No	DWC-PCIE-G**X**-PREM-N-V2-SRC
Gen**X**	Standard	Yes	DWC-PCIE-G**X**-STND-A-SRC
Gen**X**	Standard II	Yes	DWC-PCIE-G**X**-STND-A-V2-SRC
Gen**X**	Plus	Yes	DWC-PCIE-G**X**-PLUS-A-SRC
Gen**X**	Plus II	Yes	DWC-PCIE-G**X**-PLUS-A-V2-SRC
Gen**X**	Premium	Yes	DWC-PCIE-G**X**-PREM-A-SRC
Gen**X**	Premium II	Yes	DWC-PCIE-G**X**-PREM-A-V2-SRC

a. Standard II, Plus II, and Premium II licenses are available for PCIe Gen2 mode and above till Gen5.
b. Premium and Premium AMBA licenses are available for PCIe Gen6.

Figure 1-1 Features Included in PCIe Controller (Without AMBA Bridge) Regular Licenses

Standard Features	Access Control Services (ACS)
	AER Header Log Multiple Entry
	Alternative Routing-Id Interpretation (ARI)
	Address Translation Unit (ATU)
	Crosslink
	Dynamic Power Allocation (DPA)
	Function Readiness Status (FRS)
	FRS Queue (FRSQ)
	Readiness Notification (RN)
	PIPE Hybrid Mode
	ID Based Ordering (IDO)
	L1 Sub-states (L1SS)
	Lightweight Notification (LN)
	Latency Tolerance Reporting (LTR)
	MSIX Table
	Number of Functions (NF) >1
	Optimized Buffer Fill Flush (OBFF)
	Readiness Time Reporting (RTR)
	32-128 Bits Data Width
	Emergency Power Reduction (PWRBRK)

Premium Features	**All Plus Features, and**
	Address Translation Service (ATS)
	DMA
	Extensible IOV
	Header Log Shared amongst VFs
	Process Address Space ID (PASID)
	Page Request Services (PRS)
	RAS DES
	Single Root I/O Virtualization (SR-IOV)
	TLP Prefix
	VF Header Log Multiple Entry
	VF Resizable BAR
	Number of Virtual Channels (VC) >1
	Virtual Functions (VFs)
	Tx Interface Progression Detection
	32-512 Bits Data Width

Plus Features	**All Standard Features, and**
	Native PCIe Enclosure Management (NPEM)
	Peer-to-Peer (P2P)
	Power Gating
	PHY Power Management
	Precision Time Measurement (PTM)
	RAS DP
	RAS DP RAM ECC
	Resizable BAR
	TLP Processing Hints (TPH)
	32-256 Bits Data Width
	Downstream Port Containment (DPC)
	eDPC

Premium II Features	**All Premium Features, and**
	HDMA
	Deferrable Memory Writes (DMWr)
	Embedded End Point (EEP)

Figure 1-2 Features Included in PCIe Controller With AMBA Bridge Regular Licenses

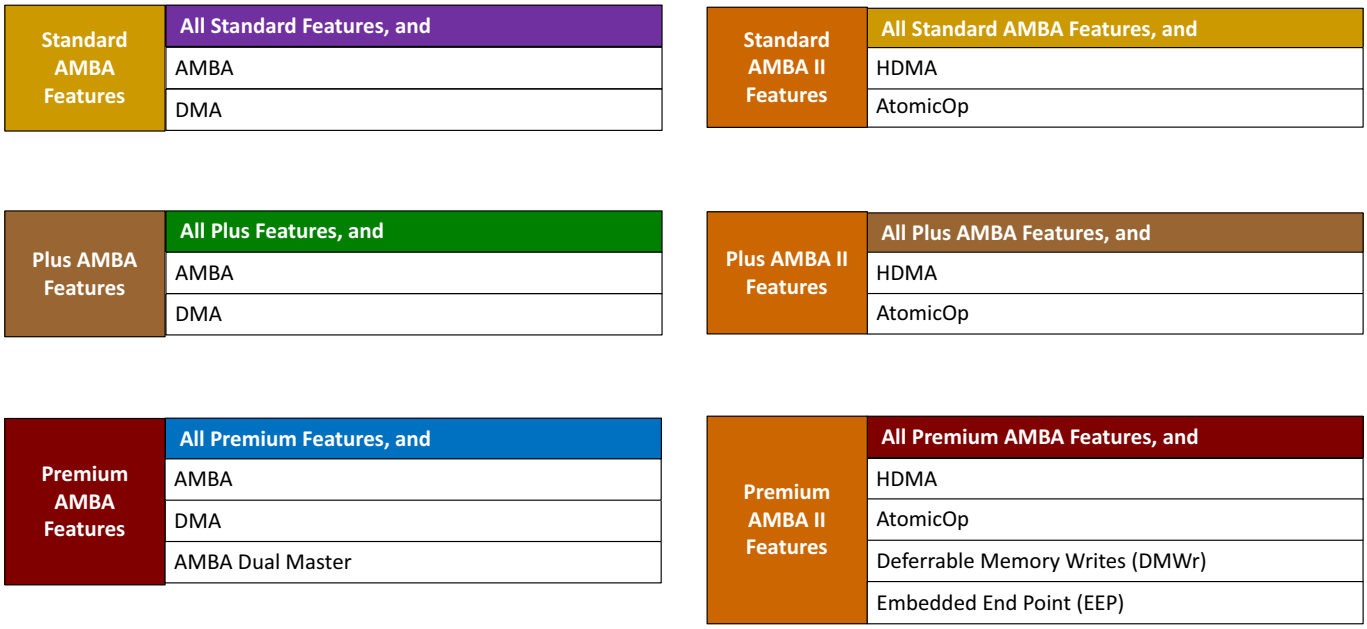
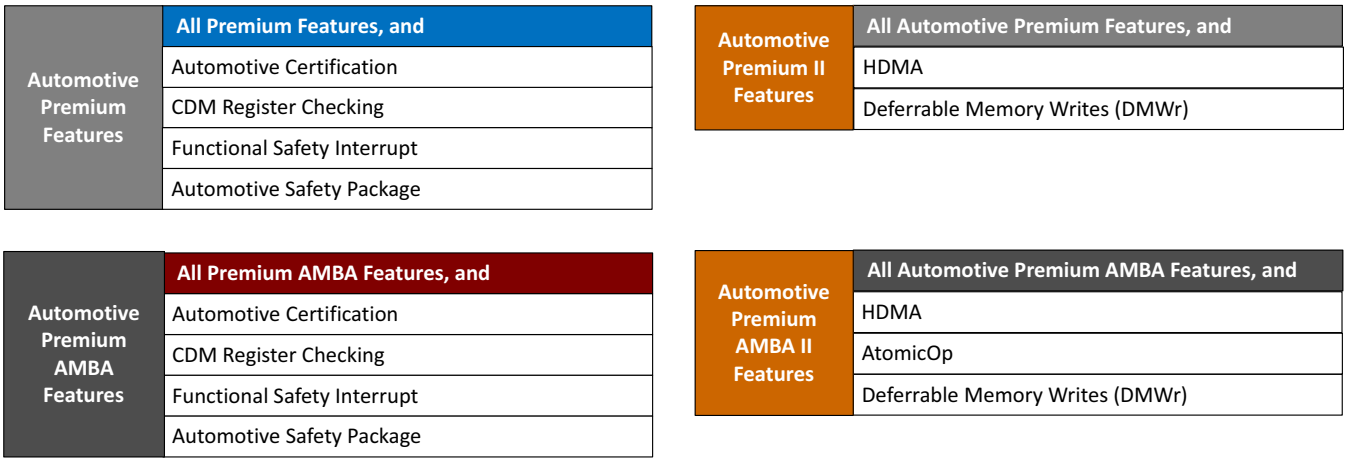


Table 1-3 lists the licenses needed for a regular configuration of the PCI Express (PCIe) controller. Figure 1-3 lists the features included in each PCIe controller license.

Table 1-4 Automotive PCIe Controller Licenses

Conventional PCIe Gen Mode X is 2,3,4, or 5	Support Type	AMBA Bridge	License X is 2,3,4, or 5
Gen**X**	Premium	No	DWC-AP-PCIE-G**X**-PREM-N-SRC
Gen**X**	Premium II	No	DWC-AP-PCIE-G**X**-PREM-N-V2-SRC
Gen**X**	Premium	Yes	DWC-AP-PCIE-G**X**-PREM-A-SRC
Gen**X**	Premium II	Yes	DWC-AP-PCIE-G**X**-PREM-A-V2-SRC
Gen**X**	Premium II	No	DWC-AC-PCIE-G**X**-PREM-N-SRC
Gen**X**	Premium II	Yes	DWC-AC-PCIE-G**X**-PREM-A-SRC

Figure 1-3 Features Included in Automotive PCIe Controller Licenses



If you have, for example, a Gen3 license (`DWC-PCIE-G3-type-N-SRC, DWC-PCIE-G3-type-A-SRC` (type: STND, PLUS, or PREM), `DWC-AP-PCIE-G3-PREM-N-SRC`, or `DWC-AP-PCIE-G3-PREM-A-SRC`), you cannot create a Gen1 or Gen2 configuration. You can only generate a Gen3 configuration that you could operate in Gen1, or in Gen2 mode. The RTL for this configuration is much different to that of a pure Gen1 or Gen2 configuration.

If you have a `DWC-PCIE-GX-type-A-SRC` (**X**: 2-5; type: STND, PLUS, or PREM) or a `DWC-AP-PCIE-GX-PREM-A-SRC` (**X**: 1-5) license, you can get DMA without AXI configuration by turning off AXI. Or, you can turn off DMA to get an AXI only configuration.

Table 1-5 CXL Controller Licenses

CXL Mode	Support Type	AMBA Bridge	License
CXL 3.0	Premium	No	DWC-CXL-30-PREM-N-SRC
CXL 3.0	Premium	Yes	DWC-CXL-30-PREM-A-SRC
CXL 2.0[a]	Premium	No	DWC-CXL-20-PREM-N-SRC
CXL 2.0	Premium	Yes	DWC-CXL-20-PREM-A-SRC

a. CXL 2.0 controller is backward compatible with the CXL1.1 controller. So if you have a CXL2.0 license, you can configure the controller in CXL1.1 mode as well.

Figure 1-4 CXL License Features And HPC License Features (for CXL and PCIe)

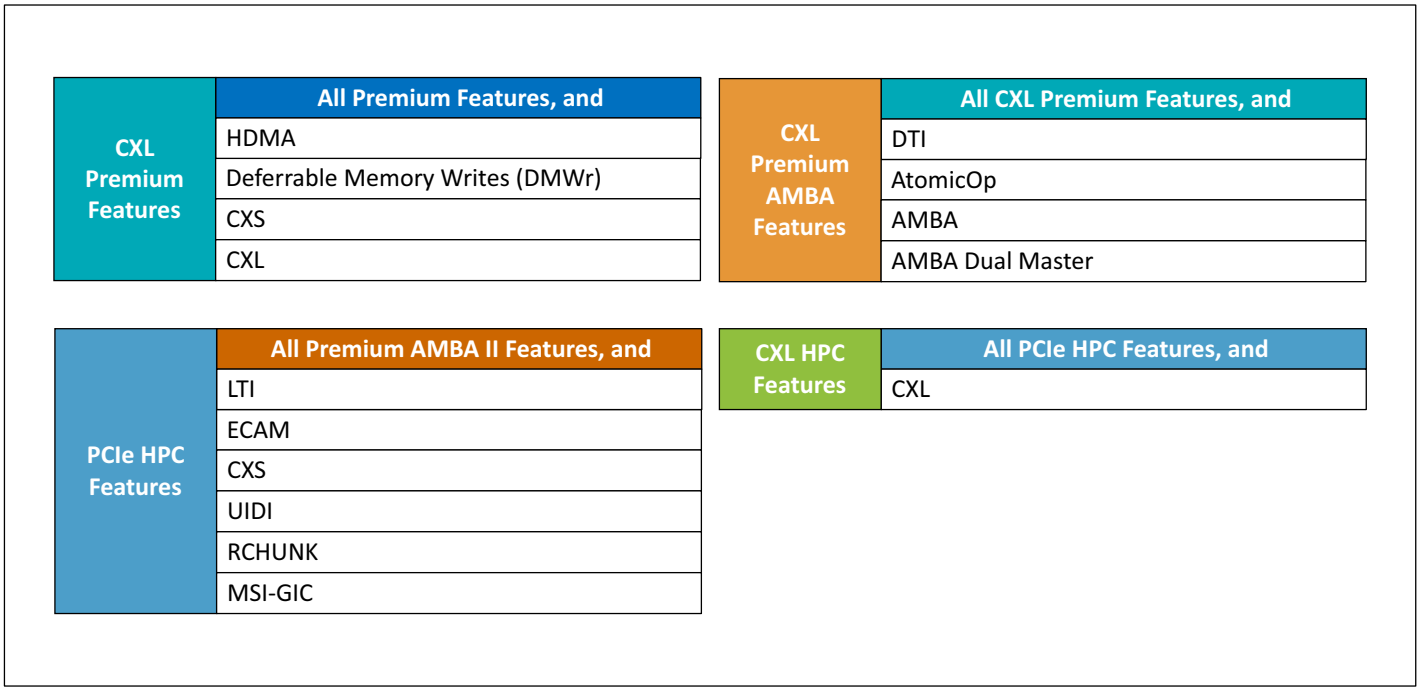


Table 1-6 CCIX PCIe Controller Licenses

Conventional PCIe Gen Mode	Support Type	AMBA Bridge	License
Gen4	Premium II	No	DWC-CCIX-G25-PREM-N-V2-SRC
Gen4	Premium II	Yes	DWC-CCIX-G25-PREM-A-V2-SRC
Gen5	Premium II	No	DWC-CCIX-G32-PREM-N-V2-SRC
Gen5	Premium II	Yes	DWC-CCIX-G32-PREM-A-V2-SRC

Table 1-7 PCIe Controller for USB4 Licenses

Conventional PCIe Gen Mode	Support Type	AMBA Bridge	License
Gen1	Premium	No	DWC-PCIE-USB4-PREM-N-SRC
Gen1	Premium	Yes	DWC-PCIE-USB4-PREM-A-SRC

Table 1-8 PCIe Controller for EEP Licenses

Conventional PCIe Gen Mode	Support Type	AMBA Bridge	License
Gen1	Premium	No	DWC-PCIE-EEP-PREM-N-SRC
Gen1	Premium	Yes	DWC-PCIE-EEP-PREM-A-SRC

Table 1-9 PCIe and CXL Controller for IDE Licenses

Conventional Gen Mode	Support Type	License
PCIe Gen1-Gen5	Security Interface Add-on	DWC-PCIE-G5-SECURITY
PCIe Gen6	Security Interface Add-on	DWC-PCIE-G6-SECURITY
CXL 2.0	Security Interface Add-on	DWC-CXL-20-SECURITY
CXL 3.0	Security Interface Add-on	DWC-CXL-30-SECURITY

Table 1-10 PCIe and CXL Controller for HPC Licenses

Conventional PCIe Gen Mode	Support Type	AMBA Bridge	License
Gen4	Premium	Yes	DWC-PCIE-G4-PREM-A-HPC-SRC
Gen5	Premium	Yes	DWC-PCIE-G5-PREM-A-HPC-SRC
Gen6	Premium	Yes	DWC-PCIE-G6-PREM-A-HPC-SRC
CXL 2.0	Premium	Yes	DWC-CXL-20-PREM-A-HPC-SRC
CXL 3.0	Premium	Yes	DWC-CXL-30-PREM-A-HPC-SRC

1.4.2 Setting License File Environment Variable

Make sure that your product's license keys are installed on your license server. For more information about installing license keys, consult https://www.synopsys.com/support/licensing-installation-computeplatforms/installation.html and the "Synopsys Licensing QuickStart Guide" at https://www.synopsys.com/support/licensing-installation-computeplatforms/licensing.html.

You must set the `LM_LICENSE_FILE` environment variable to include a pointer to a license server that contains your PCI Express license key.

Note You must set this environment variable BEFORE you install the .run file; otherwise, only encrypted source files are installed and you receive errors if you try to configure the PCI Express Controller using coreConsultant.

To set the license file environment variable:

1. Set the license variable to include your license file or to point to your license server. Use either of:

```
% setenv LM_LICENSE_FILE ${LM_LICENSE_FILE}:<my_license_file>
% setenv LM_LICENSE_FILE ${LM_LICENSE_FILE}:<port@host>
```

2. Verify the license setup:

```
% echo $LM_LICENSE_FILE
% lmstat -a -c $LM_LICENSE_FILE -f DWC-PCIE-DM-32BX4
```

Note Use these commands to check the license setup for all of your component's required licenses as described in "Checking License Requirements" on page 11.

If you encounter any problems setting the license file environment variable, see "Licensing" on page 28.

Caution SNPSLMD_LICENSE_FILE variable must be set to LM_LICENSE_FILE, or left undefined. Otherwise, coreConsultant cannot locate the license key.

1.5 Installing the PCI Express Controller

This section provides required steps and information to download and install the PCI Express Controller image.

1.5.1 Downloading PCI Express Controller

The latest version of the PCI Express Controller is available through the DesignWare Download Web site.

1. Go to https://www.synopsys.com/dw/mydesignware.php (a SolvNetPlus ID is required).
2. Expand DesignWare Cores and select the **PCI Express** product for which you have a license.
3. Click **dw_iip_DWC_pcie_ctl** on the IP Directory Component Detail page.
4. For PCIe Controller: Click **dw_iip_DWC_pcie_ctl_6.00a.run** on the Designware Download page to download the file to a Unix file server.

   For PCIe Automotive Controller: Click **dw_iip_ap_DWC_ap_pcie_ctl_6.00a.run** on the Designware Download page to download the file to a Unix file server.

   Make sure to save the .run file to a directory outside of any existing DESIGNWARE_HOME tree.

1.5.2 Setting Up Your Environment

Before you install the PCI Express Controller's .run file, you must set the following environment variables.

1. Set the `DESIGNWARE_HOME` environment variable to your installation directory:

   ```
   % setenv DESIGNWARE_HOME <path to PCI Express Controller_Installation_Base_Directory>
   ```

2. Set the `LM_LICENSE_FILE` variable, if you have not already done so. Use either of:

   ```
   % setenv LM_LICENSE_FILE ${LM_LICENSE_FILE}:<my_license_file>
   ```

   ```
   % setenv LM_LICENSE_FILE ${LM_LICENSE_FILE}:<port@host>
   ```

3. Include the following in your PATH environment variable:

   `$DESIGNWARE_HOME/bin`

   `$DESIGNWARE_HOME/bin` is required in your PATH environment variable as it contains the, dwh_install, and dw_vip_setup scripts, which provide important diagnostic information in coreConsultant about the version of your DWC components. For more information, see Table A-1 on page 29.

Table 1-1 summarizes the environment variables you might need to set when using the PCI Express Controller. The example .setup file in "Example of Setup File" on page 36 shows how to configure the commonly used environment variables for the PCI Express Controller.

1.5.3 Installing the PCI Express Controller

The .run file you downloaded is a self-extracting image that installs itself and performs some set-up operations.

For more information about command options, enter:

```
% ./dw_iip_DWC_pcie_ctl_6.00a.run --help
```

For a list of the .run file command options, see "Options for .run Files" on page 37.

1. Change permissions on the downloaded .run file:

   ```
   % chmod u+x dw_iip_DWC_pcie_ctl_6.00a.run
   ```

   If you want to view the README information before performing the installation:

   ```
   % dw_iip_DWC_pcie_ctl_6.00a.run --readme
   ```

2. Execute the .run file:

   ```
   % dw_iip_DWC_pcie_ctl_6.00a.run
   ```

3. When prompted, enter the Project ID that you specified at the time of purchase. Without a project ID, encrypted files are installed.

For tips on how you can debug problems with installation, see "Troubleshooting and Support" on page 27.

1.5.4 Installing Automotive PCI Express Controller

The .run file you downloaded is a self-extracting image that installs itself and performs some set-up operations.

For more information about command options, enter:

```
% ./dw_iip_ap_DWC_ap_pcie_ctl_6.00a.run --help
```

For a list of the .run file command options, see "Options for .run Files" on page 37.

1. Change permissions on the downloaded .run file:

   ```
   % chmod u+x dw_iip_ap_DWC_ap_pcie_ctl_6.00a.run
   ```

   If you want to view the README information before performing the installation:

   ```
   % dw_iip_ap_DWC_ap_pcie_ctl_6.00a.run --readme
   ```

2. Execute the .run file:

   ```
   % dw_iip_ap_DWC_ap_pcie_ctl_6.00a.run
   ```

3. When prompted, enter the Project ID that you specified at the time of purchase. Without a project ID, encrypted files are installed.

For tips on how you can debug problems with installation, see "Troubleshooting and Support" on page 27.

1.5.5 Deliverables

The deliverables for the PCIe controllers include:

- Synthesizable RTL source code compliant with IEEE Standard for SystemVerilog - Unified Hardware Design, Specification, and Verification Language IEEE Std 1800™-2012.
- Synopsys coreConsultant tool for automated configuration, synthesis, and simulation
- Synopsys PHY simulation model to be used as placeholder for simulation purposes only.
- A Verilog Testbench (VTB)
  - Allows you to re-execute the example tests on your configuration of the controller for the purpose of sanity checking your generated RTL in coreConsultant environment before moving the RTL to your SoC level verification.
  - Demonstrates connectivity and many types of transfers.
  - VTB is not intended for extensive verification.

Note	The VC VIP library license shipped with the controller is intended only to verify the controller interfaces in a specific controller configuration out-of-the-box in the coreConsultant, to confirm that the controller meets the requirements. Do not use this VC VIP library license as a full-featured verification model at the subsystem or SoC level.

- Software Samples and Drivers
  - A Linux driver for PCIe RP controller is available at: https://git.kernel.org/pub/scm/linux/kernel/git/stable/linux.git/tree/drivers/pci/controller/dwc/pcie-designware.c

    This driver is provided by Synopsys as an example, and is not subject to warranty, support, or maintenance.
  - A software sample of the PCIe controller is available at: https://www.synopsys.com/dw/ipdir.php?c=dwc_pcie_controller_sw_samples

    The DesignWare PCIe IP software sample provides information about how you can use the pre-built images for testing the PCIe controller.

1.5.5.1 Verification Environment Overview

The verification environment for the controller includes a packaged VTB and separate VIP components. The VTB runs the packaged self-checking regression tests through coreConsultant to validate the configured controller. For more information, see the “Simulating the Controller” section in the *User Guide*.

1.5.5.2 CoreConsultant Overview

The Synopsys coreConsultant tool allows you to configure, simulate, synthesize, and export the controller to your design flow. The final output from the coreConsultant design flow is a set of RTL files (the configured RTL controller) and scripts to allow you run various standalone tests within your own design flow. The coreConsultant features and tasks include:

- A Graphical User Interface (GUI) to guide you through design flow activities.

  All activities may also be performed through a command line interface.
- Interactive parameter selection.

  The coreConsultant tool checks for consistent settings and automatically derives any dependent parameters from your choices.
- Testbench simulation and synthesis configuration consistent with your parameter choices.

1.5.5.3 Synthesis Overview

The coreConsultant tool is your interface to Synopsys tools for ASIC synthesis of the controller. Synthesis scripts and constraints can be exported from coreConsultant and reused with non-Synopsys tools to synthesize the controller in your own design flow.

1.6 Installing Tools and Verification IP Components

This section includes information for the supported tools that allow you to configure, synthesize, and verify the controller. Instructions for installing coreConsultant, and VIP are also provided in this section. If you need to install a synthesis or simulation tool, see the product documentation for that specific product.

1.6.1 Verifying Supported Tool Versions and Verification IP Components

The tools listed in Table 1-11 have been tested for use with the PCI Express Controller product.

Attention

- You must use the tool and VIP versions specified in Table 1-11. Older or newer tool versions might work, but are NOT supported or verified.
- You must use the operating system version specified in

  https://www.synopsys.com/support/licensing-installation-computeplatforms/licensing/scl-supported-os.html

Table 1-11 Supported Tool Versions

Tool	Supported Versions	Purpose
IP Configuration Tools		
coreConsultant	2022.06	Used for configuring the controller, and running simulation, and synthesis tools
coreAssembler	2022.06	Configure, automatically interconnect, and synthesize multiple Synopsys IP components.
Verilog RTL Simulation Tools		
Synopsys VCS[a]	2021.09	No VHDL RTL simulators are supported.
IP Implementation Tools		
Design Compiler (DC)	2022.03	ASIC Synthesis (contains DFT Compiler)
Formality	2022.03	Formal verification
PrimeTime	2022.03	Timing and signal integrity
Fusion Compiler	2022.03	RTL to GDSII implementation
Spyglass	2021.09-SP1	Lint, CDC, RDC, and DFT Tool
VC Spyglass	2021.09-SP1	Lint, CDC, and RDC Tool
Synplicity	2021.09	FPGA Synthesis
ProtoCompiler	2020.12-SP1	FPGA Synthesis for HAPS
Xilinx Vivado	2022.1	Xilinx Vivado should be used to simulate Virtex 7 based PHYs.
RTL Architect	2022.03	Early physically aware RTL exploration.

Tool	Supported Versions	Purpose
VIP for Verilog Testbench (VTB)		
Synopsys VIP Library	T-2022.03	Used by the VTB simulations. Two licenses are included with the controller. You must download the VIP and install in $DESIGNWARE_HOME as outlined in "Downloading and Installing Verification IP Components" on page 24. **Note:** Contact Synopsys support through SolvNet to download VIP Version IDE feature.
PCIe SVT VIP	T-2022.03	
AMBA SVT VIP	S-2021.12	
CXL Subsystem SVT VIP	T-2022.03	
Python	3.8.1 and above	VTB simulations require Python to setup the VIPs.
Performance Analysis		
DBD-SQLite	1.58	Used in the performance analysis flow
Perl	5.8.3	Perl DBI is used for driving the SQLite database in the performance analysis flow

a. You need a VCS license to run simulations. Compilation and elaboration of the RTL source code with NCSim and ModelSim/QuestaSim is supported. But compilation, elaboration, or simulation of packaged customer deliverables with NCSim and ModelSim/QuestaSim is not supported.

System Verilog RTL Design of the controller is compliant with IEEE Standard for SystemVerilog - Unified Hardware Design, Specification, and Verification Language IEEE Std 1800™-2012

Synopsys recommends DC-NXT for front-end synthesis.

Full RTL to GDSII flow with Fusion Compiler is not possible within coreConsultant.

Synopsys recommends you use coreConsultant to generate design constraints and, optionally, Fusion Compiler Reference Methodology (FCRM) scripts for execution in your own implementation flow.

1.6.2 Setting Environment Variables for Tools and Verification IP

This section provides a summary of the environment variables.

Table 1-12 Environment Variables for PCI Express Controller

Environment Variable	Description
DESIGNWARE_HOME	Path to the PCI Express Controller installation base directory

Environment Variable	Description
LM_LICENSE_FILE	Path to license file for Synopsys tools such as Design Compiler, VCS, PrimeTime, any third-party tool) SNPSLMD_LICENSE_FILE variable must be set to LM_LICENSE_FILE, or left undefined. Otherwise, coreConsultant cannot locate the license key.
SYNOPSYS	Path to Synopsys tools tree (Design Compiler, VCS); not a required variable
VRO_CACHE_DIR	Path to the directory where VIP compilation is done. This is an optional environment variable that you can use to create .vro files outside the $DESIGNWARE_HOME directory.
LD_LIBRARY_PATH	Path to tools and OS libraries
VCS_HOME	Path to VCS installation directory
VCS_CC	Path to SunPro C or gcc compiler
PATH	Must include the following paths: ■ $DESIGNWARE_HOME/bin ■ $SYNOPSYS/bin ■ $SYNOPSYS/<platform>/syn/bin ■ Path to coreConsultant bin/ directory ■ Path to Formality bin/ directory (if used) ■ Paths to simulator binaries: ❑ $VCS_HOME/bin
XILINX	Path to the Xilinx ISE tools tree
QUARTUS_ROOTDIR	Path to the Altera Quartus tools tree
LMC_HOME	The Xilinx Rocket I/O simulation models require the LMC_HOME environment variable to be set. When the Xilinx ISE tools are installed then the LMC_HOME variable usually points to: LMC_HOME=$XILINX/smartmodel/lin/installed_lin Where the SWIFT models are not installed in the previous path, then you must use 'compxlib' to compile the SWIFT models and point the LMC_HOME to the location where the models are located. Also the LD_LIBRARY_PATH has to be updated as follows LD_LIBRARY_PATH=$LMC_HOME/lib/linux.lib:$LD_LIBRARY_PATH For further information on Rocket IO simulation models, see Xilinx documentation

1.6.3 Downloading and Installing coreConsultant

Synopsys' coreConsultant is a tool that you use to configure, verify, and synthesize the PCI Express Controller. If you do not have a supported version of coreConsultant installed on your system or network, you must download and install it.

1. Download coreConsultant from the SolvNetPlus Download Center, at: https://solvnet.synopsys.com/DownloadCenter/dc/product.jsp
2. Select coreConsultant version mentioned in Table 1-11 and download two files: a common file and a platform-specific file.
3. Install coreConsultant following the instructions in *coretools_INSTALL_README.txt*
4. Add the path to the coreConsultant binary path variable in your .cshrc file:

   ```
   % vi ~/.cshrc
   set path = ($path <Tools_Directory>/<version#>/bin)
   % source ~/.cshrc
   % rehash
   ```

5. Verify the coreConsultant installation:

   ```
   % which coreConsultant
   ```

   This command must return the path to your coreConsultant installation location.

1.6.4 Downloading and Installing Verification IP Components

The testbench provided with PCI Express Controller uses Verification IP. If you do not have supported versions of VIP installed (specified in Table 1-11), then you must download and install them.

1. Download "*Synopsys VIP Library*" from the SolvNetPlus Download Center, at: https://solvnet.synopsys.com/DownloadCenter/dc/product.jsp
2. Select "VC VIP Library" version mentioned in Table 1-11 and download the following files:
   - vip_pcie_svt_<*vip version*>.run
   - vip_amba_svt_<*vip version*>.run
   - vip_cxl_subsystem_svt_<*vip version*>.run
3. Install the VIP in $DESIGNWARE_HOME by following the instructions in *Synopsys_VC_VIP_Library_README.txt*

1.7 Next Steps

Now that you have completed installation and set up your environment, the next steps are to configure, synthesize, simulate, and export your PCI Express Controller into your design.

Read the *DesignWare Cores PCI Express Controller Databook* and *User Guide* to learn about the PCI Express Controller and the configuration options. The documents are available in the doc directory of your workspace (*workspace/doc/*). The documents are also available in the coreConsultant Help Menu.

1. Create a workspace for the PCI Express Controller.

   A workspace is a local copy of your DWC_pcie_ctl controller installation in which you can configure, verify, and synthesize your own implementation of the DWC_pcie_ctl.

   To create a workspace:

   a. Invoke coreConsultant:

      ```
      % coreConsultant &
      ```

   b. Create a new workspace:

      i. Select **File > New Workspace** in the coreConsultant console.

      ii. Enter the requested information in the New Workspace dialog box.

      iii. Optionally, for "Installed coreKit path": select <*install_dir*>*/iip/DWC_pcie_ctl/latest*.

2. Complete the Specify Configuration activity using the default parameter values. Click Apply in the Specify Configuration dialog.

   This creates the RTL for the default configuration and populates the product documentation (in *workspace/latest/doc*).

 **Note** You can create several workspaces so that you can experiment with different design alternatives.

A

Troubleshooting and Support

This appendix provides troubleshooting information and details on how to contact customer support should you need further assistance during installation and set up.

A.1 Troubleshooting

This section provides troubleshooting tips if you encounter problems with licensing, installation, setting up your environment, and supported tools.

A.1.1 Licensing

Q: *I did a source installation, but when I invoked coreConsultant to configure the controller, I got encrypted RTL. Why?*

A: You receive this error when your source installation was not done properly. Either the Project ID (PID) was not entered correctly or not entered at all, or the LM_LICENSE_FILE was not set properly—that is, not pointing to the server that has a source license. You must set either the LM_LICENSE_FILE environment variable BEFORE you install the controller. For more information about setting this environment variable, see "Setting License File Environment Variable" on page 16. The SNPSLMD_LICENSE_FILE variable must be set to LM_LICENSE_FILE, or left undefined. Otherwise, coreConsultant cannot locate the license key.

A.1.2 Installation

Q: *How can I make sure that the source installation was done properly?*

A: You can make sure that the source installation was done properly in one of two ways:

Configure the IP in coreConsultant and check the <workspace>/src directory for source RTL.

The .run installer script writes out a log file that you can use to debug any issues with installation. The log file is located in the installation directory and is named as follows:

<image>_<yyyymmdd>_<hhmmss>_<processid>.log

By default, this log file is retained only if errors occur; it is removed if installation completes successfully. To retain the log file irrespective of the installation status, you can use the `--keep-log` switch with the .run installer script:

./<product_name>_<version>.run --keep-log

Note

A source license gives you access to all of the files when you configure your controller. If you do not have a source license, you only have access to a limited number of files (such as, the top-level <controller_name>.v and the <controller_name>_cc_constants.v files). The remainder of the files are encrypted.

Q: *During installation, I get the following message, "Not enough disk space". Why?*

A: Some organizations limit the maximum allowable disk space for individual users. Check to ensure you have the proper requirements.

Q: *How do I verify that I installed the DWC_pcie_ctl correctly?*

A: After you have correctly downloaded and installed the controller, the product deliverables are unpacked into the $DESIGNWARE_HOME directory (environment variable you set that points to the DWC_pcie_ctl's installation root directory).

To view the contents of the DWC_pcie_ctl directory in the $DESIGNWARE_HOME path, enter the following command at a Unix prompt:

```
% ls -l $DESIGNWARE_HOME/iip/DWC_pcie_ctl/latest
```

Note The latest directory is a symbolic link to the DWC_pcie_ctl/<current_version> directory.

"DESIGNWARE_HOME Directory Structure" on page 39 illustrates the directory structure after you have installed the DWC_pcie_ctl product in the $DESIGNWARE_HOME directory.

Q: *How can I verify the version of my installed DesignWare Cores product to make sure I have the latest version?*

A: To verify whether your DesignWare Cores products are current, use one of the following methods:

Subscribe to MyDesignWare notifications on a component basis, where you receive an e-mail when a component updates or has new/updated STAR information.

Enable automatic update checking in coreConsultant to check the components in your design against both your DesignWare Cores and the currently supported Synopsys components.

Table A-1 provides more information about these features.

Table A-1 DesignWare Component Update Features

DesignWare Update Feature	Description
MyDesignWare Notifications	Enables you to receive product updates, technical articles, in-depth application notes and more for products of interest to you. You can add or remove selected subscriptions at any time. Sign-up through your SolvNet user account at: https://www.synopsys.com/dw/mydesignware.php MyDesignWare subscriptions include: ■ DesignWare Technical Bulletin ■ DesignWare Component Notifications
coreTools Update Checking	When you complete the Specify Configuration activity in coreConsultant, it checks your component version against the most recent versions available both for download from Synopsys, and in your local $DESIGNWARE_HOME library. A report gives you newer version information, if available, and lists STARs created/fixed for the components you are using. You can manually check at any time using Help > Check for IP Updates. For more information about Automatic/Manual IP update checks in coreConsultant, see "Component Update Checking" in the *coreConsultant User Guide*. NOTE: Components are not automatically updated; this operation only generates a report. You must make these component updates manually.

A.1.3 Tools

Q: *I have a DesignWare license and installed the image properly. When I invoke coreConsultant, I get the following message, "Command not found" Why?*

A. You get this message because coreConsultant was not installed or the $PATH is not updated with the path to the coreConsultant tool installation directory. It is not a part of an image and has to be installed separately. For more information about installing coreConsultant, see"Downloading and Installing coreConsultant" on page 24. The other possibility is not having DESIGNWARE_HOME/bin in the PATH.

Q: *How can I tell if coreConsultant installed?*

A: Issue the following command, which should return the path to your coreConsultant installation directory. If not, complete the steps in "Downloading and Installing coreConsultant" on page 24.

```
% which coreConsultant
```

Q:*How can I verify if my tools are correctly set up to work with coreConsultant?*

A: After completing the DWC_pcie_ctl installation and setting the required environment variables, confirm system and coreConsultant access to the tools:

1. Check that you have access to the supported tools specified in Table 1-11, as follows:

   ```
   % echo $SYNOPSYS
   % which coreConsultant
   % which <verilog_simulator>
   ```

2. Set DESIGNWARE_HOME to the DWC_pcie_ctl installation base directory where you installed the DWC_pcie_ctl files, then invoke coreConsultant:

   ```
   % setenv DESIGNWARE_HOME <PCI_Express_Installation_Base_Directory>
   % coreConsultant &
   ```

3. Click the DWC_pcie_ctl link to create a new configuration.
4. In the coreConsultant menu bar, select Edit > Tool Installation Roots to verify valid versions of all tools needed. These might include:
   - Design Compiler (dc_shell)
   - PrimeTime (pt_shell)
   - Formality (fm_shell)
   - TestMAX™ (tmax)
   - Synplify FPGA (synplify)

   If you want to use the 64-bit execution, then check if you selected the 64-bit option in Edit -> Tool Installation Roots
5. Exit coreConsultant by selecting File > Exit from the menu bar.

A.2 Synopsys Statement on Inclusivity and Diversity

Synopsys is committed to creating an inclusive environment where every employee, customer, and partner feels welcomed. We are reviewing and removing exclusionary language from our products and supporting customer-facing collateral. Our effort also includes internal initiatives to remove biased language from our engineering and working environment, including terms that are embedded in our software and IPs. At the same time, we are working to ensure that our web content and software applications are usable to people of varying abilities. You may still find examples of non-inclusive language in our software or documentation as our IPs implement industry-standard specifications that are currently under review to remove exclusionary language.

A.3 Customer Support

To obtain support for your product, prepare the required files and contact the support center using one of the methods described:

- Prepare the following debug information, if applicable:
  - For environment set-up problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, select the following menu:
    - **File > Build Debug Tar-file**

    Check all the boxes in the dialog box that apply to your issue. This option gathers all the Synopsys product data needed to begin debugging an issue and writes it to the <*core tool startup directory*>/debug.tar.gz file.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD).
    - Identify the hierarchy path to the DesignWare instance.
    - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- *For the fastest response*, enter a case through SolvNetPlus:

  a. https://solvnetplus.synopsys.com

Note SolvNetPlus does not support Internet Explorer. Use a supported browser such as Microsoft Edge, Google Chrome, Mozilla Firefox, or Apple Safari.

  b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).

  c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

  Make sure to include the following:
  - **Product L1:** DesignWare Cores
  - **Product L2:** PCI Express

  d. After creating the case, attach any debug files you created.

  For more information about general usage information, refer to the following article in SolvNetPlus:

  https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources

- Or, send an e-mail message to mailto:support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
  - Attach any debug files you created.
- Or, telephone your local support center:

- North America:
  Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
- All other countries:
  https://www.synopsys.com/support/global-support-centers.html

B

Example Setup File

The following example setup file demonstrates how to configure the required environment. The example shows all three supported simulation tools. Choose the commands for the tool you are using. In all cases, replace the example directory paths and placeholders (in <...>) with the correct paths and terms for your tool installations.

Note When you create your setup file, you might want to name it *.setup* and then place it in the root of your DWC PCI Express product installation directory.

B.1 Example of Setup File

```
# Synopsys Setup
setenv SYNOPSYS <synopsys_install_dir>
set path = ($path $SYNOPSYS/bin)
set path = ($path $SYNOPSYS/<platform>/syn/bin)
# DESIGNWARE_HOME
setenv DESIGNWARE_HOME <PCI_Express_Installation_Base_Directory>
# coreConsultant Setup
set path = ($path <cC_install_dir>/bin)
# VCS Setup
setenv VCS_HOME <vcs_install_dir>
setenv VCS_CC /opt/SUNWspro/bin/cc
set path = ($path ${VCS_HOME}/bin)
# Formality Setup
set path = ($path <fm_install_dir>/bin )
# License Setup
setenv LM_LICENSE_FILE ${LM_LICENSE_FILE}:<my_license_file|port@host>
```

C

Options for .run Files

The .run (`dw_iip_DWC_pcie_ctl_6.00a.run` or `dw_iip_DWC_pcie_ap_ctl_5.71a.run`) file is a self-extracting image that contains the product (`DWC_pcie_ctl` or `DWC_pcie_ap_ctl`). Executing the .run file without optional switches extracts (installs) the image to a $DESIGNWARE_HOME, if available, or to a specified directory.

You can choose only one of the following optional switches:

--help	Displays this message and exits.
--readme	Displays additional installation information, if available and exits.
--check	Checks image integrity and exits.
--dir <path>	Installs product into <path> instead of $DESIGNWARE_HOME

If you are doing an installation, you can use either of the following options:

--keep-log	Keeps the installer log file regardless of the error count. By default, the log is deleted when there are no errors.
--quiet	Eliminates confirmation prompts.

D

DESIGNWARE_HOME Directory Structure

This appendix provides examples of a DESIGNWARE_HOME directory—a top-level view and the controller directory structure **after** you have installed the controller into the DESIGNWARE_HOME directory.

Figure D-1 Example of a DESIGNWARE_HOME Directory - Top-Level View

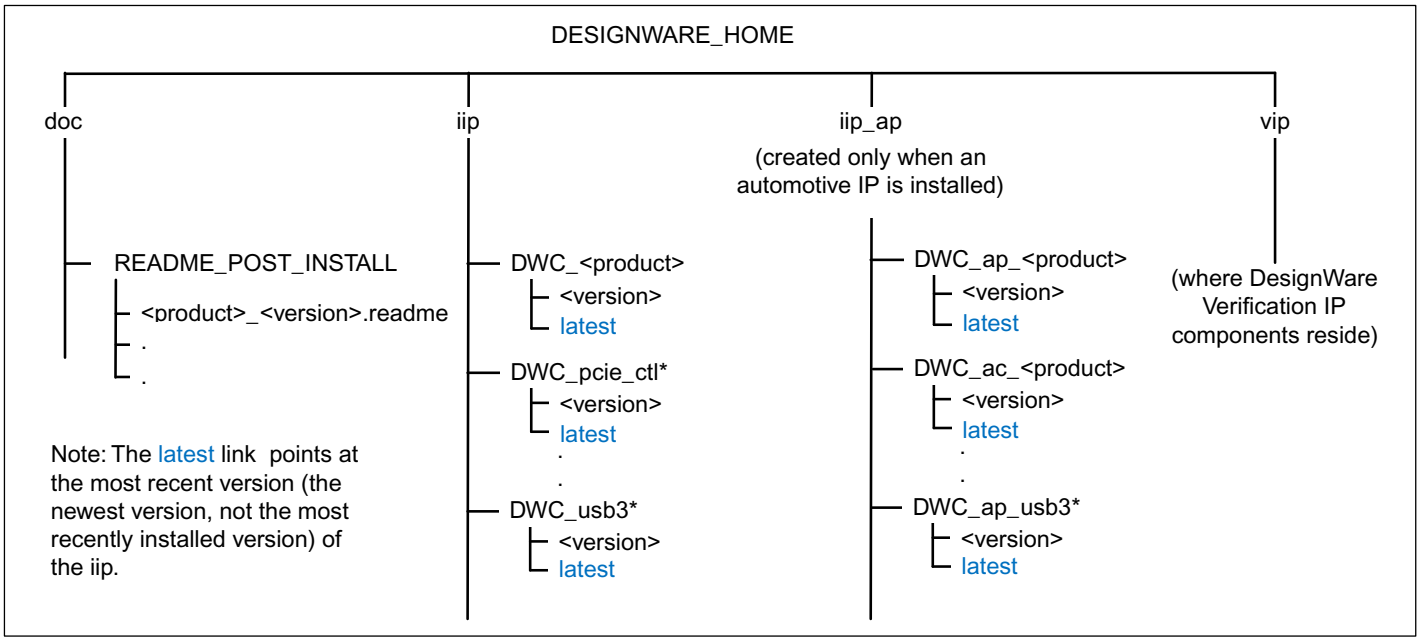


Figure D-2 Directory Structure of $DESIGNWARE_HOME/iip/DWC name/latest After Controller Installation

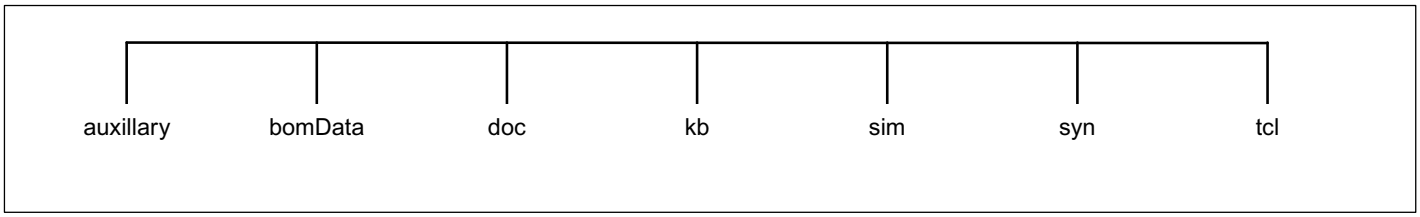


Table D-1 Description of the Directories in $DESIGNWARE_HOME/iip/DWC name/latest

Directory	Description
auxiliary	Scripts and text files used by coreConsultant.
bomData	Build Of Material data used by coreConsultant to create the RTL based on the configuration selected.
doc	Contains the DWC name product documentation, such as the Databook and Release Notes (.pdf files).
kb	Contains knowledge base information used by coreConsultant. These are binary files containing information regarding the state of the design.
sim	Contains test stimulus and output files.
syn	Contains synthesis files for the DWC name.
tcl	Contains synthesis intent scripts.