SYNOPSYS®

DesignWare® Cores 32G PHY IP Integration Review Checklist

Application Note

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Revision History

Date	Document Version	Description
April 2021	1.10a	Added: ■ “Synopsys Statement on Inclusivity and Diversity” ■ Table 5-8: “Tapeout and Silicon Readiness Review”
October 2020	1.00a	Initial Version

Preface

This document describes the 16G PHY hardware emulation that enables you to generate test and characterization vectors and perform ATE testing on 32G PHY macros. In addition, this document provides the procedure for each test in the ATE test suite.

Web Resources

- DesignWare IP product information: http://www.designware.com
- Your custom DesignWare IP page: http://www.mydesignware.com
- Documentation through SolvNet: https://solvnet.synopsys.com (Synopsys password required)
- Synopsys Common Licensing (SCL): http://www.synopsys.com/keys

Synopsys Statement on Inclusivity and Diversity

Synopsys is committed to creating an inclusive environment where every employee, customer, and partner feels welcomed. We are reviewing and removing exclusionary language from our products and supporting customer-facing collateral. Our effort also includes internal initiatives to remove biased language from our engineering and working environment, including terms that are embedded in our software and IPs. At the same time, we are working to ensure that our web content and software applications are usable to people of varying abilities. You may still find examples of non-inclusive language in our software or documentation as our IPs implement industry-standard specifications that are currently under review to remove exclusionary language.

Customer Support

To obtain support for your product, contact Support Center using one of the following methods:

- *For fastest response*, enter a case through SolvNetPlus:
  a. https://solvnetplus.synopsys.com
  b. Click the Cases menu and then click **Create a New Case** (below the list of cases).
  c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

     Make sure to include the following:

     - **Product L1:** DesignWare Cores
     - **Product L2:** 32G PHY

  For more information about general usage information, refer to the following article in SolvNetPlus:

  https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources

- Or, send an e-mail message to support_center@synopsys.com (your e-mail will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product name, Sub Product name, process, and Tool Version number in your e-mail (as identified above) so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood.
  - Attach any debug files you created.
- Or, telephone your local support center:
  - North America:
  - Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
  - All other countries:

    https://www.synopsys.com/support/global-support-centers.html

5 32G PHY IP Integration Review Checklist

This appendix contains the Integration Review Checklist of Synopsys PHY into your ASIC/SoC.

Note

- Section numbers may change between PHY databooks.
- Check STARs: are all current STARs on the web addressed?

For your PHY IP product, see https://www.synopsys.com/dw/mydesignware.php

The following integration reviews are offered by Synopsys as part of the Standard Core Support.

- Table 5-1, "Logical Integration Review"
- Table 5-2, "Synthesis Review"
- Table 5-3, "Post P&R Static Timing Review"
- Table 5-4, "GDS/Physical Integration/Layout Review"
- Table 5-5, "Package/Board Review"
- Table 5-6, "PCIe Protocol Specific Details"
- Table 5-7, "Applicable to All Protocols"
- Table 5-8, "Tapeout and Silicon Readiness Review"

These visual reviews are focused on helping the customer improve the odds of ASIC/SoC success. Synopsys recommends customers to include time for the Reviews on their planning as they typically allow early detection of the most typical customer pitfalls.

Note

Contact Synopsys for XLS version of the PHY IP Integration Review Checklist. The column "Comments to be Filled by Customer and Sent Back to Synopsys" in the XLS file needs to be completed by the customer and sent back to Synopsys prior to the respective integration review.

Table 5-1 Logical Integration Review

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
1.	Integration	What is your top module?	Check uPCS level signals if you use PHY for PCIe or SATA. For other protocols, check PHY level signals.	
2.	Integration	Please specify your configurations/top level wrappers.	Example: x16_x8x8, x4_x2x2 (Aggregation/Bifurcation options). Please attach a diagram if possible.	
3.	Integration	Have you simulated with actual PHY model in the Controller simulation environment? (not the generic PHY model suggested by coreConsultant).	The intent is to ensure that the PIPE connectivity is correct. If you use Synopsys Controller, use coreConsultant. Refer to <pkg>/phy/ipxact/*_iip.config	
4.	Integration	Have you run the recommended Verilog Testbench (VTB) tests provided in the controller package?	The intent is to run functional simulation for Controller + PHY together. CoreConsultant provides the VTBs for the Synopsys controller, and for either a generic PHY, or a Synopsys specific PHY.	
5.	Integration	Have you reviewed the TESTBENCH.README files provided in the package?	<pkg>/phy/testbench/TESTBENCH.README & ATE_TESTBENCH.README <pkg>/upcs/testbench/TESTBENCH.README & ATE_TESTBENCH.README	

Table 5-1 Logical Integration Review (Continued)

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
6.	Integration	Make sure “Hand-Placed Logic” added during synthesis/PnR does not change.	PHY databook: 8.10.2.1, “Hand-Placed Logic Constraints” section PCS databook: 6.2.1, “Hand-Placed Logic Constraints” section Hand-instantiation is used to ensure that these cells never get optimized away during the synthesis and meet the timing requirement. All hand placed cells are replaced by appropriate cells manually.	
7.	Integration	1. Ensure upcs_pwr_en, upcs_pwr_stable, phyN_pcs_pwr_stable, phyN_pma_pwr_en, and phyN_pma_pwr_stable are connected correctly. Refer to the diagram in the PCS databook. 2. Is the output signal pma_pwr_en in RAW_PCS connected to ana_pwr_en of PMA input? 3. OR gate is an optional power enable over-ride from SoC. If power gating is not in use, make sure pg_mode_en=1'b0. 4. The inputs pcs_pwr_stable and pma_pwr_stable must only be asserted after the supplies ramp up and are at 90% of nominal or higher. 5. Ensure power is on during test mode/customer diagnostic through “Optional Additional Power enables”. See figure 5-28 and 4-12.	PHY databook: 5.17, “Power Gating” section Figure 5-25, “Power Gating Connectivity for External PMA Switch” 4.17 PCS databook: Figure (6-18) “Power-Gating Controls for Multi-Protocol 32G PCS and PHY”	

Table 5-1 Logical Integration Review (Continued)

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
8.	Integration	Have you connected the Reference Resistor and Reference Resistor Contention Bus per PHY databook?	PHY databook: 8.8, “Reference Resistor” section Follow the instruction shown in Figure 8-8, “Reference Resistor Contention Bus - Multiple PHYs Sharing a Single Resistor” 8.8.1, “Reference Resistor Contention Bus” section	
9.	Integration	Most of the protocols support AC coupling. Ensure rxX_term_acdc = 1 for such protocols. If you intend to use DC coupled link, consult with Synopsys to make sure the PHY version supports DC coupling for each protocol use case.	PHY databook: Appendix B, “Lane Configuration Settings” Figure 4-4, “RX Termination”	
10.	Integration + Verification	Have you integrated an External ROM for each PHY? The sample FW is in phy/include/*phy_xN_ns_pcs_raw_ext_rom.fastsim or *phy_xN_ns_pcs_raw_ext_rom.bin **Note:** SNPS PHY IP comes with an optional external ROM interface that can be used to store the FSM firmware code. The external ROM interface is enabled by default. To disable it and use only the PHY IP internal hard-coded lookup table based ROM, define the {PREFIX}_NO_EXT_ROM_SUPPORT macro. Note that Synopsys recommends using an external ROM.	PHY databook: 4.3 “Raw PCS” 5.16 “ROM Interface”	

Table 5-1 Logical Integration Review (Continued)

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
11.	Integration+Verification	■ Have you integrated mandatory SRAM for each PHY instance? ■ Can you change sram_ext_ld_done to 1'b1 after sram_init_done=1'b1? **Note:** Do not tie sram_ext_ld_done to 1'b1. ■ SRAM_BYPASS should be programmed before phy_reset is negated. ■ When sram_bypass=0, can you update firmware into external SRAM and assert sram_ext_ld_done=1 after sram_init_done=1. (The sample firmware is in phy/include/*phy_xN_ns_pcs_raw_mem_sram_fastsim.fw or *phy_xN_ns_pcs_raw_mem_sram.fw) ■ Can you bypass SRAM during debug? This is to make sure we have ability to root cause problems related with firmware loading in silicon debug. ■ Can you load firmware in the first Power on Reset (POR)?For PCIe: Is SRAM firmware update prior to linking to Gen1 feasible?	PHY databook: 5.15 “External SRAM Support” section	

Table 5-1 Logical Integration Review (Continued)

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
12.	Tune bits	Are all parameter control signals (protocolP_ext_*) driven by programmable registers? The pcs_laneX_protocol[1:0] is as “PHY Mode[1:0]” in PIPE 4.3 specification. ■ The Protocol0 is for PCIe ■ The Protocol1 is for USB ■ The Protocol2 is for SATA Signals corresponding to unused protocol can be tied to 0. *Note:* It is mandatory that you drive the inputs (protocol[0,1,2]_ext_*, phy_ext_ctrl_sel, protocol_ext_mpll\{a,b}_recal_bank_sel, protocol_ext_mpll\{a,b}_recal_bank_sel_ovrd_en, protocol_ext_sup_misc_ovrd_en, and protocol0_esm_ext_sup_misc_r1 using external, programmable registers in your SoC/ASIC with the phy_ext_ctrl_sel and protocol_ext_mpll{a,b}_recal_bank_sel_ovrd_en default values set to 0. The SOC registers should be defaulted to the same values which are hardwired within the upcs/rtl: <pkg>/upcs/include/<IPNAME>_pcie_esm_ref_100m.v <pkg>/upcs/include/<IPNAME>_pcie_ref_100m.v	PCS databook: 4.13, “External Protocol Override Signals” section 6.14, “PHY Configuration Overrides” section	

Table 5-1 Logical Integration Review (Continued)

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
13.	Configuration inputs	Most of the PHY signals are driven by protocol PCS, however, there are signals which are driven by SoC, this check point is to ensure all such signals are driven properly. The list of such signals can be found in PIPE Wrapper Signal Descriptions of the PCS databook and signal description section and Appendices A and B of the PHY databook.	PHY databook: Appendix A, “Support Configuration Settings” Appendix B, “Lane Configuration Settings” PCS databook: “Signals Descriptions” chapter	
14.	Clock source	Are reference clock frequency and jitter requirements met as recommended in section 9 of the PHY databook?	PHY databook: Chapter 10, “Reference Clock Implementation” PCS databook: 4.3.3, “Reference Clock Input” section	
15.	Clock source	If you use repeat clock, make sure it is supported by PHY for your protocol data rate.	PHY databook: Chapter 10, “Reference Clock Implementation” PCS databook: 4.3.3, “Reference Clock Input” section	
16.	Clock source	Make sure reference clock is available to all instances of PHY irrespective of power state (L1.2/CPM) of PHY macros in the reference clock repeater module.	PHY databook: 5.17, “Power Gating” section PCS databook: 4.3.3, “Reference Clock Input” section	
17.	Clock source	Ensure any reference clock inputs that are not being used are tied to ground.	PHY databook: 10.2 “Reference Clock Implementation”	
18.	Clock source	Is refa/b_clk_sel[1:0] set properly for your reference clock input choice? **Note:** Any reference clock inputs that are not being used should be tied to ground.	PHY databook: 4.2.4.1 “Reference Clock Input” 10.2 “Reference Clock Implementation”	
19.	Test pins	Are the test pins de-asserted for normal operation?	PHY databook: 6.1, “Test Modes” section	

Table 5-1 Logical Integration Review (Continued)

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
20.	Reserved signals	Are the input signals that are reserved driven to an appropriate value? Look for the keyword “reserved” in the databook?	PHY databook: Chapter 3, “Signal Descriptions” PCS databook: “Signals Descriptions” chapter	
21.	Transmit level	Are the Transmit de-emphasis and Transmit launch amplitude set appropriately? If you use PCIe uPCS/PIPE logic, this requirement is handled automatically.	PHY databook: 5.10, “TX Equalization and Adaptation” section	
22.	Clock setting	Are the mpll{a,b}_multiplier and ref_clk_div2_en set to the proper setting for your reference clock frequency?	PHY databook: Appendix A, “Support Configuration Settings”	
23.	BSCAN	If using boundary scan, are corresponding signals set correctly, boundary scan chains integrated properly, and boundary scan mode set accordingly?	PHY databook: 6.1.1, “Boundary Scan (ACJTAG)” section	
24.	CREG	Is there an access to the control registers in both functional as well as test mode?	PHY databook: 5.14, “Control Register Interface” section	
25.	Test	In ATE test mode, setup should meet the following basic requirements: - PHY is powered up and out of reset. - Reference clock is available and running. - JTAG pins are accessible at top level. - Requirements listed in Section 2.1 titled “Tester Requirements of ATE application note” are met.	ATE application note: “Tester Requirements” section	
26.	Test	Make sure AC coupling capacitor and reference resistor are available at ATE board.	ATE application note: “Load Board Requirements” section PCB and Package Design Guide	

Table 5-1 Logical Integration Review (Continued)

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
27.	Test	Are the scan chains integrated properly and the scan mode set accordingly? General guideline is to limit the number of scan flip-flops to be clocked at the same time and allow some skew between scan clocks, so that the instantaneous current can be handled appropriately without resulting in a large IR drop.	PHY databook: 6.1.5, “Scan (At-Speed, Stuck-At)” section	
28.	Test	When PHY IP is used as DUT in ATE, are the initial pin conditions as per Appendix A of ATE test application note? If DUT is PIPE wrapper, refer to “UPCS PIPE”, and if DUT is PHY wrapper, refer to “PHY Top-Level”.	ATE application note: Appendix A	
29.	Test	Clock grouping: Are scan clocks grouped following the clock grouping script: pma/atpg/<metal_stack>/tetramax/clock_group.tcl?		
30.	Verification	Has a simulation run without <IPNAME>_SHORT_RESET ifdef macro being defined? (Set FAST_RX_STARTUP_CAL bit= 1 and all other FAST bits= 0). *Note:* Do not use Scaledown0 simulation mode as an SoC sign-off criteria. For SoC-level sign-off criteria, run a few Non Scale Down (also called normal reset or long reset) simulations without the <IPNAME>_SHORT_RESET macro defined. For normal reset simulations, set FAST_RX_STARTUP_CAL bit to ‘1’ and all other FAST bits to ‘0’.	PHY databook: 7.5, “Fast Simulation Mode” section Appendix C, “Configuration and Compile Macro ifdef Settings” Macros Affecting Simulation, TESTBENCH.README	
31.	Verification	Can you modify PHY registers while PHY FSM is stalled for debug or synthesized netlist?	PHY databook: 7.5, “Fast Simulation Mode” section	
32.	Verification	Are all inputs driven to non “X”, including JTAG?		

Table 5-1 Logical Integration Review (Continued)

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
33.	Verification	Have you run a functional simulation, make sure your simulation timescale is set to 1ns/10fs for the PHY?	The intent is to make sure PHY timescale is not over-ridden	
34.	Verification	phy_reset must be asserted or ref_clk_en must be negated whenever reference clock (ref_alt/pad_clk_p/m) source may glitch or become unstable. **Example:** During PCIe PERST# warm reset, phy_reset must be asserted or ref_clk_en must be negated. New PCIe motherboards are found to turn off the reference clock during PERST# warm reset.	PHY databook: 5.2 “PHY Initialization Sequence”	
35.	Check STARs	Are all current STARs on the Web addressed? See https://www.synopsys.com/dw/mydesignware.php for your PHY IP product.	Product Open STARs	

Table 5-2 Synthesis Review

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
36.	Synthesis Scripts	Have you referenced clock definitions from the synthesis scripts?	PHY level: <pkg>/phy/synth/scripts UPCS level: <pkg>/upcs/synth/scripts dwc_[protocol]_xN_ns.tcl / dwc_[protocol]_xN_ns_funcs.tcl	
37.	Synthesis Scripts	Have you updated synthesis scripts for reference clock period?	dwc_[protocol]_xN_ns.tcl	

Table 5-2 Synthesis Review (Continued)

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
38.	Synthesis Scripts	Have you referenced all the false paths and exclusive clock constraints from the synthesis scripts?	dwc_[protocol]_xN_ns.tcl	
39.	Synthesis Scripts	Is there any error in the synthesis run?		
40.	Synthesis Scripts	Is there a timing violation after synthesis?		
41.	Verification	Description: Have you run SDF annotated gate level simulation at both min and max corners?	dwc_SerDes_gate_level_simulations_appnote.pdf <pkg>/pma/timing/<metal_stack>/sdf/*.sdf	
42.	Check STARs	Are all current STARs on the Web addressed? See https://www.synopsys.com/dw/mydesignware.php for your PHY IP product.	Product Open STARs	

Table 5-3 Post P&R Static Timing Review

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
43.	Timing	Have you closed timing?		
44.	Timing	Is there any hold violation?		
45.	Timing	Have you inserted and accounted for isolation cells/Bypass multiplexers on the PHY?		
46.	Timing	Have you accounted for clock tree jitter on the input reference clock?	PHY databook: 10.1, “Reference Clock Requirements” section	
47.	Timing	Have you accounted for clock tree jitter on clock from the PHY?		
48.	Timing	Have you met the TX lane-lane clock skew in each corner libs? (Mandatory for PCIe with multi-lane link. Not necessary for a single lane PCIe link.)	PHY databook: 5.5, “TX Data Path” section 5.16, “Aggregation and Bifurcation Support” section PCS Clock Domain	

Table 5-4 GDS/Physical Integration/Layout Review

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
49.	GDS	Have the layers above the IP been properly filled? (Refer to OBS drawings in PMA LEF file). *Note:* Generally, PHY IP PMA comes pre-filled. When you run dummy fill at the chip level, no fill shapes are added within the PMA.	PHY databook: 8.3, “PMA Fill” section Dummy Fill	
50.	GDS	Are all the powers and grounds isolated?	PHY databook: 9.3.2, “Package and Board Guidelines for Power Supplies” section	
51.	GDS	Ensure that Level Shifter or Isolation cells are added between different power domains, or power gating is used: - Level Shifters are required for signals between different power level domains.	PHY databook: 5.17, “Power Gating” section 9.3, “Supplies Requirements” section	
52.	GDS	Have the provided back-to-back diodes with the snap-on pads between the core vss and gd diodes been connected for ESD protection? (Make sure that the resistance from gd to the first power clamp is within the specific requirement, for example, 0.3 Ohms).	PHY databook: 8.6.3, “ESD Back-to-Back Diode Connection to Core VSS” section	
53.	GDS	Verify that there are no new DRC errors inside the PHY boundary.	FOUNDRY_DOC_REVS or <pkg>/docs/readme_[version].txt	
54.	GDS	XOR the GDSII of the PHY in your implementation against the PHY as released by Synopsys.	FOUNDRY_DOC_REVS or <pkg>/docs/readme_[version].txt	
55.	GDS	Verify that you have not placed any overlapping structures inside the PHY boundary on the layers below the top metal layer.	PHY databook: Chapter 8, “Physical-Level Implementation”	

Table 5-4 GDS/Physical Integration/Layout Review (Continued)

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
56.	GDS	Verify your clock routing, make sure it is shielded and ensure that you meet Reference Clock Requirements mentioned in the databook such as random jitter, reference clock skew, etc.	Reference Clock Routing Guidelines for phy_ref_alt_clk_m and phy_ref_alt_clk_p	
57.	GDS	Has the recommended minimum distance that the PHY can be placed from any adjacent cell been met? For example, 10 µm.	PHY databook: 8.2.2, “PMA Abutment” section	
58.	GDS	PHY hard macro may abut the die seal ring as long as it does not violate bump-to-seal ring edge design rule (for example, UBM-to-seal edge spacing of 50 µm to 300 µm). *Note:* The PMA hard macro is designed to be placed with preference for the north or south side of the die, as shown in Figure 8-2. Preferred placement of the PHY is on the north or south edge of the die. If you place the PHY on the east or west edge, it will complicate the on-die interface routing as well as the package routing of the TX and RX pairs. If placing the PMA on the east/west side is required, contact Synopsys support.	PHY databook: 8.2, “PMA Placement” section Chapter 8, “Physical-Level Implementation”	
59.	GDS	Have you ensured that PAD and PHY are abutted and aligned?	PHY databook: Chapter 8, “Physical-Level Implementation”	
60.	GDS	What is the relative location of the IP in the SOC?	PHY databook: Chapter 8, “Physical-Level Implementation”	
61.	GDS	Have you ensured that the LVS/DRC switch settings are as per Synopsys recommendations?	FOUNDRY_DOC_REVS or <pkg>/docs/readme_[version].txt	

Table 5-4 GDS/Physical Integration/Layout Review (Continued)

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
62.	GDS	Have you ensured that the LVS/DRC sign off deck is the same as the Synopsys sign off deck?	FOUNDRY_DOC_REVS or <pkg>/docs/readme_[version].txt	
63.	GDS	Have you passed LVS/DRC/ANTENNA/ERC with the PHY at block level and chip level?	FOUNDRY_DOC_REVS or <pkg>/docs/readme_[version].txt	
64.	GDS, Package + Board	Is external Reference Resistor parasitic capacitance < 20 pF for GDS, Package & PCB? (Each PHY has a loading of 1.5 pF).	PHY databook: Table 9-4, “Reference Resistor Requirements”	
65.	Check STARs	Are all current STARs on the Web addressed? See https://www.synopsys.com/dw/mydesignware.php for your product.	Product Open STARs	

Table 5-5 Package/Board Review

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
66.	Package	Are all the power supplies isolated?	PHY databook: 9.3.2.1, “Power Supply Sharing” section	
67.	Package	Is the ground common?	PHY databook: 9.3.2.1, “Power Supply Sharing” section	
68.	Package	Is the noise on the power distribution less than VPH: < 3% Vpp of DC level? VP: < 5% Vpp of DC level?	PHY databook: 9.3.1, “Power Supplies Delivery to Pads” section	
69.	Board	Are the power supplies isolated through a choke?	PHY databook: 9.3.2, “Package and Board Guidelines for Power Supplies” section	
70.	Board	Is the ground common?	PHY databook: 9.3.2.1, “Power Supply Sharing” section	
71.	Board	Have the AC coupling caps on superspeed TX lines been placed and what is the correct value?	PHY databook: 9.6, “Board Requirements for External Components” section	
72.	Board	Has the reference resistor been placed?	PHY databook: 9.4.1, “Package and Board Requirements for Reference Resistor” section	
73.	Board	Has any additional power decoupling capacitors been added? Additional decoupling capacitors are recommended.	PHY databook: Chapter 9, “Board- and Package-Level Implementation”	
74.	Board	Has the Reference Clock met the Electrical Specifications such as RJ & DJ?	PHY databook: 10.1, “Reference Clock Requirements” section	
75.	Board	Are the voltages on the power supplies as per databook?	PHY databook: 9.3, “Supplies Requirements” section	

Table 5-5 Package/Board Review (Continued)

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
76.	Board	Is an external 200 ohm 1% precision resistor connected to the resref pin?	PHY databook: 9.4, “External Reference Resistor” section	
77.	Board	Have you ensured that all differential signals are matched?	PHY databook: 9.2, “RX and TX Differential Signal Guidelines” section	
78.	Board	Have you run power integrity simulations with your board and package model?	PHY databook: 9.2, “RX and TX Differential Signal Guidelines” section	

Table 5-6 PCIe Protocol Specific Details

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
79.	PCIe Protocol	For PCIe, ensure that FOM is the default.	PHY databook: 5.12, “RX Equalization and Adaptation” section	
80.	PCIe Protocol	Ensure that direction change does not rely on HOLD/HOLD/HOLD to halt RX Adaptation. Include dither MAC HW to stop when it gets close.	PHY databook: 5.12, “RX Equalization and Adaptation” section	
81.	PCIe Protocol	PCIe recommended presets are Presets 0/1/2/3/4/7/8/9 for lower jitter (for example, 0x39F) or each speed or by Default - PCIe Controller GEN3_RELATED_OFF.RATE_SHADOW_SEL = 0; GEN3_EQ_CONTROL_OFF.GEN3_EQ_PSET_REQ_VEC = 0x39F (Gen-3) - PCIe Controller GEN3_RELATED_OFF.RATE_SHADOW_SEL = 1; GEN3_EQ_CONTROL_OFF.GEN3_EQ_PSET_REQ_VEC = 0x39F (Gen-4).	See <pkg>/phy/ipxact/*_iip.config	

Table 5-7 Applicable to All Protocols

No.	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
82.	All protocols	Ensure that RX Adaptation is not aborted by negating rxX_adapt_req before rxX_adapt_ack is asserted. Aborting results in an RX settings which are less than optimal.	PHY databook: 5.12, “RX Equalization and Adaptation” section	
83.	Check STARs	Have you reviewed all STARs at www.mydesignware.com?		

Table 5-8 Tapeout and Silicon Readiness Review

No	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
84.	Tapeout readiness	Have you completed the “Logical Integration Review”? List the associated SolvNet case(s).	Refer to “Logical Integration Review”	
85.	Tapeout readiness	Have you completed the “Synthesis Review”? List the associated SolvNet case(s).	Refer to “Synthesis Review”	
86.	Tapeout readiness	Have you completed the “Post P&R Static Timing Review”? List the associated SolvNet case(s).	Refer to “Post P&R Static Timing Review”	
87.	Tapeout readiness	Have you completed the “GDS/ Physical Design/PHY IP Physical Integration/Layout Review”?	Refer to “GDS/Physical Integration/Layout Review”	
88.	Tapeout readiness	Have you completed the “Package/Board Review”? List the associated SolvNet case(s).	Refer to “Package/Board Review”	
89.	Tapeout readiness	Have you reviewed the “PCIe Protocol Specific Details section of the integration checklist”? List the associated SolvNet case(s).	Refer to “PCIe Protocol Specific Details”	
90.	Tapeout readiness	Have you reviewed the “Applicable to All Protocols section of the integration checklist” List the associated SolvNet case(s).	Refer to “Applicable to All Protocols”	
91.	Tapeout readiness	What PHY IP version are you using for tapeout? Provide full details.	Check PHY IP Release readme	
92.	Tapeout readiness	What PHY IP patches have been installed on top of the full version you are using for tapeout? List all the patch(es) that have been used.	Check PHY IP patch(es) Release readme(s)	
93.	Tapeout readiness	Have you checked with Synopsys if the PHY IP version (and subsequent patches) is the latest for the tapeout? If not, open a SolvNet case and check with Synopsys. You cannot mix and match the hard macro PMA and soft-RTL from different PHY versions.		

Table 5-8 Tapeout and Silicon Readiness Review (Continued)

No	Item	Description	Reference in PHY IP Databooks / Application Notes / Readme / Other PHY IP Package Content	Comments to be Filled by Customer and Sent Back to Synopsys
94.	Tapeout readiness	Did you use Hard Macro PMA and Soft-RTL from same PHY version? Mention Yes or No in the comments. **Note:** It is mandatory that Hard Macro PMA and Soft-RTL should be used from same full version of the PHY IP. Mix and match of PMA and Soft-RTL from different PHY versions is not allowed. It is okay to install patch(es) that were specifically sent by Synopsys. Patches contain only incremental updates and are not full PHY IP versions. If you have any questions on this topic, open a SolvNet case and check with Synopsys.		
95.	Tapeout and Silicon readiness	Have you checked with Synopsys if the PHY IP Firmware version you currently have is the latest and if new firmware versions are available or in planning by Synopsys? If not, open a SolvNet case and check with Synopsys.		
96.	Tapeout and Silicon readiness	Have you reviewed and addressed are all the current STARs on the Web? If you have any questions on the current STARs, open a SolvNet case and check with Synopsys.	See https://www.synopsys.com/dw/mydesignware.php for your product.	