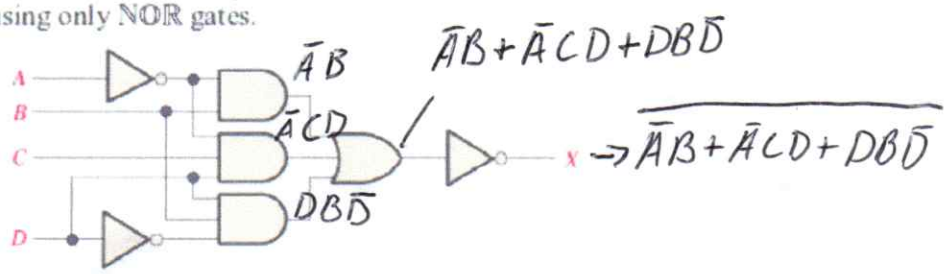
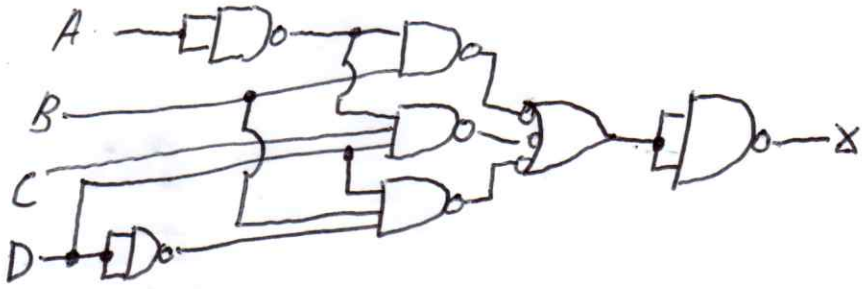
1) Write the output expression for the logic circuit in the figure below. Implement the logic
   a. using only NAND gates
   b. using only NOR gates.



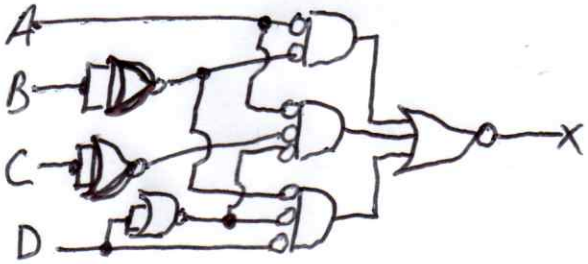
$\bar{A}B+\bar{A}CD+DB\bar{D}$

$\rightarrow \overline{\bar{A}B+\bar{A}CD+DB\bar{D}}$

NAND



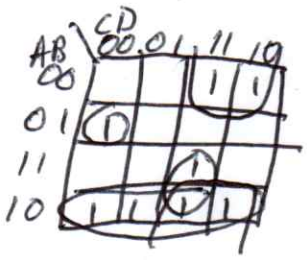
NOR



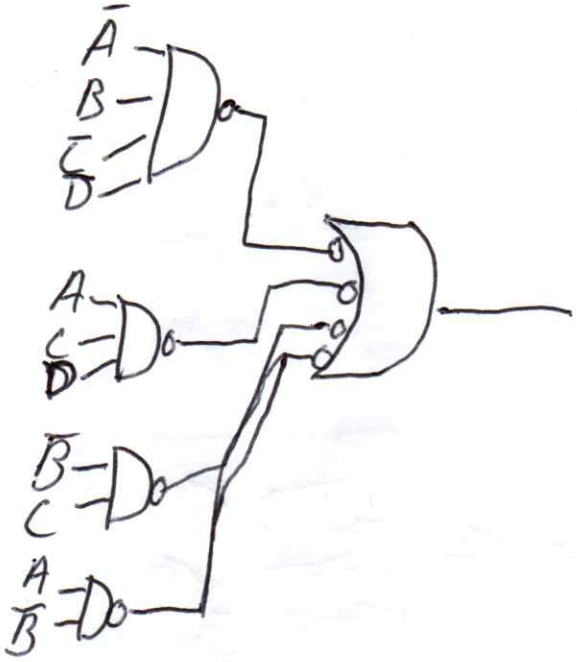
2) Given the following truth table, find out the binary expression for output F in **standard SOP** form. Simplify the expression and reduce it to **SOP** form using **Karnaugh Map**. Create the NAND/NAND two-level implementation for the minimized SOP expression.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0

0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1



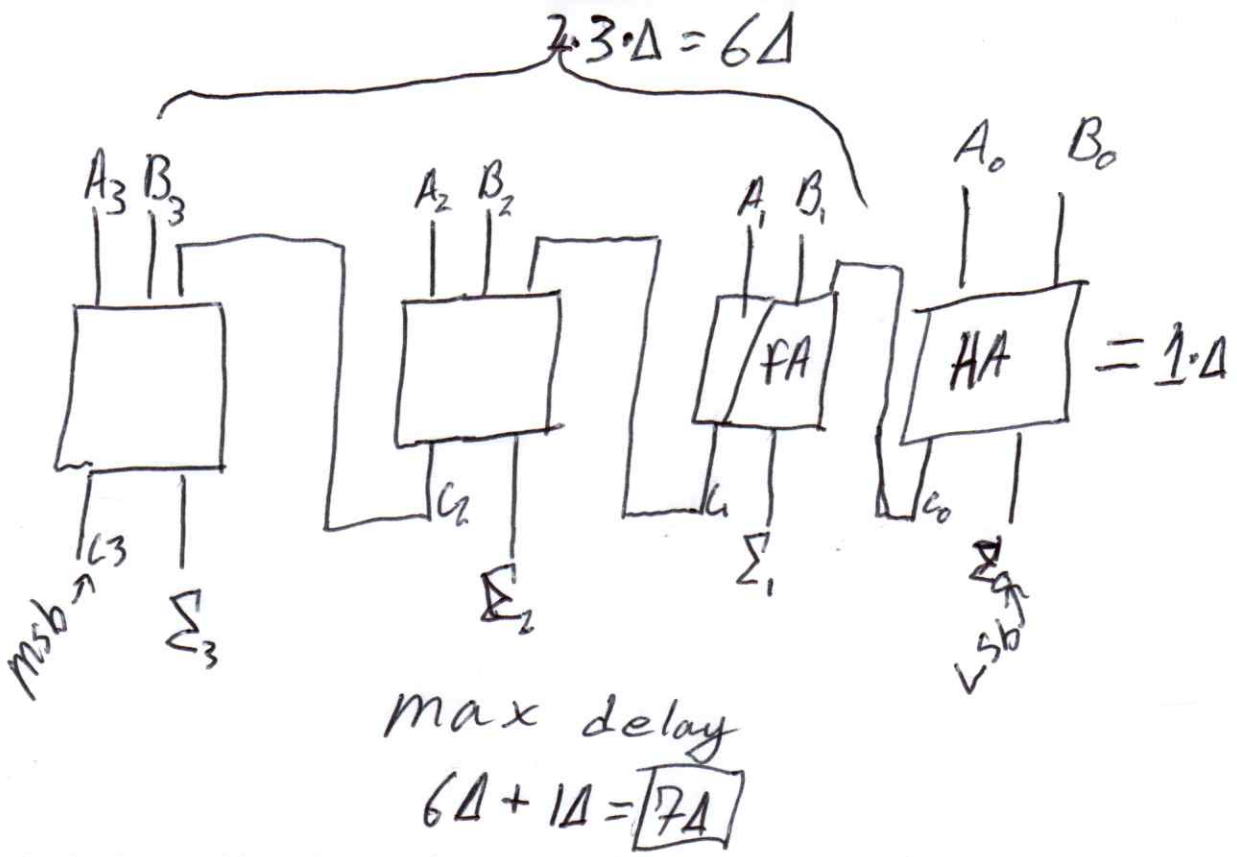
$\bar{A}B\bar{C}\bar{D} + ACD + \bar{B}C + A\bar{B}$



3) Explain what is the difference between a half adder's function, inputs and outputs and a full-adder's. Consider you want to design a circuit to add two 4-bit numbers, and you have half adders and full adders available to use as components.
   a. Draw a block diagram of your 4-bit adder, using half and full adders. Do not draw a gate-level diagram. Show and label all inputs and outputs.
   b. Assume that a half adder has a maximum propagation delay of δ, and a full adder has a maximum propagation delay of 2δ. What is the maximum propagation delay for your 4-bit adder, from LSB input to MSB output?

Half adder only has 2-1Bit inputs and outputs a sum with a carry.

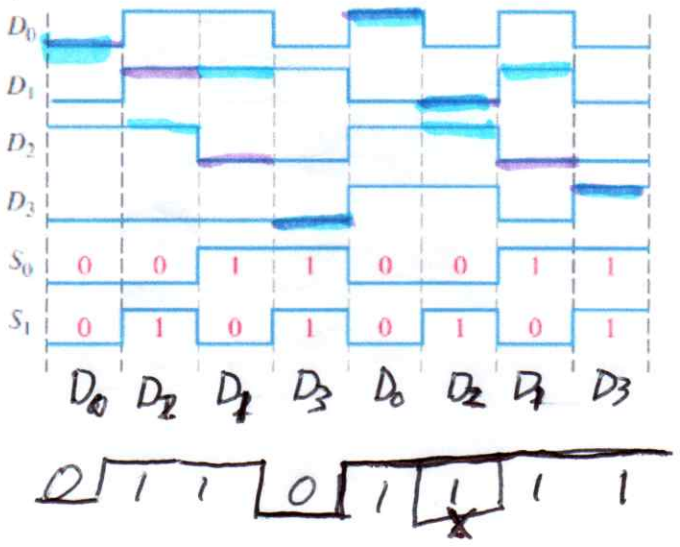
A full adder is much the same except they have a carry input.

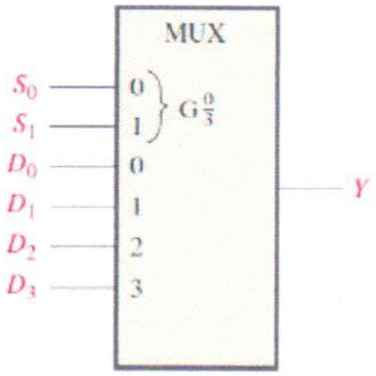


max delay

$6\Delta + 1\Delta = \boxed{7\Delta}$

4) The data input and data select waveforms as shown below are applied to the multiplexer as shown in figure below. Determine the output waveform Y in relation to the inputs.



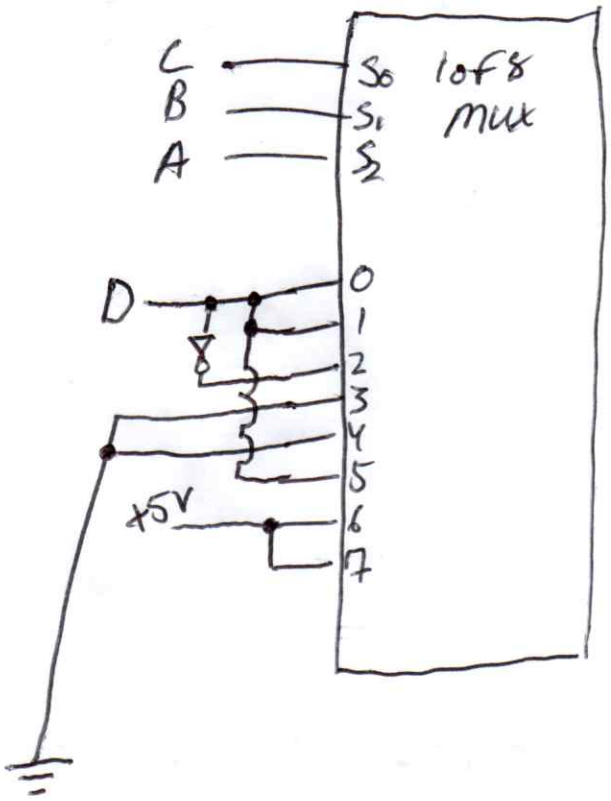


5) Implement the Boolean function represented by following truth table with a 1 of 8 multiplexer.

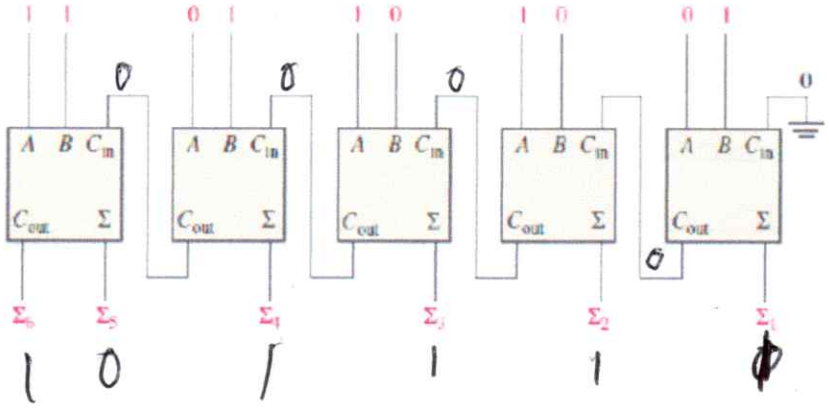
A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0

$f = D$

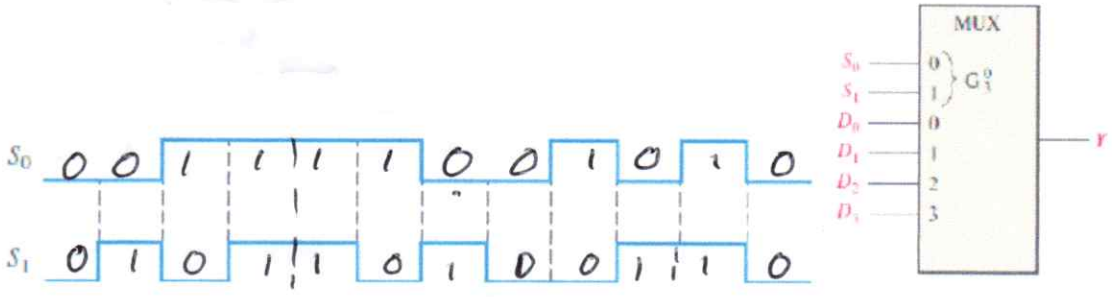
0	0	1	1	1	F=D
0	1	0	0	1	F=$\bar{D}$
0	1	0	1	0	
0	1	1	0	0	F=0
0	1	1	1	0	
1	0	0	0	0	F=0
1	0	0	1	0	
1	0	1	0	0	F=D
1	0	1	1	1	
1	1	0	0	1	F=1
1	1	0	1	1	
1	1	1	0	1	F=1
1	1	1	1	1	



6) For the parallel adder in figure below, determine the sum by analysis of the logical operation of the circuit.



7) For the multiplexer in figure below, are sequenced by the waveform as below. If $D_0 = 1$, $D_1 = 0$, $D_2 = 0$, and $D_3 = 1$, determine the output waveform.



D_0 D_2 D_1 D_3 D_3 D_1 D_2 D_0 D_1 D_2 D_3 D_0