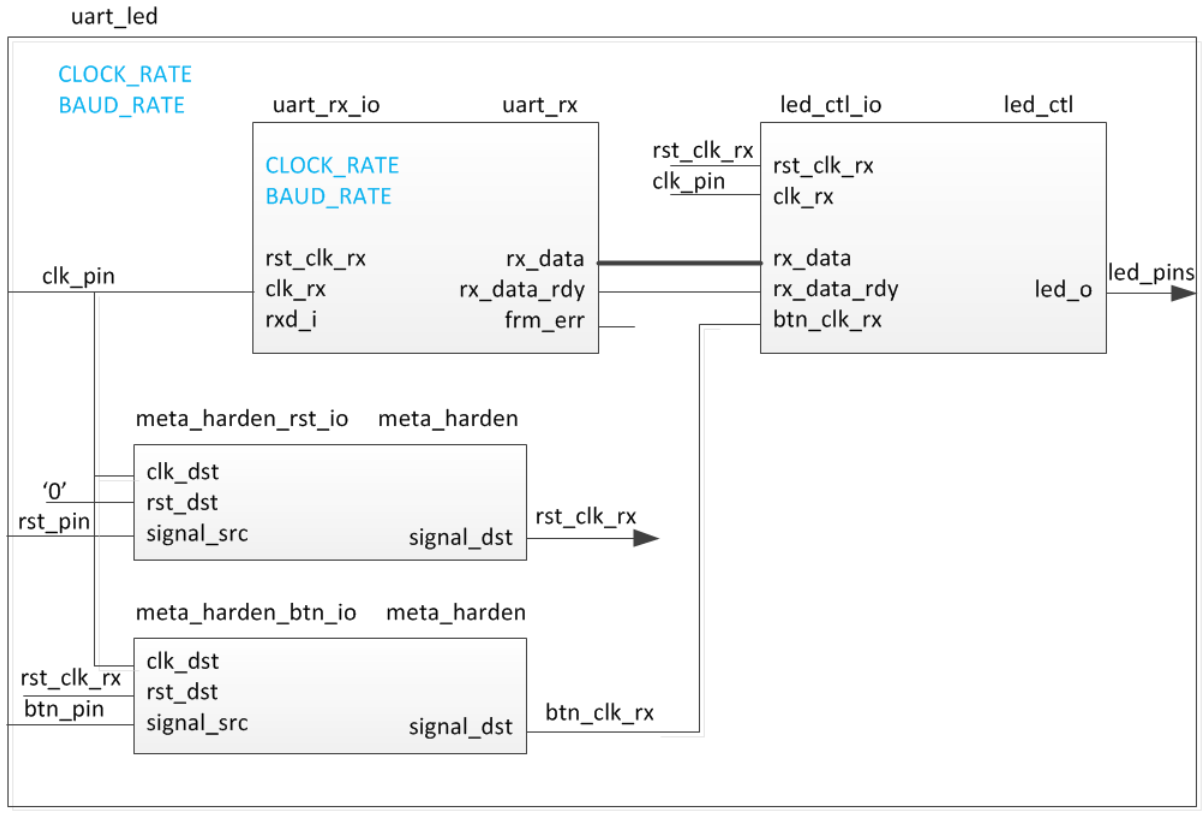
Lab2 Intro
Synthesizing a RTL Design

Introduction

- This lab uses a simple uart-led design. The design takes an input via a terminal operating at 115200 baud and displays the binary equivalent of the ASCII character the user has typed on the 4 LEDs and 4 PMODB Pins. If the BTNU is pressed then the upper and lower nibbles of the binary number gets swapped.
- You will synthesize the design with the default settings as well as with some settings changed and observe the effect

The Design



Procedure

- Create a project using Vivado IDE using the provided HDL files and timing constraints
- Elaborate the design and view noise report and the schematic
- Synthesize the design with the default settings
- Open the synthesized design and view schematic
- View various reports including the timing summary, resource utilization, and power
- Write a checkpoint
- Synthesize the design with one of the settings changed
- Compare the generated schematic, timing summary, power and resource utilization
- Write another checkpoint
- Read previously written checkpoints and perform the same analysis

Summary

- In this lab you applied the timing constraints and synthesized the design. You viewed various post-synthesis reports. You wrote checkpoints and read it back to perform the analysis you were doing during the design flow. You saw the effect of changing synthesis settings.

Adaptable.
Intelligent.

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