FPGA Design Flow using Vivado 2018.2

XILINX.

Course Objectives

- **After completing this course, you will be able to:**
  - Describe general FPGA architectures
  - Understand the Vivado design flow
  - Create and debug HDL designs
  - Synthesize and implement HDL designs
  - Utilize the available synthesis and implementation reports to analyze a design (utilization, timing, power, etc.)
  - Configure FPGAs and verify hardware operation
  - Create and apply I/O and timing constraints
  - Use the Project Manager to navigate through the design flow
  - Identify file sets (HDL, XDC, simulation)
  - Analyze designs by using the cross-selection capabilities, Schematic viewer, and Hierarchical viewer

Course Outline
Day 1

The course consists of the following modules:

- 7-Series Architecture Overview
- Vivado Design Flow
- Lab 1: Vivado Design Flow
- Synthesis Technique
- Lab 2: Synthesizing a RTL Design
- Implementation and Static Timing Analysis
- Lab 3: Implementing the Design

Course Outline
Day 2

- IP Integrator
- Lab 4: Using the IP Catalog and IP Integrator
- Xilinx Design Constraints
- Lab 5: Xilinx Design Constraints
- Hardware Debugging
- Lab 6: Hardware Debugging

Prerequisites

- Basic HDL knowledge (VHDL or Verilog)
- Digital design knowledge and experience

Platform Support

- **Vivado Design Suite: System Edition 2018.2**
- **Xilinx University boards**
  - PYNQ-Z1, PYNQ-Z2
- **Supported Operating Systems**
  - Windows 7 SP1 Professional (64 Bit)
  - Windows 10 Professional (64 Bit)
  - Red Hat Enterprise Workstation Linux 6.6, 6.7, 6.8, and 6.9 (64 Bit)
  - Red Hat Enterprise Workstation/Server Linux 7.2 – 7.4 (64 Bit)
  - SUSE Linux Enterprise 11.4 and 12.3 (64 Bit)
  - Cent OS Linux 6.7, 6.8, and 6.9 (64 Bit)
  - Cent OS Linux 7.2, 7.3, and 7.4 (64 Bit)
  - Ubuntu Linux 16.04.3 LTS (64 Bit)

Note on target board/device

The lab is written for PYNQ-Z2 and PYNQ-Z1.

- Both PYNQ-Z2 and PYNQ-Z1 target the XC7Z020clg400-1
  - The procedure in the lab has no difference between the two boards

Adaptable.
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