

Aug 27th, 2019

Computer Systems

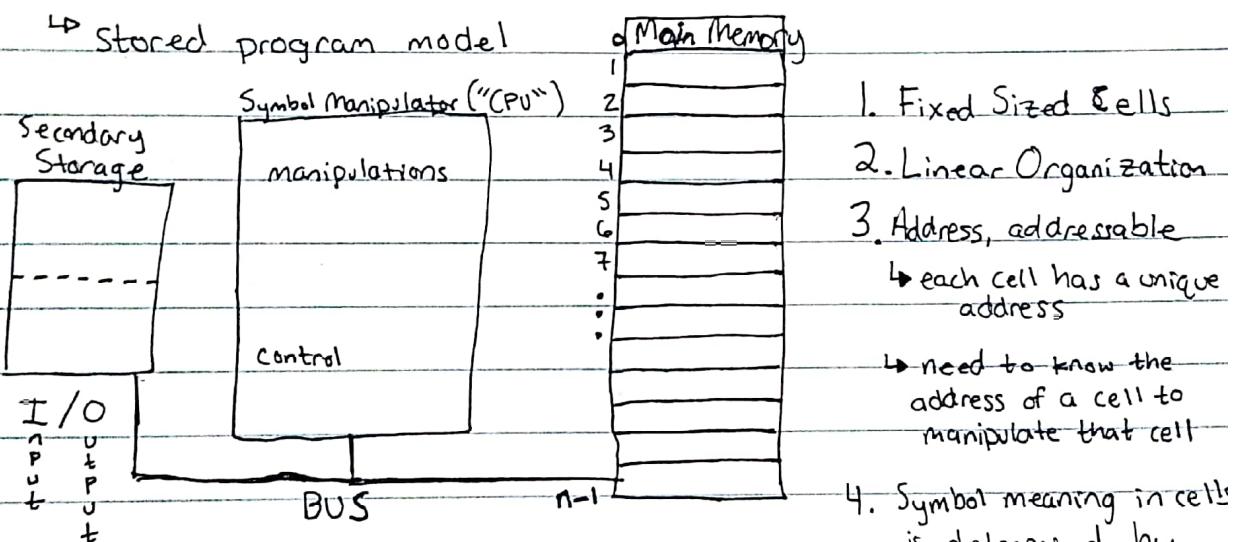
08/02/10 → symbols with multiple meanings based on context

Computers manipulate symbols to achieve contextually useful things

Any mutually exclusive unambiguous 2 state representation can be used as symbols

→ Photons, electrons, punch cards, etc.
on or off, hole or no hole

John Van



"word" size → cell size (16, 32, 64, etc)

BUS can transfer one word at a time

↳ Van — bottleneck

$$\begin{array}{r} 10: \quad \text{BR } 4 \\ 10 \\ 10+2=12 + 2(4) \\ 12+8=20 \end{array}$$

Aug 2th

Computer Systems

Data → numbers, characters, boolean, (instructions)

↳ multiple ways to do any of these

↳ Primitive Types - architecture recommended representations

→ size (word size)

- - - - -

Positional Representation of numbers

$$123 \rightarrow 3 \cdot 10^0 + 2 \cdot 10^1 + 1 \cdot 10^2$$

$d_{n-1} \dots d_2, d_1, d_0$ ~~↓~~ ~~↓~~ ~~↓~~

$$d_0 \cdot 10^0 + d_1 \cdot 10^1 + d_2 \cdot 10^2$$

$d_{n-1} \dots d_2, d_1, d_0, d_{-1}, d_{-2}, d_{-3}$ Fractions

$$0.123 \rightarrow 1 \cdot 10^{-1} + 2 \cdot 10^{-2} + 3 \cdot 10^{-3}$$

Bin → Dec expected

Dec → Bin expected

$$23_{10} \rightarrow ?_2$$

base $\sqrt{23}_{10}$

$2 \overline{) 23}_{10} \quad \begin{matrix} 11 & r(1) \\ & d_0 \end{matrix}$

$2 \overline{) 11}_{10} \quad \begin{matrix} 5 & r(1) \\ & d_1 \end{matrix}$

$2 \overline{) 5}_{10} \quad \begin{matrix} 2 & r(0) \\ & d_2 \end{matrix}$

$2 \overline{) 1}_{10} \quad \begin{matrix} 0 & r(1) \\ & d_3 \end{matrix}$

$2 \overline{) 1}_{10} \quad \begin{matrix} 0 & r(1) \\ & d_4 \end{matrix}$

10111 ✓

$2 \overline{) 23}_{10} \quad \begin{matrix} 11 & r(1) \\ & d_0 \end{matrix}$

$8 \overline{) 23}_{10} \quad \begin{matrix} 2 & r(2) \\ & d_1 \end{matrix}$

$8 \overline{) 2}_{10} \quad \begin{matrix} 0 & r(2) \\ & d_2 \end{matrix}$

$27_8 = 23_{10} = 10111_2$

0 ... maxINT

0 ... $2^{\text{cell size}} - 1$

$$1 \text{ byte} \rightarrow 0 \dots 2^8 - 1 = 255$$

$$16 \text{ bits} \rightarrow 0 \dots 2^{16} - 1 = 65535$$

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Computation Theory

Language is our framework to work in

- ↳ a (possibly infinite) set of finite length strings over a finite length alphabet

String \rightarrow possibly empty, finite sequence of symbols drawn from the alphabet Σ

$\rightarrow \epsilon$ is the empty string

$\rightarrow \Sigma^*$ is the set of all possible strings over an alphabet Σ

$\rightarrow |s|$ is the number of symbols in s

$\hookrightarrow |\epsilon| = 0, |1001001| = 7$

$\rightarrow \#_c(s)$ is the number of symbol c in s

$\hookrightarrow \#_a(\text{adam}) = 2$

Concat $\rightarrow x = ad, y = am \quad xy = adam$

$\hookrightarrow |xy| = |x| + |y|$

ϵ is the identity for concatenation of strings

$\forall x (x\epsilon = \epsilon x = x)$

Concatenation is associative So:

$\forall s, t, w ((st)w = s(tw))$

Replication ; repeated concatenation

$$w^0 = \epsilon$$

$$w^{i+1} = w^i w$$

$$a^3 = aaa, \quad a^* b^3 = bbb$$

Reverse w^R

if $|w|=0$ then $w^R = w = \epsilon$

if $|w| \geq 1$ then

$$\exists a \in \Sigma (\exists u \in \Sigma^* (w = ua))$$

$$\text{So define } w^R = a u^R$$

- Relations of strings

Substrings \rightarrow part of a string

proper substrings \rightarrow a substring that is not the original string (doesn't include everything)

every string is a substring of itself

ϵ is a substring of every string

Prefix s is a prefix if

$$\exists x \in \Sigma^* (t = sx)$$

abba \rightarrow $\epsilon, a, ab, abb, abba$
proper prefix

Suffix s is a suffix if

$$\exists x \in \Sigma^* (t = xs)$$

abba \rightarrow $\epsilon, a, ba, bba, abba$
proper suffix

Defining a Language

~~finite or infinite~~ finite or infinite set of strings over a finite alphabet Σ

$$\text{ex. } \Sigma = \{a, b\}$$

some languages over Σ :

$$\emptyset, \{\epsilon\}, \{a, b\}, \{\epsilon, a, b, aa, bb, aba\}$$

Σ^* language contains every possible string combo from Σ

$$L = \{x \in \{a, b\}^*: \text{all } a's \text{ precede all } b's\}$$

$\epsilon, a, aa, aabb, bb$ are in L

aba, ba, abc are not in L

$$L = \{\} = \emptyset$$

$$L = \{\epsilon\}$$

Functions on Languages

Set operations

- Union
- Intersection
- Complement

Language Operations

- Concatenations
- Kleene Star (*)

if L_1 and L_2 are languages over Σ

$$L_1 L_2 = \{w \in \Sigma^*: \exists s \in L_1 (\exists t \in L_2 (w = st))\}$$

$$L_1 = \{\text{cat, dog}\}$$

$$L_2 = \{\text{apple, pear}\}$$

$$L_1 L_2 = \{\text{catapple, catpear, dogapple, dogpear}\}$$

Language Concat

$$L \{ \epsilon \} = \{ \epsilon \} L = L$$

\emptyset zero for concat

$$L \emptyset = \emptyset L = \emptyset$$

$$L_1 = \{a^n : n \geq 0\}$$

$$L_2 = \{b^n : n \geq 0\}$$

$$L_1 L_2 = \{a^n b^m : n, m \geq 0\}$$

$$L_1 L_2 \neq \{a^n b^n : n \geq 0\}$$

Kleene Star

$$L^* = \{\epsilon\} \cup$$

$$\{w \in \Sigma^*: \exists k \geq 1$$

$$(\exists w_1, w_2, \dots, w_k \in L (w = w_1 w_2 \dots w_k))\}$$

All possible combinations of the strings in a language

+ Operator

$$L^+ = LL^*$$

$$L^+ = L^* - \{\epsilon\} \text{ if } \epsilon \notin L$$

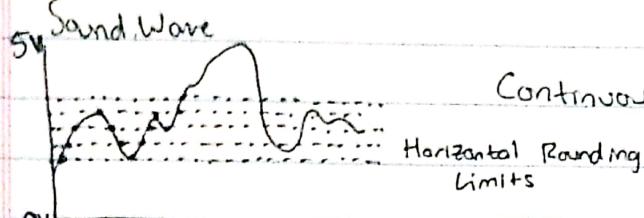
Decision Problems

↳ yes or no (true or false) answerable questions/problems

→ Given language L and string w , is w in L

Aug 28th, 2019
Electronics

Sound Wave



Continuous Analog Signal

Analog to Digital Converters

[ADC]



→ Horizontal Line Width determined by bit length

10 bit ADC from 0 - 5 Volts

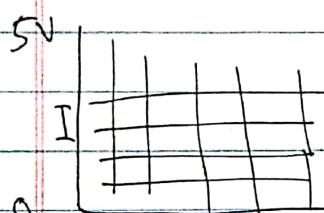
$$\hookrightarrow \frac{(5-0)}{2^{10}} = \text{Horizontal Line Width}$$

Sample Frequency

44.1kHz (CD Audio Quality)

Sample rate

Bit Depth of CD 16-bit



$$\frac{5-0}{2^{16}} = \frac{5}{65536} \approx 76.3 \mu\text{V}$$

$$23\mu\text{s} \quad T = \frac{1}{f} = \frac{1}{44100} \approx 23\mu\text{s}$$

$$V_{RMS} = \left[\frac{1}{T} \int_0^T V(t)^2 dt \right]^{1/2}$$

$$V(t) = V_0 \sin^2 \left(\frac{2\pi}{T} t \right)$$

$$f = \frac{1}{T}$$

$$V_{RMS}^2 = \frac{1}{T} \int_0^T V(t)^2 dt$$

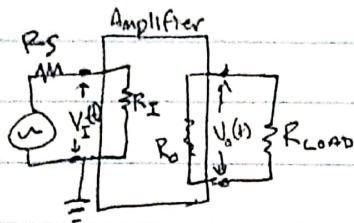
$$\Rightarrow = V_0^2 \sin^2(2\pi f t)$$

$$V_{RMS}^2 = \frac{1}{T} \int_0^T V_0^2 \sin^2 \left(\frac{2\pi}{T} t \right) dt$$

$$\frac{V_0^2}{T} \int_0^T \sin^2 \left(\frac{2\pi}{T} t \right) dt$$

$$V_{RMS} = \frac{V_{PEAK}}{\sqrt{2}}$$

$$\frac{V_0^2}{T} \int_0^T \frac{1}{2} (1 - \cos(2 \cdot \frac{2\pi}{T} t)) dt$$



$$P_o = \frac{i_o V_o}{i_i V_i}$$

$$V_o(t) = V_i(t) A$$

↳ Amplification Factor

$$5 - 1.25 \text{ mA} (1 \text{ k}\Omega) = 5 - 1.25 = 3.75$$

$$5 \left(\frac{3}{4}\right) = \underline{\hspace{2cm}}$$

Current Gain $A_i = \frac{i_o}{i_i}$

$$G = (A_v)^2 \frac{R_i}{R_L}$$

Voltage Gain $A_v = \frac{V_o}{V_i}$

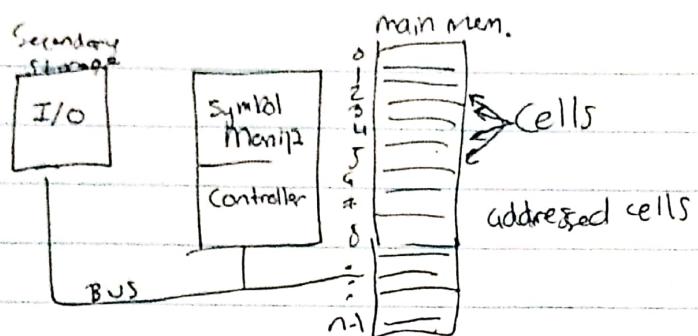
Power Gain P_o / P_i

C	0	0	0	0
A	0	1	0	1
B	0	0	1	1
O	1	1	0	0

1	1	1	1
0	1	0	1
0	0	1	1
1	0	0	1

A	B	C _{IN}	C _{OUT}	Σ	Σ SOP Forms
0	0	0	0	0	$\bar{A} \bar{B} C$
0	0	1	0	1	$\bar{A} \bar{B} \bar{C}$
0	1	0	0	0	
1	0	0	0	1	$A \bar{B} C$
1	0	1	1	0	
1	1	0	1	0	$A \bar{B} \bar{C}$
1	1	1	1	1	$A B C$

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-3, -2, -1, 0, +1, +2, +3

Sign magnitude representation

► write the absolute value and polarity separately

$$\begin{array}{r}
 +1 \quad -1 \quad +1 \quad -1 \\
 +2 \quad -2 \quad -2 \quad +2 \\
 \hline
 +3 \quad -3 \quad -1 \quad +1
 \end{array}$$

Many steps to do addition

0 Pos	0	0	two symbols for 0
1 NEG	0	1	and zero has a sign
	1	0	► not good
	1	-1	

Complement System

19 -1
 18 -2
 17 -3
 16 -4
 :
 03 +3
 02 +2
 01 +1
 00 0

no longer symmetric
but zero only has one

Cannot exceed maxint

$$-(2^{n-1} - 1) \leftrightarrow + (2^{n-1} - 1)$$

EZ

Symmetric

Harder to manipulate

$$\begin{array}{r}
 01 \quad +1 \\
 02 \quad +2 \\
 03 \quad +3 \\
 \hline
 18 \quad -2 \\
 21 \quad +1 \\
 \% \\
 20 \quad -1 \\
 \hline
 01 \rightarrow +1 \\
 17 \rightarrow -3
 \end{array}$$

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One's Complement

↳ Symmetric

→ two representations
for \emptyset

→ 0 is signed

$$0000 \quad 0$$

$$0001 \quad +1$$

$$0010 \quad +2$$

$$0011 \quad +3$$

$$0100 \quad +4$$

$$0101 \quad +5$$

$$0110 \quad +6$$

$$0111 \quad +7$$

$$\underline{1000} \quad -7$$

$$1001 \quad -6$$

$$1010 \quad -5$$

$$1011 \quad -4$$

$$1100 \quad -3$$

$$1101 \quad -2$$

$$1110 \quad -1$$

$$1111 \quad 0$$

$$\begin{array}{r} 0001 \quad +1 \\ 0010 \quad +2 \\ \hline 0) 0011 \quad +3 \quad \checkmark \end{array}$$

$$\begin{array}{r} 100 \\ 1110 \quad -1 \\ 1101 \quad -2 \\ \hline 1) 1011 \quad -4 \text{ END ROUND} \\ \text{CARRY} \end{array}$$

$$1100 \quad -3 \quad \checkmark$$

$$\begin{array}{r} 001 \\ 0001 \quad +1 \\ 1101 \quad -2 \\ \hline 0) 1110 \quad -1 \quad \checkmark \end{array}$$

$$\begin{array}{r} 110 \\ 1110 \quad -1 \\ 0010 \quad +2 \\ \hline 1) 0000 \quad \text{ERC} \\ 0001 \quad +1 \quad \checkmark \end{array}$$

$$\bar{A}BC, \bar{A}\bar{B}C, A\bar{B}\bar{C}, ABC$$

$$A(\bar{B}C + B\bar{C} + BC) + \bar{A}(BC)$$

$$A(\bar{B}C + B(\bar{C} + C)) + \bar{A}(BC)$$

$$A(\bar{B}C + B) + \bar{A}BC$$

2 ORS

~~3 ANDS~~ 3 ANDS

2 NOTS

$$A\bar{B}C + AB + \bar{A}BC$$

3 ANDS, 2 NOTS, 1 OR

Two's Complement
↳ Asymmetric

$$\begin{array}{r} 11^{\textcircled{0}} \\ 1111 -1 \\ 1110 -2 \\ \cancel{1101} -3 \checkmark \end{array}$$

$$\begin{array}{r} 10^{\textcircled{0}} \\ 1100 -4 \\ 1101 -3 \\ \cancel{1001} -7 \checkmark \end{array}$$

$$\begin{array}{r} 0000 \\ 0010 +2 \\ 1101 -3 \\ 1111 -1 \end{array}$$

$$\begin{array}{r} 11^{\textcircled{1}} \\ 1101 -2 \\ 0010 +3 \\ \cancel{0001} +1 \checkmark \end{array}$$

BINARY CODED DECIMAL

0	0000
1	0001
:	:
8	1000
9	1001

Used rarely

Often as a means

To avoid base 2 to base 10 conversion losses

BINARY CARDINAL

		SIGN MAG	1's Comp.	2's Comp	ALL FINITE
0000	0	+0	0	0	
0001	1	+1	1	1	
0010	2	+2	2	2	
0011	3	+3	3	3	
0100	4	+4	4	4	
⋮	⋮	⋮	⋮	⋮	⋮
1101	13	-5	-2	-3	
1110	14	-6	-1	-2	
1111	15	-7	-0	-1	

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$$\begin{array}{r} 0000 0 \\ 0001 +1 \\ 0010 +2 \\ 0011 +3 \\ 0100 +4 \\ 0101 +5 \\ 0110 +6 \\ 0111 +7 \\ 1000 -8 \end{array}$$

$$-(2^{n-1}) \leftrightarrow (2^{n-1} - 1)$$

No complement
has a sign bit!

At best it's a sign
indicator bit

Shortcut

$$0011 +3$$

↳ find 1's comp

$$1100$$

→ add 1

$$1101 -3 \checkmark$$

to avoid base 2 to base 10 conversion losses

FLOATS/REALS

$A_{19} 29^{th}, 19$
Comp. Sys.

	123.45
$2 \overline{123}$	$\frac{6}{*2}$
$2 \overline{101}$	$\boxed{\times} .39$
$2 \overline{101}$	$\boxed{\times} .8$
$2 \overline{130}$	$\boxed{\times} .6$
$2 \overline{115}$	$\boxed{\times} .2$
$2 \overline{115}$	$\boxed{\times} .4$
$2 \overline{13}$	$\boxed{\times} .8$
$2 \overline{11}$	$\boxed{\times} .6$

1111011.0111001...

FLOATS are approx.

$$\begin{aligned}
 \bar{A} + A\bar{B} &= \bar{A} + \bar{B} \\
 \cancel{A}(\cancel{A}\cancel{\bar{B}}) & \\
 \cancel{A}\cancel{\bar{B}} & \\
 \bar{A}\bar{B} & \\
 \bar{A} + A\bar{B} & \\
 \cancel{A}\cancel{\bar{B}} & \\
 A(\bar{T} + \bar{B}) & \\
 A(0 + \bar{B}) & \\
 A(\bar{B}) & \\
 \bar{A}\bar{B} &
 \end{aligned}$$

	0	1	\bar{A}	0	1
$A+B = 0$	1	0	$\bar{A}\bar{B}$	0	1
1	0	0		1	00

$$!(A \parallel B) \rightarrow (!A \& !B) \quad \begin{array}{l} \stackrel{A}{B} = D \\ \stackrel{A}{B} = D \end{array}$$

Negative AND NAND

~~AB~~ A B $\bar{A} + \bar{B}$ $\bar{A}\bar{B}$ $\bar{A}\bar{B}$

	A		A	
	0	1	0	1
$\bar{A}\bar{B}$	0	1	$\bar{A} + \bar{B}$	1
B	1	0	1	0

$$\begin{array}{r}
 4a = 4 \\
 \cancel{4} \cancel{4}
 \end{array}$$

$$a = 1$$

$$\begin{array}{r} 24r3 \\ 6 \overline{)147} \\ \underline{-12} \\ 27 \\ \underline{-24} \\ 3 \end{array}$$

$$0.24 \overline{)124} \quad 4_{10}$$

$$0.4 \quad 4$$

~~10010011~~

$$\begin{array}{r} 24r3 \\ 6 \overline{)147} \\ \underline{-12} \\ 27 \\ \underline{-24} \\ 3 \end{array}$$

$$6 \overline{)124} \quad 4_{10}$$

$$6 \overline{)4} \quad 0_{10}$$

$$403_{10} = 147_{10}$$

$$\begin{array}{r} 73_{r1} \\ 2 \overline{)147} \end{array} \quad \begin{array}{r} 36_{r1} \\ 2 \overline{)73} \end{array} \quad \begin{array}{r} 18_{r0} \\ 2 \overline{)36} \end{array} \quad \begin{array}{r} 9_{r0} \\ 2 \overline{)18} \end{array} \quad \begin{array}{r} 4_{r1} \\ 2 \overline{)9} \end{array} \quad \begin{array}{r} 2_{r0} \\ 2 \overline{)9} \end{array} \quad \begin{array}{r} 1_{r0} \\ 2 \overline{)2} \end{array} \quad \begin{array}{r} 0_{r1} \\ 2 \overline{)1} \end{array}$$

10010011

10010011

~~2175~~

$$\begin{array}{r} 0_{r1} \\ 2 \overline{)1}_{r0} \\ 2 \overline{)2}_{r1} \\ 2 \overline{)5}_{r0} \\ 2 \overline{)10}_{r1} \\ 2 \overline{)2}_{r1} \\ 2 \overline{)4}_{r1} \\ 2 \overline{)3}_{r1} \\ 2 \overline{)8}_{r1} \\ 2 \overline{)17}_{r1} \end{array}$$

$$\begin{array}{r} .6 \\ 2 \\ 1.2 \\ .4 \\ .8 \\ 1.6 \end{array}$$

1.2

.4

$$\begin{array}{r} 01110101_2 \\ 0xF5 \end{array}$$

10101111

~~10010011~~

0xAF

$$\begin{array}{r} 26_{10} \\ 16 \overline{) 333 } \\ 32 \\ \hline 13 \end{array}$$

$$16 \overline{) 20 }^{1r4}$$

$$16 \overline{) 1 }^{0r1}$$

0x14D

00010100

~~10000111~~₂

111

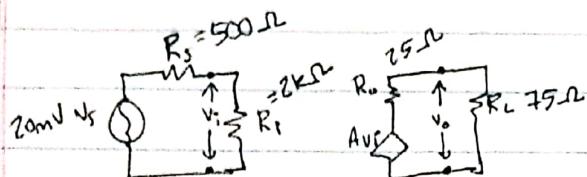
10000111

0000	0
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

F

$$\begin{array}{r} 0001 +1 \\ 1110 -2 \\ \hline 0) 1111 -1 \checkmark \end{array}$$

Exercise 1.2



$$\begin{array}{r} 500 \\ 16 \\ \hline 3000 \\ 5000 \\ \hline 8000 \end{array}$$

$$A = 500$$

$$V_s = 20mV$$

$$I_i = \frac{20mV}{500 + 2000\Omega} \approx \frac{2}{250} \approx 8\mu A$$

$$R_s = 500\Omega$$

$$\nexists V_i = I_i R_i = (8\mu A) \cdot 2000$$

$$R_i = 2k\Omega$$

$$V_i \approx 16mV$$

$$R_o = 25\Omega$$

$$R_L = 75\Omega$$

$$V_A = A V_i = 500 (16mV) = 8 \text{ Volts}$$

$$V_o = \left(\frac{75}{75+25} \right) (8V) = 6 \text{ Volts}$$

$$\text{What } A_v = \frac{V_o}{V_{o,i}} = ?$$

$$A_v = \frac{6 \text{ Volts}}{16mV} \approx \frac{6}{0.016} \approx 375$$

$$A_{VS} = \frac{V_o}{V_s} \quad A_i = ?$$

$$A_p = \frac{P_o}{P_s}$$

Sep 3rd, 2019

Floating Point Representation

Computer Systems

↳ PDP-11 Based Rep

12.75₁₀

$$\begin{array}{r} 6_{10} \\ 2 \overline{) 112} \\ 3_{10} \\ 2 \overline{) 16} \\ 1_{10} \\ 2 \overline{) 1 } \\ 1100_2 \end{array} \quad \begin{array}{r} .75 \\ \frac{1}{2} \\ .50 \\ \frac{1}{2} \\ 00_2 \\ .11 \end{array}$$

Need to deal with both very large
and very small numbers based
on application

Significant digits and scale
↳ Scientific notation

1100.11₂

0	10000100	10011000... 0
POS EXP	$4+128=132$	MANTISSA

→ Normalization

1100.11 * 2⁰

110.011 * 2¹

11.0011 * 2²

1.10011 * 2³

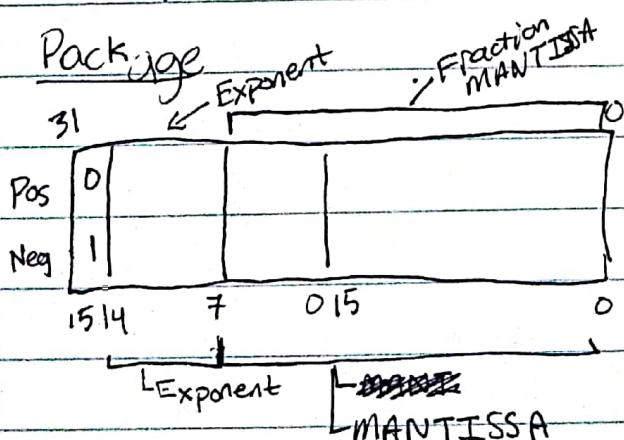
• 110011 * 2⁴

↳ Normalize to a fraction

with the leading decimal being

a 1

→ Since the one is always there, why
store it? We don't



- POS/NEG

- Sig. Dig.

- exponent

↳ +127 - -128

256 1111 1111 +127

⋮

+2

+1

128 1000 0000 -0

=2

exp +128

"Excess 128 Rep" 0 0000 0000 -128

Floats ARE APPROX! Don't check for equality

$$\begin{array}{r} 1.2 * 10^1 \\ 2.0 * 10^2 \\ \hline \end{array}$$

10^3

$$\begin{array}{r} 10000001 \quad 129 \\ 10000010 \quad 130 \\ \hline 00000011 \quad 259 \\ -128 \\ \hline 131 \rightarrow 3_{\text{EXP}} \checkmark \end{array}$$

= ✓

± ✓

± CONSTANTS ✓

exp + 128

exp2 + 128

exp + exp2 +

Take away one of the excess

All 0 exp → Rep for 0

$$\begin{array}{r} +2 \quad 1000 \quad 0010 \quad 130 \\ -1 \quad 0111 \quad 1111 \quad 127 \\ \hline & & 256 & 258 \\ & & \hline & -128 \\ & & \hline & 129 + 1 \checkmark \end{array}$$

$|A - B| < \epsilon$

A	$+.11 * 2^1$	0 10000001 (1) 100...0
B	$+.11 * 2^2$	0 10000010 (1) 100...0
C	$+.111 * 2^2$	0 10000010 (1) 110...0

View them as integers and they sort the same as they do as floats

With 16 bit words and 2 words / float

↳ ≈ 7 decimal places (single precision)

(Not PDP-11) 4 words ≈ 15 decimal places (double precision)

Booleans

All zeros is false

Anything other than zero will be true

Characters

Alphabet, Punctuation

↳ I/O contextual shapes

→ Culturally Sensitive

N Characters

$$\lceil \log_2 N \rceil$$

(EVERYONE ELSE)

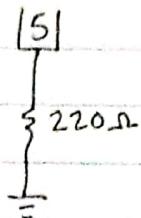
(IBM)

Standardized to ASCII and EBCDIC

Unit Record - Punch Card

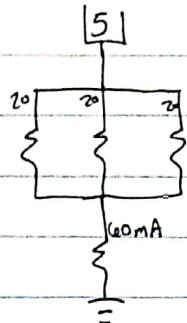
UNICODE - ISO 10646

221



511

330



221 ~~IL~~ 9.8mA

511 4.5mA

680 3.5mA

330 6.9mA

909 2.7mA

75kΩ

$$f(x) = e^x$$

$$V = IR$$

$$\frac{I}{R} \quad \frac{1}{R}$$

$$\frac{1}{X}$$

$$\frac{I}{\frac{1}{R}} = IR$$

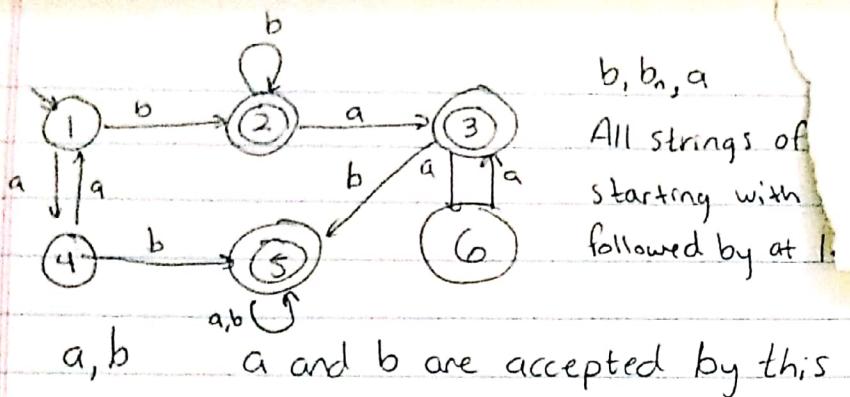
Pumpkin Drop Demo Ideas

Merch Ideas

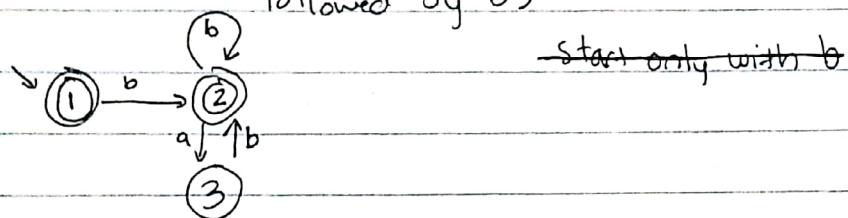
Expo Ideas

Long Term Projects (Semester)

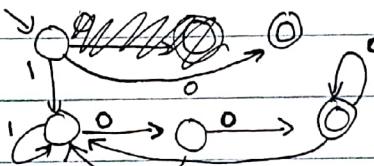
External Events



- a. $\{w \in \{a,b\}^*: \text{every } a \text{ in } w \text{ is immediately preceded and followed by } b\}$



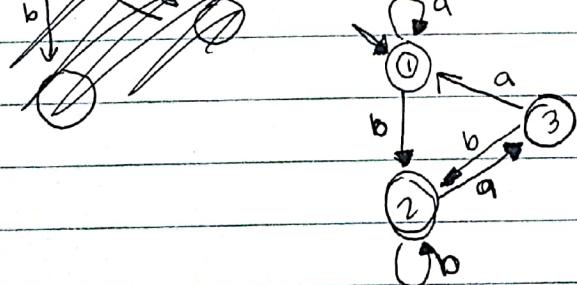
- b. $\{w \in \{a,b\}^*: w \text{ corresponds to a binary encoding, without leading leading zeros, of natural numbers that are evenly divisible by } 4\}$



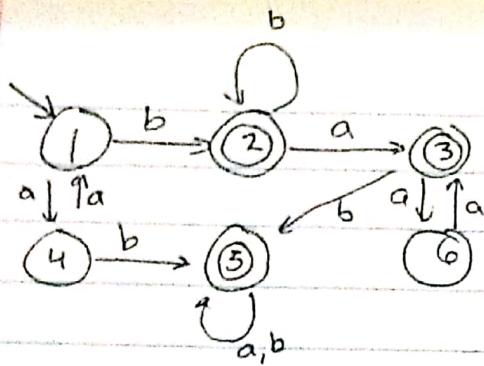
- c. $\{w \in \{a,b\}^*: w \text{ does not end in } ba\}$

ends in b ✓

ends in a only if from an a



Even a 's \rightarrow at least 1 $b \rightarrow$ zero or odd a 's



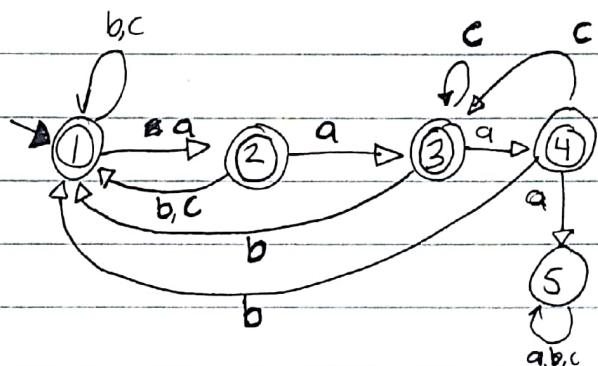
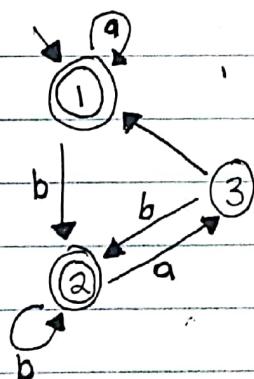
State 1 \rightarrow even number of a's -

* State 2 $\xrightarrow{4}$ odd number of a's $\xrightarrow{5}$ a b followed by anything

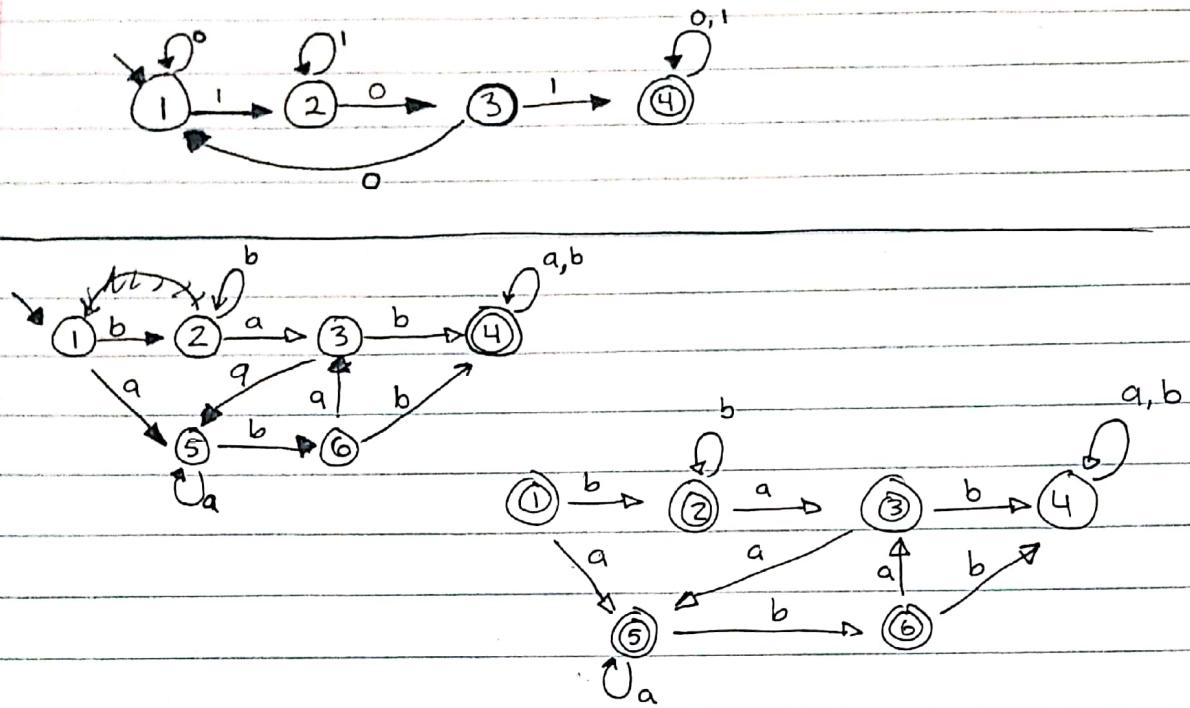
Any string that begins with an odd number of a's
followed by a b followed by nothing or and combination
of a's and b's

And!

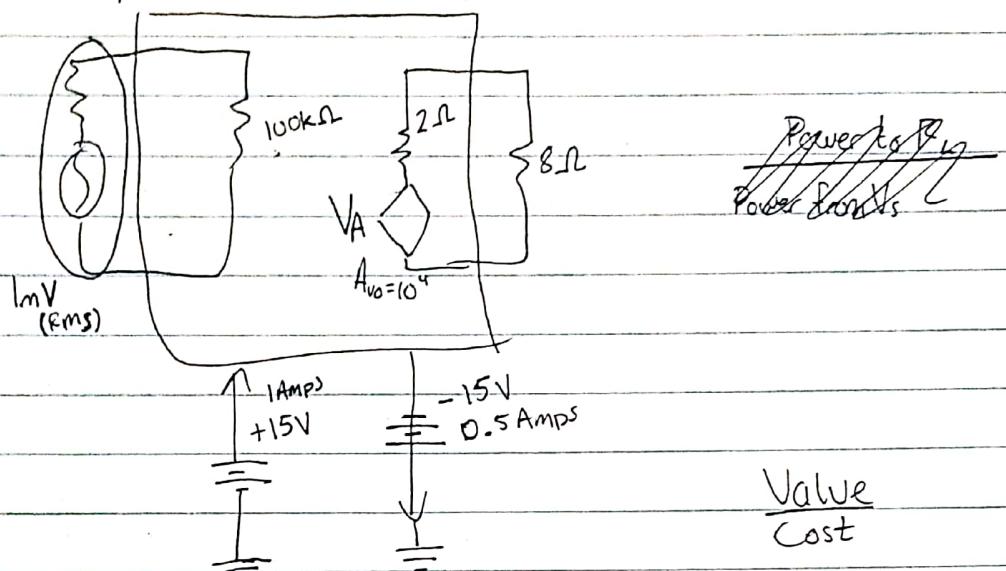
not end in ba



$\omega \in \{0,1\}^*$: ω has "101" as a substring



Amplifier efficiency



Power from R_L

$$\text{Power from } V_s + 15W + 7.5W \\ (\text{from + pin}) \quad (\text{from - pin})$$

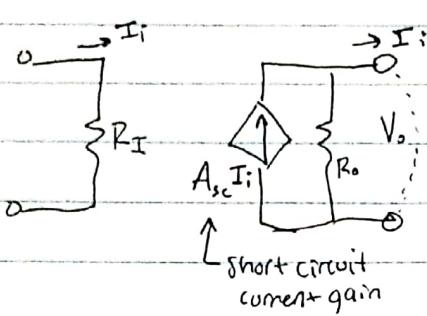
$$\frac{(1mV)^2}{100k\Omega} = P_I = 1 * 10^{-4} \text{ Watts}$$

$$1mV * 10^4 = 10 \text{ Volts}$$

$$\frac{V_o^2}{R_L} = P_o = \frac{64}{8} = 8 \text{ Watts}$$

$$V_o = 10 \left(\frac{8}{8+2} \right) = 8 \text{ Volts}$$

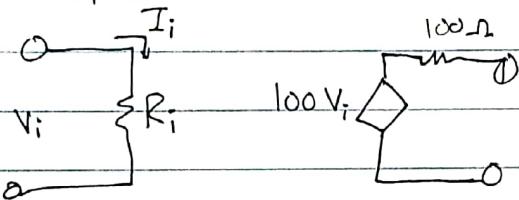
$$\text{Eff} \rightarrow \frac{8 \text{ Watts}}{22.5W + 10^{-4}W} \approx 35.5\%$$



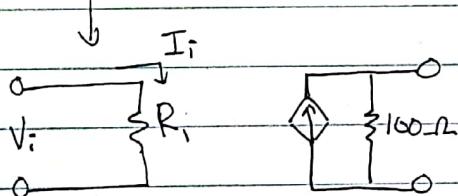
Short Circuit
Current Gain = A_{osc}

$$= \frac{I'_o}{I_i}$$

Example 1.5



Norton



$$A_{osc} = \frac{I_{osc}}{I_i}$$

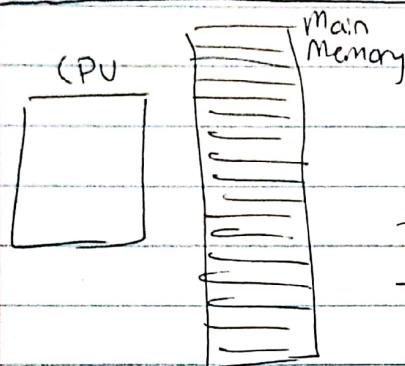
$$= \frac{100i}{100\Omega} \times \frac{1k}{Vi} = 1k$$

Computer Systems

UNICODE (16 bits/char)

context (which language)

followed by 16 bit chars



each cell has an address

(on PDP-11, 16 bit addresses)

- Data

- Instructions

Instructions - bit pattern to say which operation we need to do

↳ operations code (op code)

→ add, subtract, multiply, Divide (N)

↳ number of operations determines size of opcode $\lceil \log_2 N \rceil$

→ 16 operations in 4 bit opcode

→ addresses (one output, two inputs)^(m)

↳ operand * input₁, input₂, output $\lceil \log_2 M \rceil$

→ address of next instruction

4 address Instruction

OP CODE	INPUT ADDR ₁	INPUT ADDR ₂	OUTPUT ADDR	NEXT INSTR ADDR
---------	-------------------------	-------------------------	-------------	-----------------

Direct Access Memory - Read cells in any order

Random Access Memory - Read cells in any order and
in ~~at~~ the same amount of time
regardless of last cell read

3 address instruction

- Drop the Next INSTR ADDR to make a 3 address instruction
- add a register to the CPU
 - ↳ program counter (PC), Instraddr register
 - ↳ store current instruction address in this register
 - ↳ usually actually stores next cell
- store next instruction directly after the current instruction
 - ↳ Branches or jumps allow you to override the auto incrementation of the PC

2 address instruction

- the second input address is where the output is placed after the operation
- → you lose the second input and need to ~~save it~~ copy it if you need it later

1 address instruction

- Load and Store
- additional "accumulator" in CPU
 - load one address
 - → operate with another address
 - store with another address

0 address (stack address)

- make the accumulator a stack and do the op on the top two things on the stack

$$X = a + b * c$$

24 25 10 33

4AI

1. MUL b, c, x, 2
 2. ADD a, x, x, 3

~~MUL~~ 10, 33, 24, 2
 ADD 25, 24, 24, 3

2 INST, 8 Addresses

3AI

2 INST, ~~6~~ 6 addresses

2AI

1. MOV 33, 24
 2. MUL 10, 24
 3. ADD 25, 24

3 INSTR, 6 addresses (longer → better)

1A

1. LOAD 33
 2. MUL 10
 3. ADD 25
 4. STORE 24

4INSTR, 4 Addresses.

STACK

1. PUSH 25

2. PUSH 10

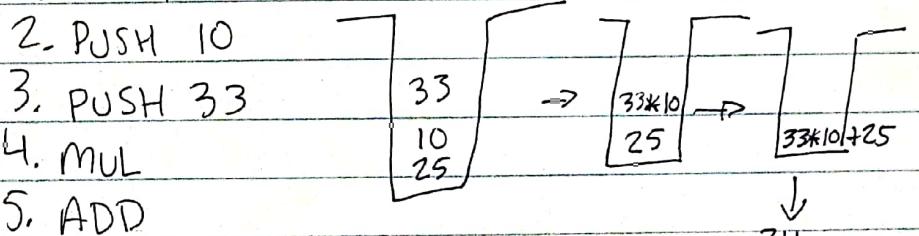
3. PUSH 33

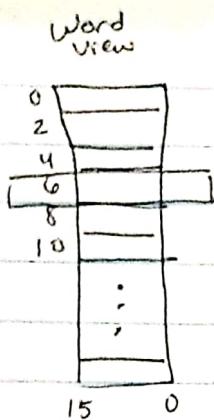
4. MUL

5. ADD

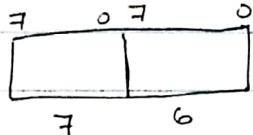
6. POP 24

(6INSTR 4 Addresses)





Word and byte addressable



WORD	
1	0
3	2
5	4
7	6
9	8

BYTE

Registers are only word addressable 16 bit

BUS is 16 bits

Registers

0	
1	
2	
3	
4	
5	
6	
7	

Roles

- Accumulator
- Help form addresses

Processor Status Word (Processor Status Register)

- 16 bits → boolean status flags

N - negative Z - zero

V - overflow C - carry out of high order bit
~~(overflow flag)~~



$$\begin{array}{r} 1000_2 \\ \times 10 \\ \hline 10000_2 \end{array}$$

4_{10}

2_{10}

8_{10} ✓

$$1000_2 = 4_{10}$$

$$101000_2 = 40_{10}$$

~~$$\begin{array}{r} 101000 \\ \times 1000 \\ \hline 01000000 \end{array}$$

$256 \quad 128 \quad 64 \quad 32 \quad 16 \quad 8 \quad 4 \quad 2$

$64 + 32$ ✓~~

$$\begin{array}{r} 101000 \\ \times 100 \\ \hline 40_{10} \end{array}$$

~~$$\begin{array}{r} 10100000 \\ \times 100 \\ \hline 128_{10} + 32_{10} = 160_{10} \end{array}$$

$64 \quad 32 \quad 16 \quad 8 \quad 4 \quad 2$

✓~~

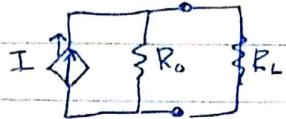
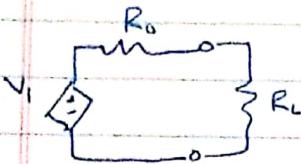
C-AND $\Sigma = X \oplus R$

$\Sigma = 1 \text{ if } (A=1, B=0) + (A=0, B=1)$
 $\text{if } (A \neq B)$

)
 $\text{if } (A \cdot \bar{B}) + (\bar{A} \cdot B)$

How

0
1
0
1
0
1



$$V_i = 3 \text{ Volts}$$

$$R_o = 100 \Omega$$

$$R_L = 10 \Omega$$

$$R_o = 100 \Omega$$

$$R_L = 10 \Omega$$

$$V_o = V_i \left(\frac{R_L}{R_o + R_L} \right)$$

$$V = IR$$

$$I = \frac{V}{R}$$

$$I = I_o + I_L = \frac{V_o}{R_o} + \frac{V_o}{R_L}$$

$$V_i = R_o I$$

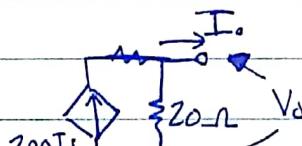
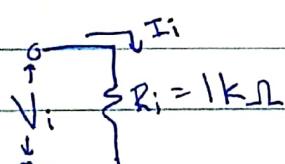
$$I = \frac{V_o(R_o + R_L)}{R_o R_L}$$

$$5 = 100 \Omega I$$

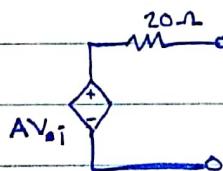
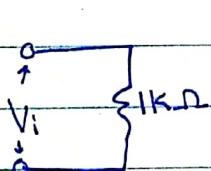
$$I = \frac{5 \text{ V}}{100 \Omega} = \frac{1}{20} \text{ Amps} = .05 \text{ Amps} = 50 \text{ mA} ?$$

Ex 1.10

Current Amp



Voltage Amp



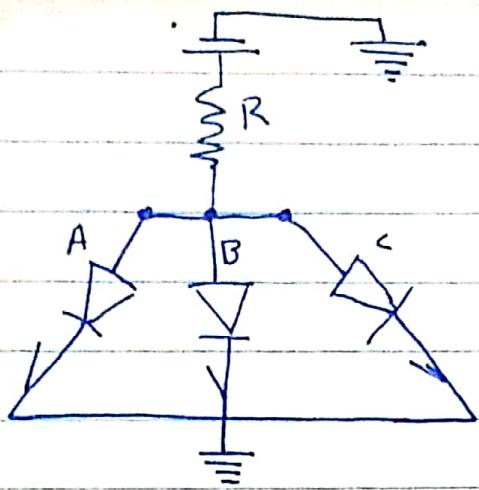
$$AV_o i = R_o I_o$$

$$200 I_i = \frac{AV_o i}{R_o}$$

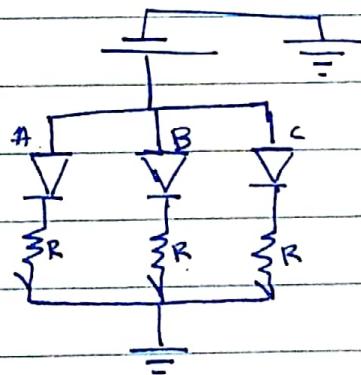
$$AV_o = R_o 200 I_i$$

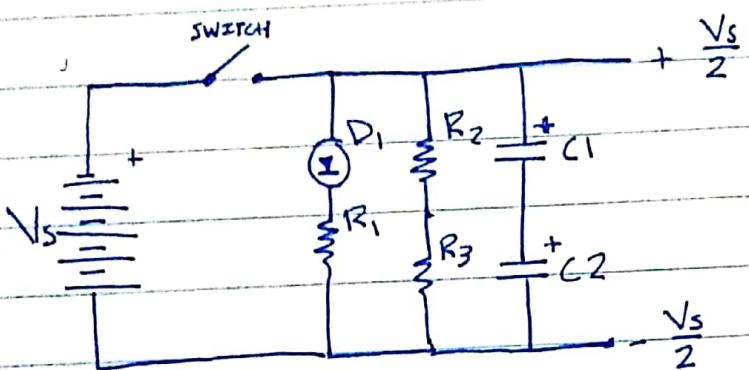
$$A_o = \frac{200 I_i R_o}{V_i}$$

$$A_o = \frac{R_o 200 I_i}{V_i}$$



VS





-0 000000 000000
1 8 6

0.0000011

.11 E5

101

10000000

10000101 128+4+1=133

S	EXP	MANTISSA
1	10000101	0000011
0	10000101	0000011

1
10B

W.D

10.10011001

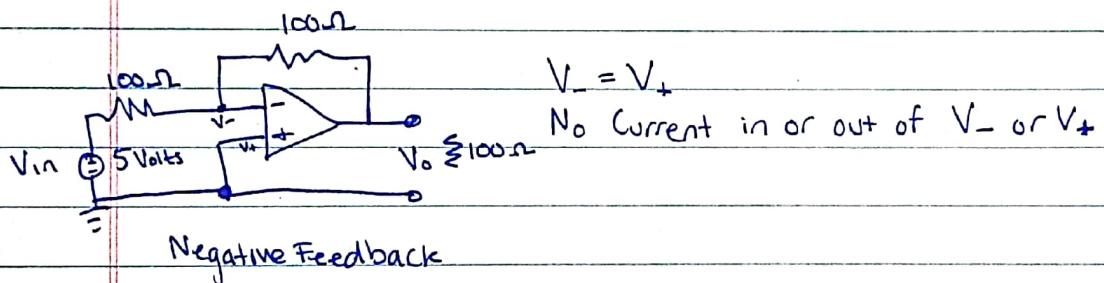
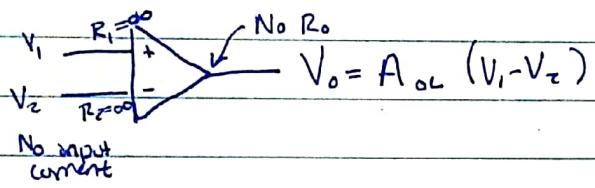
10.1001

10.1010

$$\Delta V_o = \Delta I = \frac{1234 eV/nm}{\lambda nm}$$

$$2.1 V \cdot e = \frac{1234}{\lambda}$$

$$\lambda = \frac{1234}{2.1} = 587 nm$$



$$i_1 = i_2 \quad \frac{V_{in} - 0}{R_1} = \frac{0 - V_o}{R_2} \rightarrow \frac{V_{in}}{R_1} = -\frac{V_o}{R_2}$$

$$V_o = -\frac{V_{in} R_2}{R_1}$$

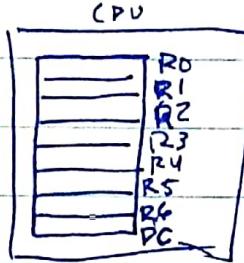
$$V_o = -\frac{R_2}{R_1} V_{in}$$

1	0	0
3	2	
5	4	
.	.	.

PDP-11 is word and byte addressable

Comp. Sys

Word addressable Registers



General Purpose Registers

Help form addresses

↳ some times index registers

Processor Status Word

R7 → Program Counter

Register (16 bit) for CPU Status

"N Z V C" boolean status bits (T-1 F-0)

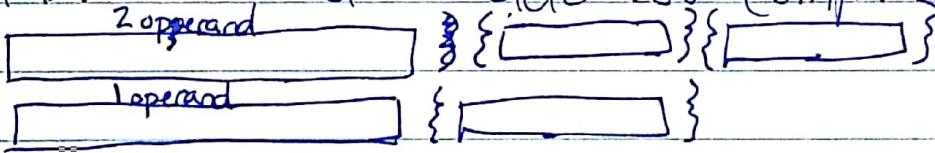
• Negative

Zero

V Overflow

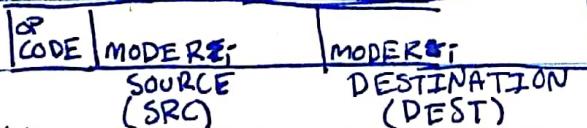
C Carry

PDP-11 is a 2-address comp.



Z operand

4 6



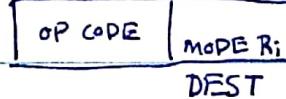
Addressing mode

2=8

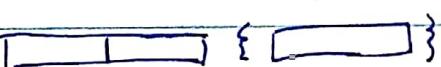
5 4 3 2 1 0

I operand

10



Extra words for extra info



High level language C/C++ $A = B + C$

m.m.



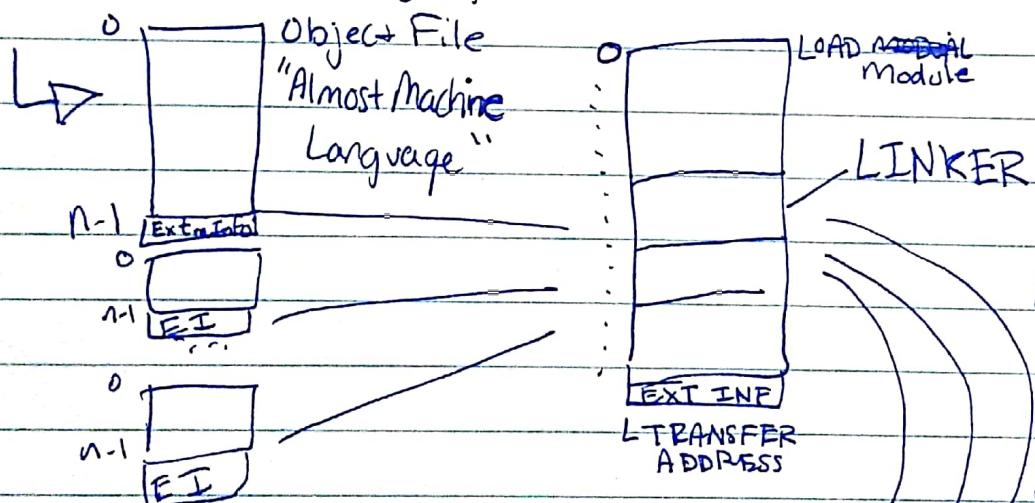
Low level language Assembler MOV 10,20

↓
substitution
via
"assembler"

AS LOW AS YOU CAN GO

Machine Language

Compile - "Translate" from higher level language to the Machine Language of the machine



LOADER
Changes
Addresses
Now That
We Know
Where the
Addresses Actually
Are

HLL Variables
 $A = B + C$

Cell of memory has address and contents. That's it.

Low No Variables!
ADD B, C
 |
 +---+
 Address

HLL \rightarrow contextual data types
determine the operand type
+ \rightarrow addition, concat, etc.

LLL \rightarrow Operator decides the type of the operands

MACRO-II TWO PASS MACRO ASSEMBLER (READ FILE TWICE)

{Label:} Operator {Operand(s)} {Comments}

[Col 1] \hookrightarrow Statement must be one line upto 127 chars
↳ one statement per line separate with a comma

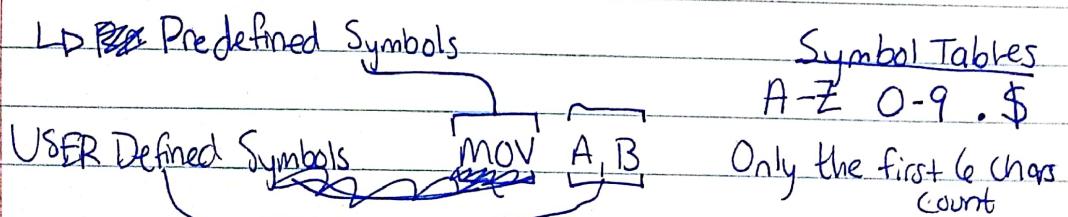
[Col 2] At least 1 space after operands

[Col 3]

Use a fixed sized font so things line up

Operators
"ADD"

Directives \rightarrow tell the software to do something. Save 10 words of memory
+ R0, R1, R2...



10 \rightarrow defaults to base 8

10. \rightarrow . is directive to signify base 10
A

No operator precedence - <...> grouping directive