Electronics Lab 05: Analogue to Digital Converters

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Abstract

We introduced comparators as a new integrated circuit and applied them in a digital to analogue converter (ADC), a very common and useful circuit. Our ADCs successfully turned an incoming signal, alternating or otherwise, into a respective $2^n - 1$ format binary output. Using 4 comparators we achieved a 4 bit output, but only used 5 potential outputs. To further this design we could build a code converter to turn our 4 bit $2^n - 1$ where n = the number of bits + 1, signal into a standard binary signal.

I. PURPOSE

To familiarize ourselves with comparators as a standardized circuit and apply them in a meaningful way. Conversion from analogue to digital, and back, is one of the most common electronic hardware applications. While we didn't go in depth into the world of ADCs, we now have a basic understanding of one way they can work and this gave us a practical use case of comparators.

II. CONCLUSIONS

A comparator based ADC is relatively simple in design but rather costly in both hardware and space. Each comparator adds only one additional layer of accuracy, not even an entire bit. It's rare that such a design would be practical in any format other than an integrated circuit. Nonetheless, our design did indeed work and it is directly scalable.

III. THEORY

We can set each comparator to turn on an led when Vin is greater than Vref with the rather simple circuit diagram seen below.

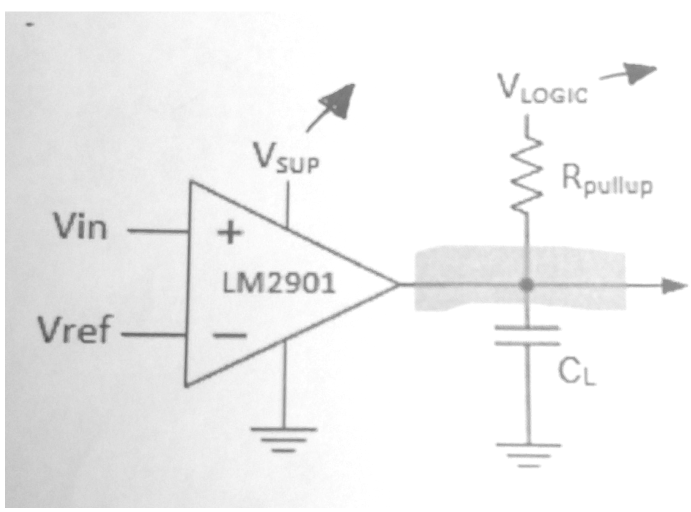

FIG. 1. Frequency and Gain Voltages

If we can build a linear increasing Vref, we can use the same Vin and multiple comparators, one for each led, to achieve a shifting binary output of signal amplitude. Since comparators have a very high input impedance we can use simple voltage dividers to achieve our varying Vref values, and a "ladder" resistor will save us some space and building complexity as well.

Below you can see a circuit diagram implementing 4 comparators, one for each led and reference voltage. Note that V_{sup} must be at least 2 Volts above V_{logic}, since we are using the LM239 comparators. That makes this design quite simple to scale, although not very space efficient.

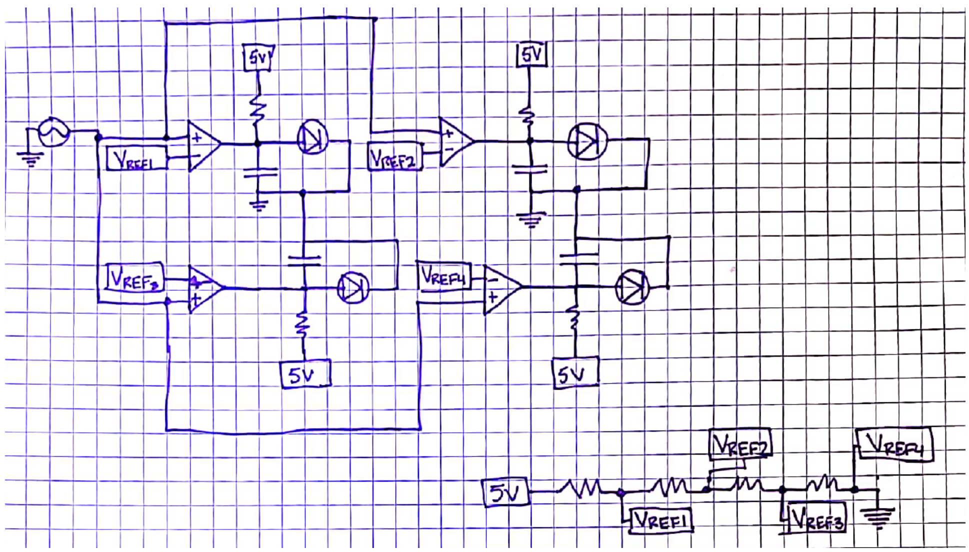

FIG. 2. Frequency and Gain Voltages

IV. ANALYSIS

One arguable flaw of this system beyond efficiency is that our output is a shifting binary output rather than a straight binary output. When we increase a level of amplitude our output does increment binarily by one, but rather the right most least significant bit turns on. That gives only n+1 usable outputs, where n is the number of comparators (bits). A normal 4 bit output has $2^4 = 16$ possible outputs, but we our only using $4 + 1 = 5$ of those outputs. This proves a not only another layer of poor efficiency but also implies the requirement for additional hardware to convert this output to a more useful format. It would certainly depend on the application, but this is arguably not the most ideal output format.