

Digital Circuits

HW 3

WHO?

Stammer?

Ch2: 2, 4, 14, 16, 24, 28, 33, 38, 40, 44

49/40

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

$$\text{SOP: } A + \cancel{B} = A + B \quad (A + \bar{A}B) \cancel{= AB}$$

POS: ~~AB~~

POS: $(A + B)$

b) $A \ B \ C \ | \ Q$

0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

SOP: $\bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + A\bar{B}C$

$= \bar{A}(\bar{B}C + B\bar{C} + BC) + A(\bar{B}\bar{C} + \bar{B}C)$

$= \bar{A}(C(\bar{B} + \cancel{B} + B) + BC) + A(C(\bar{B} + B))$

$= \bar{A}C + B\bar{C} + A\bar{C}$

$= \bar{A}C + \bar{B}(B + A)$

POS: $(A + \bar{B} + \bar{C})(A + \bar{B} + C)(\cancel{A + B + C})$

c) $A \ B \ C \ | \ Q$

0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

SOP: $\bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$

$= A(\bar{B}C + B\bar{C})$

$= \bar{A}\bar{B}C + AB$

POS: $(\bar{A} + \bar{B} + \bar{C})(\bar{A} + B + \bar{C})(\bar{A} + B + C)(A + \bar{B} + \bar{C})$

✓

d) POS: $\cancel{ABCD} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + \cancel{ABC\bar{D}}$

POS: $(\bar{A} + \bar{B} + \bar{C} + \bar{D}) + (\bar{A} + B + \bar{C} + \bar{D}) + (\bar{A} + B + \bar{C} + D) + (A + \bar{B} + \bar{C} + D) + (A + \bar{B} + C + D) + (A + B + \bar{C} + \bar{D}) + (A + B + \bar{C} + D)$

$+ (A + B + C + \bar{D}) + (A + B + C + D)$

e) SOP: $\bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D}$

$$\begin{aligned}
 14(a) Y &= \bar{A}BC + \bar{A}\bar{B}\bar{C} \\
 &= \bar{A}(BC + \bar{B}\bar{C}) \\
 &= \bar{A}(B(C + \bar{C})) \\
 Y_s &= \bar{A}\bar{B}
 \end{aligned}$$

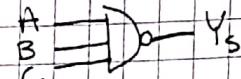
A	B	C	Y	Y _s	✓
0	0	0	0	0	
0	0	1	0	0	
0	1	0	1	1	
0	1	1	1	1	
1	0	0	0	0	
1	0	1	0	0	
1	1	0	0	0	
1	1	1	0	0	

14(a)



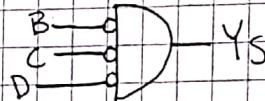
$$\begin{aligned}
 b) Y &= \bar{ABC} + A\bar{B} \\
 &= \bar{A} + \bar{B} + \bar{C} + A\bar{B} \\
 &= \bar{A} + \bar{C} + \bar{B} (\cancel{+A}) \\
 Y_s &= \bar{ABC}
 \end{aligned}$$

A	B	C	Y	Y _s	✓
0	0	0	1	1	
0	0	1	1	1	
0	1	0	1	1	
0	1	1	1	1	
1	0	0	1	1	
1	0	1	1	1	
1	1	0	1	1	
1	1	1	0	0	



$$\begin{aligned}
 c) Y &= ABC\bar{D} + A\bar{B}C\bar{D} + (\cancel{A} + \bar{B} + \bar{C} + \bar{D}) \\
 &= ABC\bar{D} + A(\bar{B} + \bar{C} + \bar{D}) + A\bar{B}C\bar{D} \\
 &= A(B\bar{C}\bar{D} + \bar{B} + \bar{C} + \bar{D}) + A\bar{B}C\bar{D} \\
 &= A(\bar{D}(B\bar{C}\bar{T}) + \bar{B} + \bar{C}) + A\bar{B}C\bar{D} \\
 &= A\bar{D}\bar{B}\bar{C} + A\bar{B}\bar{C}\bar{D} \\
 Y_s &= \bar{B}\bar{C}\bar{D}
 \end{aligned}$$

A	B	C	D	Y	Y _s	✓
0	0	0	0	1	1	
0	0	0	1	0	0	
0	0	1	0	0	0	
0	0	1	1	0	0	
0	1	0	0	0	0	
0	1	0	1	0	0	
0	1	1	0	0	0	
0	1	1	1	0	0	
1	0	0	0	1	1	
1	0	0	1	0	0	
1	0	1	0	0	0	
1	0	1	1	0	0	
1	1	0	0	0	0	
1	1	0	1	0	0	
1	1	1	0	0	0	
1	1	1	1	0	0	

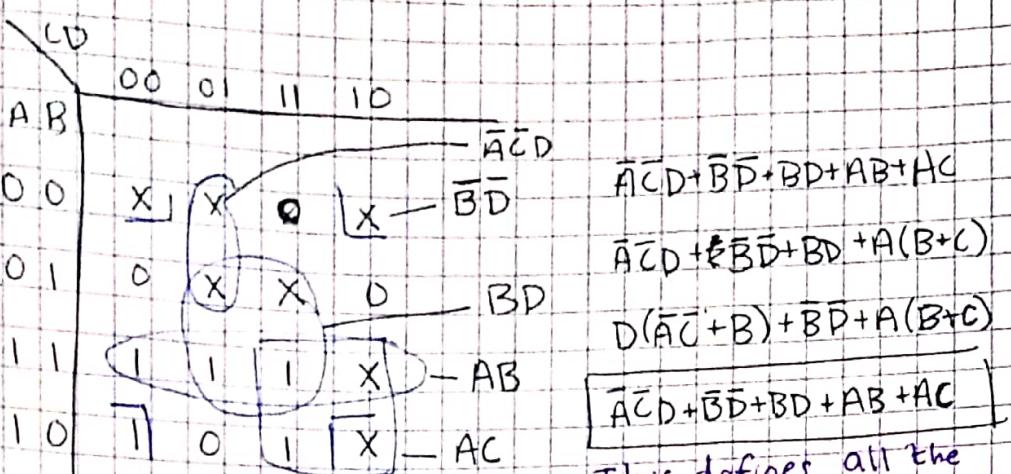


$$\begin{aligned}
 24.) Y &= (AD) + (A\bar{C}D) + (\bar{A}\bar{B}C) + (ABC\bar{D}) \\
 &= \bar{A}D + A\bar{C}D + A\bar{B}C + ABC\bar{D}
 \end{aligned}$$

$$Z = BD + A\bar{C}D$$

✓

AB	CD	Q
0 0	0 0	X
0 0	0 1	X
0 0	1 0	X
0 0	1 1	0
0 1	0 0	0
0 1	0 1	X
0 1	1 0	0
0 1	1 1	X
1 0	0 0	1
1 0	0 1	C
1 0	1 0	X
1 0	1 1	1
1 1	0 0	1
1 1	0 1	1
1 1	1 0	X
1 1	1 1	1



This defines all the X's as true.
Take away the $\bar{A}\bar{C}D$ grouping to fix it.

So, $\bar{B}\bar{D} + DB + AB + AC$
 $AB + AC$

- 33.) Sunny days (5) with no ants (A)
also on days with with hummingbirds(h)
also on days where there are ants(a) and ladybugs(L)

E = Enjoy

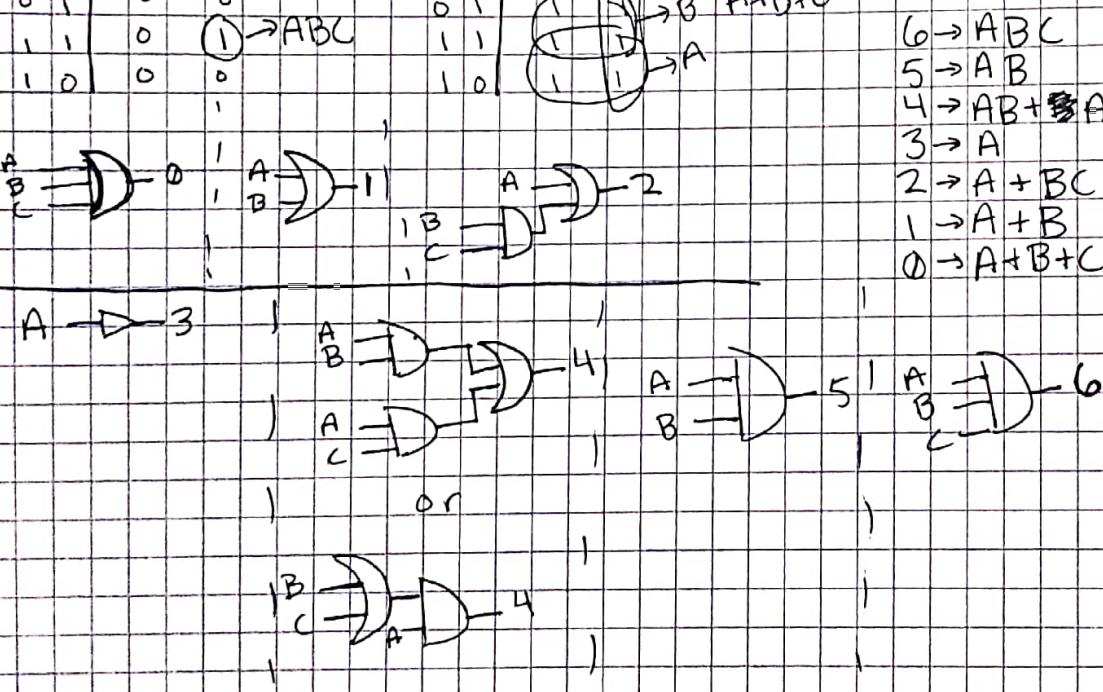
✓ ✓
you don't have
to fix them or
fix though!

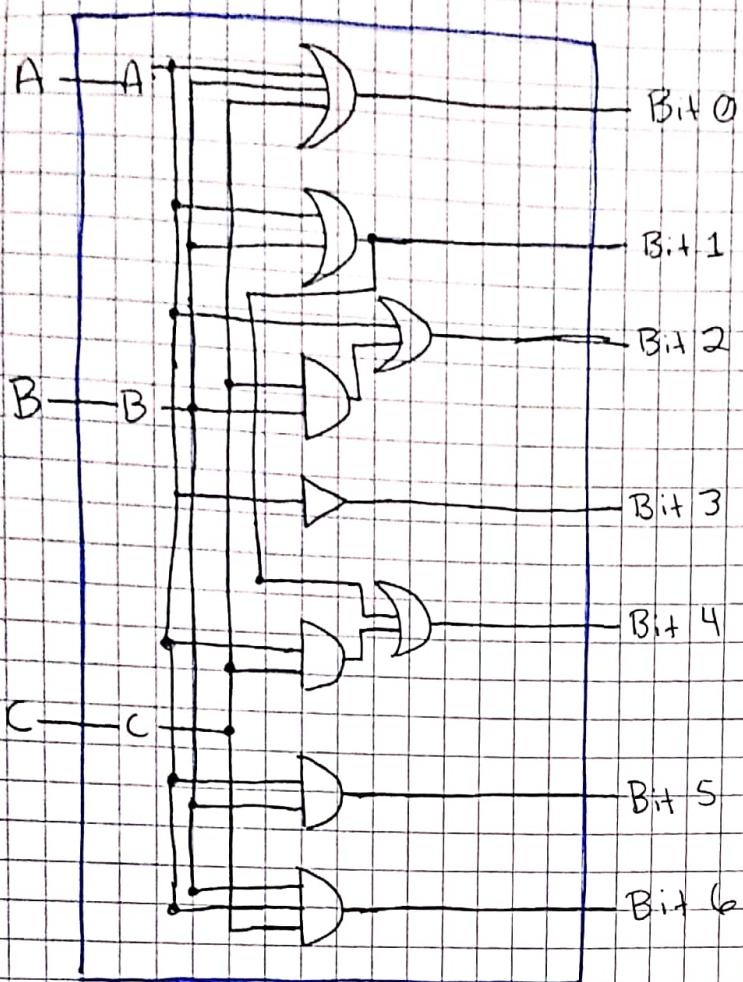
$E = SA + H + AL$

38.) 00,00,00,0,0.

Repeat Karnaugh maps
for each bit. Only
bit 0 and bit 6 shown.

$6 \rightarrow ABC$
 $5 \rightarrow AB$
 $4 \rightarrow AB + AC \rightarrow A(B+C)$
 $3 \rightarrow A$
 $2 \rightarrow A + BC$
 $1 \rightarrow A + B$
 $0 \rightarrow A + B + C$





40.

$$\begin{aligned}
 Y &= \overline{AB} + CD(\overline{AB} + \overline{AB}) \\
 &= \overline{AB} + CD(A \oplus B)
 \end{aligned}$$

44.

AND	30 ps
NOR	30
NOR	30
NAND	20

110ps depending on the inputs and the state

Physics 332 Computer Organization Lab 2: Introduction to Logic Gates

Purpose: There are three objectives to this lab.

1. The first objective is to introduce construction of circuits using the bread boards (see Appendix B).
2. The second is to show how logic gates are constructed from simpler electronic components such as transistors.
3. The final objective is to introduce students to logic gates on integrated circuits (IC).

Introduction: There are two (and sometimes three!) logic states in digital electronics: Either 'On' (i.e 'HI' or '+5 Volts') or 'Off' (i.e. 'LO' or '0 Volts'). These correspond to the binary states 1 and 0 respectively. The inputs to a logic gate (e.g. an AND gate) determine its output. The different states of logic gates can be summarized in Truth Tables. Truth Tables display the different combinations of inputs and their associated outputs. This Truth Table for a dual input AND gate is an example:

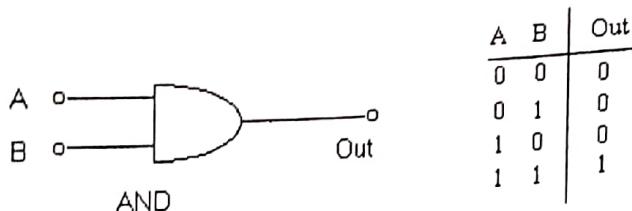


Figure 1

Construct the following circuits and answer the associated questions.

The output of all of the gates constructed in this lab will be tested using a LED (light emitting diode). In addition to the regular properties of a diode, a LED also emits light when current passes through it. The LEDs are labeled 0-7 at the top of your "Trainer". Each of these diodes is connected to ground through a resistor **inside** of the "Trainer" (figure 2). This ground connection essentially 'completes' the circuit so electricity can flow. You can only see the LED itself. When the LED is lit, it indicates an input of +5 Volts. If you prefer, you can use an LED and a ~300Ohm resistor directly on your breadboard as an indicator.

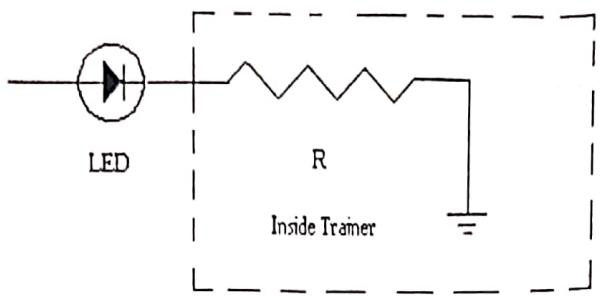


Figure 2

I.) Transistor Logic Gates

Logic gates are made from transistors. Note that the gates constructed with the transistors will use a +5 Volt input to represent 'HI' and 0 Volt input to represent a 'LO'.

Recall the basic rules for the transistors. The transistor has 3 leads: the collector (c), emitter (e), and base (b). For the NPN transistor (shown in figure 6) current will easily flow from the collector to the emitter if the base voltage is 0.6 Volts greater than the emitter voltage. In other words the emitter-collector connection can be thought of as a closed switch. If the base voltage is not larger than the emitter voltage, then the emitter-collector connection can be thought of as an open switch since no current can flow from the collector to the emitter. The current flowing in the base is always negligible.

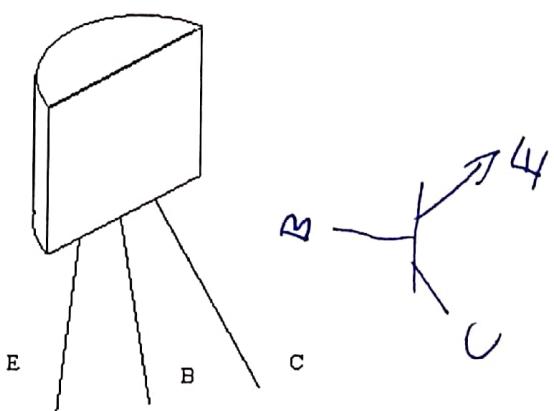


Figure 3

Consider the following circuit

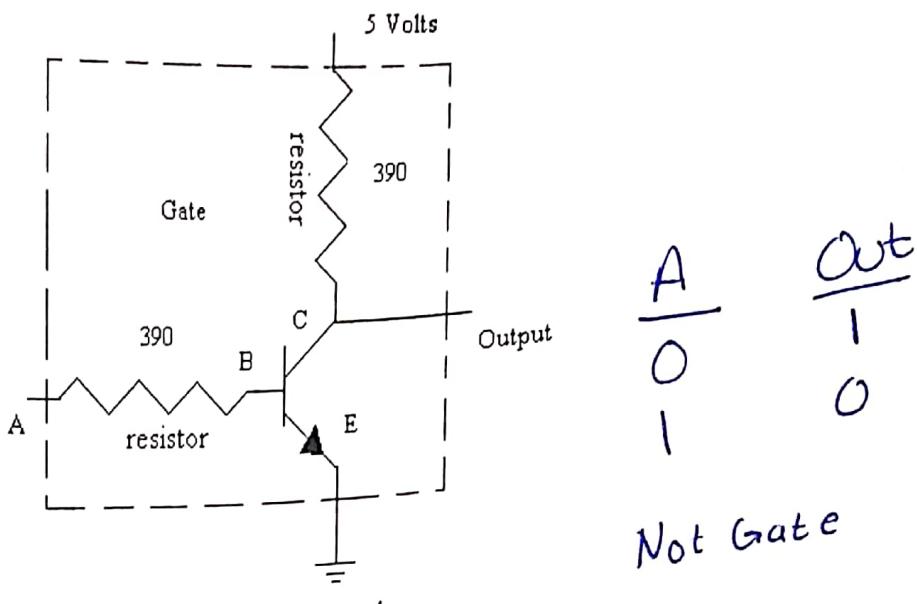


Figure 4

Questions

- 1.) What kind of gate is this? To answer this question, build the circuit with a 3904 transistor¹ and measure its Truth Table. A is the input. Use the Power Supply on the Kit for the 5 Volts (use the red or pos terminal). Use figure 3 to determine E, B, and C. Remember, the output of this circuit should be hooked up to one of the LEDs.

- 2.) Select the integrated circuit (see Appendix A of this lab) that corresponds to the circuit in figure 4 and construct a circuit* using one of the gates on the chip. For the IC, use +5 Volts as the HI signal and 0 Volts as the LO. Remember, the output of this circuit should be hooked up to one of the LEDs. Measure the Truth Table for the gate you selected and compare it to the Truth Table for the circuit above. Did you select the correct integrated circuit?



* To use the integrated circuit (IC), you must supply power to the chip just like the transistor gate used here which needs a 5 Volt power hook up. However, you do not need to use a resistor. Look at the pin layout on the last page of this lab. The pins are labeled from 1 to 14 (or some other number)

¹ Note, other NPN transistors will work, eg a 2222. The EBC layout will differ through, so make sure you check the appropriate spec sheet.

depending on the number of pins on the chip). Now pick up the chip. Notice the notch on the top of the chip.

Consider the following circuit

Expected

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

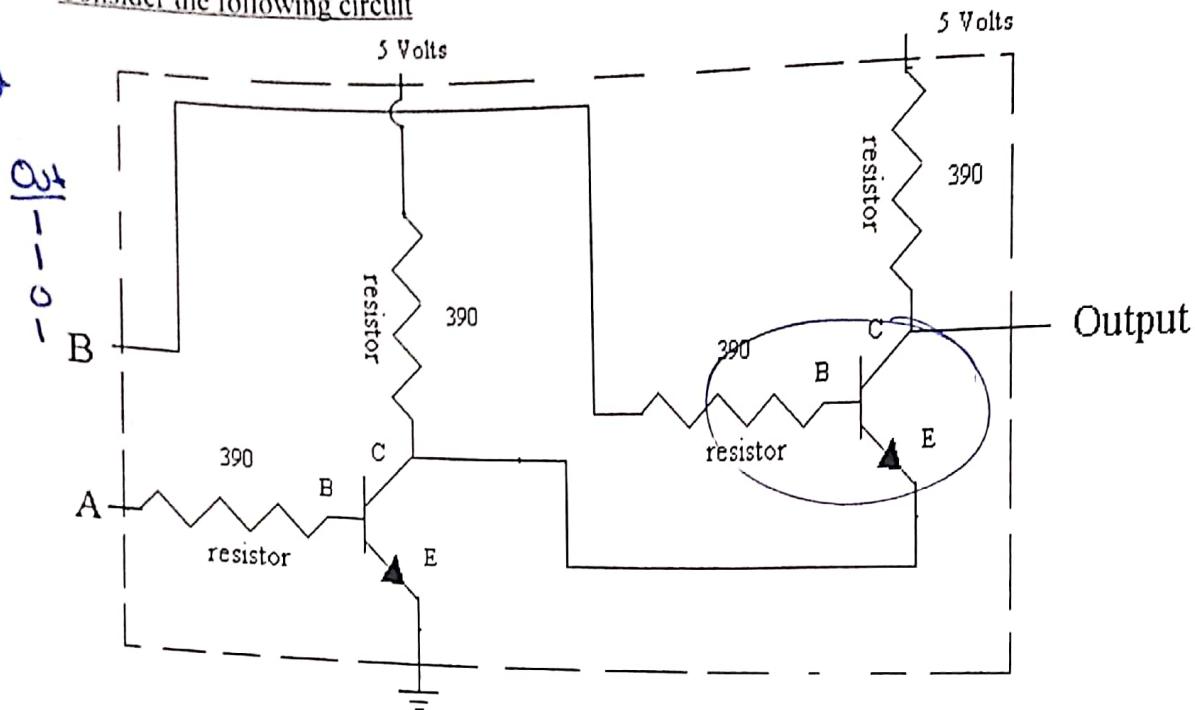


Figure 5

Questions

- 3.) What kind of gate is this? To answer this question, build the circuit and measure its Truth Table. A and B are the inputs. Remember, the output of this circuit should be hooked up to one of the LEDs.

NAND GATE - Only off when A and B are true

- 4.) Select the integrated circuit (see Appendix A of this lab) that corresponds to the circuit in figure 5 and construct a circuit using one of the gates on the chip. Measure the Truth Table for the gate you selected and compare it to the Truth Table for the circuit above. Did you select the correct integrated circuit?

A	B	O
0	1	1
0	0	1
1	1	0
1	0	1

II.) The XOR Gate

There is one last important gate to study. It is called the exclusive OR gate which is often called the XOR gate.

- 6.) Choose the chip that has dual input XOR gates and measure its Truth Table.

0	0	0
0	1	1
1	0	1

How is the XOR gate different from the OR gate?

XOR IS False when all inputs are true

- 7.) Finally, using the XOR chips, investigate how IC's interpret a pin that is not hooked to ground or to +5 Volts (i.e. it is left 'floating'): Let one of the input gates 'float' and connect the other gate input to ground or +5 Volts. What is the output in both cases? Is a floating input interpreted as HI or LO?

The chips don't know what it is and built up noise and even capacitance could cause the value to fluctuate.
Do the same test for an OR gate. Is a floating input interpreted the same way?

III.) 7-Segment Display

The 7447 IC has 4 inputs labeled A, B, C, and D. It also has 7 outputs which can be used to light the 7 LEDs (labeled a-g) in a 7-segment display. The pinouts for the display and the chip are in the appendix.

Connect the 7447 to the 7 segment display.

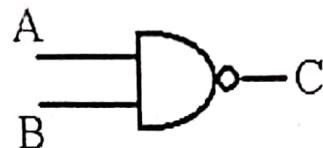
For the 7447, you can leave pins 3, 4, and 5 disconnected. Pins 1, 2, 6, and 7 are the inputs. You should hook these to the Data Switches. The Data Switches give a +0 Volt output and a +5 Volt output depending on the position of the switch. Pins 9 - 15 should be hooked up to the display. Before hooking the switches up to the 7447, make sure they work by using a testing LED.

A	B	OR
0	0	0
0	1	1
1	0	1
1	1	1

5.) The NAND and NOR gates are often referred to as universal gates since any other gate can be constructed from a combination of them.

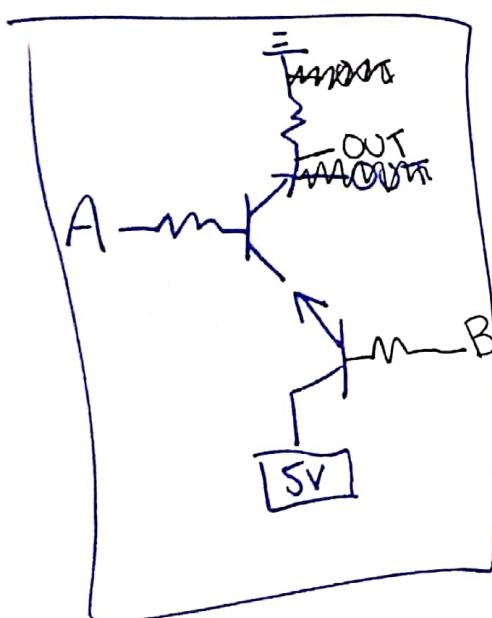
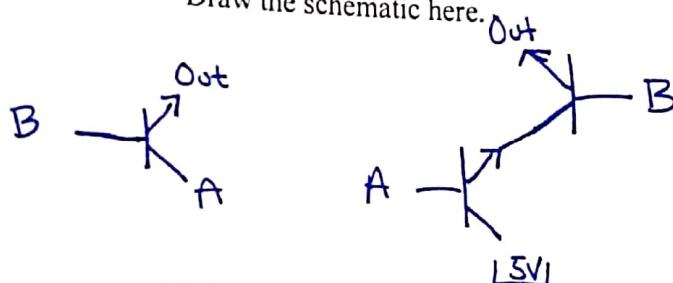
- a) How can you use one (and only one) NAND gate to make the logic gate that corresponds to figure 4? Using the logic circuit symbol for a NAND gate, draw the schematic. (Hint look at the TT for the NAND gate)

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0



Hook A and B together. Then when A is false C is true, and when A is true (thus making B true), C is also true

- b) Using the experience you have gained from this lab, build an AND gate from transistors. Test your circuit to make sure it works. Draw the schematic here.



Appendix A: Integrated Circuit Pin Layouts

All of the chips shown here and most of the chips that we will use in the future can be found in the CMOS Logic Data book or The TTL Data Book. Both books are on the book shelf in the lab. To find pin layouts or other information about a chip, just look for its number in the index. Note how the chips are labeled. For example the AND gate is on a chip labeled MM74HC08. Any chip that has the number 74 XX 08 is an AND gate. The same is true for any other chips.

MSB?

- 8.) Try turning on one or two data switches. What does the 7-segment display read? Try other data switch combinations. Create a "Truth Table" for the 7447 IC that has the 4 inputs (A, B, C, and D) and indicates the corresponding display (1, 2, ...).

D	C	B	A	# ₁₀	# ₁₆
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	10	A
1	0	1	1	11	B
1	1	0	0	12	C
1	1	0	1	13	D
1	1	1	0	14	E
1	1	1	1	15	F

Q	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	1	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	0	0	1	1
A	0	0	0	1	1	0	1
B	0	0	1	1	0	0	1
C	0	1	0	0	0	1	1
D	1	0	0	1	0	1	1
E	0	0	0	1	1	1	1
F	0	0	0	0	0	0	0

- 9.) What function does the 7447 perform?

It displays a binary input as decimal digits on the 7 segment display

Lab Reports: There are two things required in the lab report

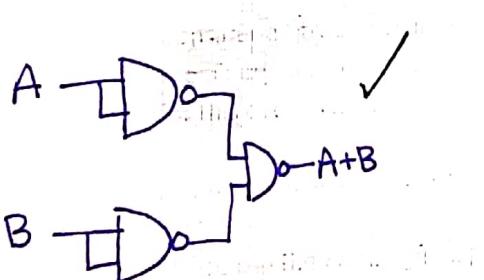
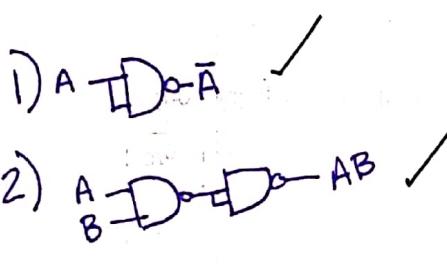
1. You need to provide the answers to the questions in the space provided.
2. You need to end the report with a conclusion that directly addresses the Purpose (at beginning of lab handout) of each lab. This is a summary of what you learned. You may provide the summary here:

13/14

Adam Stammer

NAND (not Negative-AND) gates are said to be universal. So...

- ✓ 1) How can you make a NOT gate out of a NAND?
- ✓ 2) How can you make an AND gate out of NANDS?
- ✓ 3) How can you make an OR gate out of NANDS? (Hint, think about DeMorgan's Theorem).
- 4) Consider a "greater than" circuit which returns $f=1$ when the binary number AB is greater than the binary number CD and $f=0$ otherwise (specifically $f = (AB > CD)$). Please create a truth table for this circuit (with columns AB CD f , take A and C to be MSB's).
- 5) Please create a Karnaugh Map for this greater than circuit.
- 6) Please use the Karnaugh map to create a minimal SOP expression for f .
- 7) Please use the Karnaugh map to create a minimal POS expression for f .

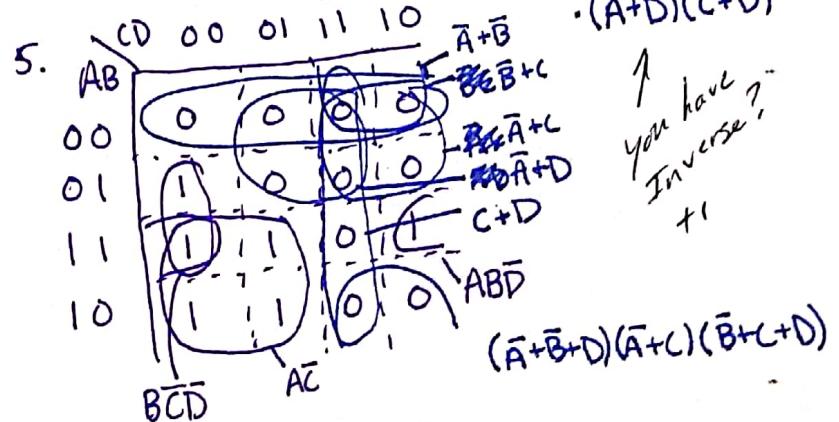


4.)

AB	CD	F
00	01	0
00	10	0
00	11	0
00	00	0
01	00	1
01	01	0
01	11	0
01	10	0
01	00	1
10	01	1
10	11	0
10	10	0
10	00	1
11	00	1
11	01	0
11	11	0
11	10	1

$$(6.) AB\bar{D} + AC + BC\bar{D} \\ = BD(A+C) + AC$$

$$(7.) (\bar{A}+\bar{B})(\bar{B}+C)(\bar{A}+C) \\ \cdot (\bar{A}+D)(C+D)$$



Physics 332; Computer Organization
Lab 3: Boolean Expressions, Logic Circuits, and Simplification

Purpose: There are three objectives to this lab.

1. The first is to practice applying the basic rules of Boolean algebra.
2. The second is to practice relating Boolean expressions to their equivalent logic circuits and vice versa.
3. The third is to practice using Karnaugh maps and Boolean algebra to simplify logic circuits.

Introduction: Basic rules of Boolean Algebra: (these may not be the same order as in lecture)

a.) $A + 0 = A$	b.) $A \cdot \bar{A} = 0$
c.) $A + 1 = 1$	d.) $\bar{\bar{A}} = A$
e.) $A \cdot 0 = 0$	f.) $A + AB = A$
g.) $A \cdot 1 = A$	h.) $A + \bar{A}B = A + B$
i.) $A + A = A$	j.) $(A + B)(A + C) = A + BC$
k.) $A + \bar{A} = 1$	l.) $\overline{AB} = \bar{A} + \bar{B}$ (deMorgan)
m.) $A \cdot A = A$	n.) $\overline{A + B} = \bar{A} \cdot \bar{B}$ (deMorgan)

Hints:

Now that you are comfortable with using transistors to build logic gates we will transition to implementing logic with discrete integrated circuit (ic) chips. This means that for this lab you only need to use + 5 Volts and Gnd – no discrete transistors or resistors are needed for this lab.

Also, since all of the boards have limited connections to ground (and +5 volts) it is very useful to run 1 wire from ground to one of the power strips (and one wire from +5 volts to one of the power strips on the bread board). Then you can use all of the connections on one power strip for the Hi and Lo signals as well as for the power to the chips.

Finally, you can use the Data Switches to provide a +5 volt or 0 volt signal for inputs to the logic gates.

- 1.) Using IC chips, construct the circuit that corresponds to $(X + Y)(X + Z)$ and also construct the circuit that corresponds to $X + Y \cdot Z$. Measure the Truth Table for each circuit and use Table 1 (next page) to show that rule j is true. Draw and label the circuit diagrams here:

Table 1

X	Y	Z	$X + Y \cdot Z$	$(X + Y)(X + Z)$
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

2.) Prove DeMorgan's Theorems by constructing truth tables (Table 2 and 3). If you want to, you may construct the circuits to actually measure the truth table with the logic circuit. For example in Rule m, you can construct the circuit corresponding to \overline{AB} and measure its truth table. Then construct the circuit corresponding to $\overline{A} + \overline{B}$ and measure its truth table.

a.) Rule 1 is $\overline{AB} = \overline{A} + \overline{B}$.

Table 2

A	B	$\overline{A} + \overline{B}$	\overline{AB}
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

b.) Rule n (DeMorgan's continued) is $\overline{A + B} = \overline{A} \cdot \overline{B}$.

Table 3

A	B	$\overline{A + B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

3.) What is the Boolean expression for the circuit shown? Using the Boolean expression predict the truth table in Table 4.

Now, test your prediction by constructing the circuit shown (not its simplified version!) and measuring its truth table in Table 4. Is your prediction correct?

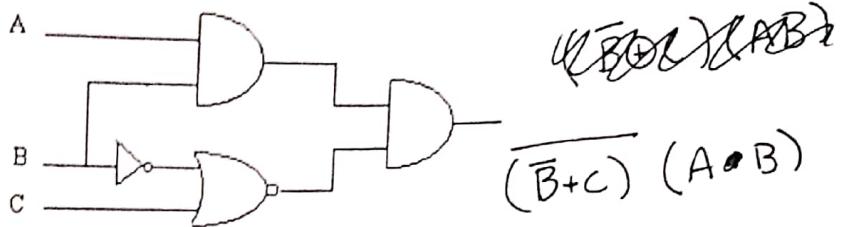


Table 4

A	B	C	Predicted	Measured from Original Circuit	Measured from Simplified Circuit (Question 4)
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	0	1
1	1	0	1	1	0
1	1	1	0	0	

- 4.) Now using Boolean algebra and DeMorgan's theorem, simplify the circuit shown in question 3. **Clearly indicate the rules of Boolean algebra that you use.** Your simplified circuit should have no more than 3 gates. To make sure your simplified circuit still represents the original circuit, measure its truth table and record it in Table 4. Draw and label the circuit diagrams here:

$$(\overline{B+C})(A \bullet B)$$

$$(\overline{B+C})(A \bullet B)$$

$$= B\bar{C}AB$$

$$= ABC$$

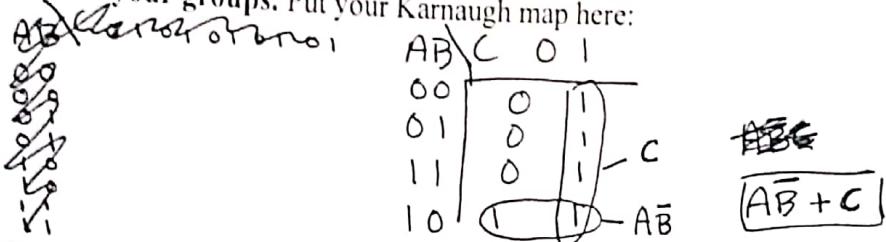
$$A\bar{B} + C(\bar{B}A + \bar{B}\bar{A}) + C \rightarrow A\bar{B} + C$$

2.) Predict the truth table for the expression $A\bar{B} + C\bar{B}A + AC + C + C\bar{B}\bar{A}$ (you should not build this circuit). You may want to convert it to standard form.

Table 5

A	B	C	Predicted	Measured from Simplified SOP (part b.)
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

- b.) Now, find the simplified SOP expression using a Karnaugh map. Clearly indicate your groups. Put your Karnaugh map here:



Check that your simplified expression is equivalent to the original expression by constructing the circuit and measuring its Truth Table in Table 5.

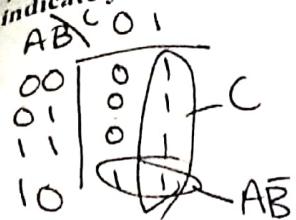
- 6.) a.) Predict the truth table for this expression $(A + C)(\bar{B} + C)(A + B + C)$ (you should not build this circuit). You may want to convert it into standard form.

Table 6

A	B	C	Predicted	Measured from Simplified POS (part b.)
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

$$\begin{aligned}
 & (A + C)(\bar{B} + C)(A + B + C) \\
 & \overline{AB} + \underline{C^2 + \bar{B}C + AC} \rightarrow \overline{AB} + C(1 + \bar{B} + A) \\
 & \bar{B}(A + C) + C(\cancel{A} + \cancel{A}) \quad (\overline{AB} + C) \\
 & (\bar{B}(A + C) + C)
 \end{aligned}$$

Now, find the simplified POS expression using a Karnaugh map. Clearly indicate your groups. Put your Karnaugh map here:



Check that your simplified expression is equivalent to the original expression by constructing the circuit and measuring its Truth Table in Table 6.



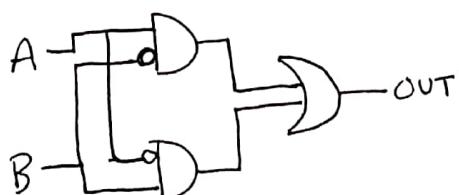
- c.) Compare the Karnaugh maps from 5 and 6. What is the relationship between them? What is the relationship between the simplified Boolean expressions in 5 and 6? (You may need to do some Boolean simplification to compare the expressions. Please indicate the rule you use in each step of your Boolean algebra)

The same

- 7.) Draw the circuit diagram and construct the circuit corresponding to the boolean expression $A\bar{B} + \bar{A}B$. Measure the truth table. What gate is this?

Table 7

A	B	$A\bar{B} + \bar{A}B$
0	0	0
0	1	1
1	0	1
1	1	0



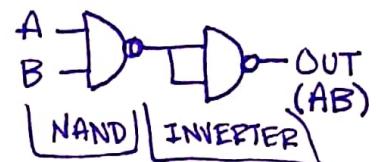
- 8.) The NAND (and NOR) gate can be used to construct any other logic gate. Hence they are called Universal gates. Design an AND gate from 2 NAND gates and design a XOR gate using 4 NAND gates. Draw the circuit diagrams for each.

* NAND \rightarrow INVERTER

If you wish to build the circuits and test if you are right, go ahead.

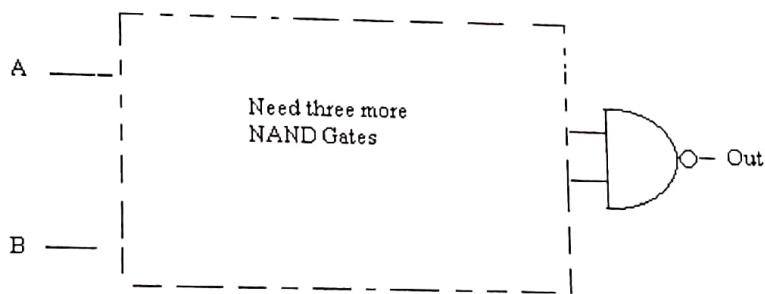
Hint for the AND gate:

Write the Boolean expression for AND operation. Note that it equals itself inverted twice (i.e rule i) and recall how to construct an inverter from a NAND gate.

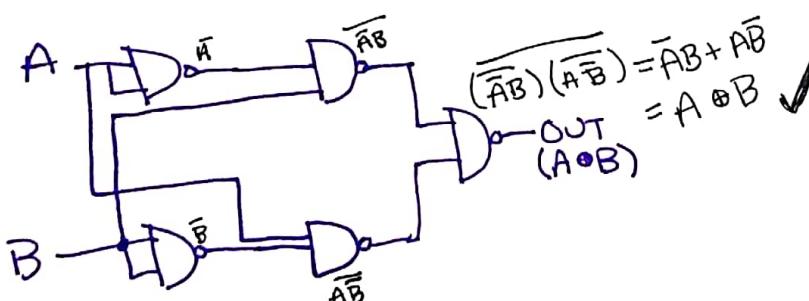


Hint for XOR gate:

- Note that one boolean expression for the XOR is $A\bar{B} + \bar{A}B$ (hopefully you learned this in question 7). Note how symmetric this expression is (if you interchange A and B, you get the same expression). This is not true with the expression $A + AB$. This symmetry should be reflected in the circuit that you build.
- You also know that there can only be one output. In other words you must have one gate leading to the output as shown:



DeMorgan's Law tells us that $\bar{A}\bar{B} = \bar{A} + \bar{B}$, a nand gate is an or gate with inverted inputs. So I found that the following is an XOR but uses 1 more NAND gate than we were specified.



A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Lab Reports: See the last page of the handout from lab 1 to review what is relevant for a lab report. In addition, for this lab report, you should include all of the work you did with Boolean algebra and Karnaugh maps.

Reports are due the week after the lab is finished.