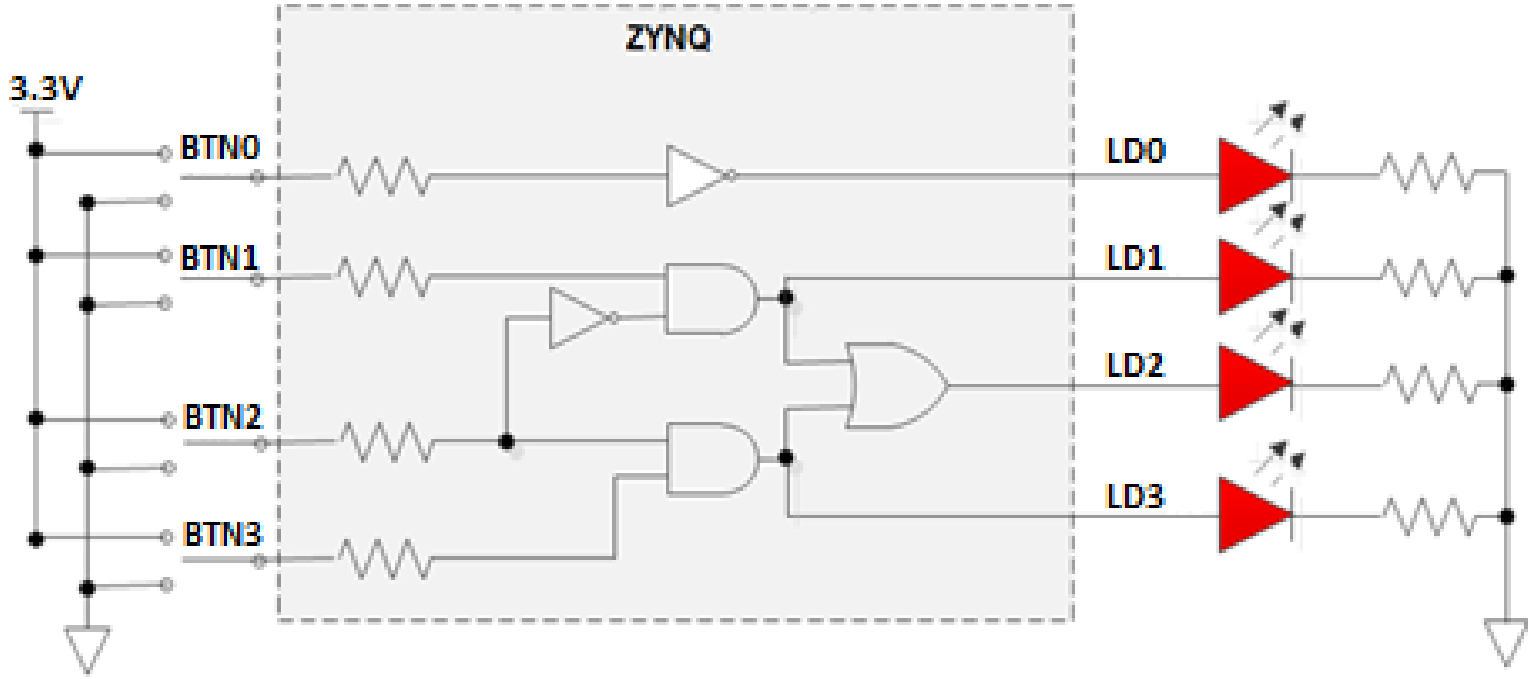
Lab1 Intro
Vivado Design Flow

Introduction

- This lab guides you through the process of using Vivado IDE to create a simple HDL design targeting the PYNQ-Z2 , or the PYNQ-Z1.
- You will simulate, synthesize, implement the design with default settings.
- Finally, you will generate the bitstream and download it in to the hardware to verify the design functionality.

The Design



Procedure

- Create a project using Vivado IDE
- Simulate the design using XSIM simulator
- Synthesize the design
- Implement the design
- Perform the timing simulation
- Generate the bitstream
- Verify the design functionality in hardware using the PYNQ-Z2 or the PYNQ-Z1

Summary

- The Vivado IDE tool can be used to perform a complete HDL design flow. The project was created using the supplied source files (HDL model and user constraint file). A behavioral simulation was done using the provided testbench to verify the model functionality. The model was then synthesized, implemented, and a bitstream was generated. The timing simulation was run on the implemented design using the same testbench. The functionality was verified in hardware using the generated bitstream.

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