```
1   --------------------------------------------------------------------------------
2   -- Company:
3   -- Engineer:
4   --
5   -- Create Date:   15:40:42 05/15/2021
6   -- Design Name:
7   -- Module Name:   C:/Xilinx/14.7/VHDL_Design_Project/TB_Timer.vhd
8   -- Project Name:  VHDL_Design_Project
9   -- Target Device:
10  -- Tool versions:
11  -- Description:
12  --
13  -- VHDL Test Bench Created by ISE for module: Timer
14  --
15  -- Dependencies:
16  --
17  -- Revision:
18  -- Revision 0.01 - File Created
19  -- Additional Comments:
20  --
21  -- Notes:
22  -- This testbench has been automatically generated using types std_logic and
23  -- std_logic_vector for the ports of the unit under test.  Xilinx recommends
24  -- that these types always be used for the top-level I/O of a design in order
25  -- to guarantee that the testbench will bind correctly to the post-implementation
26  -- simulation model.
27  --------------------------------------------------------------------------------
28  LIBRARY ieee;
29  USE ieee.std_logic_1164.ALL;
30
31  -- Uncomment the following library declaration if using
32  -- arithmetic functions with Signed or Unsigned values
33  --USE ieee.numeric_std.ALL;
34
35  ENTITY TB_Timer IS
36  END TB_Timer;
37
38  ARCHITECTURE behavior OF TB_Timer IS
39
40      -- Component Declaration for the Unit Under Test (UUT)
41
42      COMPONENT Timer
43      PORT(
44           reset : IN  std_logic;
45           clock : IN  std_logic;
46           timer_reset : IN  std_logic; -- To Reset Timer --
47           FourHzPulse : OUT  std_logic; -- Four Hz Pulse --
48           MotorPulseOutput : OUT  std_logic; -- Pulse For Stepper Motor --
49           CounterOutput : OUT  std_logic_vector(4 downto 0) -- Timer Output --
50          );
51      END COMPONENT;
52
53
54     --Inputs
55     signal reset : std_logic := '0';
56     signal clock : std_logic := '0';
57     signal timer_reset : std_logic := '0';
```

```
58
59      --Outputs
60      signal FourHzPulse : std_logic;
61      signal MotorPulseOutput : std_logic;
62      signal CounterOutput : std_logic_vector(4 downto 0);
63
64      -- Clock period definitions
65      constant clock_period : time := 10 us;
66
67    BEGIN
68
69      -- Instantiate the Unit Under Test (UUT)
70      uut: Timer PORT MAP (
71             reset => reset,
72             clock => clock,
73             timer_reset => timer_reset,
74             FourHzPulse => FourHzPulse,
75             MotorPulseOutput => MotorPulseOutput,
76             CounterOutput => CounterOutput
77           );
78
79      -- Clock process definitions
80      clock_process :process
81      begin
82         clock <= '0';
83         wait for clock_period/2;
84         clock <= '1';
85         wait for clock_period/2;
86      end process;
87
88
89      -- Stimulus process
90      stim_proc: process
91      begin
92         -- hold reset state for 100 ns.
93         reset <= '1';
94
95         wait for 100 ns;
96         reset <= '0';
97
98         -- insert stimulus here --
99         -- If timer_reset Is 0, Meaning Timer Will Not Be Reset --
100        timer_reset <= '0';
101        wait for clock_period*10000;
102
103        -- If timer_reset Is 1, Meaning Timer Will Be Reset --
104        timer_reset <= '1';
105
106        wait;
107     end process;
108
109   END;
110
```