```
Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.10 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.10 secs

--> Reading design: Traffic.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "Traffic.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "Traffic"
Output Format                      : NGC
Target Device                      : CoolRunner2 CPLDs

---- Source Options
Top Module Name                    : Traffic
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
Mux Extraction                     : Yes
Resource Sharing                   : YES

---- Target Options
Add IO Buffers                     : YES
MACRO Preserve                     : YES
XOR Preserve                       : YES
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Keep Hierarchy                     : Yes
Netlist Hierarchy                  : As_Optimized
```

```
RTL Output                          : Yes
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Verilog 2001                        : YES

---- Other Options
Clock Enable                        : YES
wysiwyg                             : NO

=========================================================================


=========================================================================
*                            HDL Compilation                            *
=========================================================================
Compiling vhdl file "C:/Xilinx/14.7/TrafficLight_Project/SyncButton.vhd" in Library work.
Architecture behavioral of Entity syncbutton is up to date.
Compiling vhdl file "C:/Xilinx/14.7/TrafficLight_Project/TimerReset.vhd" in Library work.
Architecture behavioral of Entity timerreset is up to date.
Compiling vhdl file "C:/Xilinx/14.7/TrafficLight_Project/Timer.vhd" in Library work.
Architecture behavioral of Entity timer is up to date.
Compiling vhdl file "C:/Xilinx/14.7/TrafficLight_Project/MotorController.vhd" in Library
work.
Architecture behavioral of Entity motorcontroller is up to date.
Compiling vhdl file "C:/Xilinx/14.7/TrafficLight_Project/TrafficLights.vhd" in Library work.
Architecture behavioral of Entity trafficlights is up to date.
Compiling vhdl file "C:/Xilinx/14.7/TrafficLight_Project/TrafficTopLevel.vhd" in Library
work.
Entity <traffic> compiled.
Entity <traffic> (Architecture <behavioral>) compiled.

=========================================================================
*                        Design Hierarchy Analysis                      *
=========================================================================
Analyzing hierarchy for entity <Traffic> in library <work> (architecture <behavioral>).

Analyzing hierarchy for entity <SyncButton> in library <work> (architecture <behavioral>).

Analyzing hierarchy for entity <TimerReset> in library <work> (architecture <behavioral>).

Analyzing hierarchy for entity <Timer> in library <work> (architecture <behavioral>).

Analyzing hierarchy for entity <MotorController> in library <work> (architecture
<behavioral>).

Analyzing hierarchy for entity <TrafficLights> in library <work> (architecture
<behavioral>).


=========================================================================
*                             HDL Analysis                              *
=========================================================================
Analyzing Entity <Traffic> in library <work> (Architecture <behavioral>).
Entity <Traffic> analyzed. Unit <Traffic> generated.

Analyzing Entity <SyncButton> in library <work> (Architecture <behavioral>).
Entity <SyncButton> analyzed. Unit <SyncButton> generated.

Analyzing Entity <TimerReset> in library <work> (Architecture <behavioral>).
Entity <TimerReset> analyzed. Unit <TimerReset> generated.
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Analyzing Entity <Timer> in library <work> (Architecture <behavioral>).
Entity <Timer> analyzed. Unit <Timer> generated.

Analyzing Entity <MotorController> in library <work> (Architecture <behavioral>).
Entity <MotorController> analyzed. Unit <MotorController> generated.

Analyzing Entity <TrafficLights> in library <work> (Architecture <behavioral>).
Entity <TrafficLights> analyzed. Unit <TrafficLights> generated.


=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <SyncButton>.
    Related source file is "C:/Xilinx/14.7/TrafficLight_Project/SyncButton.vhd".
    Found finite state machine <FSM_0> for signal <State>.
    -----------------------------------------------------------------------
    | States             | 7                                              |
    | Transitions        | 18                                             |
    | Inputs             | 6                                              |
    | Outputs            | 4                                              |
    | Clock              | clock                    (rising_edge)         |
    | Reset              | reset                    (positive)            |
    | Reset type         | asynchronous                                   |
    | Reset State        | car                                            |
    | Power Up State     | gateclose                                      |
    | Encoding           | automatic                                      |
    | Implementation     | automatic                                      |
    -----------------------------------------------------------------------
    Summary:
        inferred   1 Finite State Machine(s).
Unit <SyncButton> synthesized.


Synthesizing Unit <TimerReset>.
    Related source file is "C:/Xilinx/14.7/TrafficLight_Project/TimerReset.vhd".
    Found finite state machine <FSM_1> for signal <state>.
    -----------------------------------------------------------------------
    | States             | 3                                              |
    | Transitions        | 9                                              |
    | Inputs             | 3                                              |
    | Outputs            | 3                                              |
    | Clock              | clock                    (rising_edge)         |
    | Reset              | reset                    (positive)            |
    | Reset type         | asynchronous                                   |
    | Reset State        | car                                            |
    | Power Up State     | train                                          |
    | Encoding           | automatic                                      |
    | Implementation     | automatic                                      |
    -----------------------------------------------------------------------
    Summary:
        inferred   1 Finite State Machine(s).
Unit <TimerReset> synthesized.


Synthesizing Unit <Timer>.
    Related source file is "C:/Xilinx/14.7/TrafficLight_Project/Timer.vhd".
```

```
    Found 1-bit register for signal <MotorPulseOutput>.
    Found 10-bit up counter for signal <counter>.
    Found 10-bit up accumulator for signal <MotorCount>.
    Found 10-bit comparator equal for signal <MotorCount$cmp_eq0000> created at line 84.
    Found 5-bit up counter for signal <timekeeper>.
    Summary:
        inferred   2 Counter(s).
        inferred   1 Accumulator(s).
        inferred   1 D-type flip-flop(s).
        inferred   1 Comparator(s).
Unit <Timer> synthesized.


Synthesizing Unit <MotorController>.
    Related source file is "C:/Xilinx/14.7/TrafficLight_Project/MotorController.vhd".
    Found finite state machine <FSM_2> for signal <State>.
    -----------------------------------------------------------------------
    | States             | 4                                              |
    | Transitions        | 16                                             |
    | Inputs             | 3                                              |
    | Outputs            | 4                                              |
    | Clock              | MotorPulseInput           (rising_edge)        |
    | Reset              | reset                     (positive)           |
    | Reset type         | asynchronous                                   |
    | Reset State        | s0                                             |
    | Power Up State     | s0                                             |
    | Encoding           | automatic                                      |
    | Implementation     | automatic                                      |
    -----------------------------------------------------------------------
    Summary:
        inferred   1 Finite State Machine(s).
Unit <MotorController> synthesized.


Synthesizing Unit <TrafficLights>.
    Related source file is "C:/Xilinx/14.7/TrafficLight_Project/TrafficLights.vhd".
    Found finite state machine <FSM_3> for signal <State>.
    -----------------------------------------------------------------------
    | States             | 3                                              |
    | Transitions        | 9                                              |
    | Inputs             | 3                                              |
    | Outputs            | 3                                              |
    | Clock              | clock                     (rising_edge)        |
    | Reset              | reset                     (positive)           |
    | Reset type         | asynchronous                                   |
    | Reset State        | traffic_green                                  |
    | Power Up State     | flash_amber                                    |
    | Encoding           | automatic                                      |
    | Implementation     | automatic                                      |
    -----------------------------------------------------------------------
    Summary:
        inferred   1 Finite State Machine(s).
Unit <TrafficLights> synthesized.


Synthesizing Unit <Traffic>.
    Related source file is "C:/Xilinx/14.7/TrafficLight_Project/TrafficTopLevel.vhd".
Unit <Traffic> synthesized.


=========================================================================
```

```
HDL Synthesis Report

Macro Statistics
# Counters                                             : 2
 10-bit up counter                                     : 1
 5-bit up counter                                      : 1
# Accumulators                                         : 1
 10-bit up accumulator                                 : 1
# Registers                                            : 1
 1-bit register                                        : 1
# Comparators                                          : 1
 10-bit comparator equal                               : 1

=========================================================================

=========================================================================
*                        Advanced HDL Synthesis                         *
=========================================================================

Analyzing FSM <FSM_3> for best encoding.
Optimizing FSM <TrafficLight/State/FSM> on signal <State[1:2]> with johnson encoding.
---------------------------
 State         | Encoding
---------------------------
 flash_amber   | 00
 traffic_green | 01
 ped_green     | 11
---------------------------
Analyzing FSM <FSM_2> for best encoding.
Optimizing FSM <StepperModule/State/FSM> on signal <State[1:2]> with sequential encoding.
-------------------
 State | Encoding
-------------------
 s0    | 00
 s1    | 01
 s2    | 11
 s3    | 10
-------------------
Analyzing FSM <FSM_1> for best encoding.
Optimizing FSM <TimerResetting/state/FSM> on signal <state[1:2]> with johnson encoding.
------------------------
 State      | Encoding
------------------------
 train      | 00
 car        | 01
 pedestrian | 11
------------------------
Analyzing FSM <FSM_0> for best encoding.
Optimizing FSM <ButtonInput/State/FSM> on signal <State[1:3]> with user encoding.
-------------------------------
 State             | Encoding
-------------------------------
 gateclose         | 000
 gateopencar       | 001
 gateopenped       | 010
 trainpassed       | 011
 trainpassing      | 100
 car               | 101
 pedestrianpassing | 110
-------------------------------
```

```
=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# FSMs                                                 : 4
# Counters                                             : 2
 10-bit up counter                                     : 1
 5-bit up counter                                      : 1
# Accumulators                                         : 1
 10-bit up accumulator                                 : 1
# Registers                                            : 1
 Flip-Flops                                            : 1
# Comparators                                          : 1
 10-bit comparator equal                               : 1

=========================================================================

=========================================================================
*                           Low Level Synthesis                         *
=========================================================================

Optimizing unit <Traffic> ...

Optimizing unit <SyncButton> ...
  implementation constraint: INIT=r      : State_FSM_FFd1
  implementation constraint: INIT=r      : State_FSM_FFd2
  implementation constraint: INIT=r      : State_FSM_FFd3

Optimizing unit <TimerReset> ...
  implementation constraint: INIT=r      : state_FSM_FFd1
  implementation constraint: INIT=r      : state_FSM_FFd2

Optimizing unit <MotorController> ...
  implementation constraint: INIT=r      : State_FSM_FFd1
  implementation constraint: INIT=r      : State_FSM_FFd2

Optimizing unit <TrafficLights> ...
  implementation constraint: INIT=r      : State_FSM_FFd1
  implementation constraint: INIT=r      : State_FSM_FFd2

Optimizing unit <Timer> ...

=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

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=========================================================================
*                             Final Report                              *
=========================================================================
Final Results
RTL Top Level Output File Name     : Traffic.ngr
Top Level Output File Name         : Traffic
Output Format                      : NGC
Optimization Goal                  : Speed
```

```
Keep Hierarchy                     : Yes
Target Technology                  : CoolRunner2 CPLDs
Macro Preserve                     : YES
XOR Preserve                       : YES
Clock Enable                       : YES
wysiwyg                            : NO

Design Statistics
# IOs                              : 13

Cell Usage :
# BELS                             : 260
#      AND2                        : 82
#      AND3                        : 9
#      AND4                        : 2
#      AND8                        : 1
#      GND                         : 1
#      INV                         : 91
#      OR2                         : 39
#      OR3                         : 2
#      XOR2                        : 33
# FlipFlops/Latches                : 35
#      FDC                         : 16
#      FDCE                        : 5
#      FDCPE                       : 10
#      FDP                         : 4
# IO Buffers                       : 13
#      IBUF                        : 5
#      OBUF                        : 8
=========================================================================


Total REAL time to Xst completion: 3.00 secs
Total CPU time to Xst completion: 3.07 secs

-->

Total memory usage is 4514324 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```