```
1   --------------------------------------------------------------------------------
2   -- Company:
3   -- Engineer:
4   --
5   -- Create Date:   22:47:17 05/19/2021
6   -- Design Name:
7   -- Module Name:   C:/Xilinx/14.7/VHDL_Design_Project/TB_TimerReset.vhd
8   -- Project Name:  VHDL_Design_Project
9   -- Target Device:
10  -- Tool versions:
11  -- Description:
12  --
13  -- VHDL Test Bench Created by ISE for module: TimerReset
14  --
15  -- Dependencies:
16  --
17  -- Revision:
18  -- Revision 0.01 - File Created
19  -- Additional Comments:
20  --
21  -- Notes:
22  -- This testbench has been automatically generated using types std_logic and
23  -- std_logic_vector for the ports of the unit under test.  Xilinx recommends
24  -- that these types always be used for the top-level I/O of a design in order
25  -- to guarantee that the testbench will bind correctly to the post-implementation
26  -- simulation model.
27  --------------------------------------------------------------------------------
28  LIBRARY ieee;
29  USE ieee.std_logic_1164.ALL;
30
31  -- Uncomment the following library declaration if using
32  -- arithmetic functions with Signed or Unsigned values
33  --USE ieee.numeric_std.ALL;
34
35  ENTITY TB_TimerReset IS
36  END TB_TimerReset;
37
38  ARCHITECTURE behavior OF TB_TimerReset IS
39
40      -- Component Declaration for the Unit Under Test (UUT)
41
42      COMPONENT TimerReset
43      PORT(
44           reset : IN  std_logic;
45           clock : IN  std_logic;
46           TrainButton : IN  std_logic; -- Train Button Input --
47           CarButton : IN  std_logic; -- Car Button Input --
48           PedButton : IN  std_logic; -- Pedestrain Button Input --
49           Found : OUT  std_logic -- Output To Reset Timer --
50          );
51      END COMPONENT;
52
53
54     --Inputs
55     signal reset : std_logic := '0';
56     signal clock : std_logic := '0';
57     signal TrainButton : std_logic := '0';
```

```
58      signal CarButton : std_logic := '0';
59      signal PedButton : std_logic := '0';
60
61      --Outputs
62      signal Found : std_logic;
63
64      -- Clock period definitions
65      constant clock_period : time := 10 ns;
66
67    BEGIN
68
69      -- Instantiate the Unit Under Test (UUT)
70      uut: TimerReset PORT MAP (
71             reset => reset,
72             clock => clock,
73             TrainButton => TrainButton,
74             CarButton => CarButton,
75             PedButton => PedButton,
76             Found => Found
77           );
78
79      -- Clock process definitions
80      clock_process :process
81      begin
82         clock <= '0';
83         wait for clock_period/2;
84         clock <= '1';
85         wait for clock_period/2;
86      end process;
87
88
89      -- Stimulus process
90      stim_proc: process
91      begin
92
93         reset <= '1';
94
95         -- hold reset state for 100 ns.
96         wait for 100 ns;
97         reset <= '0';
98
99         -- insert stimulus here --
100
101        -- Observe When The Found Output Is 1 --
102        wait for clock_period*10;
103        TrainButton <= '1';
104        CarButton <= '0';
105        PedButton <= '0';
106
107        wait for clock_period*10;
108        TrainButton <= '0';
109        CarButton <= '1';
110        PedButton <= '0';
111
112        wait for clock_period*10;
113        TrainButton <= '1';
114        CarButton <= '0';
```

```
115         PedButton <= '0';
116 
117         wait for clock_period*10;
118         TrainButton <= '0';
119         CarButton <= '0';
120         PedButton <= '1';
121 
122         wait for clock_period*10;
123         TrainButton <= '0';
124         CarButton <= '1';
125         PedButton <= '0';
126 
127         wait for clock_period*10;
128         TrainButton <= '0';
129         CarButton <= '0';
130         PedButton <= '1';
131 
132         wait for clock_period*10;
133         TrainButton <= '1';
134         CarButton <= '0';
135         PedButton <= '0';
136 
137         wait;
138      end process;
139 
140   END;
141 
```