A Survey of Recent MARTe Based Systems

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Acknowledgements

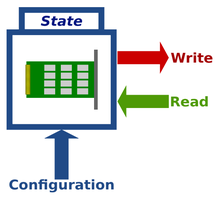
This work was supported by the European Communities under the contract of Association between EURATOM/IST and was carried out within the framework of the European Fusion Development Agreement. See the Appendix of F. Romanelli et al., Fusion Energy Conference 2008 (Proc. 22nd Int. Conf. Geneva, 2008) IAEA, (2008). The viewsand opinions expressed herein do not necessarily reflect those of the European Commission.

MARTe

Main ideas

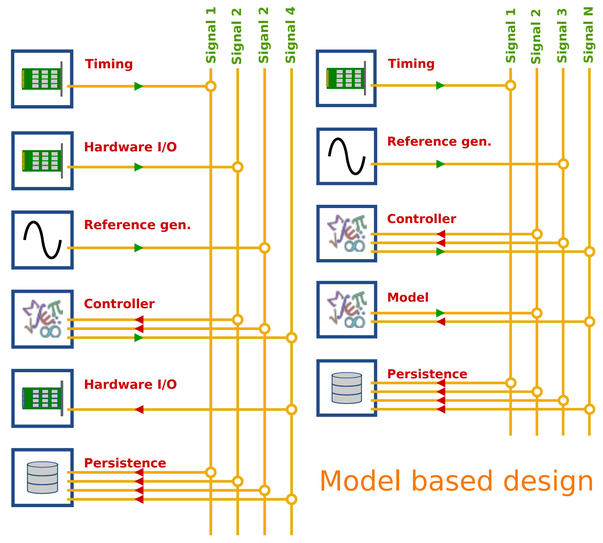
- Multi-platform C++ middleware
  -Debug and develop in non RT targets
- Simulink-like way of describing the problem
- Reusability and maintainability
- Simulation
- Data driven
- Runs in Linux, Linux+RTAI, VxWorks, Solaris andMS Windows
- Provide live introspection tools without sacrificing RT
- Advanced RT proof logging mechanism

GAMs



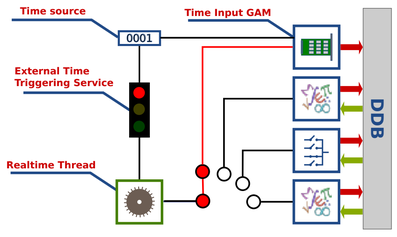
- Define boundaries
- Functional division
- Same goals, same module
- Reusability and maintainability
- Simulation
- Replace actuators and plants with models

Connecting GAMs



Model based design

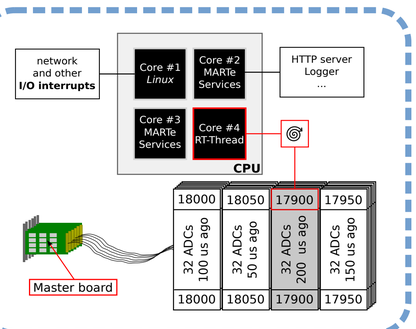
Synchronisation

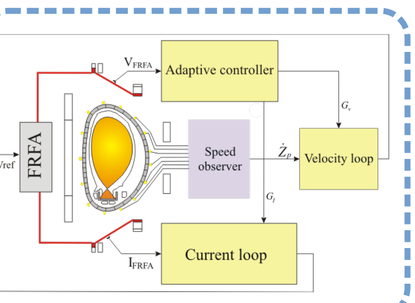


- Asynchronous
  –Get latest available value
  –Verify acceptable latency (sample too late?)
- Synchronous
- Routinely used both schemes
- ADC, time input, ...
- Network
- From another control loop

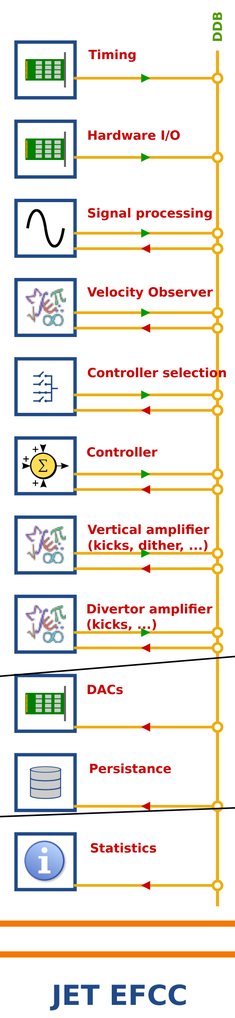
JET VS

- Elongated tokamak plasmas are susceptible to a vertical axisymmetric instability
- Dedicated Vertical Stabilisation System required
- Essential system for operation
- Growth rate of 1000s-1
- Loss of control can produce forces in the order of the 100's of tonnes

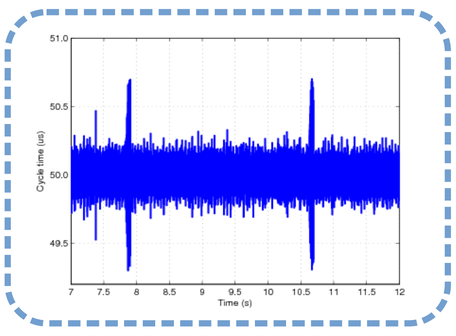


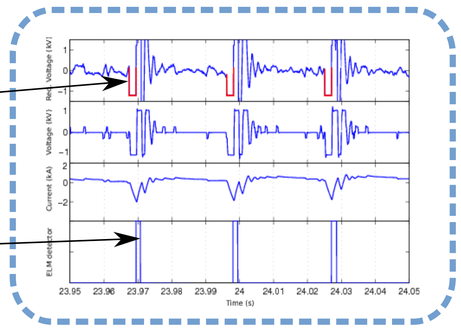


- A kick is constant voltage applied for a given period of time
- Technique used to trigger ELMs



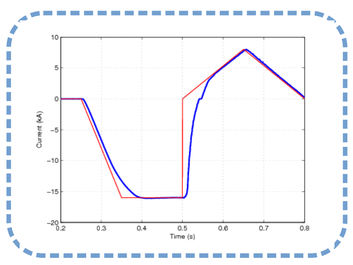
Architecture	ATCA/PCIe
Processor	Intel Core2 Quad
O.S.	RTAI
Inputs	198 18 bits ADCs @2MHz
Outputs	5 DACs
Cycle time	50 us

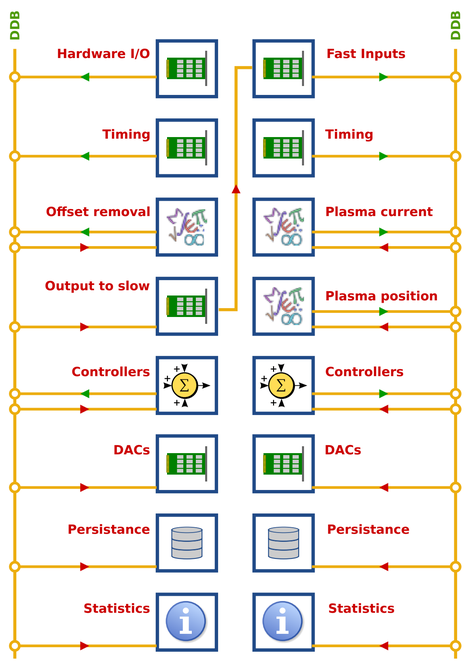




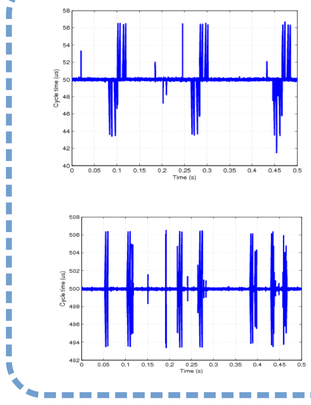
COMPASS

- Plasma control system upgrade for COMPASS tokamak
- Two control loops with different frequencies
  -50 and 500 us
  -Horizontal and vertical field
  -Plasma current and shape



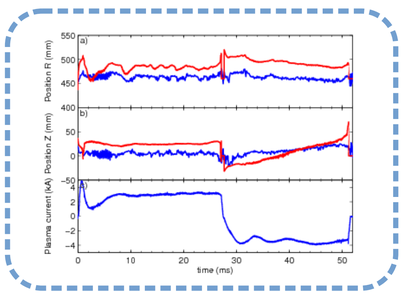


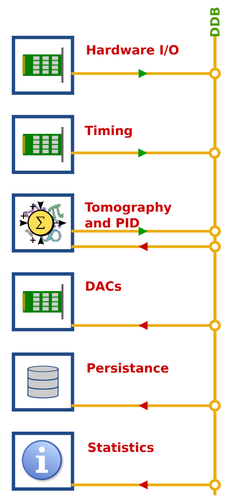
Architecture	ATCA/PCIe
Processor	Intel Core2 Quad
O.S.	Linux
Inputs	12 18 bits ADCs @2MHz
Outputs	5 RS-232
Cycle time	50 and 500 us



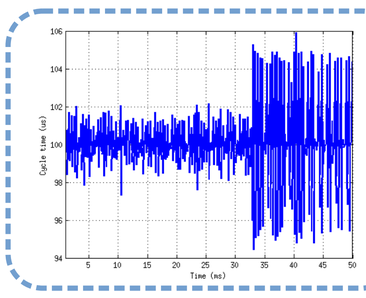
ISTTOK Tomography

- Alternating plasma Current(AC) discharges in ISTTOK
  -Longer pulses
- During current reversal magnetic measurements are unreliable
- Tomography good candidate to provide plasma position



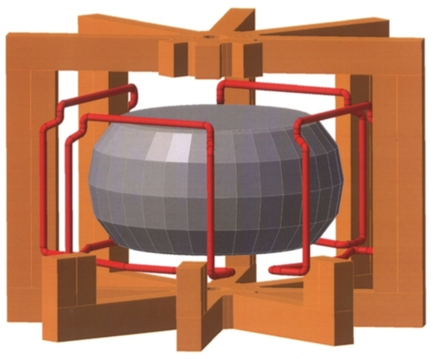


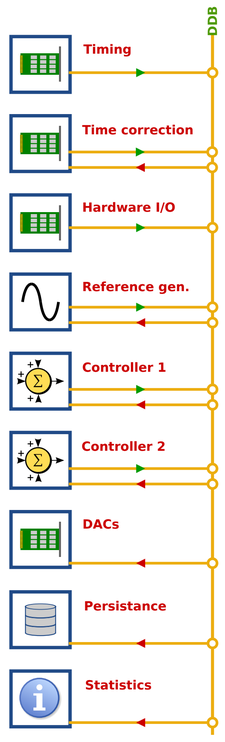
Architecture	ATCA/PCIe
Processor	Intel Core2 Quad
O.S.	Linux
Inputs	30 18 bits ADCs @2MHz
Outputs	2 RS-232
Cycle time	100 us



JET EFCC

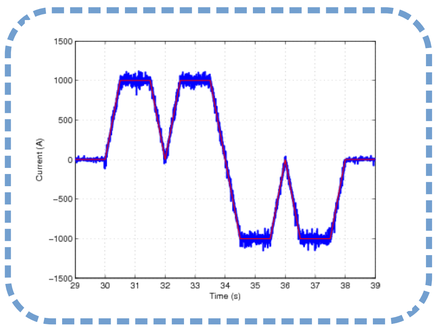
- Error Field Correction Coils change magnetic topology at the plasma boundary
- Important for instability mitigation and ELM control
- Requires current control in the EFCC coils

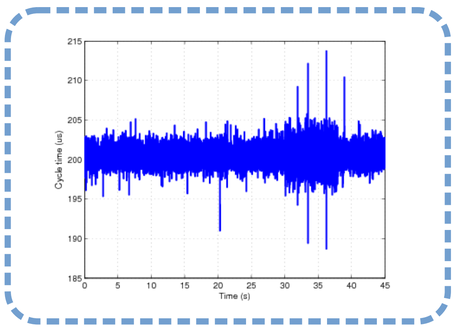




Architecture	VME
Processor	MVME5100 PowerPC
O.S.	VxWorks
Inputs	10 12 bits ADCs @330 kHz
Outputs	2 DACs
Cycle time	200 us

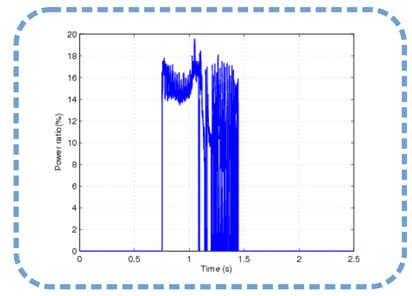
- Internal timer is adjusted to JET central time
- Development and debug of algorithms in non-rt system

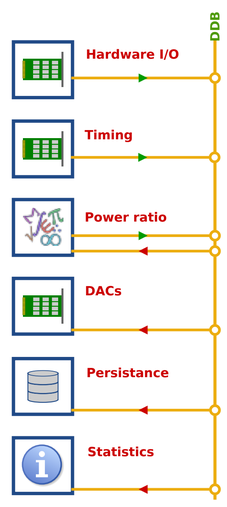




FTU LH Power Ratio

- Upgrade main FTU feedback control system
  -Receive ration between reflected and transmitted power from LH system
- Change plasma position to maximize coupling with LH source





Architecture	VME
Processor	Intel Core2 Duo
O.S.	RTAI
Inputs	16 12 bits ADCs @500 kHz
Outputs	16 DACs
Cycle time	250 us