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# **MARTe2 Users Meeting**

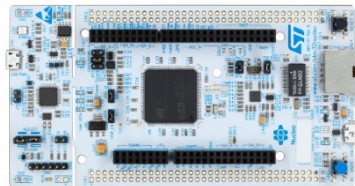
## **CRIO, RPI, STM32 demo**

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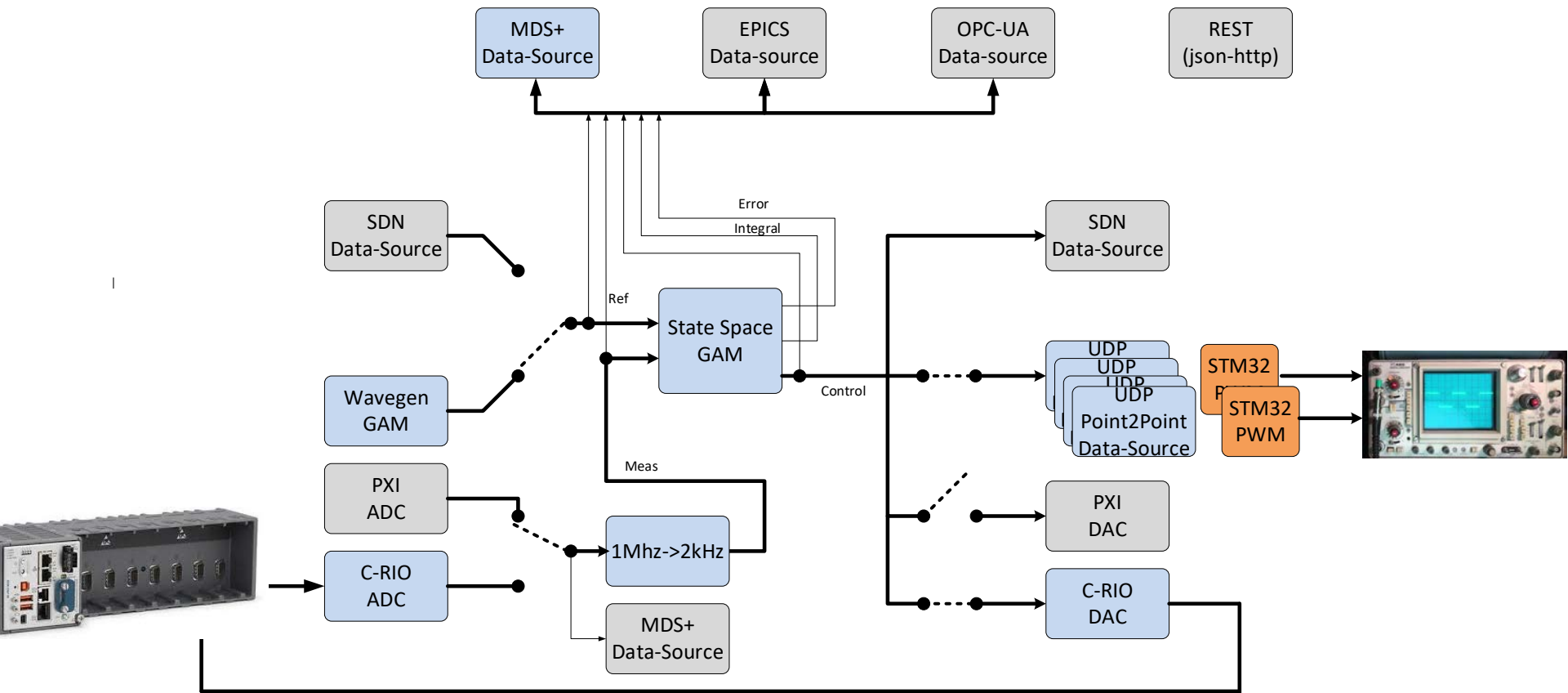
May, 2019



- Demonstrate real-time interfaces between MARTe2, CRIO and **BareMetal**
  - Using SDN
  - STM32F746G-DISCO
  - STM32F746ZGT-NUCLEO
- Configuration file:
  - <https://vcis-gitlab.f4e.europa.eu/aneto/MARTe2-demos-padova/blob/develop/Configurations/RTApp-9157-1.cfg>



# CRIO – STM – RPI interface



- Configuration file:  
<https://vcis-gitlab.f4e.europa.eu/aneto/MARTe2-demos-padova/blob/develop/Configurations/RTApp-9157-1.cfg>

- **LabView**
  - Implement FPGA design
  - Export variables using the LabView C-API generator tool
  - Expose these variables in the MARTe2 configuration file
    - **No need to recompile**

```
+NiDevice = {  
  Class = NI9157Device  
  NiRioDeviceName = RIO0  
  NiRioGenFile = "NiFpga_Test.lvbitx"  
  NiRioGenSignature = "5580A3D7E3CD37531FCD6557CFCD3824"  
  Open = 1  
  Configuration = {  
    NiFpga_TestGTD0001_ControlU8_options = 2  
    NiFpga_TestGTD0001_ControlBool_stop = 0  
    NiFpga_TestGTD0001_ControlBool_use_counter = 1  
    NiFpga_TestGTD0001_ControlU16_maxV = 5  
    NiFpga_TestGTD0001_ControlU16_DacResolution = 16383  
  }  
}
```

- **MXI**
  - Asynchronous read/write
    - MARTe2 interface for configuration
    - MARTe2 DataSource monitoring/update
  - FIFO streaming
    - MARTe2 real-time I/O DataSource

- **STM32CubeMX**
  - Configure hardware
  - Generate and compile BSP
  - Cross-compile MARTe2
  - Link MARTe2 & BSP
  - Configuration file
    - Compiled as string or
    - Loaded from serial interface
  - Generate and load firmware

<https://www.st.com/en/development-tools/stm32cubemx.html>

- **Circle bare metal library**
  - Cross-compile MARTe2
  - Link MARTe2 & Circle
  - Generate and load firmware
    - Configuration file compiled as string

<https://github.com/rsta2/circle>



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# Thank you for your attention

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